Radiation-Induced Charge Trapping in Shallow Trench Isolations of FinFETs

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***Abstract*— We provide comprehensive experimental data and technology computer-aided design simulations to clarify total-ionizing-dose mechanisms in 16-nm Si FinFETs. In n-channel FinFETs irradiated to ultra-high doses the transconductance evolution rebounds (increase up to 3-10 Mrad followed by a decrease), while the drain-to-source leakage current steadily augments until reaching a plateau at very large doses. These effects result from positive charge trapping deep in the sidewalls of the shallow trench isolation (STI) and negative trapped-charge accumulation localized in the upper STI corners. Larger sizes of inter-fin STI enhance the leakage current degradation of transistors with smaller numbers of fins. Hydrogen-induced border-trap and/or interface-trap generation at the Si/oxide interface at the STI corners leads to increased low-frequency noise at doses > 10 Mrad(SiO_2). These results show that the quality of oxides and interfaces in the upper region of the STI adjacent to the device channel is crucial for the tolerance to ultra-high radiation of modern FinFET technologies.**

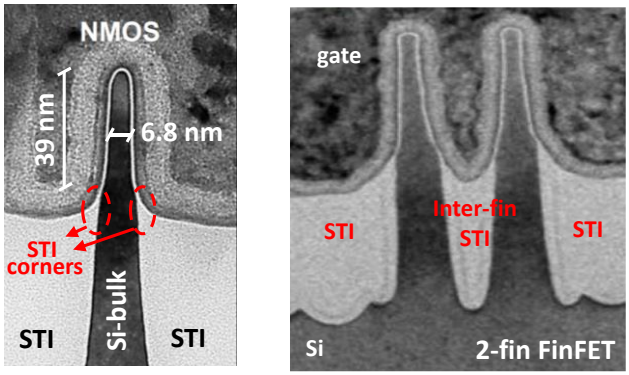
***Index Terms*—Total ionizing dose, radiation effects, 16 nm, FinFET, shallow trench isolation, low frequency noise, charge trapping, bias condition.**

I. Introduction

THE scaling down of the metal-oxide-semiconductor (MOS) devices has generally resulted in increased tolerance to total ionizing dose (TID) [1]-[3]. The ultra-thin gate oxide thickness of the gate stack of Si-based field-effect transistors (FETs) has reduced densities of charge trapped in gate oxides and increased the likelihood of charge neutralization due to tunneling electrons [1],[4],[5]. However, the decrease of channel width and length has led to new TID-induced effects related to other critical insulators and modern production processes, e.g., shallow trench isolation (STI) oxides [6]-[10], spacer dielectrics [11]-[13], and halo implantation [14].

Several recent studies on MOSFET and FinFET technologies have identified the STI as the single most important issue for devices exposed to ionizing radiation, particularly at ultra-high doses [15]-[22]. In planar Si CMOS technologies, irradiation induces positive charge buildup in the STI, which is thicker and has higher defect densities than SiO_2 gate oxides [6],[10]. Positive charge in the STI increases off-state leakage current in n-channel FETs due to the activation of lateral parasitic transistors [9],[19],[20] and induces parametric drifts in n- and p-channel FETs. The worst-case degradation is found in narrow-channel transistors due to the radiation-induced narrow-channel effect (RINCE) [6],[9],[10]. For example, positive charge trapped in the STI of pFETs can lead to decreased densities of holes in regions of the device channel that are close to the STI, often leading to large shifts in the transconductance g_m and threshold voltage V_{th} of narrow pFETs [6],[9],[14],[17]. Similar width-dependent effects occur in n-channel MOSFETs: positive charge in STI enhances the number of carriers (electrons) in the regions close to the STI, significantly improving the g_m of narrow nFETs [6],[9].

As technology nodes have advanced, TID effects have been widely explored in FinFETs [20]-[32]. Si-based FinFET technologies have exhibited TID-induced degradation with complex dependences on irradiation bias conditions [23], channel lengths [20], fin geometry [28], fin orientation [32], and fin/finger numbers [21]. Experiments at ultra-high doses up to 1 Grad(SiO_2) have been performed to analyze the transistor response and identify the critical TID mechanisms [20],[22]. In [20], 16-nm FinFETs irradiated in the ON-condition ($V_{gs} = V_{dd}$) exhibited significant TID-induced degradation of g_m and I_{off}.



(a) (b)

Fig. 1. (a) TEM images of single channel fin fabricated in TSMC 16-nm FinFET technology. (b) TEM image of a commercial Intel 10-nm FinFET designed with 2-fins. After [33] and [34], respectively.

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pFinFETs showed monotonic g_m degradation with accumulated dose that depends on the number of fin/fingers due to the different dimensions of lateral and inter-fin STI [20],[21]. In contrast, nFinFETs showed increases in I_{off} and an interesting rebound of g_m with no V_{th} degradation [22]. Similar g_m rebound and I_{off} increases in nFinFETs also are observed at low doses, as < 1 Mrad(SiO_2) [31],[32]. While these effects have been tentatively attributed to activation of negatively charged traps outside the channel region [22], the underlying mechanisms remain unknown.

In this paper we present comprehensive experimental data and TCAD simulations that clarify the origin of these TID mechanisms in nFinFETs. Ultra-high dose irradiation is used to magnify the degradation to help understand the underlying causes for the g_m rebound and increase in I_{off}. We find that these effects result from two mechanisms in different regions of the STI: (1) positive charge trapping in the deep STI sidewalls, and (2) negative trapped-charge in the upper STI corners. Build-up of negative charge depends strongly on the bias applied during irradiation, in contrast to the trapped positive charge, which is relatively insensitive to the applied bias. Low-frequency noise measurements suggest that the negative trapped charge in the upper STI corner is most likely due to acceptor-like interface and/or border traps. Technology computer-aided design (TCAD) simulations are presented that strongly support this interpretation of the experimental data.

II. Devices and Experimental Details

A. Devices

The FinFETs under test were core transistors fabricated in a commercial 16 nm bulk CMOS technology, rated to a nominal V_{dd} of 0.9 V. The devices were part of a custom array composed of several accessible transistors with channel length L = 72 nm or 240 nm. All tested transistors have the same fin width and fin height, sharing source and bulk contacts with separate drain and gate contacts.

For reference, Fig. 1(a) shows a TEM image of a single fin transistor fabricated from Taiwan Semiconductor Manufacturing Company (TSMC) 16-nm FinFET technology [33]. For the devices depicted in Fig. 1(a), the channel width (W) is constant to ~85 nm, which is calculated as $2*h_{fin}+w_{fin}$, where h_{fin} is the height of the fin (~39 nm) and w_{fin} is the width of the fin is (~7 nm). The image highlights two upper sides of the STI, forming two triangular SiO_2 regions, which are distinctive structural characteristics of FinFET devices. These regions will be fundamental for the following discussions and are called "STI corners". Transistors with 2, 5, or 10 fins were tested in this study to investigate the variation of TID-induced effects with fin number (n_{fin}). As highlighted by Fig. 1(b) for 10-nm Intel FinFETs, the dimensions of the lateral delimiting STI oxides are larger than inter-fin STI, while the STI corners are identical regardless of delimiting or inter-fin STI [34].

B. Exposure conditions and measurement setup

The irradiation was conducted using a Seifert Model RP 149 X-ray irradiator at the University of Padova, Italy, at a dose rate of 4.5 Mrad(SiO_2)/h [35]. All doses are expressed in SiO_2. The total exposure time was ~ 9 days to reach 1 Grad. After the exposure, transistors were annealed at 100 °C for 24 h. Devices were biased in three different conditions during irradiation and annealing: "OFF" (V_{gs} = 0 V, V_{ds} = 0 V), "ON" (V_{gs} = 0.9 V, V_{ds} = 0 V) and "DIODE" (V_{gs} = 0.9 V, V_{ds} = 0.9 V). All other terminals were grounded.

DC static characteristics of transistors were measured at room temperature before exposure, after irradiation, and after high-temperature annealing. The threshold voltage V_{th} is calculated as $V_{gs\text{-}int}$ - V_{ds}/2, where $V_{gs\text{-}int}$ is extracted in the linear mode of device response (V_{ds} = 50 mV) as the gate-voltage axis intercept for a linear extrapolation of the I_d-V_{gs} curve at the point of maximum first derivative [36]. Low-frequency noise was measured in a frequency span between 0.5 Hz and 1 kHz at V_{ds} = 50 mV at several values of $V_{gt} = V_{gs} - V_{th}$.

The array structure of each tested die contained 12 nFinFET transistors fabricated with different channel lengths and fin numbers. Considering the high sensitivity of transistors to electrostatic discharge, and the time required for performing an irradiation test at ultra-high doses (~5 days for 500 Mrad or ~9 days for 1 Grad), at least 3 dies were tested in each bias condition, for a total of >36 tested transistors per bias condition. Results in this paper are presented for representative channel lengths and fin numbers, with at least two nominally identical devices evaluated for all experimental conditions. Nominally identical devices irradiated and annealed under similar conditions show parameter shifts that typically vary by less than ± 10%; dedicated tests to evaluate device-to-device variability were performed and analyzed in previous work [27].

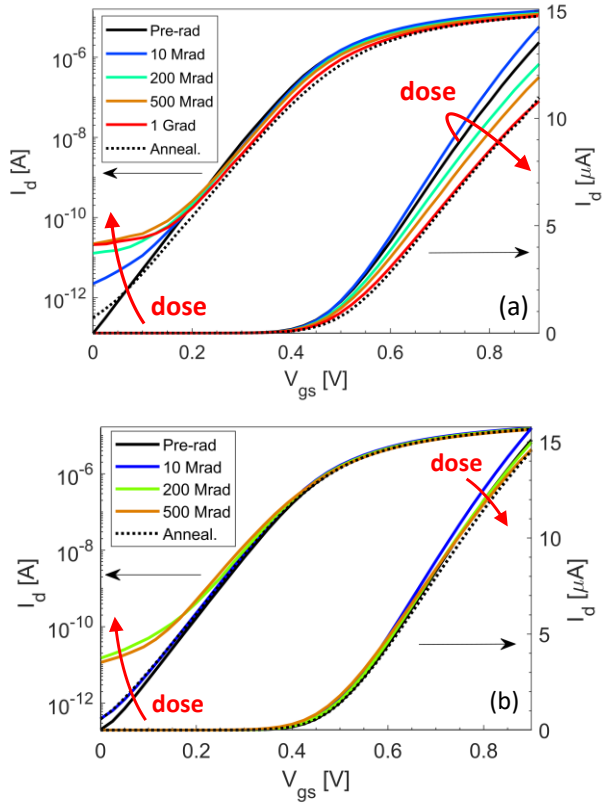

Fig. 2. Radiation-induced degradation of I_d-V_{gs} curves in the linear regime (V_{ds} = 50 mV) for nFinFETs with L = 72 nm. The devices were irradiated and annealed at 100 °C for 24 h in (top) ON-bias and (bottom) OFF-bias conditions.

III. DC Measurements

A. TID tolerance at different bias conditions

Fig. 2 shows the DC response for a nFinFET irradiated and annealed for 24 h at 100°C in the ON- and OFF-bias conditions. The worst-case degradation is observed when the devices are irradiated in the ON-condition, as the TID induces significant variation in the slope of the curves, i.e., the transconductance g_m. In both cases, the maximum drain current increases until 10 Mrad (blue curve), and then decreases at higher doses due to g_m loss. The leakage current, defined as the I_d at V_{gs} = 0 V, increases with cumulative dose by ~100× during irradiation. Annealing at high temperature induces an almost complete recovery of the leakage current (see black dotted curve) with negligible effects on the transistor response at $V_{gs} > V_{th}$. The different behavior of the leakage current and g_m suggests that effects originate from two different mechanisms.

The maximum drain current $I_{on\text{-}lin}$ is plotted as a function of dose in Fig. 3 for OFF-, ON-, and DIODE-bias conditions. At 500 Mrad, the value $\Delta I_{on\text{-}lin}$ of ON-biased devices decreases by 18%, vs. a 5% decrease for the OFF-biased. The curves of the ON-biased (red) and DIODE-biased (green) transistors almost overlap, suggesting an insensitivity of TID effects to the lateral drain-to-source electric field. However, the significant differences between the OFF-biased devices and ON- and DIODE-biased devices show that the results are still strongly influenced by the applied gate bias.

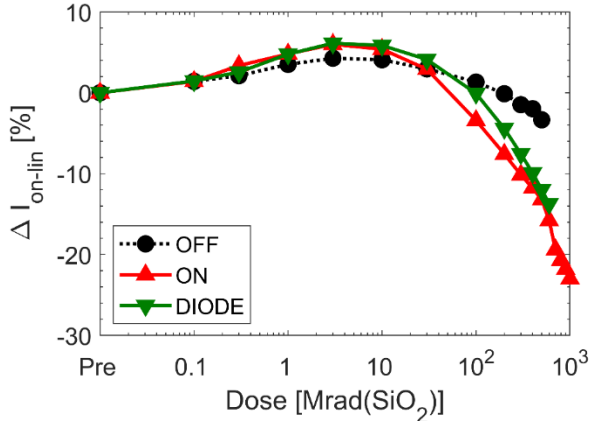

Fig. 3. Degradation of maximum drain current $\Delta I_{on\text{-}lin}$ as a function of dose for nFinFETs with L = 72 nm. The $I_{on\text{-}lin}$ is defined as the drain current at V_{gs} = 0.9 V with V_{ds} = 50 mV. Devices were irradiated in different bias conditions: OFF (V_{gs} = 0 V, V_{ds} = 0 V), ON (V_{gs} = 0.9 V, V_{ds} = 0 V), and DIODE (V_{as}=0.9 V, V_{ds} = 0.9 V).

Increases in $\Delta I_{on\text{-}lin}$ are observed at doses up to 10 Mrad, with a peak observed at ~ 3 Mrad. Similar effects are also observed in planar MOSFET technologies [6],[9] exposed at similar dose rates. At doses above 10 Mrad the on-current decreases constantly in all conditions in the explored dose range.

To help identify the cause of the I_{on} degradation, Fig. 4 shows the radiation-induced degradation in terms of (a) maximum transconductance $\Delta g_{m\text{-}MAX}$, (b) threshold voltage ΔV_{th}, and (c) subthreshold swing ΔSS. Three significant effects are apparent in Fig. 4:

1) *g_m rebound at 10 Mrad*. Values of g_m clearly increase at doses < 10 Mrad and decrease at doses > 10 Mrad. Considering the worst-case, ON-biased nFinFETs, Δg_m is +5% at 10 Mrad and decreases to –15% at 500 Mrad. As the Δg_m trend is similar to $\Delta I_{on\text{-}lin}$, the dominant effect in the inversion-regime is related to the degradation of the transconductance g_m.

2) *Slight degradation of V_{th} and SS*. Values of V_{th} shift less than 15 mV, while SS increases by <10 mV/dec after devices are irradiated to 500 Mrad. These shifts are relatively small and contribute little to the overall TID degradation. The modest ΔV_{th} shifts indicate almost negligible charge trapping in the gate oxide and/or at its Si/SiO_2 interface [1]-[4],[15]-[22].

3) *Influence of irradiation bias condition on g_m*. ON-biased devices exhibit the highest Δg_m, meaning that the TID mechanism degrading the g_m is strongly influenced by the intensity of the electric field applied to the oxides.

All these dependences will be important to the discussions of degradation mechanisms in Section IV.

B. Off-leakage current

Fig. 5 plots I_{off} as a function of accumulated dose, where I_{off} is calculated as the I_d at V_{gs} = 0 V with V_{ds} = 0.9 V. In contrast to g_m and I_{on}, I_{off} shows monotonic degradation. ON-irradiated transistors exhibit similar I_{off} degradation compared to OFF-irradiated devices, as both increase monotonically by ~100× at 500 Mrad. Inspection of all other terminals shows that leakage is flowing from drain to source. At doses > 100 Mrad, the I_{off}

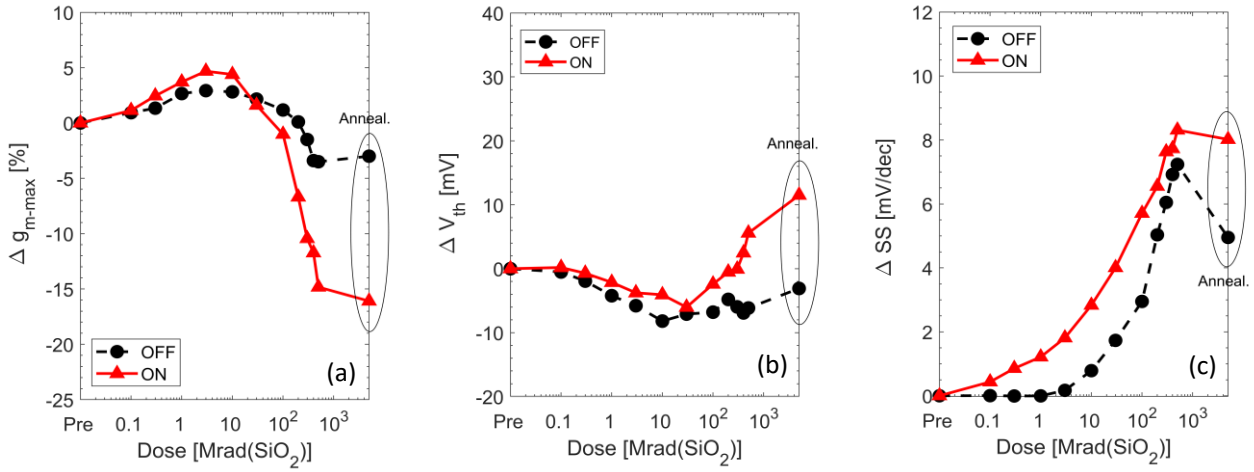

Fig. 4. Degradation of (a) maximum transconductance $\Delta g_{m\text{-}MAX}$, (b) threshold voltage ΔV_{th}, and (c) subthreshold swing ΔSS, as functions of dose in nFinFETs with L=72 nm. Transistors were irradiated and then annealed for 24 h at 100 °C in the OFF- and ON-bias conditions. Measurements are carried out at room temperature in the linear regime (V_{ds} = 50 mV).

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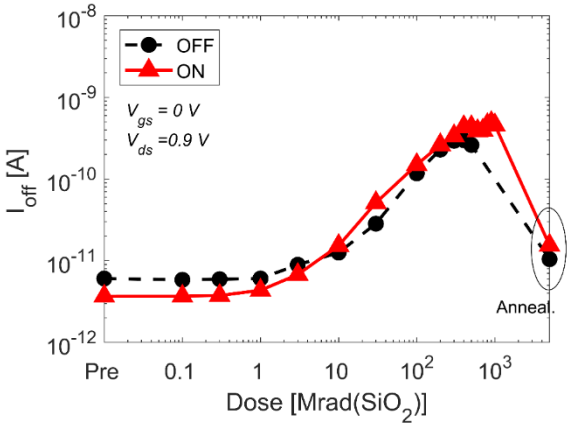

Fig. 5. Increase of drain leakage current I_{off} at V_{ds} = 0.9 V as a function of cumulative dose for nFinFETs with L=72 nm. Transistors were irradiated and then annealed for 24 h at 100 °C in the OFF- and ON-bias conditions.

reaches a plateau and settles at about 5×10^{-10} A, independently of the applied gate bias during irradiation. Annealing devices at 100 °C for 24 h restores I_{off} to pre-irradiation values.

I_{off} increases indicate positive charge trapping in the STI that activates parasitic leakage paths close the STI sidewall, similar to effects seen in irradiated planar nMOSFETs [6],[8],[17] and FinFETs [28],[31]. The I_{off} plateau at doses >100 Mrad may be induced by the saturation of positive charges in STI sidewalls at ultra-high doses or by the equilibrium of annealing (de-trapping) and trapping occurring during long-time irradiations. More importantly, the insensitivity of I_{off} to applied gate bias suggests that the leakage most likely occurs in deeper regions of the STI sidewalls, where the electric field intensity, and thus charge yield, is not influenced by V_g [1],[4],[8],[15],[16],[18].

C. TID effects dependence on fin number

We evaluated the dependence of the TID response on the number of fins by testing nFinFETs fabricated with different fin numbers and same channel length (L = 240 nm). The devices were irradiated up to 500 Mrad in the ON-bias, i.e., worst-case bias condition. Fig. 6(a) shows the g_m degradation of nFinFETs with 2, 5 and 20 fins. The curves nearly overlap, indicating practical insensitivity of Δg_m to the number of fins. At 500 Mrad, values of Δg_m are –12%, –10%, and –11% for 2-fin, 5-fin, and 20-fin transistors, respectively. As in Fig. 4(a), all devices exhibit positive g_m shifts at doses <10 Mrad and turnaround at ~10 Mrad, with g_m decreasing at ultra-high doses.

In contrast, I_{off} degradation depends strongly on the fin number of the transistors. Fig. 6(b) shows I_{off} normalized by its initial value ($I_{off}/I_{off\text{-}pre}$) for nFinFETs with 2, 5, and 20 fins. Worst-case is found for transistors having 2 fins (blue curve). These show an I_{off} increase of ~10× after 500 Mrad vs. ~2.5× for the 20-fin devices (the increase of 100x reported previously was for the shorter L = 72 nm transistors). In all cases, high temperature annealing induces an almost complete recovery of the I_{off}, similar to the results in Fig. 5. The dependence of I_{off} is most likely induced by the higher-volume oxides of lateral STI compared to intra-fin STI (see Fig. 1b), similar to the fin dependence found in p-channel FinFETs [21]. Enhanced positive charge densities in the lateral STI may induce higher I_{off} degradation in the first and last fins in sequences, compared with those in central positions. Consequently, transistors with

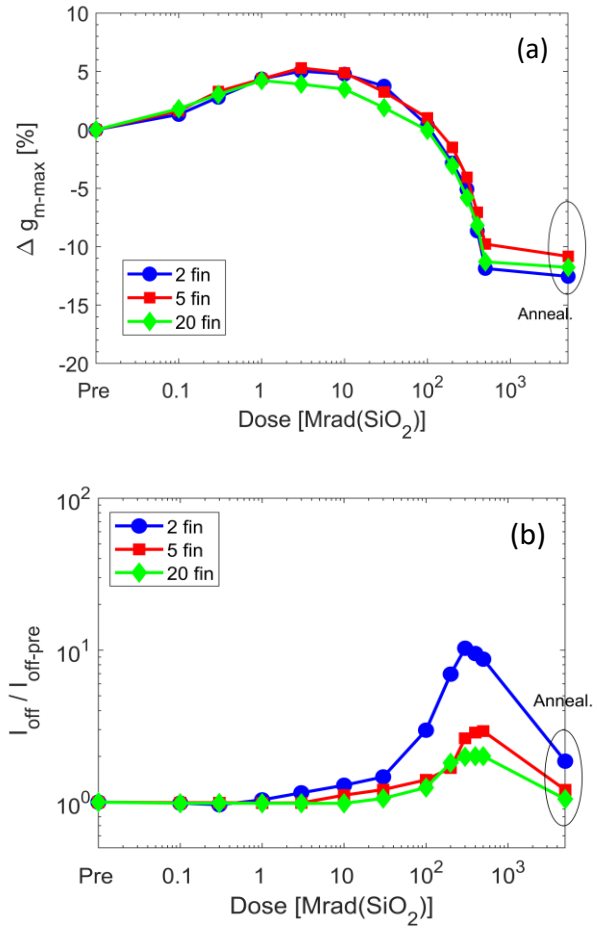

Fig. 6. Influence of the number of fins on TID-induced effects as a function of dose: (a) $\Delta g_{m\text{-}lin}$ and (b) $I_{off}/I_{off\text{-}pre}$. nFinFETs with L = 240 nm were irradiated up to 500 Mrad(SiO$_2$) and annealed at 100 °C for 24 hours in the ON-bias condition.

low numbers of fins have relatively higher I_{off} degradation compared to transistors having higher numbers of fins.

The differing g_m and I_{off} dependences on numbers of fins highlights that the significant TID degradation can occur in two different regions of STI. In particular, I_{off} is evidently induced by positive charges trapped in deep regions of the STI sidewalls, as suggested by its dependence on fin-number and its relative independence of irradiation bias. On the other hand, g_m may be induced by negative trapped-charge buildup in the upper corners of the STI, as suggested by its independence of fin-number and its strong dependence on irradiation bias.

IV. Low-Frequency Noise Response

Low-frequency noise (LFN) was measured at several gate voltages to obtain insights into TID-induced defects [37]-[51]. The analysis shown here focuses on devices with long channels (L = 240 nm), as the noise response of short-channel transistors in pre-rad condition is typically dominated by Lorentzian noise generated by a single pre-existing prominent defect, which dominates over the 1/f noise response, resulting in random telegraph noise [46]-[50].

Fig. 7 shows the LFN response of nFinFETs irradiated and annealed in the (a) ON- and (b) OFF-bias conditions. The FinFETs show 1/f noise with typical device-to-device

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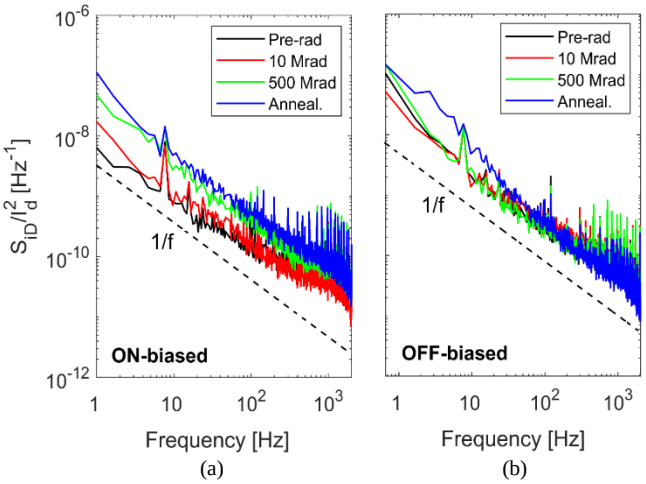

Fig. 7. Low-frequency noise response for nFinFETs with L = 240 nm and n_{fin} = 2. Devices were irradiated up to 500 Mrad(SiO_2) and annealed at 100 °C for 24 h in (a) ON- and (b) OFF-bias conditions. The noise was measured at V_{ds} = 50 mV and V_{gt} = 0.2 V at room temperature.

variability [37], [38]. In ON-biased devices, the noise is approximately constant after 10 Mrad and increases at 500 Mrad. This LFN increase indicates activation of new traps, as the channel and newly generated defects localized in the near-interfacial gate oxide can exchange charge through tunneling and/or thermally-assisted processes, which allows for the capture/emission of electrons by border traps [37],[38],[44]. Recent revaluation of LFN also shows a potentially significant role for hydrogen-mediated defect activation and passivation in LFN for some devices, e.g., via the alternating defect activation and passivation of interface traps at the semiconductor/oxide interface [47],[51]. As a consequence, increases in LFN noise magnitudes at doses >10 Mrad indicate generation of border traps and/or increases in intensity of hydrogen-assisted defect activation and passivation processes at Si/oxide interfaces [37],[47],[51]. It is worth noting that the significant increase in magnitude of LFN does not occur until g_m begins to drop, after 10 Mrad (see Fig. 4a). High temperature annealing in Fig. 7 (blue curve) slightly increases the LFN, again in agreement with the slight changes in g_m after annealing. In contrast, OFF-biased FinFETs show stable LFN response, which is relatively insensitive to cumulative dose.

Fig. 8 plots the low-frequency noise magnitude at 10 Hz as a function of $V_{gt} = V_{gs} - V_{th}$ for nFinFETs irradiated in the ON-bias condition. When the slope $|\beta|$ of the noise vs. V_{gt} curve is approximately equal to 2, the effective density of the traps is uniform in space and energy [37],[39],[40],[42]. In pristine and in devices irradiated to 10-Mrad, $|\beta|$ is ~2, indicating an approximately uniform spatial and energetic trap distribution. At 500 Mrad, the noise increases significantly and $|\beta|$ is ~1.6, indicating that the newly generated traps are less uniform in space and energy than the defects leading to the noise in the as-processed devices. For annealed devices, the S_{Id}-V_{gt} curve shows a slight increase in magnitude at low V_{gt} with $|\beta|$ of ~1.6, while $|\beta|$ is ~2.1 for high V_{gt}. Hence, there is not only an increase of effective defect density during irradiation and annealing, but also a change in spatial and energy distribution [37],[38],[44].

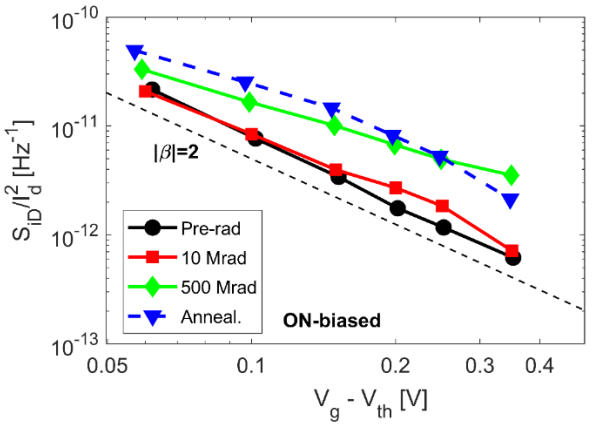

Fig. 8. 1/f noise magnitudes at f = 10 Hz vs. $V_{gs} - V_{th}$ at V_{ds} = 50 mV for nFinFETs with L = 240 nm. Devices were irradiated up to 500 Mrad(SiO_2) and then annealed in the ON-bias condition.

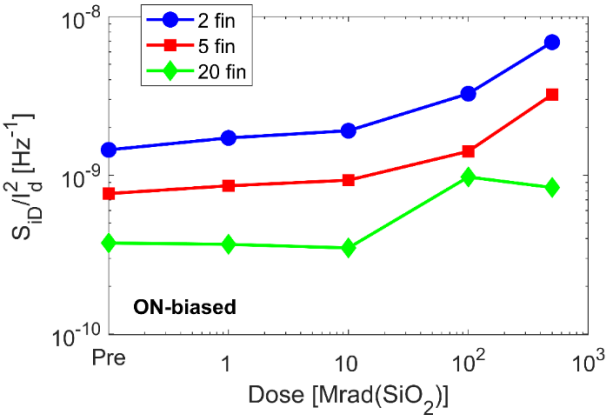

Fig. 9. Low-frequency noise magnitudes for nFinFETs with L=240 nm and several fin numbers. Devices were irradiated and annealed in the ON-bias condition with noise measured at V_{ds} = 50 mV and V_{gt} = 0.2 V at room temperature. The out-of-trend increase of LFN of 20-fin device at 100 Mrad is most likely caused by higher-than-normal contact noise during this test.

Fig. 9 shows the noise at 10 Hz as a function of dose for transistors of L = 240 nm with different fin numbers. The noise magnitude scales inversely with channel area, i.e., the number of fins, and increases with dose [37],[38],[48]. The low-frequency noise magnitude of all FinFETs increases substantially after 100 Mrad(SiO_2), similar to the g_m drop in Fig. 4(a). The increase of LFN is independent of the number of fins, as all FinFETs exhibit a 4× increase of the LFN magnitude.

We conclude that, in ON-biased transistors, the LFN measurements at doses >10 Mrad and subsequent high-temperature annealing indicates the activation of border and/or interface defects, which are spatially and/or energetically non-uniform, and independent of fin-number. These results all suggest that the increase in noise is most likely due to the trap activation processes related to the STI corners [38],[47],[52]-[54], which lead to the decreases in g_m for similar dose and annealing conditions.

V. Mechanisms Identification and Discussion

On the basis of the above experimental results, we have proposed TID-induced mechanisms that could justify the evolution of g_m and I_{on} at high doses in Figs. 3 and 4. Silvaco

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TCAD simulations are now presented to illustrate how these basic mechanisms influence the electrical response of the transistors. The results provide strongly supporting evidence for the following sequence:

- *1st mechanism*: fast generation of positive charge, holes and H^+, in the SiO_2 of STI. This mechanism is responsible for the g_m increase at doses <10 Mrad and for the continuous I_{off} increase.

- *2nd mechanism*: slow activation of donor-like traps, capable of trapping negative charge in the upper corners of the STI (see Fig. 1(a)). This mechanism is responsible for the g_m decrease at doses >10 Mrad and the increase of the LFN magnitude.

Charge trapping in the STI can contribute to the LFN of devices, as reported in [52]-[54]. Fig. 10 shows a Silvaco TCAD model developed through the Devedit and Deckbuild tools, including the Atlas and Victory Process. The geometrical structure is based on TEM images shown in Fig. 1 with meshing optimized close to the material interfaces. The gate stack is formed by ~2 nm of HfO_2 (brown), ~6 nm of Al (gray), and a thick layer of Ti (green). Doping profiles in the Si channel have been retrieved from publicly available information and set to 10^{16} cm^{-3} of B in the channel region [26]. All the physics for modelling the semiconductor device are set to the default Silvaco parameter values. The color scale in Fig. 10 indicates the electric field intensity E when V_{gs} = 0.9 V. The FinFET layout introduces distinctive regions visible as triangular oxide regions in the upper STI corners, which are characterized by the highest values of electric fields. This agrees well with the strong influence of bias on Δg_m in Fig. 4(a). It is likely that the negative charge formation (mechanism #2) may be related to H^+ transport and de-hydrogenation processes at the Si/SiO_2 interface [12],[13],[55]-[61], leading to the accumulation of negatively charged interface traps in the STI corners. Interface-trap formation in the STI corner is enhanced under high electric fields as in the cases of ON- and DIODE-biases, as shown also by LFN measurements. This contrasts with results for OFF-bias, for which electric fields are small in the STI corners.

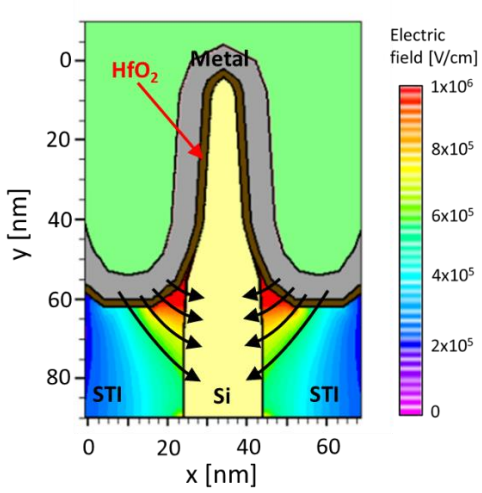

Fig. 10. TCAD simulation of the nFinFETs for V_{gs} = 0.9 V. The color scale indicates the intensity of the electric field in the STI, while the black arrows show the direction of the electric field.

Fig. 11 illustrates the proposed TID-induced mechanisms degrading g_m. TCAD simulations are performed in nFinFETs at V_{gs} = 0.9 V (channel ON). The color scale indicates the electron density in the Si channel fin. TID effects were simulated by adding fixed charges in specific regions of the STI oxide [15],[16],[18],[62]. Positive charge was added as fully ionized donor traps (Q_{STI}), which are uniformly distributed throughout the STI, in agreement with the relatively small electric field reaching the STI sidewalls. Negative charge, accounting for mechanism #2, was added as fully ionized acceptor traps (Q_{e^-}) uniformly distributed at the Si/STI interface from the top STI corner down to a depth of 15 nm, represented by the red regions of Fig. 10 under the highest electric field.

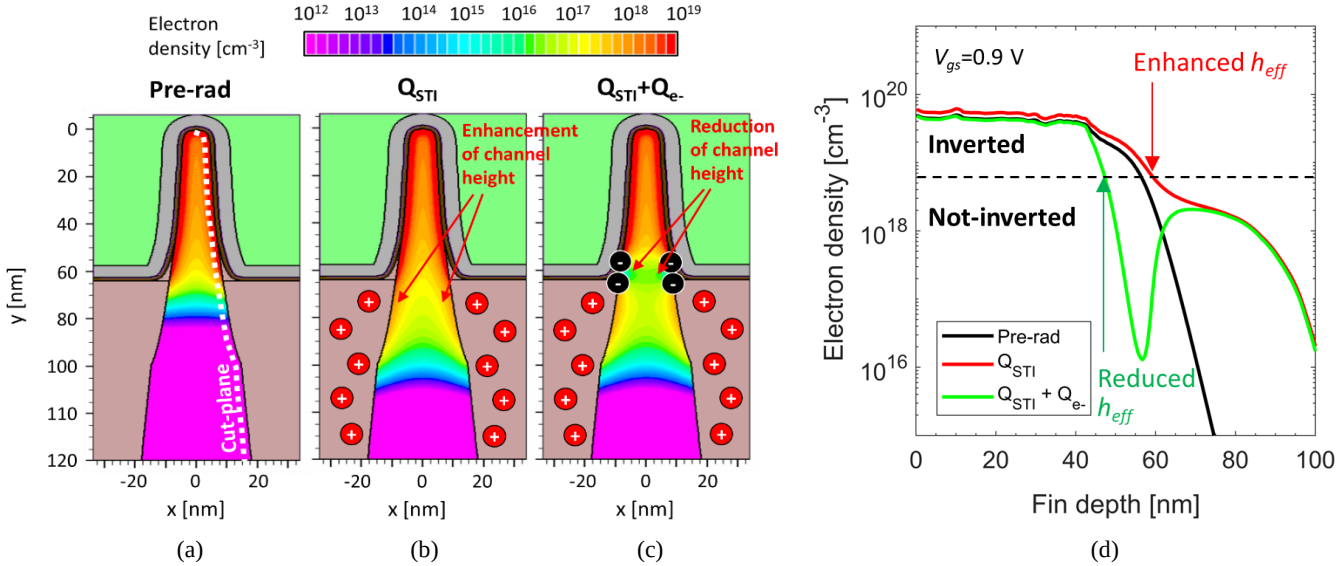

Fig. 11. TCAD simulation of nFinFETs when V_{gs} = 0.9 V (channel ON). The images show TID-induced mechanisms degrading $g_{m\text{-}max}$. The color scale illustrates the electron density in the Si channel fin: (a) pre-irradiation without trapped charges in the oxides, (b) at high doses with positive trapped charge in STI (Q_{STI} = 5×10^{17} cm^{-3}), and (c) at ultra-high doses with positive and negative trapped charge (Q_{STI} = 5×10^{17} cm^{-3} Q_{e^-} = 7.5×10^{12} cm^{-2}). The Q_{STI} are uniformly distributed in the STI, while the Q_{e^-} are localized at the Si/SiO_2 interface close to the upper corners of the STI. (d) The plot shows the electron density in the Si fin as a function of fin depth (coordinate y in (a)), considering the cutline shown in (a), i.e., at 1 nm from the Si/SiO_2 interface, with Q_{STI} = 5×10^{17} cm^{-3} and Q_{e^-} = 7.5×10^{12} cm^{-2}.

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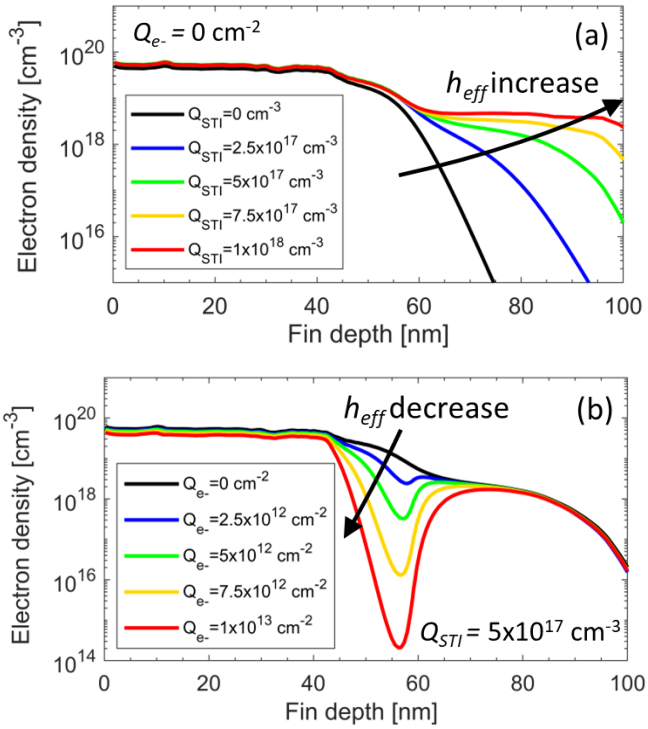

Fig. 12. TCAD simulations of nFinFETs when V_{gs} = 0.9 V (channel ON). The plots show electron density concentrations as functions of fin depth along the cutline in Fig. 11(a), showing the modulation of the effective channel height h_{eff}. (a) Several densities of positive charge Q_{STI} are shown, with Q_{e^-} = 0 cm^{-2}. (b) Several densities of negative charges Q_e are shown, with Q_{STI} = 5×10^{17} cm^{-3}.

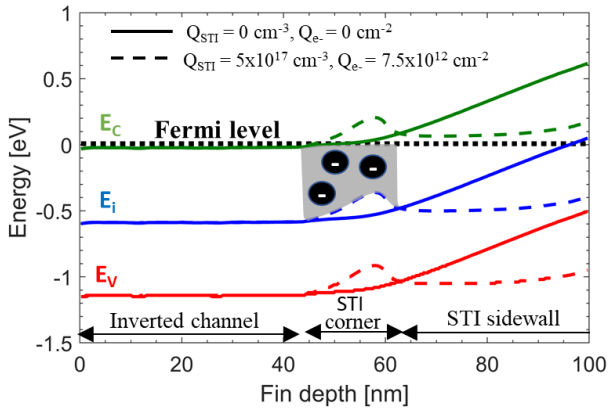

Fig. 13. Simulated band diagrams as a function of fin depth, considering the cutline shown in Fig. 11(a), i.e., at 1 nm from the Si/SiO$_2$ interface. The band diagram refers to a nFinFET biased with V_{gs} = 0.9 V. Continuous line refers to the pre-irradiation condition and dotted lines refer to Q_{STI} = 5×10^{17} cm^{-3} and Q_e = 7.5×10^{12} cm^{-2}. The plot shows that interface traps located in the STI corner are charged negatively, as the Fermi level is above the intrinsic level.

In the pre-irradiation condition in Fig. 11(a), the channel region is inverted, and the fin is characterized by a high density of electrons. Fig. 11(b) simulates the condition at 10 Mrad, when positive charges are trapped in STI with Q_{STI} = 5×10^{17} cm^{-3}, in agreement with typical expected charge trapping in the STI [14],[63]. Positive charge enhances the effective height (h_{eff}) of the device channel, which extends a little deeper into the fin substrate. Fig. 11(c) simulates ultra-high dose effects, considering the contribution of negative trapped charge in the STI corners at Q_{e^-} = 7.5×10^{12} cm^{-2}, which is in range of density of interface traps expected at STI corner/semiconductor interfaces [13],[19],[64]. This negative charge compensates for the effect of positive charge, depleting the Si channel region near the STI corners, and thus reducing the h_{eff}.

Variations in h_{eff} that occur as a result of radiation-induced charge trapping in the STI are highlighted in Fig. 11(d), which shows the electron density as a function of fin depth, evaluated at a cutline at 1 nm from the Si/SiO$_2$ interface. Depth of 0 nm corresponds to the top of the fin, with increases in value moving down in the fin substrate. Depths with high e$^-$ densities (> 5×10^{18} cm^{-3}; see dotted line in Fig. 11(a)) identify the h_{eff}, corresponding to inverted Si regions. For example, before irradiation (black curve), h_{eff} is ~55 nm. The value of h_{eff} increases to ~59 nm when positive Q_{STI} = 5×10^{17} cm^{-3} are added, and h_{eff} decreases to ~46 nm when negative Q_{e^-} = 7.5×10^{12} cm^{-2} are added in addition to Q_{STI}.

The initial increase of h_{eff} in Fig. 11(b) and the associated reduction of h_{eff} in Fig. 11(c) agree well with the turnaround of the experimental g_m visible in Fig. 4(a), as g_m is approximately proportional to the effective channel height h_{eff}. Modulation of h_{eff} may occur due to both positive charges in STI and negative charges in the STI corners. The simulation results in Fig. 12 highlight the h_{eff} modulation effect induced by several densities of Q_{STI} and Q_{e^-}. In Fig. 12(a), the electron concentration is plotted for different densities of Q_{STI}. Positive charges in the STI contribute to enhancement of the inversion layer close to the upper corner of the STI, thus increasing h_{eff}. In Fig. 12(b), the effects of electron trapping in the STI corner is studied for different densities of Q_{e^-} when positive charges are trapped in the STI (Q_{STI} = 5×10^{17} cm^{-3}). The plot highlights the effects induced by negative charges on the h_{eff}. The black curve refers to only positive trapped charge, representing the condition at 10 Mrad with highest h_{eff}. By increasing densities of compensating trapped negative charge in the STI corners, h_{eff} decreases with slight changes in electrical response of the main channel, consistent with the constant V_{th} and *SS* in Fig. 4.

The slight increase of the *SS* and increase of the LFN at doses > 10 Mrad suggest that the nature of the negative charges of mechanism #2 are most likely interface traps, whose generation is typically slow, electric-field driven and temperature dependent [55]-[61]. Moreover, the amphoteric nature of interface traps [65],[66] fits with this explanation of both g_m and I_{off} degradation. As shown by the band diagram of Fig. 13, interface traps located at the STI corners are negatively charged when the channel is in inversion, causing a drop in g_m.

In contrast, these interface traps are partially filled when devices are in the subthreshold region, and thus affecting much less the I_{off}, for which the increase relies primarily on positive charges trapped in the STI sidewalls. The interface traps at the STI corners can be partially filled with positive or negative charges, depending on the position of the Fermi energy with respect to the intrinsic level of Si. The mechanism increasing the I_{off} current is shown in Fig. 14 through simulations at V_{gs} = 0 V (channel not inverted). The color scale indicates the electron density in the Si channel fin, as in Fig. 11. In Fig. 14(a), the p-substrate region is in-accumulation, having an e$^-$ density of 10^{10} cm^{-3}. In Fig. 14(b), positive charge (Q_{STI} = 5×10^{17} cm^{-3}) is added in the STI, leading to an increase in e$^-$ density in the Si regions close to STI sidewalls. These Si regions with high e$^-$ density activate two parasitic leakage paths deep in the STI sidewalls, responsible for the increase of I_{off} [8],[15],[16],[18],[26]. Fig. 14(c) represents the case, in which

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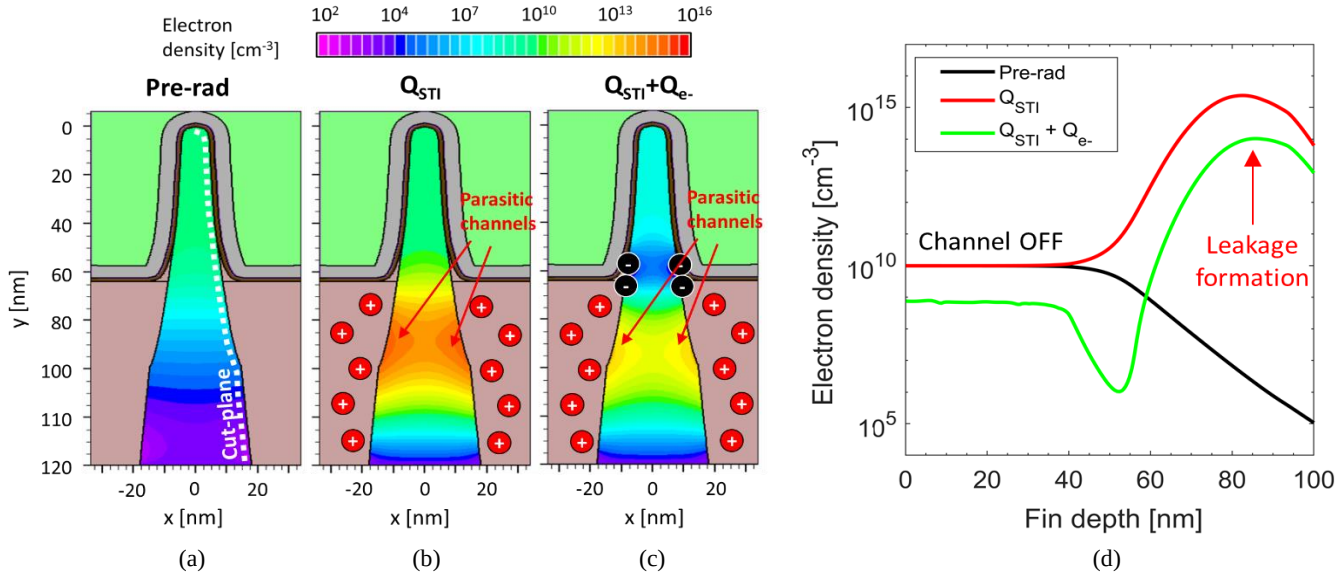

Fig. 14. TCAD simulation of nFinFETs when V_{gs} = 0 V (channel OFF). The images show TID-induced mechanisms increasing the I_{off} current. The color scale shows the electron density in the Si channel fin: (a) pre-irradiation without any trapped charge in the oxides, (b) at high doses with positive trapped charge in STI (Q_{STI} = 5×10^{17} cm^{-3}), and (c) at ultra-high doses with positive and negative trapped charge (Q_{STI} = 5×10^{17} cm^{-3} and $Q_{e\text{-}}$ = 7.5×10^{12} cm^{-2}). Values of Q_{STI} are uniformly distributed in the STI, while the $Q_{e\text{-}}$ are localized at the Si/SiO$_2$ interface close to the upper corners of the STI. (d) Electron density in the Si fin as a function of fin height, considering the cutline shown in Fig. 11(a), i.e., at 1 nm from the Si/SiO$_2$ interface.

the Fermi level is higher than the intrinsic level, thus the case with negative trapped charge. Even at relatively high $Q_{e\text{-}}$ = 7.5×10^{12} cm^{-2}, the parasitic transistors are still activated, in agreement with the continuous increase of the I_{off} of Fig. 5. This effect is highlighted in Fig. 14(d), which shows e$^-$ density as a function of fin depth. The peak in e$^-$ density is found in the deep Si regions, before and after negative $Q_{e\text{-}}$ charge is added in the STI corners. The height of the e$^-$ density peak depends mainly on Q_{STI}, while can still be slightly influenced by $Q_{e\text{-}}$. In conclusion, in case of partially filled positive interface traps or in case of partially filled negative interface traps, the parasitic transistors located in the deep Si regions are still conducting, leading to the I_{off} increase visible in Fig. 5.

VI. Conclusions

The results of this work clarify the nature of TID mechanisms in n-channel FinFETs, identifying critical TID issues related to charge trapping in the upper corners of STI oxides. 16-nm Si nFinFETs irradiated up to ultra-high doses exhibit a turnaround in g_m above 3-10 Mrad and a continuous increase in drain leakage current at higher doses. Worst-case degradation is found when positive bias is applied to the gate, with V_{th} and *SS* relatively insensitive to accumulated dose.

Experimental results, combined with TCAD simulations, identify two different dominating TID mechanisms that induce non-uniform charge trapping in the STI oxides. The first mechanism is related to positive charge trapping in the STI sidewalls. Positive charge causes a monotonic increase of the drain-to-source leakage current and improves g_m due to an increase in the effective channel height. The larger dimensions of the lateral STI oxides compared with the smaller dimensions of intra-fin STI enhance the relative I_{off} degradation of transistors with smaller number of fins. On the other hand, a second slower mechanism appears at doses >10 Mrad causing the formation of negative trapped charge in the upper corners of the STI. The negative charge compensates the effect of positive charges, and degrades the transistors g_m due to reduction of the effective channel height. The generation of border/interface traps and activation of hydrogen assisted processes at Si/oxide interface lead to significant increases in low-frequency noise at doses > 10 Mrad. These results resolve several puzzling issues from previous studies of FinFETs at ultrahigh radiation doses, and point to the need to continuously monitor and improve the channel/STI interfaces of advanced MOS technologies.

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