Radiation-Induced Effects in SiC Vertical Power MOSFETs Irradiated at Ultrahigh Doses

S. Bonaldo, *Member, IEEE*, C. Martinella, *Member, IEEE*, S. Race, *Graduate Student Member, IEEE*, N. Für, S. Mattiazzo, M. Bagatin, *Member, IEEE*, S. Gerardin, *Member, IEEE*, A. Paccagnella, *Senior Member, IEEE*, and U. Grossner, *Senior Member, IEEE*

***Abstract*— Total-ionizing dose (TID) and displacement damage (DD) are investigated in SiC power MOSFETs at ultrahigh doses with 10-keV X-ray and 3-MeV protons. Significant parametric shifts in the electrical responses of the devices are observed depending on the bias condition and on the fabrication technology. Worst TID degradation is measured when positive gate bias is applied during the irradiation, due to positive charge trapping in the gate oxide. Devices built in the latest generation SiC technology reveal a smaller subthreshold swing degradation, thanks to a better quality of the SiC/SiO_2 interface. Devices exposed to 3-MeV protons exhibit a complex combination of TID and DD effects. The *I–V* and capacitance–voltage (*C–V*) measurements in SiC power MOSFETs identify two main degradation mechanisms: 1) TID-induced charge trapping in the gate oxide and SiC/SiO_2 interface and 2) DD-induced lattice damage in the SiC drift region, which degrades the series resistance of the devices.**

***Index Terms*— Displacement damage (DD), protons, silicon carbide (SiC) power MOSFETs, total-ionizing dose (TID), ultrahigh doses, X-rays.**

I. Introduction

THE wide bandgap semiconductor silicon carbide (SiC) has emerged as the most viable alternative to silicon (Si) for next-generation high-efficiency and high-power-density applications [1], [2]. Due to the high thermal conductivity and the higher energy required for ionization and defect formation, compared to Si, SiC technology has been considered very suitable for harsh working conditions, including high-temperature and high radiation exposure applications [3]. These advantages make SiC-based power electronics desirable for space, avionics, and nuclear industry, as well as high-energy physics experiments [4], [5], [6], where electronics work at ultrahigh ionizing radiation doses >10 Mrad(SiO_2) [7], [8].

In such environments, commercial SiC power devices can be affected by total-ionizing dose (TID) causing the trapping of charges in the dielectric layers, i.e., gate silicon dioxide (SiO_2) [9]. TID effects in several SiC device types have been explored mostly up to 2 Mrad(SiO_2) [10], [11], [12], [13], [14], [15], reporting higher TID degradation with respect to other wide bandgap power technologies, such as AlGaN/GaN HEMTs exposed to doses of 100 Mrad(SiO_2) [16]. Studies on the previous generation of SiC power MOSFETs produced by the manufacturer used in this work showed a significant negative shift of the threshold voltage and an increase in interface trap density with increased subthreshold swing accumulated doses when exposed to 1.5 Mrad(SiO_2) [10]. However, the TID response of newer generations of SiC power MOSFETs at ultrahigh doses is still unknown and its exploration may be useful for improving the knowledge of the basic degradation mechanisms occurring in SiC-based devices.

Energetic particles and their collision cascades can also induce displacement damage (DD) effects [9]. DD phenomenon displaces atoms from their original crystalline lattice sites generating primary defects, e.g., vacancies, interstitials, and anti-site defects [17]. Some of these defects are electrically active as they act as trapping centers, which could significantly modify the carrier transport properties in semiconductors, such as carrier mobility, carrier concentration, and carrier lifetime [18]. Most publications investigating DD in 4H-SiC devices consider SiC junction barrier Schottky (JBS) and SiC PiN diodes structures as SiC radiation detectors [19], [20]. Only a few experiments have been performed on 4H-SiC power MOSFETs with protons [21], [22], neutrons [22], [23], and electrons [23]. The DD-induced degradation of electrical characteristics of transistors may be related to [22]: 1) carrier removal in the n-type drift region due to generation of deep acceptor centers and 2) carrier mobility and carrier lifetime degradation due to the generation of Z1/Z2 centers (bandgap position E_C-0.68 eV) and related E2 (E_C-0.60 eV) and E3 (E_C-0.72 eV) energy levels.

Energetic particles can also induce destructive single-event effects (SEEs) [9], such as single-event burnout (SEB) [24], [25], [26], [27] and single-event gate rupture (SEGR) [28], [29], or nondestructive SEEs as single-event leakage current (SELC) [4] [30], [31], [32]. If the latter represents the main criticality for heavy-ion exposure, SEB and SEGR are the main effects observed for low LET particles, such as high-energy neutrons or protons.

This work explores the TID and DD effects at ultrahigh doses for two different generations of commercial SiC vertical

Manuscript received 30 December 2023; accepted 28 January 2024. Date of publication 14 February 2024; date of current version 18 April 2024. *(S. Bonaldo and C. Martinella contributed equally to this work.) (Corresponding author: C. Martinella.)*

S. Bonaldo, M. Bagatin, S. Gerardin, and A. Paccagnella are with the Department of Information Engineering, University of Padua, 35131 Padua, Italy (e-mail: stefano.bonaldo@dei.unipd.it).

C. Martinella, S. Race, N. Für, and U. Grossner are with the Advanced Power Semiconductor Laboratory (APS), ETHZ, 8092 Zurich, Switzerland (e-mail: martinella@aps.ee.ethz.ch).

S. Mattiazzo is with the Department of Physics and Astronomy, University of Padua, and with INFN of Padua, 35131 Padua, Italy.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TNS.2024.3366190.

Digital Object Identifier 10.1109/TNS.2024.3366190

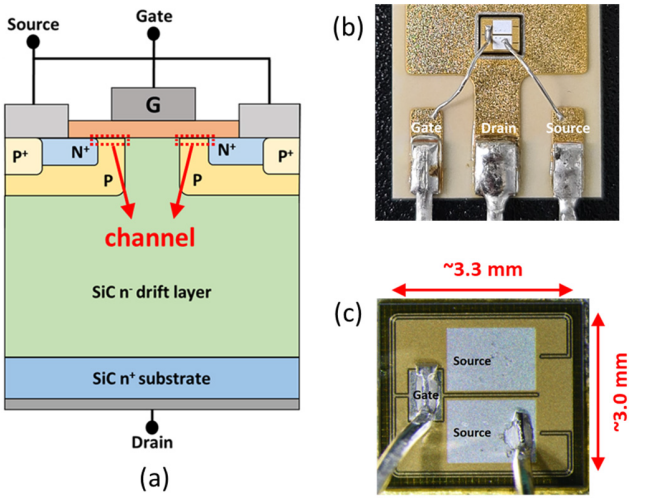

Fig. 1. (a) Schematic layout of a single unit cell of the SiC power MOSFET designed with planar gate (not to scale). (b) DUT soldered on a DCB board and bonded to the gate and source pads with Al wires. (c) Bare die from the second generation Cree/Wolfspeed used for the test.

power MOSFETs, exposed to X-rays and 3-MeV protons. The static (I–V) and dynamic capacitance–voltage (C–V) characteristics of SiC power MOSFETs have been investigated before and after the exposure. I–V measurements highlight important TID-induced negative shifts of the threshold voltage for both the second and third generations, suggesting buildup of positive charge in the relatively thick gate oxide during both experiments, as discussed in Section III. In addition to TID degradation, DD signatures on the I–V and C–V characteristics of devices tested with 3-MeV protons are presented in Section IV.

II. Devices and Experimental Details

A. Devices Under Test

The devices under test (DUTs) are vertical second and third-generation SiC planar-gate MOSFETs fabricated by Cree/Wolfspeed, USA. The devices are designed as a series of multiple cells, which are connected in parallel. Fig. 1(a) shows the 2-D schematic representation of a single cell containing two horizontal channel areas highlighted in red. Second-generation devices (CPM2-1200-0080B) have $R_{DS(ON)}$ = 80mΩ and a pitch size of ∼9 μm. The gate oxide is composed of 40-nm SiO_2. The recommended operational gate–source voltage is in the range of −5/+20 V with a maximum drain-to-source voltage of 1200 V. The third-generation devices (CPM3- 1200-0075A) have a $R_{DS(ON)}$ = 75mΩ, smaller pitch, and an operational gate–source voltage of −4/15 V with improved SiC/SiO_2 interface quality [33]. A common approach for reducing the defect density at the SiC/SiO_2 interface, which is typically two orders of magnitude higher than in Si/SiO_2 [34], is treating the SiO_2 gate oxide with nitrous oxide (N_2O) or nitric oxide (NO) anneal processes [35].

Bare dies were chosen to directly expose the chip surface to the beam. The devices were soldered on a customized direct bonded copper (DBC) board, as shown in Fig. 1(b). The drain connection was established by the soldering, whereas the gate and source were connected by single aluminum wire bonds with 300 μm diameter, as in Fig. 1(c).

B. Irradiation Condition and Measurement Setups

Two experiments were performed. The first experiment was conducted at the University of Padova, using a 10-keV X-ray irradiator at a dose rate of 3.1 Mrad(SiO_2)/h for a total exposure time of ∼32 h to reach 100 Mrad(SiO_2). All dose values are calculated in Mrad(SiO_2). Several gate-bias conditions were applied to the series of SiC MOSFETs during the irradiation:

1) "GND" (V_g = 0 V);
2) "Semi-ON" (V_g = 5 V);
3) "ON" (V_g = 20 V for second gen and V_g = 15 V for third gen);
4) "$-V_g$" (V_g = −5 V for second gen and V_g = −4 V for third gen).

The values of the electric field (E) in the gate oxide for the four conditions were obtained from numerical simulations as 0 V/cm, 1.0 MV/cm, 4.7 MV/cm, and −0.67 MV/cm. The drain and source terminals were biased at 0 V. After the exposure, the devices were annealed with all terminals connected to ground for 24 h at 100 °C.

The second experiment was performed using protons provided by the CN accelerator at the INFN-Laboratori Nazionali di Legnaro, Padova. The proton beam has a kinetic energy of 3 MeV and a penetration range of 53 μm in SiC (ECIF simulations [36]). The beam intensity was monitored with a Faraday cup before and after each exposure in the DUT active area, as well as during the exposure in the area surrounding the DUT. Second-generation devices with $R_{DS(ON)}$ = 80mΩ were tested under "ON"-bias condition (V_g = 20 V). The proton irradiations were performed in a vacuum chamber, using a dose rate of 51.6 krad/s, for a total dose of 100 Mrad, equal to a total fluence of 6.7 × 10^{13} cm^{-2}. After the exposure, the devices were annealed under bias (V_{gs} = 20 V and V_{ds} = 0 V) for 24 h at room temperature and 24 h at 100 °C.

For both experiments, the I–V static responses were measured at room temperature before exposure, at several irradiation steps, and after the annealing. Similarly, C–V characteristics were measured at room temperature before and after the irradiations, and after the annealing. The measurements were performed using a Keysight E4990A impedance analyzer. The test fixture Keysight 16047E was used to mount the DUTs. A frequency of 30 kHz was selected as the optimal tradeoff to avoid undesired parasitic effects at higher frequencies and reduce the noise effects at lower frequencies [37]. At least two devices were tested for each set of conditions.

C. Evaluation of Electrical Stress Effects

Irradiations with X-rays require about ∼29 h to reach 100 Mrad(SiO_2). In order to distinguish degradation induced by electrical stress from that induced by irradiation, the SiC-based MOSFETs were stressed without radiation under the bias conditions for the same amounts of time required for devices to be irradiated.

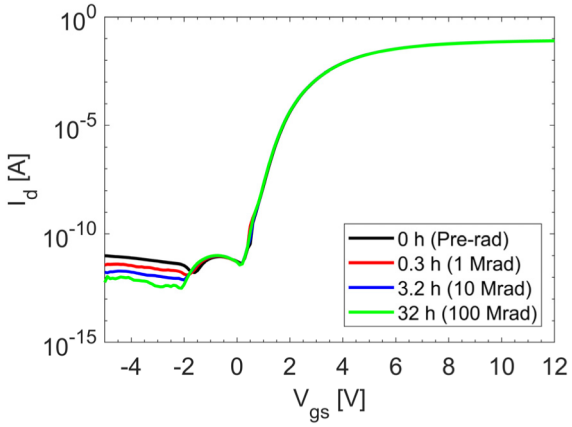

Fig. 2. Electrical stress-induced degradation of I_d–V_{gs} curves in the linear regime (V_{ds} = 50 mV) for SiC MOSFET. The device was biased for a total time of 32 h at room temperature in the "ON" bias, in order to evaluate the degradation induced by the electrical stress without X-ray exposure.

In Fig. 2, the device is tested under the electrical stress induced by the "ON"-bias condition, i.e., the highest bias at V_{gs}. In general, these SiC DUTs are commercial and show excellent stability in time, as in contrast to other previous SiC devices [38], [39], [40]. After ∼29 h, the threshold voltages shift less than 8 mV for each examined bias condition with some decreases in the leakage currents in the subthreshold region. The contribution of the stress-induced effects is almost negligible compared to the radiation-induced effects shown in Section III.

III. Experimental Results X-Rays

A. TID Response for the Second Generation Devices at Different Bias Conditions

Fig. 3(a) shows the transfer characteristics (I_d–V_g) of a second-generation SiC power MOSFET in the saturation regime (V_{ds} = 5 V) irradiated and annealed at 100 °C for 24 h in the ON-bias condition. During the irradiation, the device exhibits a negative shift of the threshold voltage V_{th}, which causes a significant drift in the working point of the device with more than 2x increase in the ON-current after 100 Mrad. After annealing, the SiC device partially recovers its response, thus indicating the formation of a significant density of stable defects.

The I_d–V_g characteristic in the linear regime (V_{ds} = 0.1 V) is shown in Fig. 3(b). During the exposure, the curves shift toward negative V_g values, indicating positive charge trapping in the relatively thick gate oxide. The magnitude of the shift decreases between 10 and 100 Mrad, indicating a possible saturation of the trapping phenomena. On the other hand, the OFF-leakage current I_{off}, defined as I_d at V_{gs} = −5 V, is almost insensitive to TID, showing the robustness of the gate oxide and the absence of STI-related effects, which typically affect planar Si-based MOS devices at ultrahigh doses [41], [42], [43]. With respect to the pristine measurement, no difference was observed in I_g–V_g after 100 Mrad, indicating no sign of damage in the gate oxide (i.e., gate rupture).

The influence of bias conditions during the irradiation on the TID sensitivity is shown in Fig. 4, which summarizes the

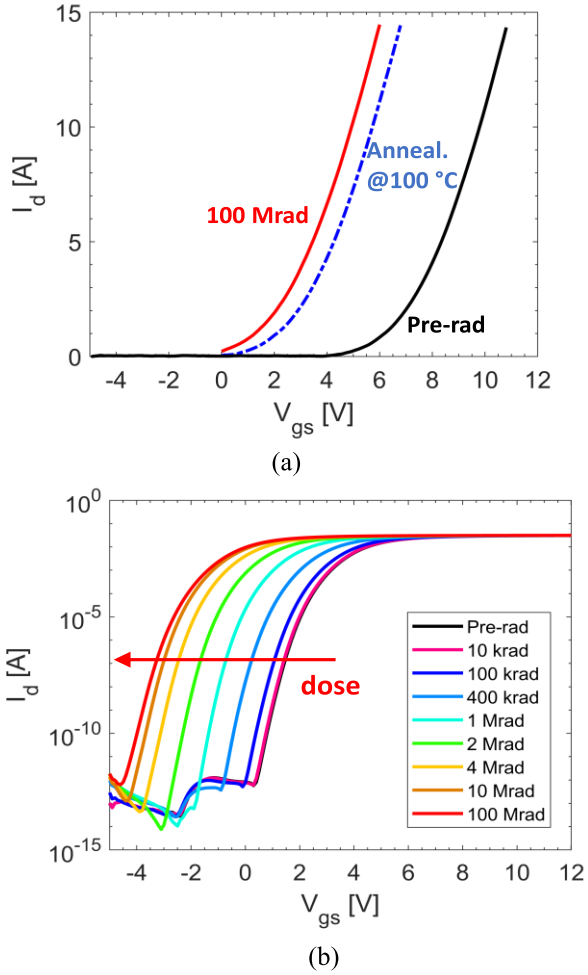

Fig. 3. I_d–V_{gs} curves of second-generation SiC V-MOSFETs in (a) saturation regime (V_{ds} = 5 V) and (b) linear regime (V_{ds} = 0.1 V). The devices were irradiated with X-rays up to 100 Mrad(SiO_2) in the "ON" condition and then annealed at 100 °C for 24 h.

degradation of: 1) maximum drain current I_{on}; 2) threshold voltage V_{th}; and 3) maximum transconductance g_{m-MAX}. All the values are calculated in the linear regime at V_{ds} = 0.1 V with I_{on-lin} extrapolated at V_{gs} = 4.5 V. The threshold voltage V_{th} is defined as $V_{gs-int} - V_{ds}/2$; $V_{gs,int}$ is extracted in the linear region (V_{ds} = 0.1 V) as the gate-voltage axis intercept of the linear extrapolation of the I_d–V_{gs} curve at the point of its maximum first derivative, i.e., of maximum g_m.

The I_{on-lin} variation of Fig. 4(a) shows a positive shift of the current in the linear regime, up to a maximum of 190%, when devices are irradiated up to 100 Mrad in "ON" bias. After 10 Mrad, charge buildup in the gate oxide saturates. Fig. 4(b) and (c) suggests that the I_{on} variation is mostly dominated by the negative shift of V_{th}, with a small contribution from the degradation of g_{m-MAX}. After 100 Mrad, V_{th} shifts up to ∼4.6 V for devices irradiated in the "ON" condition, while the g_m variation is relatively small, −6%. Comparing the different gate-bias conditions during the exposure, the largest TID degradation is observed for the devices tested in "ON" and "semi-ON" conditions, which induce almost identical V_{th} degradations. Slight differences between the "ON"- and "semi-ON"-biased devices are not significant and may be induced by the device-to-device variability. In both cases, their ΔV_{th}

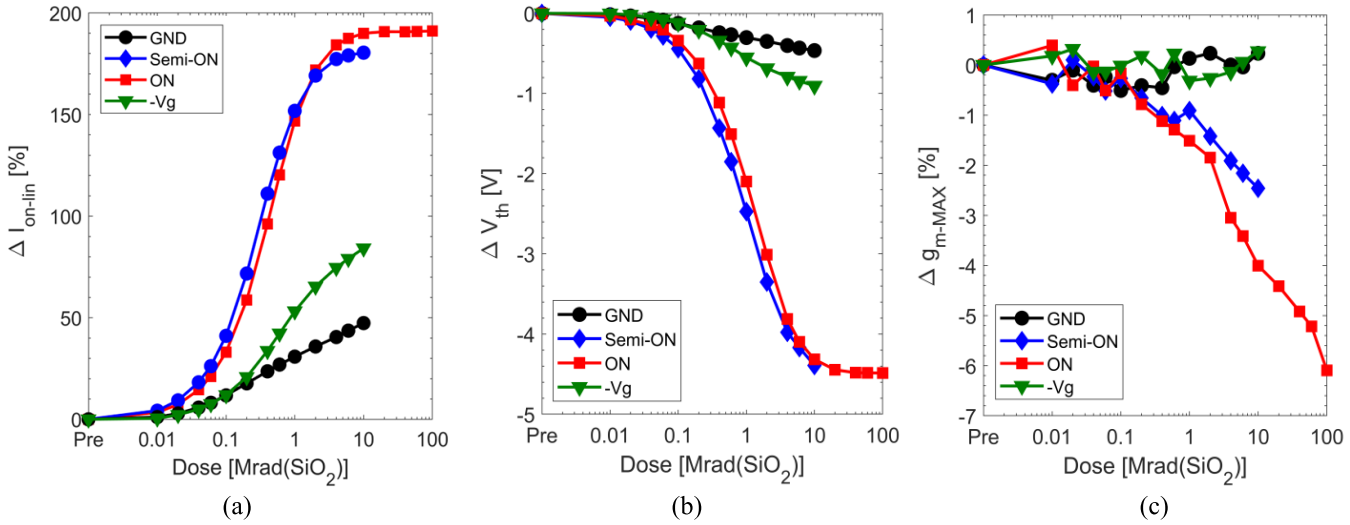

Fig. 4. Degradation of (a) maximum drain current ΔI_{on-lin}, defined as the I_d variation at $V_{gs} = 4.5$ V, (b) threshold voltage ΔV_{th}, and (c) maximum transconductance Δg_{m-MAX} as a function of dose in second-generation SiC V-MOSFETs. Irradiations were performed in different bias conditions.

becomes stable at doses >10 Mrad. This saturation trend of V_{th}, as well as the absence of any rebound in the ΔV_{th} curves, suggests that the TID phenomenon at doses >10 Mrad may be slowed down by the saturation of TID-induced positive charge trapping in the gate oxide.

On the other hand, the "$-V_g$"-bias condition induces V_{th} shifts that are much lower than the "ON" condition, as ΔV_{th} is -0.95 for "$-V_g$" versus $\Delta V_{th} = 4.5$ V for "ON" after 10 Mrad. The different TID sensitivity with the applied bias underlines the relevance of the direction and intensity of the electric field, which affects the charge yield, as well as the trap cross sections, and may drift the positive trapped charges in different directions. Among all the conditions, the lowest TID effects are observed for the "GND" case, most likely due to the limited charge yield when ground bias is applied at the gate terminal [42], [44], [45].

The modest degradation of g_{m-MAX} is not dominant on the overall device performance but suggests possible activation of scattering centers, as interface traps, at the SiO_2/SiC interface when the devices are irradiated under the "ON" and "semi-ON" biases. The generation of interface traps under positive irradiation biases is also suggested by the modest increase of the subthreshold swing (ΔSS) with the accumulated dose. As reported in Fig. 5, "ON"- and "semi-ON"-biased devices show increases in the SS at doses >1 Mrad with worst degradation for "ON"-bias device, resulting in ΔSS of 82 mV/dec after 100 Mrad. In contrast, ΔSS for the "GND"- and "$-V_g$"-biased transistors is negligible as <10 mV/dec after 10 Mrad, consistent with the negligible (<1%) g_m variation reported in Fig. 4(c).

The influence of the bias condition on the SS and g_m was also observed in Si planar MOSFETs, where the electric field plays an important role in the direction of the transport of H^+ [46], [47], [48]. e.g., in the case of positive gate bias, typically used in n-channel MOSFETs, the H^+ drifts toward the oxide/channel interface, thus activating traps at the Si/SiO_2 interface [46], [49]. It is more likely that SiC power devices may also be affected by trap activation mechanisms related to

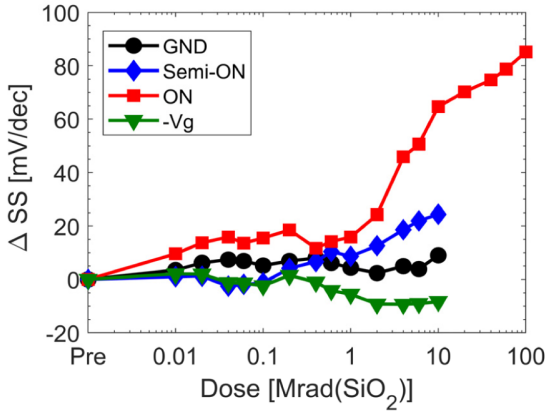

Fig. 5. Subthreshold swing variation ΔSS as a function of dose of SiC V-MOSFETs fabricated in the second-generation technologies. The devices were irradiated in several bias conditions.

H^+ and/or other contaminants moving into the oxide layers and at their interface. However, interface traps in SiC devices could have a different nature compared to the defects typical of Si MOS devices and it is challenging to determine their effects on wide bandgap materials since deep interface traps can potentially have fixed charged states. Anyway, it is worth noting that the variations in the SS are here almost negligible if compared to the overall V_{th} shift, clearly indicating that the dominant TID-induced effect is induced by the positive fixed charge trapped in the gate oxide.

B. CV Analysis for X-Ray Irradiations

The input capacitance measurements (C_{gg}–V_g) before the irradiation, after the exposure, and after the annealing are shown in Fig. 6(a) for the device with the highest TID degradation ["ON" condition, 100 Mrad(SiO_2)]. A rigid shift of the curve toward the left is observed after 100 Mrad due to the positive charge trapped in the gate oxide. Partial recovery is visible after 24 h of annealing at room temperature, indicating a decrease in the amount of the trapped charge, in agreement

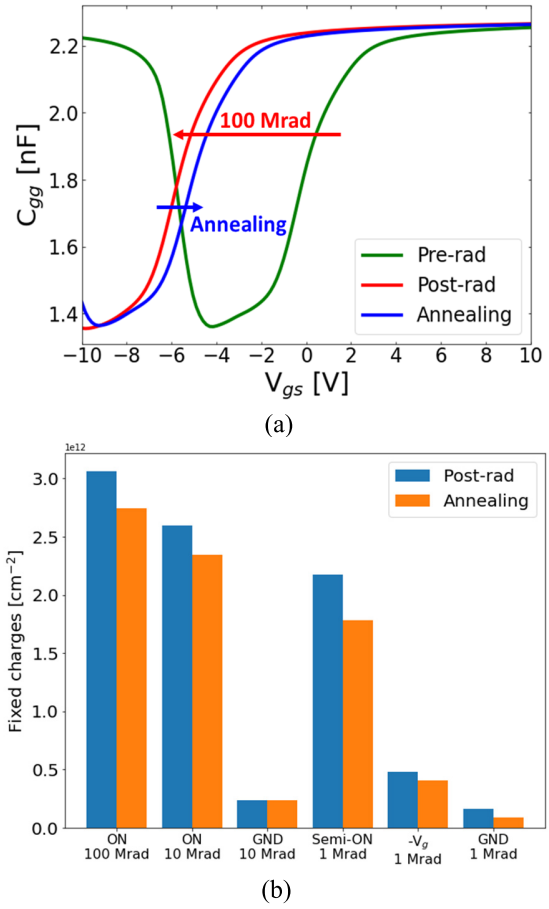

Fig. 6. (a) C_{gg}–V_{gs} before the irradiation, after the exposure at 100 Mrad(SiO_2) in "ON" state, and after the annealing. (b) Estimation of the oxide-trap density (N_{ot} [cm^{-2}]) before and after annealing for each condition of irradiation in second-generation SiC V-MOSFETs.

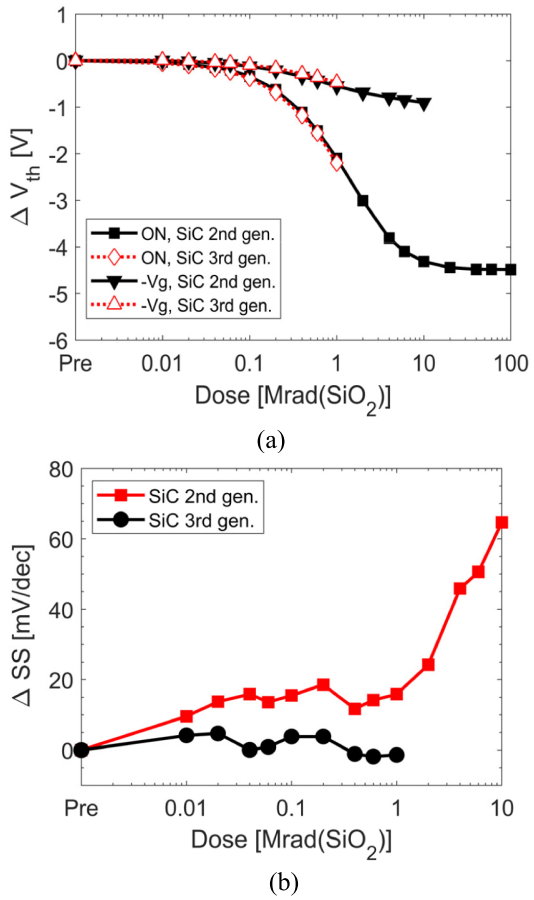

Fig. 7. Comparison for SiC V-MOSFETs fabricated in the second- and third-generation technologies of (a) threshold voltage shift ΔV_{th} for irradiations in "ON" and "$-V_g$" conditions and (b) subthreshold swing variation ΔSS in "ON" condition.

with the recovery in I_d–V_{gs} visible in Fig. 3(a). No stretch-out of the C–V curve is measured, indicating little or negligible changes in the interface trap density (D_{it}) [50]. In other words, the radiation leads to a rigid translation of the C–V curves. Fig. 6(b) shows an estimation of the oxide-trap densities (N_{ot}[cm^{-2}]) as a function of the different gate-bias conditions and doses. Two estimations are shown for each case: after the irradiation and after the annealing process. N_{ot} was calculated assuming a single charge per trap through the equation

$$N_{ot} = \frac{|\Delta V_{th}| E_{ox}}{q t_{ox}} \quad (1)$$

where q is the electron charge [C], ε_{ox} [F/cm] is the oxide permittivity, t_{ox} [cm] is the oxide thickness, and ΔV_{th} [V] is the threshold voltage shift extracted from the CV analysis.

C. Comparison of Second- and Third-Generation SiC Power V-MOSFETs

A comparison of the ΔV_{th} degradation as a function of dose in SiC V-MOSFETs fabricated in the second- and third-generation technologies for the "ON" and "OFF" conditions is shown in Fig. 7(a). The exact same ΔV_{th} degradation rate is observed for the two technologies up to 1 Mrad. Similarly, Fig. 7(b) shows the subthreshold swing variation for the "ON" bias conditions. A higher increase of ΔSS is observed on the second-generation devices already at low doses. Conversely, no variation of ΔSS is observed for the third-generation devices up to 1 Mrad, suggesting a higher tolerance of the SiC/SiO_2 interface. It is reasonable that the manufacturer has significantly improved the interface quality in the third generation of SiC devices by decreasing the number of active defects at the interface, thus limiting the impact of the interface traps during the X-ray exposure [33]. The combination of these results indicates that the dominant TID degradation is still related to positive charge trapping in the gate oxide in the two MOSFET generations and confirms the negligible contribution of D_{it} for the ΔV_{th} degradation.

IV. Experimental Results With 3-MeV Protons

A. TID and DD for the Second-Generation Devices

Fig. 8 shows the transfer characteristics (I_d–V_g) of SiC power MOSFET of the second generation irradiated with 3-MeV protons in "ON" condition. After 100 Mrad, the device exhibits significant drift in its working operational point, with a decrease of ~80% in the drain current at $V_{gs} = 9$ V. Finally, the annealing test at 100 °C does not allow the device to recover its performance, but it induces an even worse degradation of the ON-current by dropping of I_d of ~90% (at $V_{gs} = 9$ V).

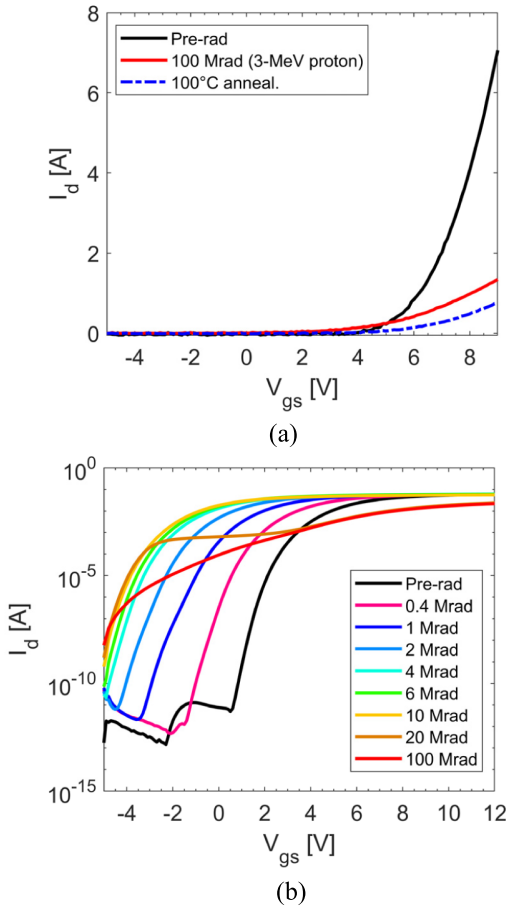

Fig. 8. I_d–V_{gs} curves of second-generation SiC V-MOSFETs in (a) saturation regime (V_{ds} = 5 V) and (b) linear regime (V_{ds} = 0.1 V). The devices were irradiated with 3-MeV protons up to 100 Mrad(SiO_2) in the "ON" condition and then annealed under bias (V_{gs} = 20 V and V_{ds} = 0 V) at room temperature and 100 °C for 24 h each.

Fig. 8(b) reports the I_d–V_g characteristic in the linear regime (V_{ds} = 0.1 V). With the exposures to 3-MeV protons, the curves shift toward negative values, indicating positive charge trapping in the gate oxide. The plot evidences large V_{th} shifts at doses <10 Mrad, and V_{th} substantially stabilizes at doses >10 Mrad, thus suggesting possible saturation of the positive charge trapping phenomena, similar to X-ray irradiations. However, another degradation effect arises in the I_d–V_{gs} of SiC devices when irradiated with protons at doses >20 Mrad. The effect is identified by a continuous drop of the drain current combined with a substantial change in the shape of I_d–V_{gs} in the regimes of channel depletion and inversion, i.e., at $V_{gs} > -2$ V.

This degradation effect was not visible during the X-ray exposure, as shown in Fig. 3(b). Thus, the difference in the damage induced by the X-rays and proton irradiations indicates the combination of two mechanisms when exposing the devices to 3-MeV protons. The first mechanism is induced by TID and dominates at doses <10 Mrad, causing positive charge trapping in the gate oxide, which is visible as negative shifts of V_{th}. The second mechanism is induced by DD and it is dominant at doses >10 Mrad, or equivalently to 6.72 × 10^{12} protons/cm^{-2} of 3-MeV protons, causing the degradation of the series resistance of the devices, most likely due to dislocated SiC atoms in the drift region of the vertical MOSFET (epilayer, substrate, and JFET regions of the device [33]). The generation of DD-induced defects leads to an increase of $R_{DS(on)}$ and, therefore, a reduction of I_{on} and g_m. It is worth noting that such DD effects were observed with 3-MeV protons and not observed in previous experiments performed with 200-MeV protons of 10^{11} cm^{-2} fluence on the same devices [51]. In addition to the higher fluence used in this work, the difference between 3- and 200-MeV proton degradation is also induced by the larger nonionizing energy loss (NIEL) of the 3-MeV protons used for our tests, which stops inside the drift region of the SiC devices (i.e., range of 53 μm in SiC) [52], [54].

Finally, no difference with respect to the pristine measurement was observed in I_g–V_g after 100 Mrad, indicating no sign of damage in the gate oxide (i.e., gate rupture).

B. Comparison of X-Rays and Proton Effects for the Second-Generation Devices

To investigate the nature of the effects visible with 3-MeV proton irradiation and to compare it with X-ray irradiations, Fig. 9 reports the degradation of the main MOSFET parameters when the devices are irradiated under the "ON"-bias condition. The degradation of I_{on} is calculated as the ratio of I_d at V_{gs} = 4.5 V and V_{ds} = 0.1 V normalized by its pristine value. The upper x-axis indicates the 3-MeV proton fluence, while the bottom x-axis indicates the TID equivalent fluence in SiO_2. As evidenced in (a), I_{on} for the proton irradiations increases with a much higher rate than X-ray irradiation, and it reaches a plateau at a fluence of ∼4 × 10^{12} cm^{-2}, equivalent to 6 Mrad. At fluences >6 × 10^{12} cm^{-2}, I_{on} starts to decrease abruptly due to the DD-induced effects. As shown in Fig. 9(b) and (c), the I_{on} variation visible at doses <10 Mrad is mostly caused by TID, with the negative shift of V_{th}, and a small contribution from the degradation of g_{m-MAX}. For higher proton fluences above ∼6 × 10^{12} cm^{-2}, DD dominates causing an increase of the ON-state resistance, and a drop of I_{on} and g_{m-MAX}. In the case of I_{on}, DD effects start to be visible at ∼10 Mrad, with intermediate effects at 15 Mrad and saturation over 20 Mrad. The DD effects are not observed during X-ray irradiation, where only TID degradation is induced by the 10-keV photons.

For the protons, ΔV_{th} was calculated from the I_d–V_{gs} curve using two different methods: 1) from g_{m-MAX}, as already described for the X-rays in Section III-A and2) in the subthreshold region as the gate-voltage shift at I_d = 10 nA. The two methods diverge in the V_{th} values at doses >10 Mrad, where the first method is not accurate in the extrapolation due to the large degradation induced by DD. Indeed, as shown in Fig. 9(c), a maximum ΔV_{th} of 0.4 V is measured with the first method at 100 Mrad versus −6.3 V retrieved from the second method, which indicates monotonic decreases of V_{th} induced by the trapping of positive charges in the gate oxide. Interestingly, ΔV_{th} for 3-MeV proton irradiations saturates at a higher level compared to X-ray irradiated devices, about −6 V versus −4.5. The highest saturation level of ΔV_{th} for 3-MeV proton irradiations suggests that 3-MeV proton exposures may induce the activation of higher densities of

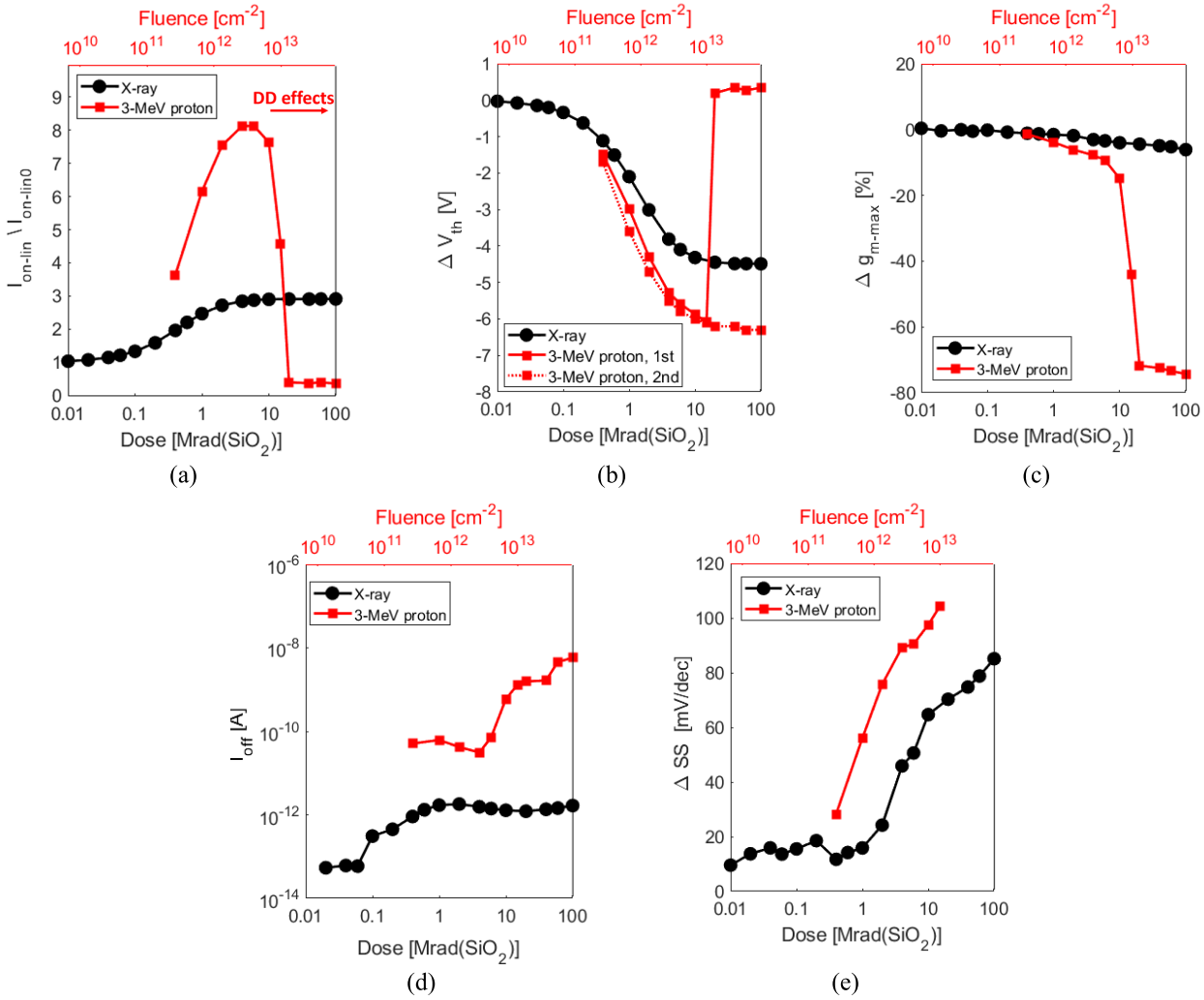

Fig. 9. Comparison of different parameters of second-generation SiC V-MOSFETs exposed to X-rays and protons in "ON" condition. Degradation of (a) maximum drain current in ON-state $\Delta I_{\mathrm{on-lin}}$, (b) threshold voltage ΔV_{th} calculated with two methods for the protons, (c) minimum drain current in OFF-state $\Delta I_{\mathrm{off-lin}}$, (d) maximum transconductance $\Delta g_{m-\mathrm{MAX}}$, and (e) subthreshold swing ΔSS as a function of dose and fluence in SiO_2. $I_{\mathrm{on-lin}}$ is defined as I_{d} at $V_{\mathrm{gs}} = 4.5$ V.

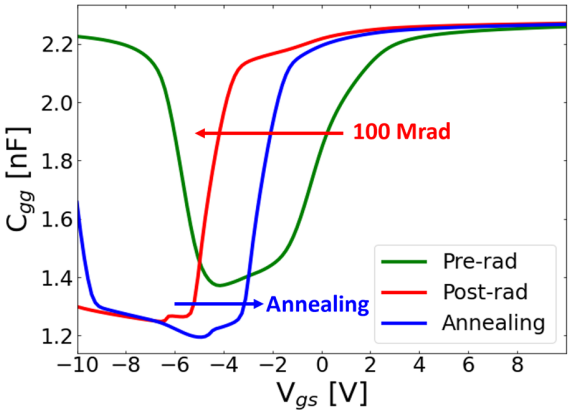

Fig. 10. C_{gg}–V_{gs} before the irradiation, after the exposure at 100 Mrad(SiO_2) in "ON" state, and after the annealing under bias ($V_{\mathrm{gs}} = 20$ V and $V_{\mathrm{ds}} = 0$ V) at room temperature and 100 °C for 24 h each for second-generation SiC V-MOSFET.

traps in the gate oxide. Indeed, it is worth noting that the highest V_{th} degradation with 3-MeV proton irradiations is not consistent with the higher charge yield of 3-MeV protons compared to one of 10-keV X-rays [55], [56].

The I_{off} degradation is shown in Fig. 9(d), where I_{off} is extracted as I_{d} at $V_{\mathrm{ds}} = 0.1$ V with $V_{\mathrm{gs}} = -5$ V, i.e., the minimum operational gate condition of the transistor. The increase of I_{off} during X-ray exposure is relatively modest, as I_{off} stays below 10^{-11} A after 100 Mrad. This is not the case for the proton irradiated samples, where I_{off} increases several orders of magnitude with a steeper increase for doses over 4 Mrad. At 100 Mrad, I_{off} is ~5 nA, losing the blocking capability in OFF-state due to the V_{th} shift of −6.3 V.

Similarly, as in the case of the X-rays, the initial degradation of $g_{m-\mathrm{MAX}}$ suggests the possible activation of interface traps at the SiO_2/SiC interface, in agreement with the increase of the subthreshold swing (ΔSS), visible in Fig. 9(e). A large increase up to 80 mV/dec is observed for doses up to 1 Mrad, with a decrease until 10 Mrad. In this region, TID effects dominate. The values for doses over 10 Mrad were not included, due to the combination of TID and DD, which complicates the methodology of extraction.

C. CV Analysis for Proton Irradiations

The input capacitance measurements (C_{gg}–V_{gs}) are shown in Fig. 10 for a SiC-MOSFET of the second generation irradiated with 3-MeV protons at 100 Mrad in the "ON"-bias condition. Three measurements are represented for the same device: before the irradiation, after the exposure, and after the annealing under bias ($V_{gs} = 20$ V and $V_{ds} = 0$ V) at room temperature and 100 °C. A shift of the curve toward the left is observed after 100 Mrad due to the positive charge generation in the gate oxide. However, the shift is not rigid as in the case of the X-rays [Fig. 6(a)], but a significant change in the C–V curve is measured, indicating modification of the interface trap density (D_{it}) distribution. Indeed, the C–V curves cannot be overlapped with a rigid V_g-shift.

After annealing, the curve shifts toward the right, indicating partial recovery in the amount of the trapped charge, consistent with the recovery in the I_d–V_{gs} visible in Fig. 8(a), alike the mechanism discussed for the X-rays. However, the $C-V$ curve does not recover the shape of pre-irradiation, suggesting the presence of D_{it} at the interface. A marginal change in the C–V shape is observed after annealing, which suggests a minimal recovery of D_{it} created during the irradiation.

V. Conclusion

SiC vertical power MOSFETs were irradiated for the first time at ultrahigh doses (100 Mrad), showing significant TID degradation, with magnitudes depending on the gate bias during the exposure. SiC MOSFETs irradiated with positive gate bias exhibit the highest negative threshold voltage shifts, due to the direction and intensity of the electric field in the gate oxide, which enhances the charge yield and favors the trapping of positive charges in the oxide. The lowest TID degradation is observed for "GND"-biased devices, due to the limited charge yield at low electric field in the gate oxide.

Similar negative threshold voltage shift is observed when comparing devices from the second and third generation exposed to X-rays, indicating similar positive charge trapping in the gate oxide. However, even if not dominant, the newer third generation of devices exhibits an almost negligible shift of the subthreshold swing, indicative of an improved SiO_2/SiC interface achieved in the most recent fabrication process.

Furthermore, the experiments with 3-MeV protons show a similar behavior to X-rays with charge trapping in the gate oxide at low doses, while a significant DD in the drift region is observed for higher doses and fluences. The defects created in the drift region lead to a severe increase of the ON-state resistance causing a reduction of I_{on} and g_m, thus degrading both the static and dynamic behavior of the power switch.

References

[1] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658–664, Apr. 2002.

[2] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[3] P. Godignon et al., "SiC Schottky diodes for harsh environment space applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2582–2590, Jul. 2011.

[4] J.-M. Lauenstein et al., "Space radiation effects on SiC power device reliability," in *Proc. IEEE Int. Reliab. Phys. Symp. (IRPS), Virtual Conf.*, Monterey, CA, USA, Mar. 2021, pp. 1–8.

[5] D. De, A. Castellazzi, S. Lopez-Arevalo, and A. Lamantia, "SiC MOSFET based avionic power supply," in *Proc. IET Conf. Publ.*, Apr. 2014, no. 628, pp. 1–6.

[6] D. Woog, M. J. Barnes, L. Ducimetière, J. Holma, and T. Kramer, "Design of an inductive adder for the FCC injection kicker pulse generator," *J. Phys., Conf. Ser.*, vol. 874, Jul. 2017, Art. no. 012096.

[7] A. Akturk, J. M. McGarrity, S. Potbhare, and N. Goldsman, "Radiation effects in commercial 1200 V 24 A silicon carbide power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 3258–3264, Dec. 2012.

[8] T. Ma et al., "TID degradation mechanisms in 16 nm bulk FinFETs irradiated to ultra-high doses," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 8, pp. 1571–1578, Aug. 2021.

[9] S. Bonaldo et al., "DC response, low-frequency noise, and TID-induced mechanisms in 16-nm FinFETs for high-energy physics experiments," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 1033, Jun. 2022, Art. no. 166727.

[10] J. M. Lauenstein, "Wide bandgap power-SiC, GaN-radiation reliability. NSREC 2020 short course," NASA Goddard Space Flight Center, Greenbelt, MD, USA, Tech. Rep., sec. 2, pp. 1–79, 2020.

[11] D. Hu, J. Zhang, Y. Jia, Y. Wu, L. Peng, and Y. Tang, "Impact of different gate biases on irradiation and annealing responses of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3719–3724, Sep. 2018.

[12] Y. Sun et al., "Investigation of total ionizing dose effects in 4H-SiC power MOSFET under gamma ray radiation," *Radiat. Phys. Chem.*, vol. 197, Aug. 2022, Art. no. 110219.

[13] T. Zhang, B. Allard, and J. Bi, "The synergetic effects of high temperature gate bias and total ionization dose on 1.2 kV SiC devices," *Microelectron. Rel.*, vols. 88–90, pp. 631–635, Sep. 2018.

[14] C. Abbate et al., "Radiation performance of new semiconductor power devices for the LHC experiment upgrades," in *Proc. 11th Int. Conf. Large Scale Appl. Radiat. Hardness Semicond. Detectors*, Jul. 2013, pp. 1–7.

[15] M. Shiozaki and T. Sato, "Characteristic degradation of power MOSFETs by X-ray irradiation and their recovery," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Dallas, TX, USA, Mar. 2022, pp. P64-1–P64-4.

[16] S. Bonaldo et al., "Total-ionizing-dose effects at ultrahigh doses in AlGaN/GaN HEMTs," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 8, pp. 2042–2050, Aug. 2023.

[17] F. Gao and W. J. Weber, "Atomic-scale simulation of 50 keV Si displacement cascades in β-SiC," *Phys. Rev. B, Condens. Matter*, vol. 63, no. 5, Dec. 2000, Art. no. 054101.

[18] T. Dalibor et al., "Radiation-induced defect centers in 4H silicon carbide," *Diamond Rel. Mater.*, vol. 6, no. 10, pp. 1333–1337, Aug. 1997.

[19] B. F. Phlips et al., "Silicon carbide PiN diodes as radiation detectors," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2005, vol. 3, no. 1596542, pp. 1236–1239.

[20] F. Nava, A. Castaldini, A. Cavallini, P. Errani, and V. Cindro, "Radiation detection properties of 4H-SiC Schottky diodes irradiated up to 10^{16} n/cm^2 by 1 MeV neutrons," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 5, pp. 2977–2982, Oct. 2006.

[21] A. A. Lebedev et al., "Effect of high energy (15 MeV) proton irradiation on vertical power 4H-SiC MOSFETs," *Semiconductor Sci. Technol.*, vol. 34, no. 4, Mar. 2019, Art. no. 045004.

[22] P. Hazdra and S. Popelka, "Displacement damage and total ionisation dose effects on 4H-SiC power devices," *IET Power Electron.*, vol. 12, no. 15, pp. 3910–3918, Dec. 2019.

[23] D.-S. Chao et al., "Influence of displacement damage induced by neutron irradiation on effective carrier density in 4H-SiC SBDs and MOSFETs," *Jpn. J. Appl. Phys.*, vol. 58, no. SB, Feb. 2019, Art. no. SBBD08.

[24] D. J. Lichtenwalner et al., "Reliability of SiC power devices against cosmic ray neutron single-event burnout," *Mater. Sci. Forum*, vol. 924, pp. 559–562, Jun. 2018.

[25] C. Martinella et al., "Impact of terrestrial neutrons on the reliability of SiC VD-MOSFET technologies," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 634–641, May 2021.

[26] D. R. Ball et al., "Ion-induced energy pulse mechanism for single-event burnout in high-voltage SiC power MOSFETs and junction barrier Schottky diodes," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 22–28, Jan. 2020.

[27] R. C. Germanicus et al., "Failure analysis of atmospheric neutron-induced single event burnout of a commercial SiC MOSFET," *Mater. Sci. Forum*, vol. 1062, pp. 544–548, May 2022.

[28] C. Abbate et al., "Gate damages induced in SiC power MOSFETs during heavy-ion irradiation—Part I," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4235–4242, Oct. 2019.

[29] N. Ikeda, S. Kuboyama, Y. Satoh, and T. Tamura, "Study of latent damage in power MOSFETs caused by heavy ion irradiation," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3388–3393, Dec. 2008.

[30] C. Martinella et al., "Heavy-ion induced single event effects and latent damages in SiC power MOSFETs," *Microelectron. Rel.*, vol. 128, Jan. 2022, Art. no. 114423.

[31] N. Fur, M. Belanche, C. Martinella, P. Kumar, M. E. Bathen, and U. Grossner, "Investigation of electrically active defects in SiC power diodes caused by heavy ion irradiation," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 8, pp. 1892–1899, Aug. 2023.

[32] C. Martinella, M. E. Bathen, A. Javanainen, and U. Grossner, "Heavy-ion-induced defects in degraded SiC power MOSFETs," *Mater. Sci. Forum*, vol. 1090, pp. 179–184, May 2023.

[33] S. Race et al., "Small-signal impedance and split C-V characterization of high-κ SiC power MOSFETs," *Mater. Sci. Forum*, vol. 1091, pp. 67–71, Jun. 2023.

[34] N. S. Saks, S. S. Mani, and A. K. Agarwal, "Interface trap profiles near the band edges in 6H-SiC MOSFETs," *Mater. Sci. Forum*, vols. 338–342, pp. 1113–1116, May 2000.

[35] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Appl. Phys. Rev.*, vol. 2, no. 2, Jun. 2015, Art. no. 021307.

[36] Univ. Jyväskylä. *ECIF Cocktail Calculator 0.2a*. Accessed: Dec. 30, 2023. [Online]. Available: http://research.jyu.fi/radef/ECIFcalc/dedx.html?save=

[37] R. Stark, A. Tsibizov, I. Kovacevic-Badstuebner, T. Ziemann, and U. Grossner, "Gate capacitance characterization of silicon carbide and silicon power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10572–10584, Sep. 2022.

[38] C. X. Zhang et al., "Effects of bias on the irradiation and annealing responses of 4H-SiC MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2925–2929, Dec. 2011.

[39] E. X. Zhang et al., "Bias-temperature instabilities in 4H-SiC metal–oxide–semiconductor capacitors," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 391–398, Jun. 2012.

[40] R. Arora et al., "Charge trapping properties of 3C- and 4H-SiC MOS capacitors with nitrided gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3185–3191, Dec. 2009.

[41] C.-M. Zhang et al., "Characterization of GigaRad total ionizing dose and annealing effects on 28-nm bulk MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 10, pp. 2639–2647, Oct. 2017.

[42] S. Bonaldo et al., "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1302–1311, Jul. 2020.

[43] F. Faccio et al., "Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2933–2940, Dec. 2015.

[44] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1706–1730, Jun. 2013.

[45] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for 10-keV X-ray and cobalt-60 irradiation of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 38, no. 6, pp. 1187–1194, Dec. 1991.

[46] D. M. Fleetwood, "Effects of hydrogen transport and reactions on microelectronics radiation response and reliability," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 523–541, May 2002.

[47] F. B. McLean, "A framework for understanding radiation-induced interface states in SiO_2 MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-27, no. 6, pp. 1651–1657, Dec. 1980.

[48] F. Faccio et al., "Influence of LDD spacers and H^+ transport on the total-ionizing-dose response of 65-nm MOSFETs irradiated to ultra-high doses," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 164–174, Jan. 2018.

[49] J. Ding et al., "Aging effects and latent interface-trap buildup in MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 12, pp. 2724–2735, Dec. 2021.

[50] L. Maresca et al., "Influence of the SiC/SiO_2 SiC MOSFET interface traps distribution on C-V measurements evaluated by TCAD simulations," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 2171–2179, Apr. 2021.

[51] C. Martinella, S. Race, R. Stark, R. G. Alia, A. Javanainen, and U. Grossner, "High-energy proton and atmospheric-neutron irradiations of SiC power MOSFETs: SEB study and impact on channel and drift resistances," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 8, pp. 1844–1851, Aug. 2023.

[52] S. R. Messenger et al., "NIEL for heavy ions: An analytical approach," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1919–1923, Dec. 2003.

[53] I. Jun et al., "Proton nonionizing energy loss (NIEL) for device applications," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1924–1928, Dec. 2003.

[54] S. Lazanu, I. Lazanu, E. Borchi, and M. Bruzzi, "Theoretical calculations of the primary defects induced by pions and protons in SiC," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 485, no. 3, pp. 768–773, Jun. 2002.

[55] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, Jun. 2003.

[56] P. Paillet et al., "Comparison of charge yield in MOS devices for different radiation sources," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2656–2661, Dec. 2002.