High-Energy Proton and Atmospheric-Neutron Irradiations of SiC Power MOSFETs: SEB Study and Impact on Channel and Drift Resistances

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***Abstract*— Accelerated single event burnout (SEB) tests with 200 MeV protons and atmospheric neutrons were performed for commercial silicon carbide (SiC) power MOSFETs with different architectures (i.e., planar gate, asymmetric trench, and symmetric trench). The average electric fields over the depletion layer width and the electric field distributions are reported for the tested conditions and compared for the three architectures, confirming the necessity of a lower de-rating for the trench design to protect from SEB, compared to planar ones. In addition to the epitaxial layer design, the influence of other design parameters on the SEB threshold is discussed. Finally, to investigate the presence of precursor damage in the pre-SEB region, a methodology is presented and used to study the radiation-induced degradation of the channel and drift resistances of devices that survived the SEB tests.**

***Index Terms*— Neutrons, protons, silicon carbide (SiC) power MOSFETs, single event burnout (SEB), split *C*–*V* measurements.**

I. Introduction

THE physical, electrical, and thermal material properties of silicon carbide (SiC) make this wide bandgap semiconductor attractive for power applications in space, avionics, and high-energy accelerators [1], [2], [3]. However, the high sensitivity of the current commercial technologies to heavy ions and low linear-energy-transfer (LET) particles prevents the adoption in these fields. For this reason, radiation tests on 4H-SiC power MOSFETs are performed to study the susceptibility to single event effects (SEE), such as single event burnout (SEB), [4], [5], [6], [7], [8], single event gate rupture (SEGR) [9] and single event leakage current (SELC) [10], [11], [12]. If the latter represents the main criticality for heavy-ion exposure, SEB and SEGR are the main effects observed for low LET particles, such as high-energy neutrons or protons. In fact, partial degradation of the device performance as in the case of the SELC effect has never been reported with protons and only in a few cases observed when testing with atmospheric neutrons [4].

In this work, SEB experiments have been performed with protons and atmospheric neutrons selecting commercial SiC power MOSFETs with different architectures. The electric fields averaged over the depletion layer width are reported for the tested conditions, together with the distribution of the electric field estimated with 1-D Technology Computer-Aided Design (TCAD) simulations. The epilayer design of the studied devices is discussed with respect to the SEB threshold. Furthermore, for devices that did not fail during the test and with the leakage currents within the datasheet requirements, additional measurements were carried out to identify any latent damage or precursor damage in the pre-SEB region. A methodology is presented to investigate the radiation-induced degradation of the channel (R_{ch}) and drift (R_{drift}) resistances.

A. SEB Mechanism in SiC Power Devices

The SEB mechanism has been the subject of debate during the last years, in particular, concerning the role of the parasitic bipolar transistor (BJT) [13]. On one side, there was the hypothesis that the conventional SEB mechanism observed in silicon MOSFETs, which involves the parasitic BJT and tunneling-assisted avalanche multiplication mechanism [14], was involved also in the SEB of SiC power MOSFETs. The role of the parasitic BJT was supported by numerical simulations [8], where avalanche breakdown coupled with a parasitic BJT in a positive feedback loop, was suggested as the reason for the simulated runaway drain current. Parasitic BJT charge amplification was also experimentally demonstrated by laser studies performed on MOSFETs and JBS diodes with the same epi-layer properties [15]. Furthermore, studies of short-circuit ruggedness suggested that the BJT can be turned on and trigger a thermal runaway [16].

On the other hand, experimental data collected during both heavy-ion and neutron irradiations showed that there exists no consistent difference in SEB tolerance between SiC diodes and SiC MOSFETs, leading to the conclusion that the parasitic BJT is not involved in the SEB failure mechanism, since there is no BJT structure in diodes [17], [18], [19], [20].

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TABLE I
LIST OF DUTs

DUT	Reference	$V_{DS(on)}$ [kV]	$R_{DS(on)}$ [mΩ]	$I_{D\ @\ 25}$ [A]	V_{BR} [V]	Gate	Ratio cell pitch	Channel direction
A	C2M0025120D	1.2	25	63	1720	planar	1	Horizontal
B	IMW120R090M1H	1.2	90	26	1483	asymmetrical trench	0.34	Single vertical
C	SCT3030KL	1.2	30	72	1926	symmetrical trench	0.65	Double vertical
D	C2M0080120D	1.2	80	36	1650	planar	0.98	Horizontal

Furthermore, compared to a Si MOSFET, the parasitic BJT in SiC MOSFETs requires higher voltage to switch on (i.e., the base–emitter forward voltage drop is higher in SiC), having also a significantly lower gain due to the high doping levels in the p-body [13]. This hypothesis was supported by numerical simulations of an ion strike in a SiC MOSFET [20] and in a SiC diode [21] structure that eliminated the n+ source diffusion region from the MOSFET, showing no significant difference in current and lattice temperature when the n+ region is included or not. In both cases, the simulated temperature eventually reaches the sublimation temperature of SiC.

The discrepancy between the two hypotheses concerning the role of the parasitic BJT was explained by additional experimental work and simulations [7], [22], [23]. By inserting high resistivity between the high potential node and the power supply of MOSFETs and JBS diodes it was attempted to suppress the SEB event [22], [23]. However, in both cases, the presence of the resistor had no impact, finding similar SEB thresholds. As the resistor was not providing protection from the SEB, it was concluded that the SEB event was happening at time scales on the order of ps and not on the order of ns or μs, therefore, before the parasitic BJT can contribute significantly to the MOSFET response [7]. This explained the similarity of SiC MOSFETs and diodes tolerance to SEB and degradation experimentally measured. Furthermore, the same time scale was identified in the SEB mechanism proposed for SiC Schottky diodes in [24]. By performing 3-D TCAD simulations of a 1.2 kV SiC MOSFET and a 1.2 kV JBS diode, Ball et al. [7] showed that for approximately 100 ps after the ion strike occurs, the current transients behave identically in both structures, while after that they begin to deviate. The redistribution of the electric field induced by the energy dissipation in the first 10 ps was shown to reach peaks at the body/drain junction and at the epi/substrate interface, with the latter resulting in a critical electric field to induce avalanche breakdown.

Furthermore, it was demonstrated that a thicker and more lightly doped epitaxial layer increases the SEB threshold in SiC JBS diodes and SiC MOSFETs with a planar gate architecture [25].

B. Devices Under Test

In this work, several references were selected from the commercially available SiC VD-MOSFET technologies as devices under test (DUTs) for the proton and neutron SEB experiments, as listed in Table I. The DUT A and D have a planar gate structure, the DUT B has an asymmetrical trench gate structure [26], whereas the DUT C has a symmetrical trench design. The three architectures are shown in Fig. 1. For the planar-gate architecture the channel is formed horizontally, as in Fig. 1(a). Differently, the channel is formed vertically in trench devices. A single channel is formed in the asymmetric trench structure as for DUT B shown in Fig. 1(b), whereas a double channel is formed in DUT C shown in Fig. 1(c). All the devices are mounted in a TO-247 package. The breakdown voltage (V_{BR}) is also reported in Table I for the four DUTs, defined as the drain–source bias (V_{DS}) at which the drain leakage current (I_D) is 1 mA at gate–source bias (V_{GS}) equal to 0 V. Namely, DUT C shows the highest V_{BR}(160% of the rated V_{DS}) and DUT B the lowest (123%). The devices were selected with similar values of nominal ON-resistance $R_{DS(ON)}$, DUT A and C with 25 and 30 mΩ, and DUT B and D with 90 and 80 mΩ, respectively. Last, the selected DUTs differ for other technological parameters in addition to the gate architecture, such as the drift layer doping and thickness and the cell pitch, i.e., the lateral size of a single MOSFET cell reported in Table I.

II. PROTON EXPERIMENT

A. Proton Irradiation

The test campaign with high-energy protons was performed at the proton irradiation facility (PIF) at the Paul Scherrer Institute (PSI), Switzerland. The objective of the experiment was to identify the maximum V_{DS} at which no SEB are observed reaching a target fluence of 10^{11} protons/cm^2. By the primary energy degrader, the beam energy can be set between 230 and 74 MeV. For this experiment, the beam was selected with an energy of 200 MeV and a flatness area of 5 cm diameter (φ), with an uncertainty of 10%. The experimental board hosted 12 DUTs aligned in four rows. During the irradiation, the devices were biased in parallel, while monitoring the sum of all the

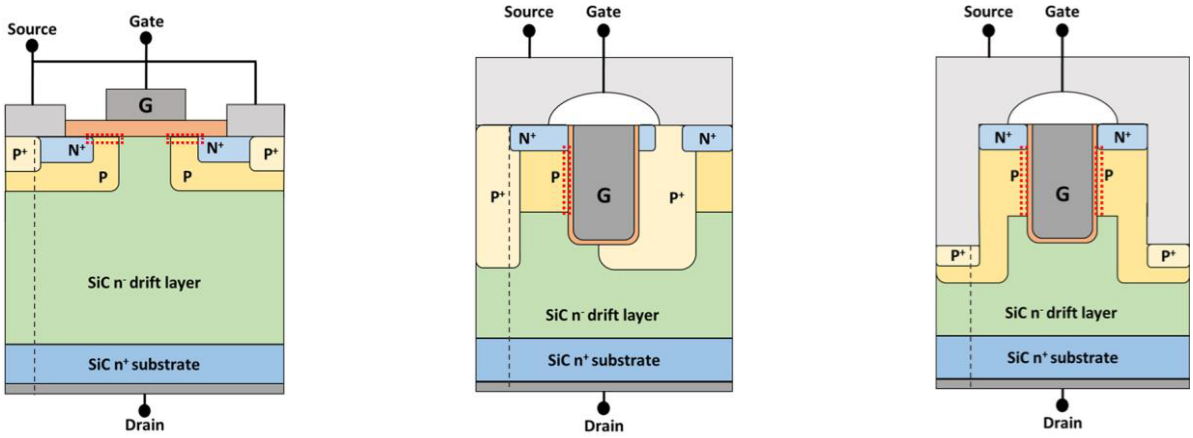

Fig. 1. Schematic layout of (a) DUT A and D, (b) DUT B, and (c) DUT C. The channels are highlighted with red dashed lines whereas the black dashed lines represent the cutlines used for the numerical simulations discussed in Section II-C.

I_{DS}, whereas the gate and source were directly grounded on the board. A limiting resistor was placed between the drain of each DUT and the SMU, to limit the leakage current in case of SEB failure. Decoupling capacitors were installed on the board used for the proton experiment, in order to filter out voltage spikes and pass through only the dc component of the signal. During both experiments, the DUTs were exposed having a constant $V_{DS} \neq 0$ V and $V_{GS} = 0$ V. If a SEB was observed during the exposure, another series of pristine DUTs was selected and the V_{DS} was lowered by 50 V for the new run. For all the runs the devices were irradiated at the normal incidence of the beam with respect to the DUTs surface.

B. SEB Results

The safe operating area at which no failure was identified for the proton irradiations with a fluence of 10^{11} protons/cm^2 (max $V_{DS} \neq 0$ V and $V_{GS} = 0$ V) are listed in Table II. The percentages with respect to the V_{BR} and the rated voltage (1.2 kV) are indicated in brackets. The number of devices that survived the specific voltage is indicated in the fourth column. The fifth column indicates the electric field averaged over the depletion layer width (E_{av}) for the tested conditions, which was identified as the critical factor for failure for both Si and SiC power devices, instead of the maximum electric field [27], [28]. The sixth column indicates the difference in the average electric field for different V_{DS} conditions. For DUT B, both values are calculated with respect to the maximum V_{DS} condition.

Trench devices show higher tolerance to SEB with respect to the planar reference for irradiations at normal incidence. For example, the safe operating area identified for DUT B (i.e., $V_{DS} = 670$ V, $E = 63.20 \times 10^4$ V/cm) indicates a similar average electric field with respect to the trench DUT C (i.e., $V_{DS} = 850$ V, $E = 64.28$ V/m), slightly higher with respect to the planar DUT D (i.e., $V_{DS} = 600$ V, $E = 60.0 \times 10^4$ V/cm) and much higher with respect to the planar DUT A (i.e., $V_{DS} = 600$ V, $E = 47.61 \times 10^4$ V/cm).

C. Numerical Simulations

Numerical simulations have been performed to investigate the electric field distribution for the four devices considering the conditions used during the test, as reported in Table II. The electric field in the structure is evaluated under the 1-D assumption in correspondence with the p-n junction between the P-well and the N-epi-layer, i.e., along the vertical cutlines shown in Fig. 1. Technical information was used to design the epilayer of the three architectures, whereas the epi-dopings were obtained from V_{BR} measurements. The P-well doping profile was assumed Gaussian and common to all the DUTs. Fig. 2(a) shows the electric field distribution along the p-well and the epilayer thickness for the four devices at the bias conditions associated with a high probability of observing SEB events (more than 50% as in Table II). The peak of the electric field and more generally the electric field distribution along the epilayer thickness is higher for the trench devices, with DUT B having the highest peak electric field, despite having the shortest epilayer thickness. A zoom over the peaks region is shown in Fig. 2(b). In this case, a second condition associated with a low probability of observing SEB (less than 50% as in Table II) is simulated for each device and reported in a dashed line. It can be observed how the dashed line in green associated with zero probability of SEB for DUT B (based on the test of 15 devices) allows a peak of the electric field higher with respect to all the other devices, for both critical and non-critical conditions.

III. Atmospheric Neutron Experiment

A. Atmospheric-Neutron Irradiation

The irradiations with atmospheric neutrons were carried out at the ChipIr beamline at the Rutherford Appleton Laboratory, U.K. [29]. The beamline design is optimized to mimic the atmospheric neutron spectrum (up to 800 MeV) with an acceleration factor of up to 10^9. The flux of neutrons above 10 MeV at the testing position is 5.6×10^6 n/cm^{-2}s^{-1}. Accelerated SEB tests were performed exposing DUT A and B at 92%, 81%, and 72% of the maximum rated voltage (i.e., 1100, 976, and 846 V) and to a maximum fluence of 2.8×10^{10} n/cm^2.

TABLE II
RESULTS FROM PROTON IRRADIATIONS AT 200 MeV

DUT	Reference	V_{DS} (% V_{BR}) (% 1.2 kV) [V]	Survived/total	E_{av}[V/cm]	ΔE_{av}[V/cm]
A	C2M0025120D	650 (37.7%) (54.1%)	0/5	51.58×10^4	3.96×10^4
		600 (34.8%) (50.0%)	15/15	47.61×10^4	
B	IMW120R090M1H	700 (47.2%) (58.3%)	2/5	66.03×10^4	2.83×10^4
		670 (45.1%) (55.8%)	5/5	63.20×10^4	
		650 (43.8%) (54.1%)	15/15	61.32×10^4	4.71×10^4
C	SCT3030KL	940 (48.8%) (78.3%)	0/5	67.14×10^4	2.86×10^4
		900 (46.7%) (75.0%)	7/15	64.28×10^4	
D	C2M0080120D	620 (37.5%) (51.6%)	0/5	62.0×10^4	2×10^4
		600 (36.3%) (50.0%)	14/15	60.0×10^4	

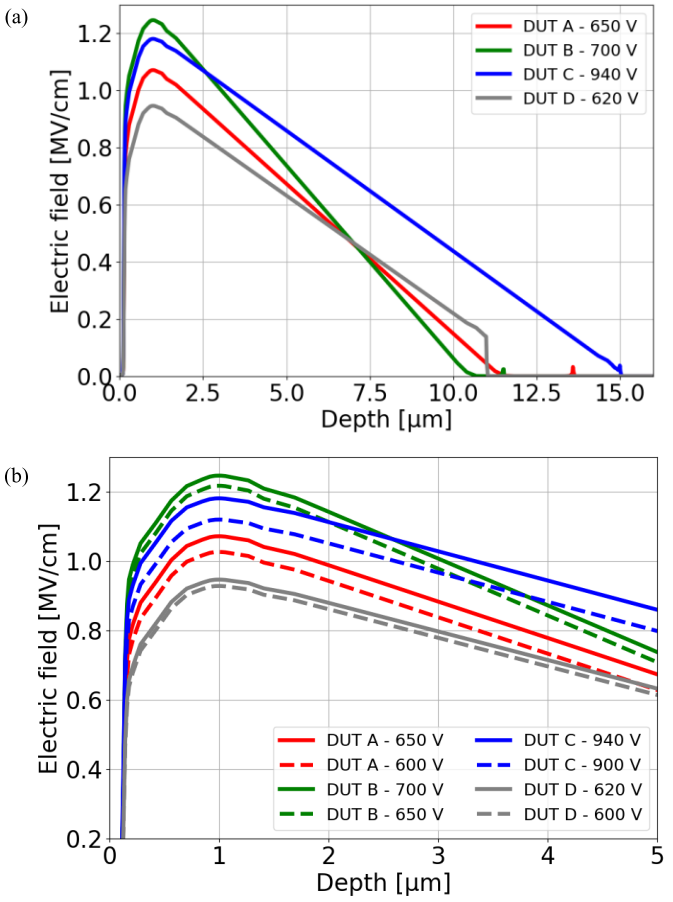

Fig. 2. (a) Estimated electric field distribution at the conditions of tests reported in Table II for DUT A–D. (b) Electric field peaks for critical and non-critical conditions for DUT A–D as reported in Table II.

DUT C was tested only at 92%, 81% of the maximum rated voltage, whereas DUT D was not included in this experiment. The details of the experimental setup and methodology were previously described in [4]. In this case, two experimental boards were used with 12 devices each biased in parallel. As in the case of the proton experiment, for each device a limiting resistor was installed between the DUT and the source measure unit, to limit the current in case of an SEB event.

B. SEB Results

The full analysis of the neutron results was previously presented in [4], together with the calculations of cross sections, failure in time (FIT) rates, and analysis of the post-irradiation-gate-stress (PIGS) test. To calculate the SEB cross sections and the FIT rates, a two-parameter Weibull distribution was fit to the data using a maximum likelihood estimation (MLE) method. The FIT rates normalized by the active area and scaled for the breakdown voltage of the devices are reported in Fig. 3. Each point is calculated considering a statistic of 24 devices. The FIT rates confirm the trend observed with high-energy protons, with higher robustness of the trench architectures (DUT B and DUT C represented in green and blue, respectively) with respect to the planar one (DUT A represented in red).

IV. POST IRRADIATION ANALYSIS

A. Analysis of Leakage Current

The leakage current analysis is used to characterize the electrical characteristics of the devices after irradiation by measuring I_{gss} and I_{dss} and comparing them with the datasheet limits.

From the post-irradiation analysis of devices tested with atmospheric neutrons, three different effects were identified:

1) No SEB, no differences in blocking capability with respect to a pristine device, and leakage currents in the datasheet limits.
2) No SEB but partial degradation of the device, which exhibited I_{gss} and I_{dss} orders of magnitude higher with respect to the pristine level.

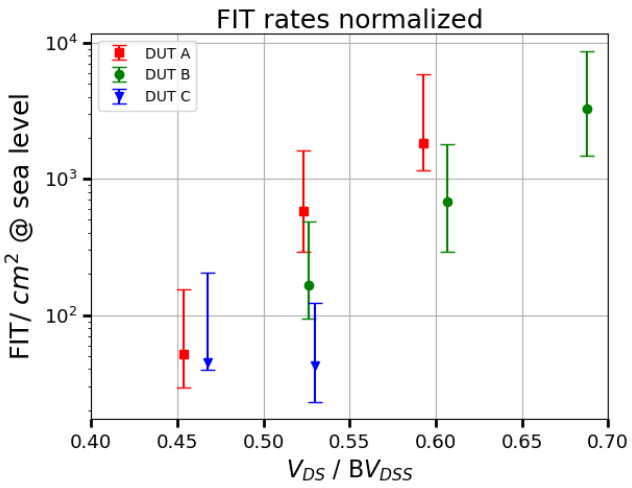

Fig. 3. FIT rates scaled by avalanche voltage and normalized with the active area. Dataset from [4]. Copyright 2021, Martinella et al., licensed under CC BY 4.0.

3) Ohmic trend of I_D caused by destructive SEB during the exposure.

Leakage currents measurements (i.e., I_D, I_G, and I_S) are reported in [4] as a function of the V_{DS} and compared with pristine values for the three references. In this work, additional analysis is carried out for the devices irradiated at 72% of the maximum rated voltage, which showed no differences with respect to a pristine device [i.e., scenario 1)].

For the devices tested with 200 MeV protons instead, only the effects described in 1) and 2) were observed and no partially degraded devices were measured, regardless of the device architecture.

B. Methodology to Calculate R_{drift} and R_{ch}

The methodology used to differentiate the contributions of R_{ch} and R_{drift} to the total $R_{DS(ON)}$ of a SiC vertical power MOSFET follows the approach discussed by Stark et al. in [30]. This characterization approach is here adopted to analyze the ON-state behavior of the MOSFETs, allowing clear identification of any possible precursor of damage in the channel or drift region. In fact, it is not straightforward to conclude from the leakage analysis that there is no degradation of conduction performance. Furthermore, the proposed technique can in general reveal important features of the devices, otherwise not accessible (i.e., R_{ch} and R_{drift} contributions, channel quality, and temperature dependence of the two resistive components).

The devices irradiated with neutrons and protons were analyzed to identify the DUTs which did not fail during the irradiation and had leakage currents in agreement with the specifications in the datasheets. DUT A was considered representative of the planar architecture, whereas DUT D was excluded from this analysis. Successively, $R_{DS(ON)}$ and C–V measurements were performed and used to extract the R_{ch} and R_{drift} contributions. For the devices tested with protons, the measurements were carried out also before the irradiation, to have a full comparison and to remove the effect of the part-to-part variation.

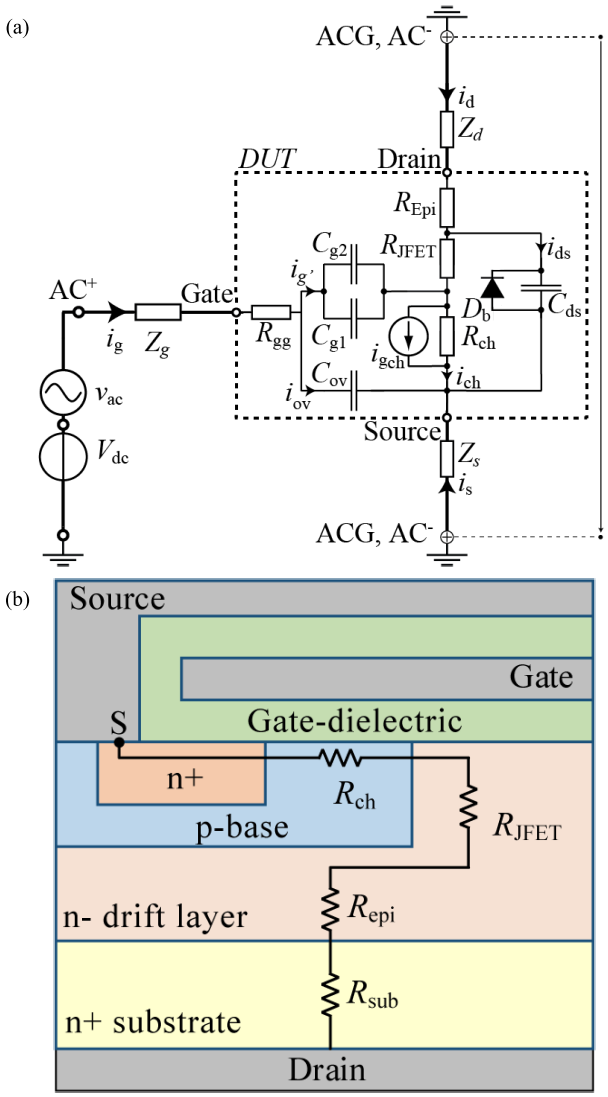

Fig. 4. (a) Small signal equivalent circuit of a power MOSFET in ON-state. ac+, ac−, and ACG represent the connection of the impedance analyzer to the power MOSFET for the measurement of C_{gg}, C_{sg}, and C_{dg}. In this model, C_{g1} and C_{g2} are the contributions of the channel and JFET regions over the total gate capacitance. (b) Simplified schematic of the planar-gate MOSFET resistances.

The methodology follows the explanation discussed in [30]. Starting from the small-signal equivalent circuit presented in Fig. 4(a), by solving Kirchhoff's system of equations a relationship can be derived for the gate–source (C_{SG}) and gate–drain (C_{DG}) capacitances. Following the demonstration presented in [30], it can be shown that

$$\frac{C_{DG}}{(C_{SG} - C_{OV})} \cong \frac{R_{ch}}{R_{drift}}$$

where

$$R_{drift} = R_{JFET} + R_{epi} + R_{substrate}. \quad (1)$$

The model is based on the following assumptions [30], [31]:

1) $C_{OV} \cong \min(C_{SG})$, where C_{OV} is the overlap capacitance between the gate and the source contacts.
2) Z_s, $Z_d \ll R_{ch}$, R_{drift}, meaning that the influence of Z_s and Z_d which are the impedances of the package and

the measurement setup at the source and drain side can be neglected with respect to the internal resistances.

3) $V_{GS} \gg V_{th}$, therefore the channel is well formed.
4) The channel transconductance $g_{ch} \approx 0$ for $V_{DS} \approx 0$.

A schematic of the different contributions to the total $R_{DS(ON)}$ for a planar structure is shown in Fig. 4(b). The model can be used also for trench architecture.

The C–V measurements were performed at room temperature using a Keysight E4990A impedance analyzer based on an auto-balancing bridge measurement technique which eliminates the influence of the ampere meter on the measured current [32]. The test fixture Keysight 16047E was used to mount the DUTs. The gate–source (C_{SG}) and gate–drain (C_{DG}) capacitances were measured at a frequency of 100 kHz having $V_{GS} = [-10 : +20$ V] for the planar devices and $V_{GS} = [-20 : +20$ V] for the trench ones. The $R_{DS(ON)}$ values were calculated from the $I_D V_{GS}$ measurement at $V_{GS} = [12 : +20$ V] and $V_{DS} = 50$ mV. The $I_D V_{GS}$ measurements were performed at room temperature using a Keithley Parametric Curve Tracer PCT-4B.

C. Results From R_{ch} and R_{drift} Calculations

Fig. 5(a)–(c) shows the calculation of $R_{DS(ON)}$, R_{ch}, and R_{drift} for the three different references before and after the irradiation with 200 MeV protons (testing conditions for DUT A: $V_{DS} = 600$ V, DUT B: $V_{DS} = 650$ V, DUT C: $V_{DS} = 900$ V). The $R_{DS(ON)}$ values for the pristine devices listed in Table II and reported in the datasheet are observed at $V_{GS} = 20$ V in Fig. 4(a) (i.e., 25 mΩ) and $V_{GS} = 18$ V in Fig. 4(b) and (c) (i.e., 90 and 30 mΩ, respectively). Comparing the devices measured before and after the irradiation, no impact is observed on R_{DS}, R_{ch}, and R_{drift} for the irradiated DUTs, meaning that no influence is observed in the channel regions or the drift layer due to irradiation. The differences observed among the different devices are due to the part-to-part variation. The same results are observed for the devices tested with neutrons but are not included for brevity.

Fig. 6(a)–(c) shows the R_{ch}/R_{drift} ratio for pristine devices and devices irradiated with protons and neutrons. For all three architectures, the R_{ch}/R_{drift} ratio is dominated by the part-to-part variation, as highlighted by the differences among pristine values and which can be significant for SiC MOSFETs as shown in [31].

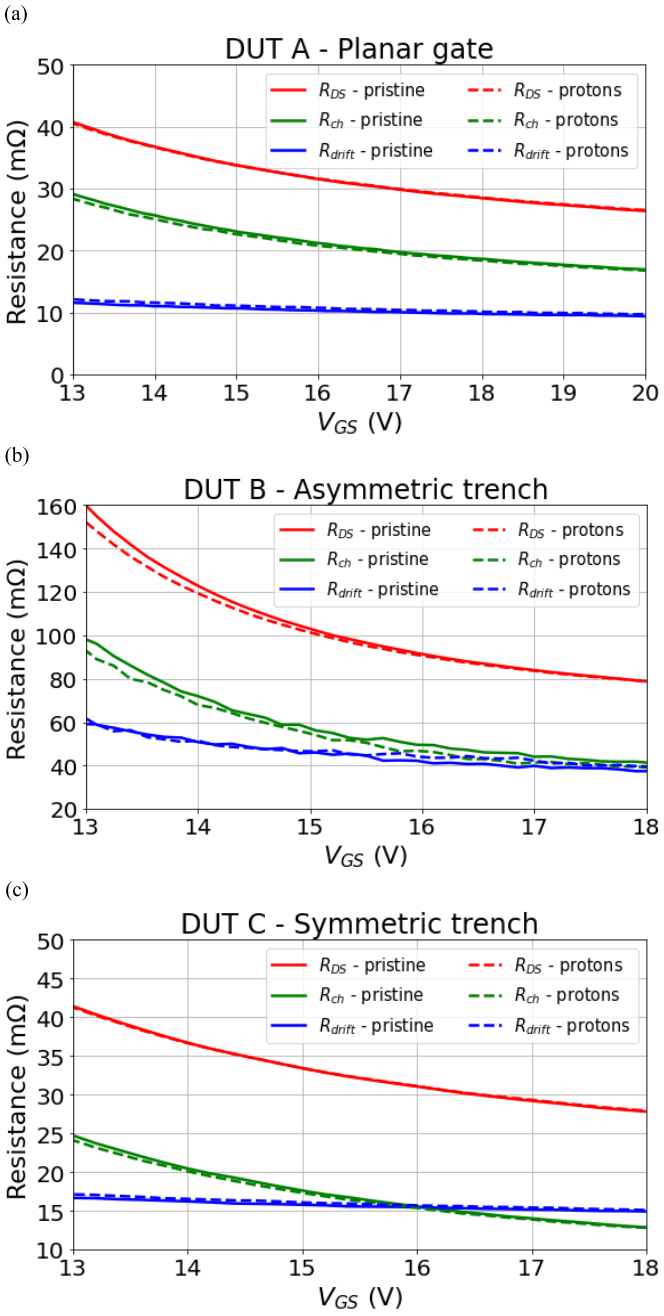

Fig. 5. Calculated R_{ch} and R_{drift} contributions over the total $R_{DS(ON)}$ for (a) planar-gate, (b) asymmetrical trench-gate, and (c) symmetrical trench DUTs before and after irradiations with 200 MeV protons. Different y-axes are used to better highlight the data.

V. Discussion

From the safe operating areas identified from the high-energy proton tests and the FIT rates obtained from the atmospheric-neutron experiment, higher robustness of the trench devices is observed with respect to the planar architecture. The electric fields averaged over the depletion layer width for the tested conditions, confirmed the possibility of a lower de-rating for the trench design to protect from SEB (∼45%–46% of the V_{BR} for DUTs B and C) with respect to the planar devices (∼34% of the V_{BR} for DUTs A and D), as in Table II. For DUT C this result confirms the discussion in [25], indicating that a thicker and more lightly doped epitaxial layer significantly increases the SEB threshold. Conversely, DUT B has the thinnest epilayer among the four devices studied in this work. Despite that, the architecture of DUT B shows the highest robustness for a non-critical condition not only in terms of the electric field averaged over the depletion layer width but also with respect to the maximum of the electric field, as obtained from the numerical simulations. This result points to the fact that there might be other contributions influencing the SEB threshold in addition to the epitaxial layer design (thickness and doping) as discussed in [25], such as for example the gate architecture and the cell pitch. Additional analysis should be carried out including different

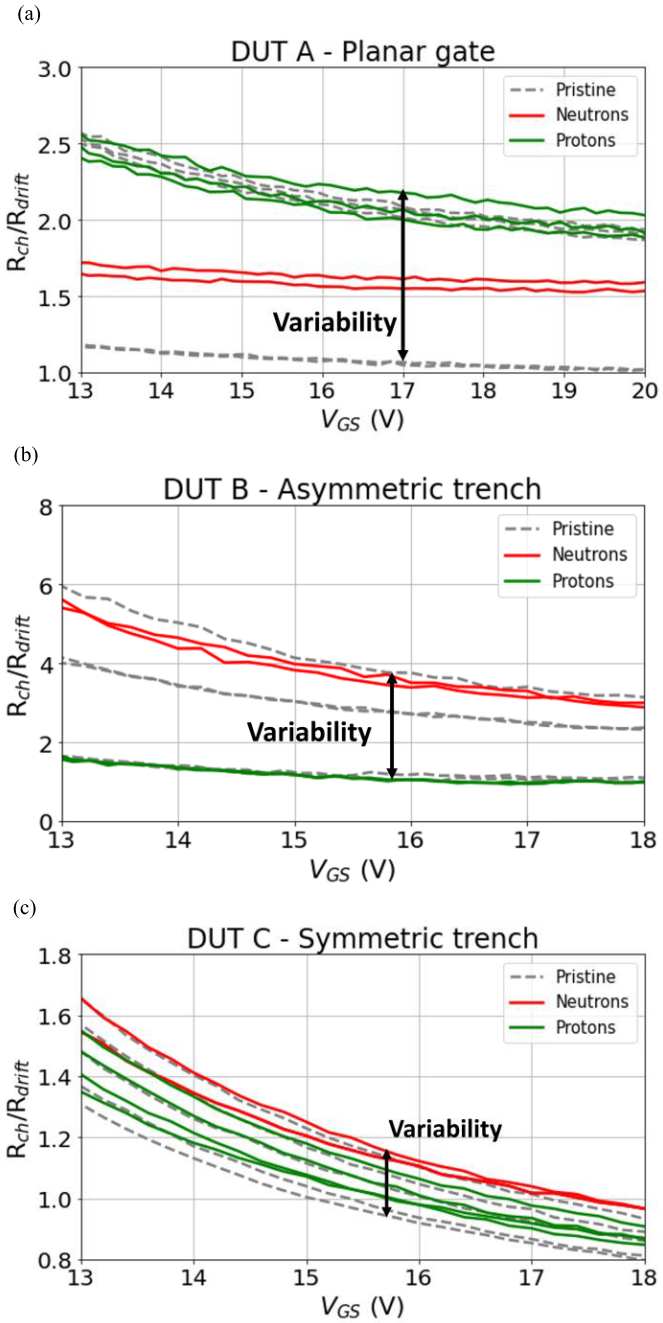

Fig. 6. Ratio R_{ch}/R_{drift} for pristine and irradiated devices with (a) planar-gate, (b) asymmetrical trench-gate, and (c) symmetrical trench DUTs. Pristine devices are represented in gray. The devices tested with atmospheric neutrons and 200 MeV protons are represented in red and green, respectively. Different y-axes are used to better highlight the data.

design parameters and addressing the influence of the angle of irradiation for the different architectures.

However, with the rated voltage typically being the only parameter available from the datasheet, the robustness of the devices is usually compared in terms of de-rating with respect to the rated voltage instead of the V_{BR}. This way of comparison would identify DUT C as the design with the highest robustness from SEB (75% of 1.2 kV) due to the overdesign of the epi. However, such a design solution compromises the electrical performance of the device (i.e., higher $R_{DS(ON)} \times A$ figure of merit). Therefore, a fair comparison among technologies should include both the analysis, with respect to the V_{BR} and the rated voltage.

Furthermore, from the R_{ch} and R_{drift} calculations, no increase in R_{drift} was observed in this study. In contrast, in the case of irradiation with higher-LET particles, signatures of bipolar degradation are observed in the pre-SEB region, both electrically and when investigating the material properties and radiation-induced defects in the device, indicating the presence of stacking defects [33], [34]. Such defects are known to cause an increase in the ON-resistance of the MOSFET and forward voltage of the body-diode [35].

Therefore, regardless of the device architecture and channel direction, no sign of bipolar degradation or body diode degradation is observed in the pre-SEB region for devices exposed to low-LET particles at normal incidence. The degradation mode observed here is caused by the energy released during the recombination of electron-hole pairs caused by excess carriers generated during the ion impact.

VI. Conclusion

Commercial SiC power MOSFETs with planar and trench architectures were irradiated with atmospheric neutrons and protons. The SEB analysis confirmed the higher tolerance of trench SiC power MOSFETs exposed to low LET particles, as observed from the safe operating area for 200 MeV protons and from the FIT rates calculated with atmospheric neutrons. The electric fields averaged over the depletion layer width were reported for the tested conditions, together with the distribution of the electric field along the epilayer thickness, confirming the necessity of a lower de-rating for the trench design in order to protect from SEB.

However, before extending the results to other references from the same or different manufacturers, an additional analysis should be carried out including the influence of other different design parameters among the three architectures and addressing the influence of the angle chosen for irradiation with respect to the channel direction.

Furthermore, in order to investigate the presence of precursor damage in the pre-SEB region, a methodology was presented to differentiate the contributions of R_{ch} and R_{drift} over the total $R_{DS(ON)}$ and used to analyze the impact of radiation on devices that did not fail with SEB during the exposure. Regardless of the device architecture, no radiation-induced damage is observed in the channel and drift regions, meaning that there is no sign of bipolar degradation in the pre-SEB region. This result highlights a different mechanism of damage for high-energy protons and atmospheric neutrons with respect to that observed with higher-LET particles.

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