Neutron-Irradiation Testing of FPGA-Embedded Hadron Fluence Sensors

R. Giordano, G. Tortone, D. Vincenzi, F. Loffredo, M. Quarto, R. Pestotnik, A. Lozar, and A. Seljak

***Abstract*— Hadron fluence monitors based on static random access memories (SRAMs) are being used at CERN and have been proposed for proton therapy facilities. Some of the limitations of the state of the art are related to the usage of separate components for sensing upsets and for reading them out, as these increase the power consumption, the board complexity, and its size. Moreover, in some cases, due to radiation-tolerance requirements, the readout logic (ROL) is fixed, and it cannot be updated once the system has been implemented. In this work, we show how to overcome the mentioned limitations by using an SRAM-based field programmable gate array (FPGA) for implementing both the sensitive element [the configuration SRAM (CRAM)] and the ROL (the firmware in the fabric). In fact, we describe the implementation of a compact, reprogrammable, low-power, actively self-reading hadron fluence sensor realized by means of a Xilinx Artix-7 FPGA. Moreover, we present the customized radiation-hardening-by-design (RHBD) techniques adopted for the ROL. We irradiated two sensor prototypes at the Jožef Stefan Institute's TRIGA Mark II research reactor, under different neutron spectra and flux conditions. We discuss our results, which include the measurements of the radiation tolerance, the single event upset (SEU) cross section of the CRAM, the sensitivity to thermal neutrons, and the failure cross section of the ROL.**

***Index Terms*— Field programmable gate array (FPGA), hadron fluence sensors, multiple bit upsets, neutrons, radiation hardening by design (RHBD), single event effects, single event upsets (SEUs), soft errors.**

I. Introduction

HADRONS may cause single event upsets (SEUs) in static random access memories (SRAMs) through indirect ionization. The hadron fluence (ϕ) is proportional to the upset count (N_{upsets}), through the equation

$$\phi = \frac{\mathrm{N_{upsets}}}{\sigma \mathrm{N_{bits}}} \tag{1}$$

where σ is the device cross section per bit and N_{bits} is the memory size in bits. The cross section depends on the device, technology, power supply voltage, type of hadrons, and their kinetic energy and must be measured by means of irradiation tests [1]. SRAM-based hadron fluence sensors are in use at CERN [2], [3], [4] and have been proposed for proton therapy applications [5].

In order to read the response from SRAMs, some radiation-tolerant readout electronics is needed. Over the last few years, flash-based field programmable gate arrays (FPGAs) have been considered for SRAM readout at CERN [6] and actually used in proton therapy [7]. A shortcoming of state-of-the-art solutions is that they require separate components for sensing upsets and for reading them out, increasing the power consumption, the board complexity, and its size. Moreover, if high total ionizing dose (TID) tolerances are needed, flash-based FPGAs cannot be used [8].

SRAM-based FPGAs [9] are programmable logic devices used for real-time data processing. The functionality of the device is determined by the content of a configuration SRAM (CRAM). The CRAM size can reach 100 Mb and can be accessed by the programmable logic through dedicated ports. Many devices have a TID tolerance over a few kGy [10], and they are hardened at transistor level against radiation-induced single-event latch-ups. However, upsets in the CRAM [11] may alter the programed elements, including routing, thus disrupting the operation of the logic implemented in the fabric [12].

The contribution of this work to the state of the art is threefold. First, we show an implementation of a novel thermal neutron and high-energy (>20 MeV) hadron fluence sensor based on an SRAM-based FPGA used both as the sensitive element (the CRAM) and as the readout logic (the programed fabric). Second, we describe the radiation-hardening-by-design (RHBD) techniques we used for protecting the readout logic (ROL) at firmware level, including architectural, place-and-route, configuration aspects, and at printed circuit board (PCB) level. Finally, we present the radiation-tolerance results of the sensor board (SB) and its firmware after neutron irradiation at a research reactor.

The rest of this article is organized as follows. In Section II, we describe the fluence SB with details about the used components. In Section III, we present the ROL architecture

Manuscript received 20 February 2023; revised 5 April 2023; accepted 5 April 2023. Date of publication 10 April 2023; date of current version 18 May 2023. This work was supported in part by the Istituto Nazionale di Fisica Nucleare (INFN), Italy, within the framework of Commissione Scientifica Nazionale V (PHI Experiment); and in part by the EU Horizon 2020 AIDAInnova under Grant 101004761.

R. Giordano is with the Dipartimento di Fisica of Università degli Studi di Napoli "Federico II", 80138 Naples, Italy, and also with the Sezione di Napoli of Istituto Nazionale di Fisica Nucleare (INFN), 80126 Napoli, Italy (e-mail: raffaele.giordano@unina.it).

G. Tortone is with the Istituto Nazionale di Fisica Nucleare (INFN) Sezione di Napoli, 80126 Naples, Italy.

D. Vincenzi was with the Dipartimento di Fisica of Università degli Studi di Napoli "Federico II", 80138 Naples, Italy, and also with the Sezione di Napoli of INFN, 80126 Napoli, Italy. He is now with the Department of Mathematics and Physics, Roma Tre University, 00146 Roma, Italy, and also with the Sezione di Roma 3 of INFN, 00146 Roma, Italy.

F. Loffredo and M. Quarto are with the Dipartimento di Scienze Biomediche Avanzate of Università degli Studi di Napoli "Federico II", 80138 Naples, Italy, and also with the Sezione di Napoli of INFN, 80126 Napoli, Italy.

R. Pestotnik, A. Lozar, and A. Seljak are with Jožef Stefan Institute, 1000 Ljubljana, Slovenia.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TNS.2023.3265740.

Digital Object Identifier 10.1109/TNS.2023.3265740

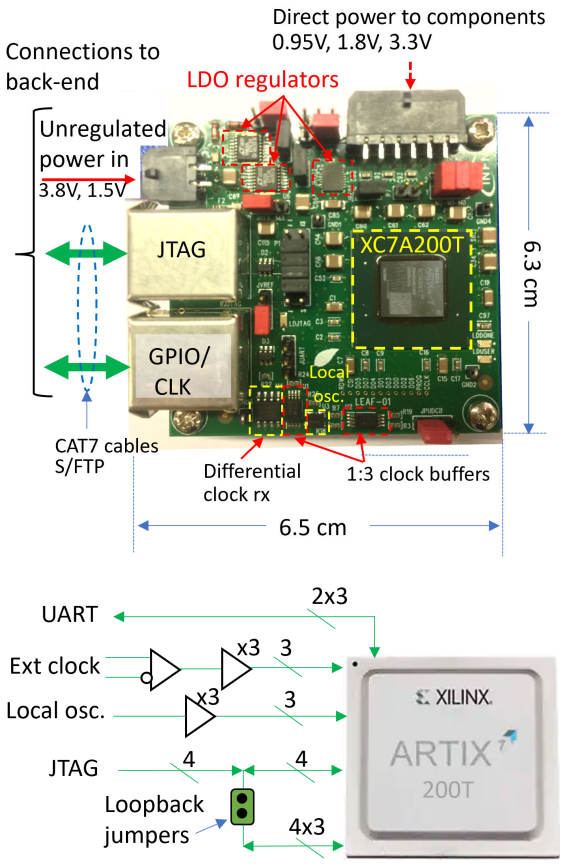

Fig. 1. Top: photograph of the fluence SB with highlighting of the active components and the connections to a readout system. Bottom: scheme of the tripled routing on the PCB.

and implementation. In Section IV, we show the sensor radiation-tolerance test results from irradiation at a nuclear reactor. In Section V, we discuss our findings and compare them to results from the peer-reviewed literature. In Section VI, we draw our conclusions.

II. Fluence SB

The SB we designed [Fig. 1 (top)] is based on a Xilinx Artix-7 200T FPGA and has the following features:

1) single integrated circuit used as sensor and readout;
2) reprogrammable ROL and digital serial interface to back-end systems;
3) compact (6.5 × 6.3 cm) PCB;
4) low power consumption (≈0.7 W);
5) usage of commercial off-the-shelf (COTS) components only.

The PCB size has been kept to a minimum to use the sensor also in space-constrained locations. In order to enhance the overall radiation tolerance, we minimized the usage of active components, which include only the FPGA, a 100-MHz crystal oscillator (Si Time SIT8008), a differential receiver (Analog Devices ADN4691), 1:3 clock buffers (Texas Instruments LMK1C1103), and analog devices low dropout (LDO) voltage regulators. One LT3070 LDO uses a 1.5-V input to generate the 0.95-V regulated power supply for the FPGA, while two LT1963 use a 3.8-V input to generate, respectively, the 1.8- and 3.3-V regulated voltages for the FPGA and the rest of the active components. It is also possible to skip the on-board regulators and provide the voltages directly via a dedicated connector supporting a four-wire scheme for sensing the voltage at the SB. This feature makes it possible to perform voltage scans during cross-section characterization tests and to operate the board even in harsh radiation environments, where the LDOs might fail. However, direct powering requires a remote sensing low-voltage power supply and more complex cabling with respect to powering via regulators. All input–output (IO) signals to the FPGA are routed over tripled PCB traces, and, except clocks, they are single-ended and unbuffered in order to minimize the active components count and maximize the overall board reliability [Fig. 1 (bottom)].

We have chosen the Artix-7 FPGA family for our sensor, since it offers a good compromise between price and configuration memory size, and from published TID gamma ray tests, it is known that devices of this family operate up to 5.5 kGy without functional issues or hard failures [13]. The configuration memory size of the 200T is 77.8 Mb arranged in 24 060 frames (18 300 for the fabric + 5760 for block RAMs), each containing 3232 bits.

As far as it concerns the LT1963 and LT3070 regulators, other works [14] report their radiation tolerance, respectively, to be up to 3.4- and 2.0-kGy gamma ray TID and 7.4 and 8.0×10^{12}-$n_{eq}cm^{-2}$ 1-MeV-equivalent-neutron fluence. The LT1963 is also reported to tolerate up to 1-kGy TID in [15]. We did not have radiation-tolerance information about the other components on the board, which we combinedly tested under neutron irradiation.

III. Readout Logic

The implementation of the ROL required us to tackle the important challenge of the impact of SEUs on the functionality. In fact, in this peculiar application of the FPGA, we faced two contradictory requirements. On the one hand, the CRAM must be as sensitive as possible to SEUs to enhance the operation as sensor. On the other hand, the firmware in the FPGA fabric must be robust against SEUs and transients. In fact, we devised a dedicated system for correcting upsets in the CRAM, i.e., a configuration scrubber, based on redundant configuration and usage of multiple configuration access ports. By redundant configuration, we refer to the fact that the content of the configuration memory locations, i.e., the frames, must be available in several copies [16]. We achieve it by properly copying each programed frame into two unused frames, realizing a tripled configuration, according to the method disclosed in [17].

Our ROL is based on the scrubber described in [18], of which here we briefly summarize the architecture. The system runs at 100 MHz and is triple modular redundant. It is built around the Xilinx picoBlaze-6 soft microprocessor with custom peripherals we devised, including block RAMs and IO logic. The main functionality is to periodically scrub the configuration memory of the FPGA by majority voting redundant configuration frames and keeping unprogrammed frames to their expected state. In order not to interfere with access to the used block RAMs, only fabric frames are readback and scrubbed. It is possible to send commands and receive output from the scrubber via a universal asynchronous receiver/transmitter (UART) or one of the device's boundary scan primitives (BSCAN) accessible via the Joint Test Action

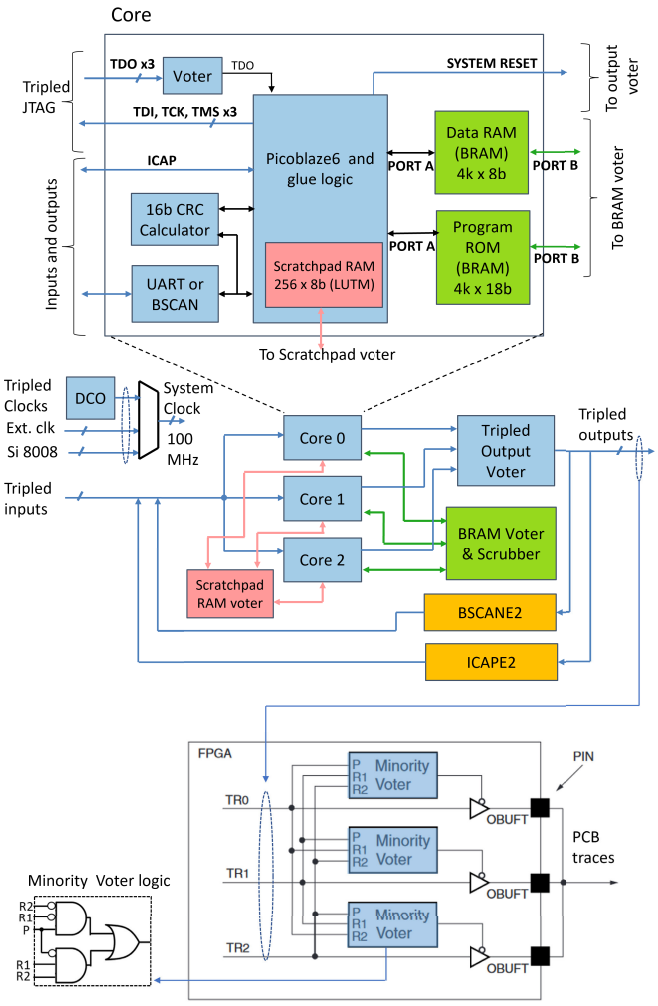

Fig. 2. Simplified block diagram of the readout logic architecture. Top: close-up on the core internals. Middle: overall block diagram. Bottom: output scheme based redundant PCB traces and minority voters.

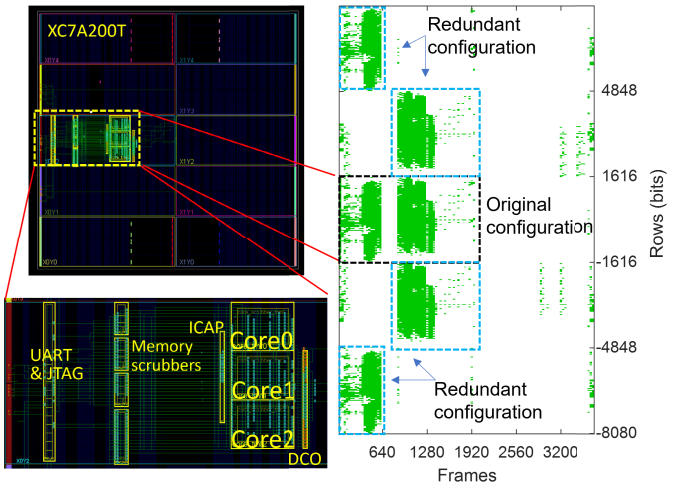

Fig. 3. Implementation view of the readout logic. Left: layout from Vivado graphical user interface (top) and close-up on blocks (bottom). Right: redundancy generated in the configuration memory. Each green pixel represents a 32 bits × 32 frames cluster in which at least 1 bit is set, i.e., a used cluster; each white pixel represents a cluster with all bits cleared, i.e., an unused cluster.

```
# 61488C04.003124 CORR_CLONE0 0x00001303 0 071B:0->1 #A629
# 61488C04.0040B2 OVERALL 0535 00000597 #5533
# 61488C04.012DE3 CORR_OPERAT 0x004013A3 0 098E:0->1 098F:0->1 #7CE1
# 61488C04.014138 OVERALL 0537 00000599 #84AC
# 61488C04.016F83 CORR_CLONE1 0x00421504 0 0606:0->1 #11E5
# 61488C04.017EAA OVERALL 0533 0000059A #2768
```

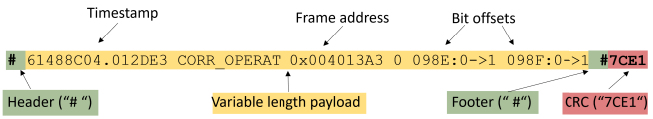

Fig. 4. Top: excerpt from the UART output. Bottom: close-up on a text line describing an upset event with the definition of header, payload, footer and CRC fields, and explanation of the upset details in the payload section.

Group (JTAG) port. The BSCAN support has been added to enable sensor control over a single signal cable, i.e., the JTAG cable. The architecture includes a number of features to enhance reliability, including for instance periodic resets of the main modules and majority-voting-based scrubbing of RAMs, whose description can be found in the abovementioned paper.

In the new design for this work (Fig. 2), we ported the scrubber to the Artix-7 family, and we added support for tripled PCB traces and for multiple configuration access ports. In fact, the ROL includes output majority voters, which are also tripled to avoid single point of failures. For each majority voter's output triplet (TR0, TR1, and TR2), three dedicated minority voter are used to disable output drivers (OBUFTs) to avoid clashes in case of SEUs. The firmware supports both the JTAG and internal configuration access port (ICAP) to readback and correct the device configuration. As per device specifications [19], the configuration access via ICAP is faster (up to 3200 Mb/s) with respect to JTAG (up to 66 Mb/s), but the ICAP is tied to specific hardware primitives, which cannot be tripled. The access to the JTAG port of the device from the fabric is possible by means of tripled loop back traces on the PCB. The self-access to the JTAG port represents a reliable alternative to the ICAP port for recovery situations. In fact, in normal operation, the ROL accesses the configuration via the ICAP, but in case of failure, it switches to the JTAG port on the fly. The abovementioned periodic resets of the ROL have been programed to happen every 300 processed frames, in case at least one frame has been corrected. As soon as the microprocessor resets, the program tries to switch back to ICAP to speed up the scrubbing. Before switching the configuration access port, the program checks its correct operation by attempting to read the device identification code. The ROL can be clocked by the local oscillator on the SB, an external clock, or by a digitally-controlled oscillator (DCO) [20] in the FPGA fabric.

To enhance the impact of the layout of the ROL on the reliability, we constrained the redundant modules to be placed and routed in distinct geometrical areas [Fig. 3 (left)], leveraging the "pblock" functionality of the Vivado design tool. We then used our custom scripts for generating redundant configuration frames [Fig. 3 (right)]. The resource utilization of the ROL (Table I) is minimal; in fact, it occupies just 2.5% of the available slices and block RAMs and 7.4% of the fabric configuration frames. The low resource occupation positively impacts the power consumption and the scrubbing period, as fewer programed frames to be protected translate to a lower

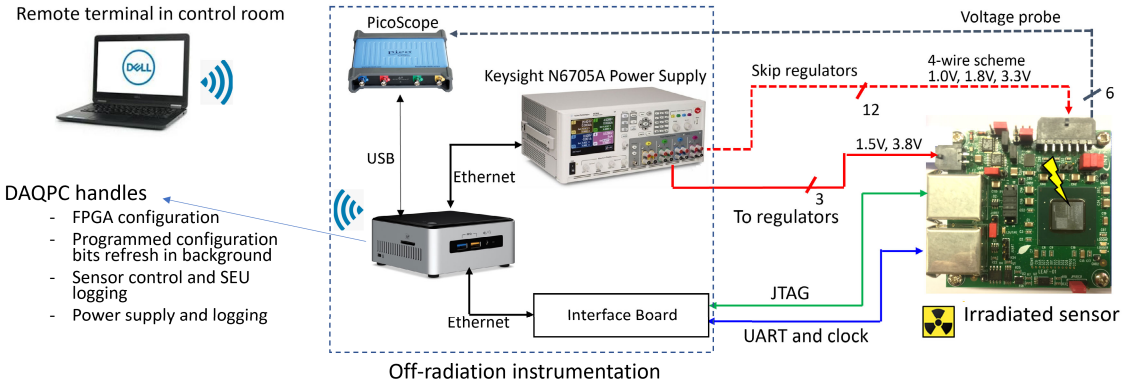

Fig. 5. Simplified block diagram of the test setup envisaged for irradiation and fault-injection tests.

TABLE I
LOGIC RESOURCES AND CONFIGURATION FRAME OCCUPATION FOR THE ROL

Logic Resource	Available	Used	%
Slices: FF	267600	1813	0.7
Slices: LUT	133800	2174	1.6
Slices: Overall	33450	823	2.5
BUFG	32	4	12.5
BUFH	120	1	0.8
IO	285	23	8.1
RAMB36	365	9	2.5
ICAPE2	1	2	50
BSCANE2	1	4	25
Fabric CRAM Frames (after redundant configuration)	18300	1354 (4054)	7.4 (22.2)

processing time. The scrubbing period was measured to be nearly 1.5 s.

The output via UART is a sequence of printable American Standard Code for Information Interchange (ASCII) characters formatted as text lines. Each line includes a header, a variable number of characters, and a footer, including a hardware calculated 16-bit cyclic redundancy check[1] (CRC; Fig. 4). The CRC makes it possible to immediately spot subtle data transmission errors and conveniently discard erroneous output bursts from the ROL in case of failure.

IV. IRRADIATION TEST RESULTS

We devised a setup (Fig. 5) to perform bench testing and irradiation testing of the sensor. The sensor is connected to a custom interface board (IB) over standard CAT7 S/FTP cables and is powered by a Keysight N6705A power analyzer. The IB feeds a 100-MHz clock signal to the sensor and provides access to its UART and JTAG ports over Ethernet. We prepared the cabling for powering the sensor either directly or via the on-board LDO regulators, and we logged the power consumption of the board in either case. A dedicated data acquisition personal computer (DAQPC) communicates via Ethernet with the power analyzer and the IB to perform FPGA configuration/readback, sensor control, power management, and measurement. A portable oscilloscope (PicoScope) was used to log the output voltages of the LDO regulators during irradiation. Cables lengths make it possible to place all the instrumentation at up to 10 m from the sensor, in order to be out of the radiation field, while a remote terminal can be in a control room, without actual limitations of distance from the instrumentation.

We irradiated two identical fluence sensors prototypes at the TRIGA Mark II reactor [21] of the Jožef Stefan Institute (JSI, Ljubljana, Slovenia). The reactor is optimized for training in reactor operation and technology, research with neutrons, and isotope production. It is water-cooled and can operate at powers up to 250 kW. There are several irradiation channels offering different combinations of thermal (<0.625 eV), epithermal ($0.625 - 10^5$ eV), and fast (>10^5 eV) neutron fluxes, and there is also a dry room for irradiating larger samples. For the irradiation tests presented in this work, we used the dry chamber and the TOK2 triangular channel, and the pertaining fluxes are reported in Table II. The dry chamber also includes a fission plate, which can be installed to increase the fast neutron component. To estimate the neutron fluences during our tests, we used the data provided by the facility [22], [23].

A typical test run consisted of the following steps:

1) power on the SB and begin current logging of all power supply output channels;
2) configure the sensor FPGA with ROL firmware and enable readout;
3) wait for an ROL failure to occur or 1 h to elapse, and, meanwhile, log upset details;
4) readback the sensor configuration and verify against the initial configuration;
5) power off the SB.

During step 3), the FPGA configuration is also periodically refreshed by means of partial reconfiguration from TCL scripts running on the DAQPC, in such a way to realize a hybrid, i.e., internal and external, scrubbing. This ensures that, even in case of failures related to upsets non-recoverable by the ROL, the operation can be resumed by means of the external scrubbing. The external scrubbing concerns only the programed frames, less than 0.5% of the total, and takes nearly 3 s. The external refresh is performed every fifth ROL scrub cycle. Upset details

[1]Specifically, we used the CRC16 based on the $x^{16}+x^{15}+x^2+1$ generator polynomial.

TABLE II
NEUTRON FLUXES AT FULL POWER IN TRIANGULAR CHANNEL AND IN THE DRY CHAMBER, AS PROVIDED BY THE FACILITY'S DOCUMENTATION

Neutron energy/channel	TOK2	Dry chamber no fission plate	Dry chamber w/ fission plate
	flux ($cm^{-2}s^{-1}$)	flux ($cm^{-2}s^{-1}$)	flux ($cm^{-2}s^{-1}$)
Thermal (<0.625 eV)	$4.5 \cdot 10^{12}$	$8.8 \cdot 10^{7}$	$8.3 \cdot 10^{7}$
Epithermal ($0.625 - 10^{5}$eV)	$3.5 \cdot 10^{12}$	$2.6 \cdot 10^{7}$	$2.9 \cdot 10^{7}$
Fast (>10^{5} eV)	$3.8 \cdot 10^{12}$	$1.7 \cdot 10^{7}$	$9.5 \cdot 10^{7}$
Total	$1.2 \cdot 10^{13}$	$1.3 \cdot 10^{8}$	$2.1 \cdot 10^{8}$
1-MeV equivalent	$3.6 \cdot 10^{12}$	-	-

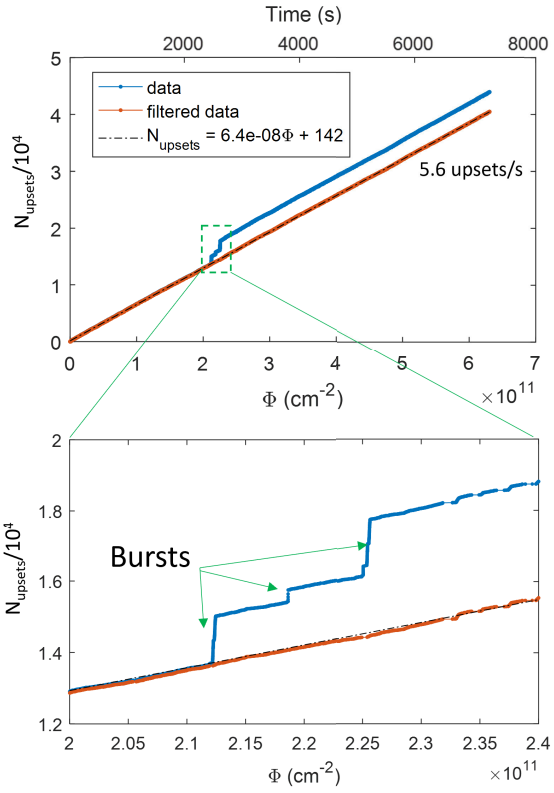

Fig. 6. CRAM upsets detected by means of hybrid scrubbing versus thermal neutron fluence in a typical irradiation run. Blue experimental points represent raw data, while orange points represent data filtered by rejecting events with a number of bitflips per frame beyond five. The best fit line of the filtered data is dashed.

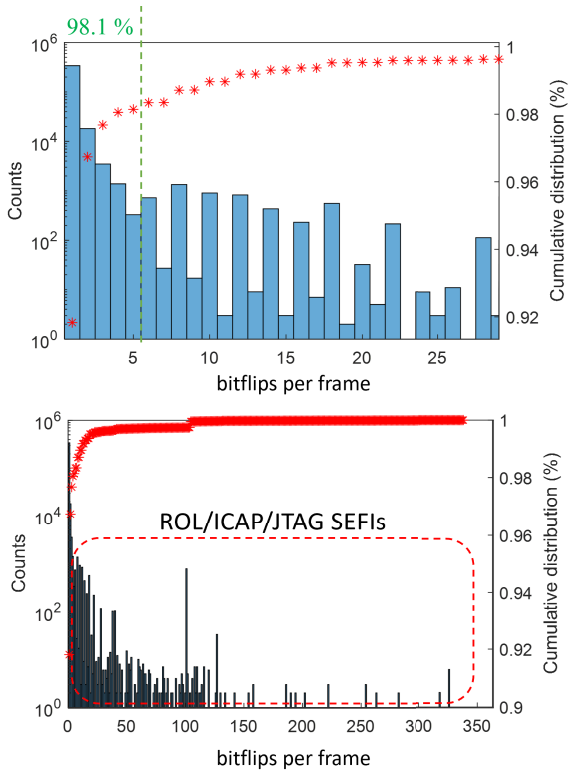

Fig. 7. Histogram and cumulative distribution of the number of bitflips per CRAM frame at each SEU detection. Top: close-up on the 1–25 bitflip range. Bottom: view of the full range.

are logged both from the UART and from the TCL scripts, and then combined off-line during data analysis.

Since shutting down and restarting the reactor require a few minutes, we decided to keep the reactor always on, even between runs, to optimize the usage of the assigned irradiation time.

A. Dry Chamber Tests

A first sensor has been irradiated in the dry chamber with total (thermal, epithermal, and fast) neutron fluxes ranging between 1.3 and 2.1 $\times$ 10^{8} $cm^{-2}s^{-1}$ for a total fluence of 1.0×10^{13} cm^{-2}. We partitioned the irradiation in 38 runs for a total irradiation time of 29 h and 43 min. With exception of a few initial calibration runs, we operated the reactor at full power. For each run, we combined the upset logs and neutron flux measurements to plot the CRAM upsets versus the neutron fluence, as, for example, shown in Fig. 6. In some cases, we measured some false readings from the ROL, where the upset count quickly increases due to a big number of fake SEUs with multiple bitflips in the same configuration frame, typically 6 and beyond. This behavior might be explained by some form of single event functional interrupts (SEFIs), due to the ROL or the configuration access ports. The SEFIs might generate incorrect readings, which are aliased as bitflips. These events have been removed by the actual upset count off-line by imposing a cut on the number of bitflips per frame. The cut restores the expected linear behavior of the upset trend.

We determined the optimal value for the cut by examining the distribution of the number of bitflips per frame. In fact, from Fig. 7, it is apparent how after five bitflips per frame the counts oscillate, instead of monotonically decrease as one would expect. It is worth noticing that the cutting at five bitflips per frame retains 98.1% of the events, so there is a negligible loss in detection efficiency. From a computational standpoint, the cut procedure is very simple, and it will be implemented online in the ROL itself for future tests and applications.

TABLE III
SUMMARY OF THE RUN CONDITIONS AND TEST RESULTS IN THE DRY CHAMBER. ROL FAILURES REFER TO FAILURES UNRECOVERABLE BY MEANS OF CRAM SCRUBBING

	Parameter	Without fission plate	With fission plate	Overall
Test conditions	Time (s)	$3.20 \cdot 10^4$	$3.04 \cdot 10^4$	$6.24 \cdot 10^5$
	Number of runs	16	22	38
	Thermal n ϕ (cm^{-2})	$2.8 \cdot 10^{12}$	$2.4 \cdot 10^{12}$	$5.3 \cdot 10^{12}$
	Epi n ϕ (cm^{-2})	$8.4 \cdot 10^{11}$	$8.6 \cdot 10^{11}$	$1.7 \cdot 10^{12}$
	Fast n ϕ (cm^{-2})	$5.5 \cdot 10^{11}$	$2.8 \cdot 10^{12}$	$3.4 \cdot 10^{12}$
CRAM Upsets	Average SEU Rate (Hz)	6.04	5.78	-
	Total N_{upsets}	$2.0 \cdot 10^5$	$1.7 \cdot 10^5$	$3.7 \cdot 10^5$
	σN_{bits} (cm^2)	$6.9 \cdot 10^{-8}$	$7.0 \cdot 10^{-8}$	$6.9 \cdot 10^{-8}$
ROL Failures	N_{fail}	-	-	27
	σ_{fail} (cm^2)	-	-	$5.1 \cdot 10^{-12}$
	Fluence between failures (cm^{-2})	-	-	$2.0 \cdot 10^{11}$
	Upsets between failures	-	-	$1.4 \cdot 10^4$

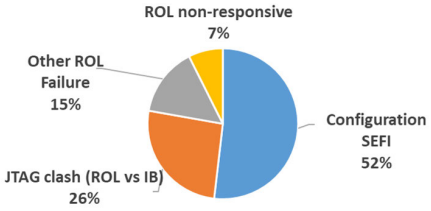

Fig. 8. Pie chart of the failure modes in dry chamber irradiation runs.

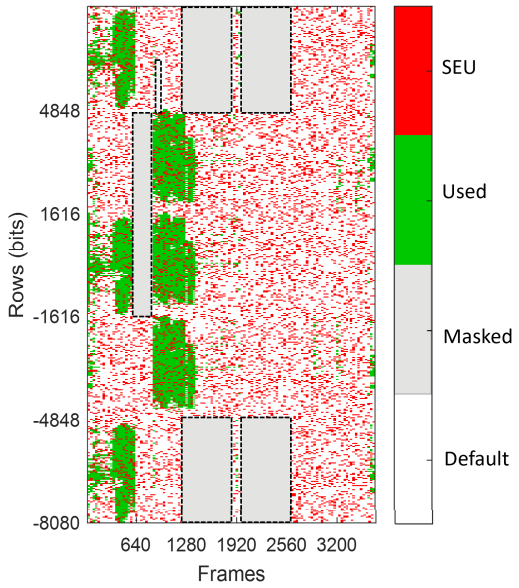

Fig. 9. Bitmap of the FPGA configuration memory with superimposition of upsets measured during a typical irradiation run. Specifically, in the shown run, we measured 1.4×10^4 upsets for a 2.2×10^{11} cm^{-2} thermal neutron fluence. Each red pixel represents a cluster of 32 bits $\times$ 32 frames in which at least an upset has been detected. Some rectangular areas, marked in gray, are masked in readback, and they do not contribute to upset detection.

Table III summarizes the details of the run conditions and the overall results. We performed our runs with and without the fission plate to test the sensor with different fractions of thermal and fast neutron fluxes. In fact, these differential measurements made it possible to note that the CRAM upset count (N_{upsets}) scales approximately with the thermal neutron fluence (ϕ); i.e., σN_{bits} does not change significantly between the two conditions. Moreover, the SEU rate and the thermal neutron flux decrease, respectively, by 4% and 6%, when setting the fission plate on. On the other hand, the SEU rate does not seem to correlate significantly with the fast and epithermal fluxes, which increase, respectively, by a factor of 5.6 and 1.2.

Considering the results averaged on all runs, under the simplifying hypothesis that configuration upsets are related to thermal neutrons only, σN_{bits} was measured to be 6.9×10^{-8} cm^2 and the sensitivity to be 1.4×10^7 n $\times$ cm^{-2}.

The failure cross section of our ROL was measured to be 5.1×10^{-12} cm^2 corresponding to a mean number of detectable upsets before failure of 1.4×10^4 (thermal neutron fluence of 2.0×10^{11} cm^{-2}). We tested the sensor by clocking the ROL from the IB and by means of the internal DCO, but the number of failure events was not sufficient to assess differences in reliability between the clocking modes.

We performed a failure mode analysis on the 27 unrecoverable soft failure events of the ROL. In these failures, not even the external scrubbing from the DAQPC could restore the correct operation. We arranged the events in four modes according to the reason for failure, determined by analyzing logs of the ROL UART and of the TCL scripts running on the DAQPC (Fig. 8). Most of the failures (52%) were related to some form of SEFI in the configuration access ports logic, which caused data to be readback incorrectly. In some events (26%), the ROL failed while still driving the JTAG pins via the loopback, which made readback and scrubbing from the DAQPC impossible. Other failures included the ROL to become unresponsive to commands via the UART (7%) and a variety of other failures (15%). However, it is important to report that, for all the soft failures, the sensor operation has always been recoverable by means of a power cycle.

No failures of the active components have been observed, except for the SIT8008 oscillator chip, which permanently failed at a total neutron fluence of 1.0×10^{11} cm^{-2}. This failure did not impact our tests, as the SB firmware supports multiple clock sources. After the oscillator chip failure, we switched to clocking from the IB.

By means of the details provided by the ROL, we built a bitmap of the upsets of the FPGA configuration (Fig. 9) for each run. We observed a uniform distribution of upsets over the CRAM, with the exception of five rectangular areas,

TABLE IV
OUTPUT VOLTAGES OF LDO REGULATORS OF A REFERENCE SENSOR AND OF THE SENSOR IRRADIATED IN THE TOK2 CHANNEL

	LT3070	LT1963-1.8	LT1963-3.3
Sensor/Parameter	V_{REG1}(V)	V_{REG2}(V)	V_{REG3}(V)
Reference	0.95	1.80	3.31
Irradiated	1.00	1.88	3.47

which are masked for readback by the device. The CRAM cells pertaining to these areas do not contribute to upset detection, and they lower the effective N_{bits} by nearly 16% (9.5 Mb). By taking into account this effect, we can estimate the thermal neutron cross section per bit to be 1.2×10^{-15} cm^{2}b^{-1}, which is in good agreement with the results from [24].[2]

During the irradiation, the voltage output from the LDO regulators remained constant.

B. TOK2 Tests

For the second sensor, we performed a high-flux test in the TOK2 channel. The TOK2 channel section is an isosceles triangle, with 78-mm sides and 83-mm base. Due to the small size of the channel, we had to run cables to the sensor only from the JTAG/UART side, so for this test, we could only power the sensor through the on-board regulators without logging the output voltages. We powered the reactor at 463 W corresponding to a flux of 6.6×10^9 $n_{eq}cm^{-2}s^{-1}$ on the sensor, tuned to have an upset rate of nearly 300 SEU/s, i.e., nearly 50 times higher than what had been measured in the dry chamber. We performed the run in "accumulation" mode, where the readout logic was disabled, i.e., not clocked, and we continuously readback upsets in the FPGA, without correcting them, over JTAG via the Xilinx iMPACT tool. We could readback the FPGA up to a fluence of 3.4×10^{12} $n_{eq}cm^{-2}$. Beyond this fluence, we observed erroneous readings of the device temperature and internal voltages (VCCINT and VCCAUX) via the iMPACT tool (Fig. 10). However, even before failure, we observed that the upset count was incorrect on some reads (nearly at 1.0 and 1.3×10^{12} $n_{eq}cm^{-2}$), as, in fact, the trend was not monotonic. After the failure, we tried to power cycle the sensor to perform a new run, but while the temperature reading went back to a correct value, the internal voltages did not. Fourteen months after irradiation, we measured the regulators output voltages and noticed they were all shifted to higher voltages with respect to a reference, i.e., not irradiated, sensor (Table IV). By powering the sensor via the direct input connector, we verified That the FPGA was fully functional and able to run the ROL firmware correctly.

V. DISCUSSION

We designed our sensor to meet typical requirements for usage at high-energy physics experiments, and our results show the tolerated neutron fluence to be higher than 10^{12} $n_{eq}cm^{-2}$. As a frame of reference, the requirement for on-detector electronics at the Belle II experiment is

[2]In the cited paper, the overall CRAM cross section results to be 1.5×10^{-15} cm^{2}b^{-1} by including contributions from single and multiple cell upsets and assuming frontal irradiation.

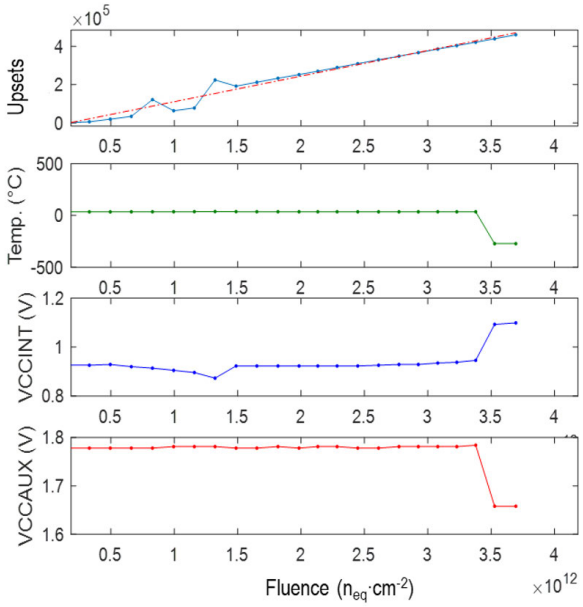

Fig. 10. Upsets, temperature, and FPGA internal voltages versus 1-MeV equivalent neutron fluence during irradiation at high flux in the TOK2 channel.

10^{11} $n_{eq}cm^{-2}$ per year [25], which for our sensor would translate to more than ten years of operation. Moreover, with respect to the SRAM-based monitors described in [2] and [7], our sensor is more compact being based on a single integrated circuit for sensing and readout. Nevertheless, our solution provides a higher TID tolerance (2 kGy versus 250 Gy [6]) because of the usage of an SRAM-based rather than a flash-based FPGA. For the same reason, our ROL may fail due to SEUs in the FPGA configuration, which instead is not an issue in [6] and [7]. However, the choice of components, the hardening of the PCB, and the hardening of the firmware lowered the failure rate of our logic to be tolerable. The fake SEU burst issues we have encountered are a common drawback among SRAM-based hadron sensors, and in fact, similar issues are also reported by Danzeca et al. [2] and Ytre-Hauge et al. [7]. The σN_{bits} for thermal neutrons for our sensors is, respectively, nearly 18.7 and 3.5 times higher than the same figure reported by Danzeca et al. [2] (3.7×10^{-9} cm^2) and by Ytre-Hauge et al. [7] (2.0×10^{-8} cm^2). This is partly due to the larger memory capacity of the device we used (65.4 versus 8 and 16 Mb) and partly due to its higher sensitivity to thermal neutrons.

It is worth mentioning that many other solutions for measuring hadron fluences exist. Among the others, these include chemical vapor deposition diamonds [26] and ^{6}LiF thermoluminescence detectors (TLDs) [27]. Differently from our sensor, these are also sensitive to photons, which is undesirable when the goal is to selectively measure hadrons. Moreover, TLDs are passive devices, require to be read with dedicated instrumentation after irradiation, and are unsuitable for online readout. Gas-filled detectors, such as ^{3}He [28] or BF_3 [29], can be employed for neutrons, but due to the gas volume and moderating materials, they are normally significantly larger than our solution.

Due to their operating principle, SRAM-based sensors, in general, and our sensor, in particular, are very well-suited for radiation monitoring aimed at protection of digital electronics, where SEUs are often a concern.

VI. Conclusion

The discussed RHBD techniques adopted for the SB, including triple modular redundancy, redundant clocks, inputs and outputs, PCB trace redundancy, reliability-driven placement and routing constraints, and redundant configuration, made it possible to implement a very robust system against SEUs in the CRAM. These techniques are indeed of general interest for the implementation of FPGA-based instrumentation in radiation areas.

The ROL failure cross section was measured to be 5.1×10^{-12} cm^2, translating to 1.4×10^4 detected upsets before failure on average. All the ROL failures observed were recoverable by means of a power cycle. The tests in different irradiation channels showed that the SB can be operated at the fluences of 10^{12} $n_{eq}cm^{-2}$ and beyond. We spotted some fake count issues, which hinder the response of the sensor, but we also provided a solution to mitigate them. The clock oscillator on the SB failed; however, this did not compromise the functionality of the sensor because of the redundant clocking scheme we had foreseen.

The promising results suggest that our sensor has potential applications for radiation monitoring at high energy physics experiments, at particle accelerators, and at proton therapy irradiation facilities.

Acknowledgment

The authors wish to thank the SER (Electronics and Detectors Service) staff of the Istituto Nazionale di Fisica Nucleare Sezione di Napoli, Naples, Italy, for their technical support to this activity, and the TRIGA staff of the Jožef Stefan Institute, Ljubljana, Slovenia, for their technical support during the irradiation test.

References

[1] R. Harboe-Sorensen et al., "From the reference SEU monitor to the technology demonstration module on-board PROBA-II," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3082–3087, Dec. 2008, doi: 10.1109/TNS.2008.2006896.

[2] S. Danzeca et al., "Qualification and characterization of SRAM memories used as radiation sensors in the LHC," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3458–3465, Dec. 2014, doi: 10.1109/TNS.2014.2365042.

[3] R. Secondo et al., "Embedded detection and correction of SEU bursts in SRAM memories used as radiation detectors," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2168–2175, Aug. 2016, doi: 10.1109/TNS.2016.2521485.

[4] D. Kramer et al., "LHC RadMon SRAM detectors used at different voltages to determine the thermal neutron to high energy hadron fluence ratio," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 1117–1122, Jun. 2011, doi: 10.1109/TNS.2011.2105891.

[5] K. S. Ytre-Hauge, A. Velure, C. H. Stokkevåg, O. H. Odland, and D. Röhrich, "First application of a novel SRAM-based neutron detector for proton therapy," *Radiat. Meas.*, vol. 122, pp. 45–52, Mar. 2019, doi: 10.1016/j.radmeas.2019.01.001.

[6] S. Danzeca. *The New Version of the Radiation Monitor system for the Electronics at the CERN: Electronic Components Radiation Hardness Assurance and Sensors Qualification*. Accessed: Apr. 5, 2023. [Online]. Available: https://tel.archives-ouvertes.fr/tel-02102187

[7] K. S. Ytre-Hauge et al., "Design and characterization of an SRAM-based neutron detector for particle therapy," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 804, pp. 64–71, Dec. 2015, doi: 10.1016/j.nima.2015.09.049.

[8] J. M. Armani, J. L. Leray, R. Gaillard, and V. Iluta, "TID response of various field programmable gate arrays and memory devices," in *Proc. 15th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, Sep. 2015, pp. 345–348, doi: 10.1109/RADECS.2015.7365686.

[9] S. M. Trimberger, *Field-Programmable Gate Array Technology*. New York, NY, USA: Springer, 1994, doi: 10.1007/978-1-4615-2742-8.

[10] H. Quinn, "Radiation effects in reconfigurable FPGAs," *Semicond. Sci. Technol.*, vol. 32, no. 4, Apr. 2017, Art. no. 044001, doi: 10.1088/1361-6641/aa57f6.

[11] V. Bocci et al., "Radiation test and application of FPGAs in the ATLAS level 1 trigger," in *Proc. 7th Workshop Electron. LHC Exp.*, 2001, pp. 137–141, doi: 10.5170/CERN-2001-005.137.

[12] M. Preston et al., "Proton- and neutron-induced single-event upsets in FPGAs for the PANDA experiment," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 6, pp. 1093–1106, Jun. 2020, doi: 10.1109/TNS.2020.2987173.

[13] X. Hu, J. Wang, R. Pinkham, S. Hou, T. Schwarz, and B. Zhou, "A multi-layer SEU mitigation strategy to improve FPGA design robustness for the ATLAS muon spectrometer upgrade," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 939, pp. 30–35, Sep. 2019, doi: 10.1016/j.nima.2019.05.045.

[14] Y. Nakazawa et al., "Radiation hardness study for the COMET phase-I electronics," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 955, Mar. 2020, Art. no. 163247, doi: 10.1016/j.nima.2019.163247.

[15] C. Deplano, "Radiation resistance testing of commercial components for the new SPS beam position measurement system," in *Proc.2nd Int. Beam Instrum. Conf.*, 2013, Art. no. WEPC11.

[16] R. Giordano, S. Perrella, V. Izzo, G. Milluzzo, and A. Aloisio, "Redundant-configuration scrubbing of SRAM-based FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 9, pp. 2497–2504, Sep. 2017, doi: 10.1109/TNS.2017.2730960.

[17] R. Giordano, "Method for generating redundant configuration in FPGAs," U.S. Patent 16 348 810, May 9, 2019.

[18] R. Giordano, D. Barbieri, S. Perrella, and R. Catalano, "Custom scrubbing for robust configuration hardening in Xilinx FPGAs," *Instruments*, vol. 3, no. 4, Oct. 2019, Art. no. 56, doi: 10.3390/instruments3040056.

[19] *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics, DS181 (V1.27)*, Xilinx, San Jose, CA, USA Feb. 2022.

[20] R. Giordano et al., "High-resolution synthesizable digitally-controlled delay lines," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 3163–3171, Dec. 2015, doi: 10.1109/TNS.2015.2497539.

[21] L. Snoj, G. Žerovnik, and A. Trkov, "Computational analysis of irradiation facilities at the JSI TRIGA reactor," *Appl. Radiat. Isot.*, vol. 70, no. 3, pp. 483–488, Mar. 2012, doi: 10.1016/j.apradiso.2011.11.042.

[22] *Dry Chamber*. Accessed: Apr. 5, 2023. [Online]. Available: https://ric.ijs.si/en/dry-chamber/

[23] *Triangular Irradiation Channels 1 and 2*. Accessed: Apr. 5, 2023. [Online]. Available: https://ric.ijs.si/en/triangular-channels-1-and-2/

[24] J. C. Fabero, G. Korkian, F. J. Franco, H. Mecha, M. Letiche, and J. A. Clemente, "Thermal neutron-induced SEUs on a COTS 28-nm SRAM-based FPGA under different incident angles," in *Proc. IEEE 22nd Latin Amer. Test Symp. (LATS)*, Oct. 2021, pp. 1–6, doi: 10.1109/LATS53581.2021.9651879.

[25] T. Higuchi, M. Nakao, and E. Nakano, "Radiation tolerance of readout electronics for Belle II," *J. Instrum.*, vol. 7, no. 2, Feb. 2012, Art. no. C02022, doi: 10.1088/1748-0221/7/02/C02022.

[26] C. Ilgner, M. Budzanowski, and B. Obryk, "Hadron fluence measurements with LiF-TLD sensors at the proton synchrotron accelerator at CERN," *Radiat. Meas.*, vol. 45, nos. 3–6, pp. 684–687, Mar. 2010, doi: 10.1016/j.radmeas.2010.02.012.

[27] G. Bassi et al., "Calibration of diamond detectors for dosimetry in beam-loss monitoring," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 1004, Jul. 2021, Art. no. 165383, doi: 10.1016/j.nima.2021.165383.

[28] H. Iwase et al., "Experimental and theoretical study of the neutron dose produced by carbon ion therapy beams," *Radiat. Protection Dosimetry*, vol. 126, nos. 1–4, pp. 615–618, May 2007, doi: 10.1093/rpd/ncm140.

[29] X. Yan, U. Titt, A. M. Koehler, and W. D. Newhauser, "Measurement of neutron dose equivalent to proton therapy patients outside of the proton radiation field," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 476, nos. 1–2, pp. 429–434, 2002.

Open Access funding provided by 'Università degli Studi di Napoli "Federico II"' within the CRUI CARE Agreement