Threshold and Characteristic LETs in SRAM SEU Cross Section Curves

Daisuke Kobayashi, *Senior Member, IEEE*, Masashi Uematsu, and Kazuyuki Hirose

***Abstract*— Characterizing the sensitivity of a static random access memory (SRAM) to single-event upset (SEU) is an essential task for assuring its soft-error reliability. However, this task often imposes a burden because it usually requires many cycles of accelerator-based irradiation tests. A model recently proposed is a very simple exponential-type equation but has strong potential to reduce the burden because of its capability to predict SEU cross sections in various conditions. The aim of the present study is to revisit the model in terms of threshold parameters called threshold linear energy transfer (LET or L) and critical charge. Although these threshold parameters are widely used as key parameters that describe whether an SEU occurs or not, they are not seen in the model. This article explores such missing threshold parameters, suggesting that they successfully appear by introducing a factor of five to the original expression.**

***Index Terms*— Error analysis, ion radiation effects, semiconductor device reliability, soft errors.**

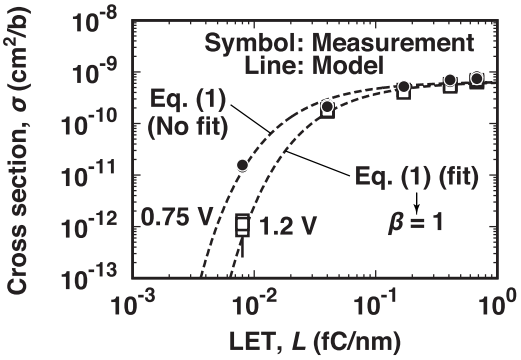

Fig. 1. Cross section curves of an SOI SRAM measured (symbols) and predicted (lines) under two voltage conditions (after [8]). The tested SRAM was fabricated in a 65-nm process, not hardened by design. Once β was determined through a fit with the 1.2-V data, the model successfully predicted the 0.75-V data without any parameter adjustment.

I. Introduction

RADIATION is a famous source of soft errors in static-random access memories (SRAMs) [1], [2], [3], [4], [5], [6], [7]. Even a single strike of particle radiation such as alpha- and cosmic-rays may induce noise charge that can overwhelm the noise margin of SRAM cell, leading to an undesired flip from a logic "1" or "0" originally kept in the cell to its counterpart. The causal radiation strike and the resultant flip are called single event (SE) and single-event upset (SEU), respectively.

Characterizing SEU sensitivity is of primary concern for assuring SRAM soft-error reliability. This process often involves cross section curves as exemplified in Fig. 1. The curve offers the evolution of SEU cross section (σ) of SRAM cell as a function of linear energy transfer (LET or L) of impinging radiation (LET expresses the linear charge density generated along the track).

For silicon-on-insulator (SOI) SRAMs, we recently proposed the following model to describe this curve [8]:

$$\sigma = \frac{A}{2}\exp\left(-\frac{\zeta C_L}{\beta d_{\mathrm{SOI}}}\frac{V_{\mathrm{DD}}-V_{\mathrm{DR}}}{L}\right). \tag{1}$$

See Table I for the symbols. This model is similar to others, such as the Weibull [9] and the Edmonds [10] models but is unique because all the parameters are physically clear and familiar to SRAM SEU researchers. In [8], this model showed its wide applicability to various SOI SRAMs and—with a slight modification from βd_{SOI} to the well-known funnel length—to other bulk-type devices.

The aim of this article is to address an issue remained in the previous study. The model was derived on an assumption that the exponential term can be written as $e^{-L_T/L}$ (see in Section II for details) where L_T represents a threshold LET, which describes the condition for SEU whether impinging radiation produces enough charge or not. In this context, the model should have yielded $\sigma \approx 0$ when $L = L_T$ but actually yields $1/e = 0.37$ of saturated value, which seems too large to qualify as zero. Rather, together with a characteristic LET (L_e) that accounts for $1/e$, the model should be expressed as

$$\sigma = \frac{A}{2}\exp\left(-\frac{L_e}{L}\right). \tag{2}$$

The threshold L_T is no longer seen. This disappearance should be addressed because L_T is the most critical parameter in soft-error reliability assessments.

II. Review of the Original Derivation

In the previous study [8], the derivation started from our experimental finding shown in Fig. 2. At a given L, as commonly observed in SRAM SEUs, σ exponentially responds to the power supply voltage V_{DD} (i.e., $\sigma \propto e^{-kV_{\mathrm{DD}}}$), where k is a slope parameter dependent on L but not on V_{DD}. Our analysis further suggested that the "straight lines" (on the semilogarithmic chart) are expected to converge on a point P

Manuscript received 28 October 2022; revised 31 January 2023; accepted 7 February 2023. Date of publication 13 February 2023; date of current version 18 April 2023. This work was supported in part by the Japan Society for the Promotion of Science (JSPS) under JSPS KAKENHI Grant JP20H02217.

The authors are with the Institute of Space and Astronautical Science (ISAS), Japan Aerospace Exploration Agency (JAXA), Sagamihara, Kanagawa 252-5210, Japan (e-mail: d.kobayashi@isas.jaxa.jp).

Digital Object Identifier 10.1109/TNS.2023.3244181

TABLE I
MODEL PARAMETERS

Symbol	Unit	Description
σ	cm^2	SEU cross section per bit
A	cm^2	Total transistor area
ζ		Circuit loading factor*1 ($\sim$2)
C_L	fF	Load capacitance
V_{DD}	V	Power supply voltage
V_{DR}	V	Data retention voltage
β		Bipolar gain [see (7)]
d_{SOI}	nm	SOI-layer thickness
L	fC/nm	LET*2

*1 This factor represents the enhancement of noise tolerance due to retarding current. See [11] for example. A survey [7] suggests $\zeta \approx 2$ across technology nodes.
*2 MeV·cm^2/mg was used in the original article [8]. In the present study fC/nm is used for simplifying the expression. 1 fC/nm $\approx$ 100 MeV·cm^2/mg for Si.

where $V_{DD} = V_{DR}$ because this point turns the SRAM static-noise margin to zero [12]. At this point, in theory, the entire region of the cell should be sensitive to any radiation strike, and thus,

$$\sigma \approx A \exp\left(-k_0 \frac{V_{DD} - V_{DR}}{L}\right). \tag{3}$$

In this transformation, another finding in an analysis of Fig. 2 was used that $k \approx k_0/L$ where k_0 is a coefficient independent of L or V_{DD}. Equation (3) was associated with the following facts.

1) Bark et al. [13] suggest that cross section curves can be normalized by using L/L_T.
2) Edmonds [10] proposes, with constants B_1 and B_2

$$\sigma = B_1 \exp\left(-\frac{Q_C}{B_2 L}\right). \tag{4}$$

3) Researchers (e.g., [14]) often use a variant of Hazucha and Svensson model [1]

$$\sigma \propto \exp\left(-\frac{Q_C}{Q_{col}}\right). \tag{5}$$

Here Q_C and Q_{col} represent critical and collected charge, respectively. The meaning of the fraction Q_C/Q_{col} is essentially the same as L_T/L. It expresses the SEU condition whether a node collects charge (Q_{col}) larger than a critical value for SEU (Q_C).

Q_C is well known to be proportional to $C_L V_{DD}$. Recently its proportionality constant was found to be determined by the circuit loading effect and constant across technology generations [7]. This finding resulted in

$$Q_C \approx \zeta C_L V_{DD} \tag{6}$$

where $\zeta = 2$ across generations. For SOI SRAMs, historically, Q_{col} is often given by

$$Q_{col} = \beta L d_{SOI}. \tag{7}$$

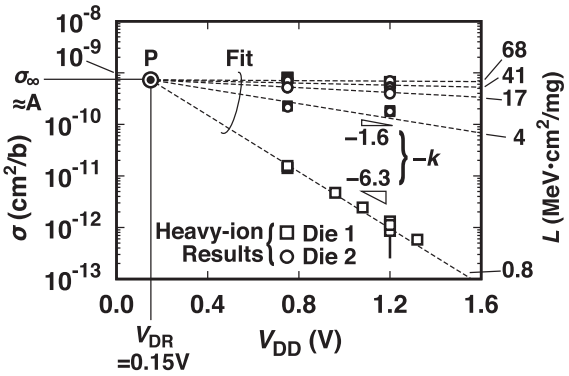

Fig. 2. Starting material of the model derivation [8]. SRAM σ measured under various L and V_{DD} conditions were supposed to converge on the point P where $V_{DD} = V_{DR}$. Measurement data were taken from heavy-ion tests with the 65-nm SOI SRAM [12], [15].

Therefore,

$$\frac{Q_C}{Q_{col}} = \frac{L_T}{L} = \frac{\zeta C_L V_{DD}}{\beta L d_{SOI}}. \tag{8}$$

Comparing (3)–(8), we derived the model (1). Note that in the comparison we also assumed that $Q_C \approx C_L V_{DD} \approx C_L(V_{DD} - V_{DR})$ and adapted A to $A/2$, taking into account that half of the transistors that make up a cell are OFF and sensitive to SEU.

III. HYPOTHESIS

It is known that the definition of L_T varies across papers [16]. Fitting of a Weibull function is one of the most popular ways to extract L_T. Another famous approach is to identify L corresponding to σ equal to 1/100 of its saturated value [16]. Following this 1/100-based definition, we propose a hypothesis that

$$L_T = \frac{L_e}{5} \tag{9}$$

which turns the original expression (1) into

$$\sigma = \frac{A}{2} \exp\left(-\frac{5\zeta C_L}{\beta d_{SOI}} \frac{V_{DD} - V_{DR}}{L}\right) \tag{10}$$

$$= \frac{A}{2} \exp\left(-\frac{5 Q_C}{Q_{col}}\right) \tag{11}$$

$$= \frac{A}{2} \exp\left(-\frac{5 L_T}{L}\right) \tag{12}$$

$$= \frac{A}{2} \exp\left(-\frac{L_e}{L}\right). \tag{13}$$

Note that 4.6 should be used rather than 5 to make 1/100 precisely ($\because e^{-4.6} = 0.0101$ whereas $e^{-5} = 0.0067$). In this study, we have selected 5 for sightly expression. Our survey in the literature could not find strict physical or mathematical reason to use the exact value of 1/100.

IV. EXPERIMENTAL

Numerical device simulation was used to investigate the validity of the hypothesis. Although the previous study [8] showed the good applicability of the original expression to various SRAMs (without the factor of 5), the study relied

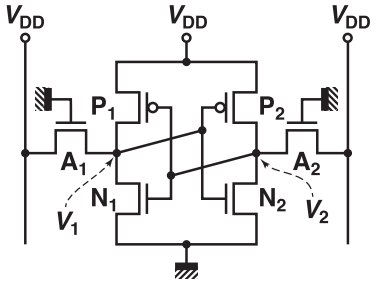

Fig. 3. Schematic of the SRAM cell. The cell operates in a retention mode for logic "1" where $V_1 = V_{DD}$ while $V_2 = 0$ V.

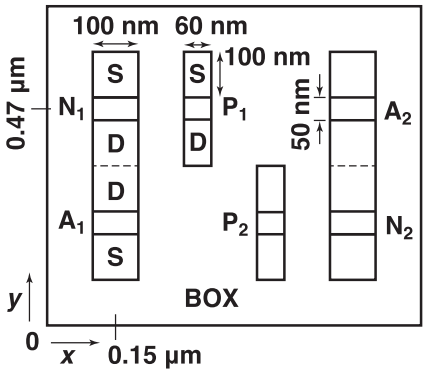

Fig. 4. Layout of the SRAM cell (in scale).

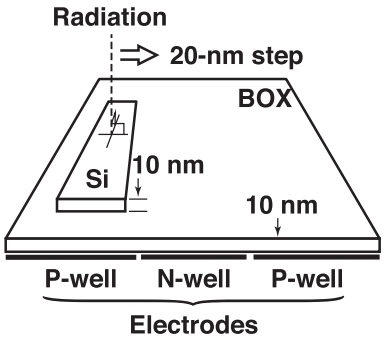

Fig. 5. Bird's eye view of the SRAM cell (conceptual drawing, not to scale).

TABLE II
MODEL PARAMETERS FOR THE SRAM CELL BEING INVESTIGATED

Symbol	Value
$A/2$	0.65×10^{-9} cm^2
ζ	2
C_L	0.18 fF
V_{DR}	0.05 V
d_{SOI}	10 nm

on literature data. Some of the model parameters were not available explicitly and hence estimated through fits of data and surveys of information about similar SRAMs. To exclude such parametric uncertainty, numerical device simulation was chosen as a main tool for investigation in the present study. Simulations were all conducted in the HyENEXSS technology computer-aided design (TCAD) platform [17].

A. SRAM Cell

A typical six-transistor SRAM cell was investigated (see Fig. 3), which was supported by no radiation hardening by design (RHBD) such as *RC* hardening [18]. The cell was kept in a retention mode for logic "1" where the access transistors (A_1 and A_2) were both OFF while the internal nodes were precharged at $V_1 = V_{DD}$ and $V_2 = 0$ V. The two bit-lines were fixed at V_{DD}. Thereby, the OFF-state N_1, P_2, and A_2 were sensitive to SEU.

The entire cell was modeled as a numerical device, as with [19] and [20]. Fig. 4 illustrates the layout of the cell. Some key dimensions, such as the gate lengths and widths are also presented. The six transistors were placed on a 10-nm-thick SiO_2 film corresponding to a buried oxide (BOX) film. For reduced computational cost, the bottom Si substrate beneath the BOX layer was removed and represented by electrodes (i.e., Dirichlet boundaries) with electron affinities of doped Si (see Fig. 5). A buried-well structure was assumed to make the bottom Si-electrodes. Recent SOI SRAMs often have p- and n-type wells beneath the BOX film for dynamic optimization of power and speed penalties [21], [22], [23], [24].

The SOI SRAM examined in the present study was not a replica of any real existing SRAMs. The dimensions and other parameters such as doping concentrations were values roughly determined through a survey of the literature [21], [22], [23], [24]. Structural simplifications were further applied. For example, the access transistors (A_1 and A_2) had the same width as that of the pull-down n-type transistors (N_1 and N_2). They are usually different in real SRAMs for proper read and write operations. Using the same width for these transistors helped to reduce the number of mesh and computation time (the simulator relies on orthogonal meshing).

The thickness of all the transistor regions on the BOX film was constant at d_{SOI} of 10 nm. No raised source/drain structure was used. Each transistor had an undoped body region (specifically, channel doping was set at 10^{15} cm^{-3}). The body region was sandwiched by the source (S) and drain (D) regions with a constant abrupt doping profile of 10^{20} cm^{-3}. The gate-stack consisted of a 1.5-nm-thick SiO_2 film covered by a metal gate. The metal gate was modeled as a Dirchlet-type electrode, as with the Si substrate. The work function of each metal gate was adjusted to make the threshold voltage of both p- and n-type transistors ~0.3 V in magnitude (measured by a constant-current method [25], [26]). Gate spacer regions and lightly-doped drain–source regions were omitted.

All the transistors were virtually interconnected. Metal wires to connect transistors were modeled in the mixed-mode framework.

Only the fundamental equation set that is an ensemble of the Poisson equation and the current-density equations was solved under the assumption of constant mobilities. Other detailed physics were omitted, such as impact ionization, band-gap narrowing, and generation and recombination of carriers.

Resultant parameters for the model (except for β) are summarized in Table II. V_{DR} of 0.05 V is a simulation result of butterfly curves under various V_{DD} (see Fig. 6). The constant factor of two is still used for ζ. The other parameters are straightforward estimations from the structure.

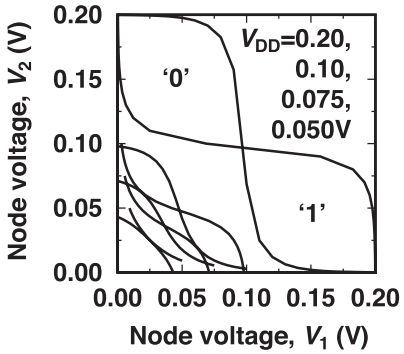

Fig. 6. Simulated butterfly curves under various V_{DD} conditions. The size of the open loops in each butterfly curve correspond to static noise margins in the retention mode (A_1 and A_2 are OFF). The loops disappear when V_{DD} reaches 0.05 V, thus $V_{DR} = 0.05$ V.

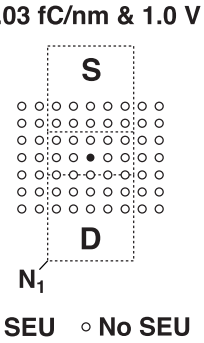

Fig. 7. Example of SEU map ($L = 0.03$ fC/nm and $V_{DD} = 1.0$ V). Only the center of N_1 exhibits an SEU in this example.

B. Single Event

The SE was assumed to be perpendicular to the top surface of the cell (see Fig. 5). A constant LET was also assumed. It deposited noise charge (electron and hole pairs) along the track constantly. The radial distribution of charge density (ρ) was modeled as

$$\rho(L, r, t) = \frac{1}{r_0\sqrt{\pi}} L\,\delta(t - t_0) \exp\left\{-\left(\frac{r}{r_0}\right)^2\right\} \qquad (14)$$

where t and r represent the elapsed time and the distance from the strike position, respectively. The delta function $\delta(t - t_0)$ dipicts the time-dependent distribution of charge. In the present study, t_0 was fixed at 1 ps. The Gaussian function describes the radial distribution of charge. The characteristic radius (r_0) was assumed to be 50 nm [27]. The first fraction is a coefficient to satisfy $\int_0^\infty \int_0^\infty (14)\, dtdr = L$.

Scanning the strike position produced an SEU map that visualized where SEU occurred, as exemplified in Fig. 7. Counting the strike position of SEU resulted in σ. A constant 20-nm step was used in the scan. This finite step resulted in the uncertainty of resultant σ. Note that the uncertainty provides no statistical information. It is a spatial discretization error (see Appendix A). The accuracy of the simulation in terms of L was also examined and expected to be within 10% (see Appendix B).

V. Results and Discussion

A. Validity of the Hypothesis

Fig. 8 shows σ of the SRAM under $V_{DD} = 1$ V. The cross section curve exhibited a typical shape in SOI SRAMs. With

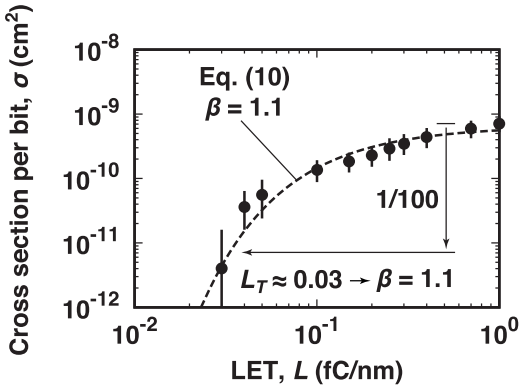

Fig. 8. Simulated cross sections (symbols). The vertical error bar shows the uncertainty of σ that stems from the finite scanning step. The horizontal error bar corresponding to the uncertainty of L is expected to be within 10% and smaller than the size of symbol. The observed $L_{1/100} \approx 0.03$ fC/nm indicates $\beta = 1.1$. Substituting this β for the hypothesized expression (10) successfully traces the simulated cross sections (dotted line).

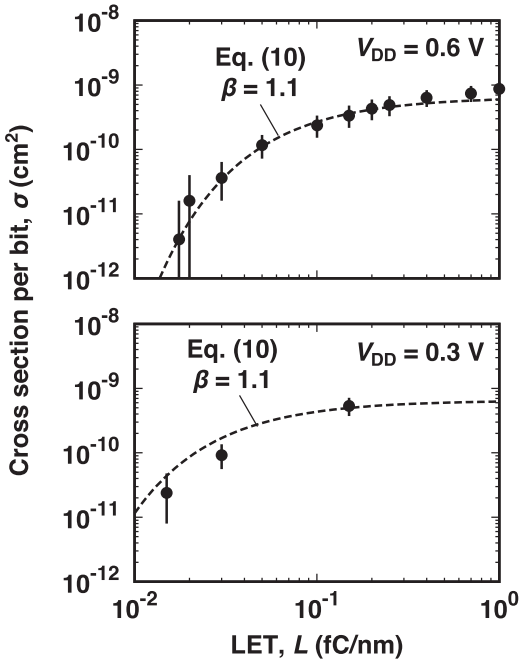

Fig. 9. Comparisons between simulated and predicted σ for $V_{DD} = 0.6$ V and $V_{DD} = 0.3$ V. The simulated cross section curves are well predicted by the hypothesized expression (10) together with $\beta = 1.1$. Note that β is extracted from the case of 1.0 V and no parameter adjustment is made for these two voltage conditions.

L increasing, σ monotonically increased and saturated at a certain value. The saturated value was $(0.7 \pm 0.2) \times 10^{-9}$ cm^2, indicating that $L_{1/100} = L_T \approx 0.03$ fC/nm. Together with other parameters in Table II, the obtained L_T straightforwardly yielded β of 1.1 for the hypothesized expression (10). Using this β, the expression (10) successfully traced the simulation results for $V_{DD} = 1.0$ V (see Fig. 8) and predicted the results for the cases where V_{DD} was scaled down to 0.6 V and further deeply to 0.3 V (see Fig. 9).

Note that the revealed agreements between the model and simulation results do not provide insight into the existence of the factor of 5. This is because the original expression (1) can also trace the simulated cross sections—even without the factor of 5—when β is divided by 5 and adapted to 0.23 (a slight difference from 0.22 or 1.1/5 is a simple round-off

error). The following detailed analysis, however, provides support for the existence of the factor of 5, while highlighting the importance of the use of numerical device simulation, i.e., the advantage of device simulation that enables monitoring signals on SRAM internal nodes, which are never accessible in real SRAM measurements.

Fig. 10(top) shows the evolution of voltage signals V_1 and V_2 monitored for the case where $L = 0.03$ fC/nm and $V_{DD} = 1.0$ V. The strike position was located at the center of N_1, corresponding to the sole SEU position for this L and V_{DD} condition (see Fig. 7). Note that the position expressed here as "center" is located at $x = 0.15$ μm and $y = 0.47$ μm. Due to the 20-nm constant resolution, this position is slightly shifted to the drain side by 0.005 μm from the exact geometrical center of the transistor ($x = 0.15$ μm and $y = 0.475$ μm). This slight difference is ignored in this study for merely simplicity of explanation.

The voltage transients indicated a flipping time of $t_F = 6.8$ ps, according to [11], where the second inverter output (V_2) exceeded the first inverter threshold voltage (0.50 V). During this flipping process [28], as shown in Fig. 10(bottom), N_1 drain terminal collected 0.41 fC, which provided $\beta = 1.3$ ($\because \beta = Q_{col}/Ld_{SOI}$). This β shows a good agreement with the value extracted from the cross section curve with the factor of 5, as summarized in Table III, justifying the hypothesis.

Since (11)–(13) do not have fabrication process dependent parameters, the hypothesis is expected to be applicable to bulk SRAMs. In fact, the factor of five accounts for the cross section curve of a recent bulk fin field-effect transistor (FinFET) SRAM, as shown in Fig. 11, where our expression (12) is compared with experimental data reported in [29]. For comparison, the authors of the present study converted the original SEU cross sections given in the reference into the event cross sections, taking into account the multicell upset (MCU) multiplicity, which is also given in the article referred to. This is because our model is expected to be suitable to describe the phenomenon that occurs inside the cell [8]. In the model, in fact, σ is limited by the total sensitive transistor area A. Actual SRAMs, however, may suffer from MCUs, exhibiting SEU cross sections larger than the limitation. Deviation is often evident in bulk SRAMs because of charge collection from the outside of the cell through the substrate [30]. The event cross section is a metric for eliminating such an "outer effect," being calculated by the number of events irrespective of multiplicity, i.e., the number of upsets in each single-event [31]. Fig. 11 demonstrates that the resultant event cross section is well explained by (12) in spite of no fit operation. In other words, the maximum event cross section (2×10^{-10} cm^2) revealed in the figure was simply substituted for $A/2$. L_T was estimated to be 0.012 fC/nm (corresponding to the left bottom point) through the 1/100-based definition and directly given to the equation. These two parameters could explain the bulk experimental result thanks to the existence of the factor of 5.

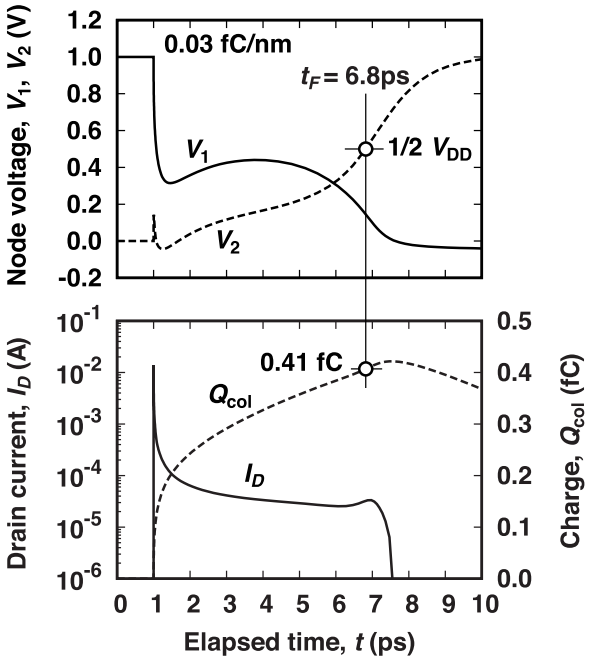

Fig. 10. (Top) Simulated evolutions of V_1 and V_2 plotted as a function of the elapsed time t for the SE strike at the center of N_1 when $t = t_0 = 1$ ns. $L = 0.03$ fC/nm and $V_{DD} = 1.0$ V. (Bottom) The evolution of the N_1 drain current alongside the voltage evolutions. The N_1 drain terminal collects 0.41 fC at the flipping time t_F, indicating β of 1.3.

TABLE III
EXTRACTED β FROM SRAM SIMULATION RESULTS. THE ORIGINAL EXPRESSION UNDERESTIMATES β DUE TO THE LACK OF THE FACTOR OF 5

	Original Eq. (1)	Hypothesized Eq. (10)	Current integral
β	0.23	1.1	1.3

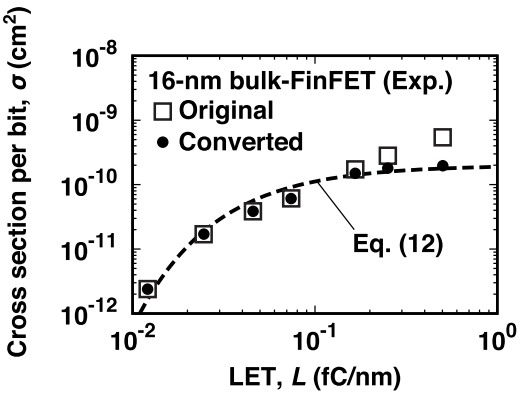

Fig. 11. Comparison with experimental data. Experimental data for a 16-nm bulk-FinFET SRAM were taken from [29, Fig. 5] and compared with (12). For comparison, the original data (SEU cross sections) were converted to the event cross sections (see text). The equation with the factor of 5 well explains the experimental results.

B. Potential for Estimating β From Single-Transistor Testing

In addition to the input and output parameters L and σ, as summarized in Table I, the model relies on seven characteristic parameters. Six of them are structure and voltage parameters, which can be measured without using radiation. The rest parameter β is the sole parameter that needs an analysis of the result of SRAM radiation test. SRAM radiation testing is often a burden because it requires the exposure of fully functional chip to radiation. It would be helpful if β can be estimated easily from simple parts other than fully functional SRAM

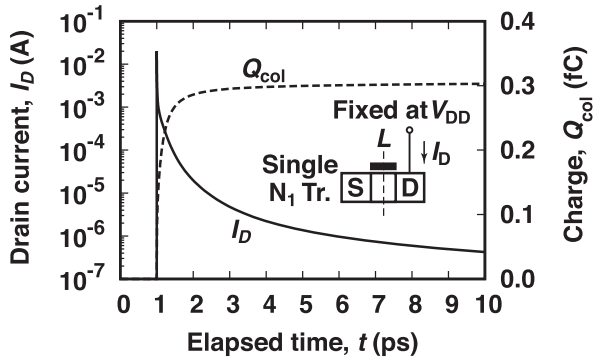

Fig. 12. Simulated transient drain current for the single N_1 biased at an OFF state where its drain terminal is fixed at 1.0 V while the others are grounded. An SE strikes at its center $L = 0.03$ fC/nm. The integral of the current converges on 0.30 fC.

chips. In this regard, this section investigates the potential for estimating β from single-transistor measurements.

As mentioned in the previous article [8], similar β are widely extracted from responses of single transistors. A transistor is situated and exposed to SE in the OFF state with its drain terminal biased at V_{DD}. The drain terminal collects

$$Q_{\mathrm{col(Tr)}} = \int_{t0}^{\infty} I_D \, dt \tag{15}$$

where I_D represents transient drain current, which can be measured with a proper apparatus [32], [33], [34], [35]. The bipolar gain for this transistor is then given by

$$\beta_{\mathrm{Tr}} = \frac{Q_{\mathrm{col(Tr)}}}{L d_{\mathrm{SOI}}}. \tag{16}$$

To investigate β_{Tr}, we performed another numerical device simulation (see Fig. 12). In the simulation, the structure of N_1 was exactly copied from the SRAM cell and situated in the OFF state where its drain terminal was constantly biased at V_{DD} while the others grounded. The simulated single-N_1 response exhibited $Q_{\mathrm{col(Tr)}}$ of 0.30 fC under the same SE condition as that investigated in Fig. 10. The resultant $Q_{\mathrm{col(Tr)}}$ of 0.30 fC corresponds to $\beta_{\mathrm{Tr}} = 1.0$, which is almost the same as those obtained by integrating the SRAM internal current and extracted by using the factor of 5 (see Table III). As a result of the introduction of the factor of 5, the favorable agreement has appeared, suggesting a possible estimation of β for the SRAM cross section curves from single-transistor drain–current measurements. This possible estimation would be worth a future investigation.

VI. Conclusion

The common 1/100-based definition of threshold LET (L_T) for SEU cross section curves suggested a missing factor of 5 in the original expression. This suggestion turned into a hypothesis that $L_T = L_e/5$, where L_e expresses a characteristic parameter that determines the exponential slope. This hypothesis was supported by the results of the numerical device simulation. A comparison with experimental data also suggested its validity. Therefore, this factor is recommended, and the expression for the model should be revised as follows

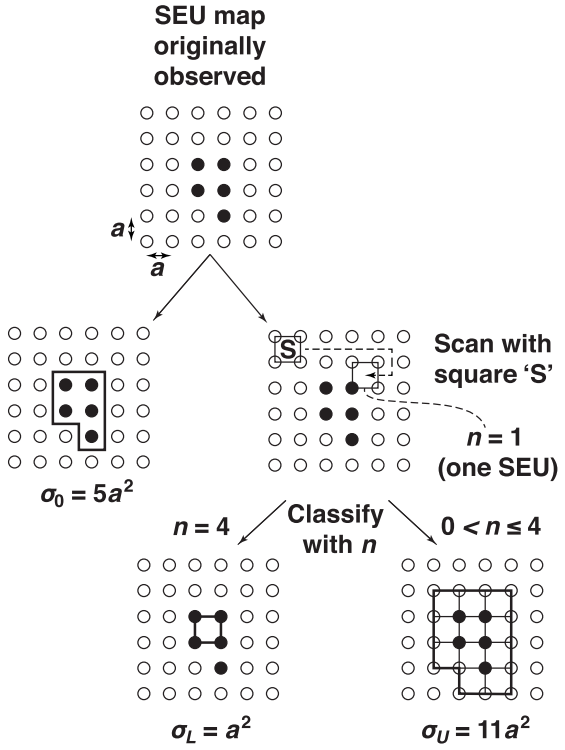

Fig. 13. Method used in this study for extracting the uncertainty of σ.

(see the text for the symbols):

$$\begin{aligned}\sigma &= \frac{A}{2}\exp\left(-\frac{5\zeta C_L}{\beta d_{\mathrm{SOI}}}\frac{V_{\mathrm{DD}} - V_{\mathrm{DR}}}{L}\right) \\ &= \frac{A}{2}\exp\left(-\frac{5Q_C}{Q_{\mathrm{col}}}\right) \\ &= \frac{A}{2}\exp\left(-\frac{5L_T}{L}\right) \\ &= \frac{A}{2}\exp\left(-\frac{L_e}{L}\right).\end{aligned}$$

The introduction of the factor of 5 also suggested a possible estimation of the bipolar gain β for the SRAM cross section curves from single-transistor drain–current measurements.

Appendix A
Uncertainty of σ

Suppose a map shown in Fig. 13(top), which exhibits a cluster of five SEU points in a scan with a constant step of a nm. The number of five straightforwardly yields $\sigma_0 = 5a^2$, as illustrated in the figure (middle and left). We used this value as a representative value of cross section and plotted by a symbol in Figs. 8 and 9. We then estimated the upper bound (σ_U) from the minimum ring of No SEU points that surrounds the SEU points [Fig. 13(bottom and right)]. On the other hand, the lower bound (σ_L) was estimated from the maximum ring of SEU points (bottom and left).

There might be a statistically better way to estimate the upper and lower bounds. Our method is, however, easy to be implemented in a computer code. The bounds can be identified by scanning a square "S", which is defined by four adjacent SE strike points [Fig. 13(middle and right)]. Each square "S"

has the area of a^2 and is classified with how many of its four corners are SEU points (n). Counting the number of squares with $n = 4$ provides σ_L whereas σ_U with $0 < n \leq 4$.

APPENDIX B
UNCERTAINTY OF L

We conducted a preliminary simulation experiment using the N_1 transistor. The amounts of charge deposited in N_1 under various SE conditions were then extracted and compared with values theoretically estimated from (14). We confirmed that their differences overall ranged within 10%. Note that in the extraction of deposited charge, a hole counting technique was used [36]. In the present study, counting holes at the drain and source terminals of N_1 provides the amount of charge deposited in it. This is because the number of holes deposited inside the transistor is expected to be preserved, in theory (unless other computational errors occur), thanks to the omission of generation and recombination processes. The holes are then discharged from the transistor region and detected at the source and drain terminals.

REFERENCES

[1] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2586–2594, Dec. 2000.

[2] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[3] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.

[4] C. Slayman, "Soft errors—Past history and recent discoveries," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep.*, Oct. 2010, pp. 25–30.

[5] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[6] P. Roche, J.-L. Autran, G. Gasiot, and D. Munteanu, "Technology downscaling worsening radiation effects in bulk: SOI to the rescue," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 766–769.

[7] D. Kobayashi, "Scaling trends of digital single-event effects: A survey of SEU and SET parameters and comparison with transistor performance," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 2, pp. 124–148, Feb. 2021.

[8] D. Kobayashi et al., "An SRAM SEU cross section curve physics model," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 232–240, Mar. 2022.

[9] E. L. Petersen, J. C. Pickel, J. H. Adams, and E. C. Smith, "Rate prediction for single event effects—A critique," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 1577–1599, Dec. 1992.

[10] L. D. Edmonds, "SEU cross sections derived from a diffusion analysis," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 3207–3217, Dec. 1996.

[11] P. Roche, J. M. Palau, G. Bruguier, C. Tavernier, R. Ecoffet, and J. Gasiot, "Determination of key parameters for SEU occurrence using 3-D full cell SRAM simulations," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1354–1362, Dec. 1999.

[12] D. Kobayashi et al., "Process variation aware analysis of SRAM SEU cross sections using data retention voltage," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 155–162, Jan. 2019.

[13] J. Bark et al., "Scaling of SEU mapping and cross section, and proton induced SEU at reduced supply voltage," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1342–1353, Dec. 1999.

[14] R. C. Harrington et al., "Empirical modeling of FinFET SEU cross sections across supply voltage," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1427–1432, Jul. 2019.

[15] D. Kobayashi et al., "Data-retention-voltage-based analysis of systematic variations in SRAM SEU hardness: A possible solution to synergistic effects of TID," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 328–335, Jan. 2020.

[16] G. C. Messenger and M. S. Ash, *Single Event Phenomena*. New York, NY, USA: Chapman & Hall, 1997.

[17] N. Kotani, "TCAD in Selete," in *Proc. Simulation Semiconductor Processes Devices (SISPAD)*, Leuven, Belgium, 1998, pp. 3–7.

[18] K. Hirose, H. Saito, Y. Kuroda, S. Ishii, Y. Fukuoka, and D. Takahashi, "SEU resistance in advanced SOI-SRAMs fabricated by commercial technology using a rad-hard circuit design," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2965–2968, Dec. 2002.

[19] P. Roche, J. M. Palau, K. Belhaddad, G. Bruguier, R. Ecoffet, and J. Gasiot, "SEU response of an entire SRAM cell simulated as one contiguous three dimensional device domain," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2534–2543, Dec. 1998.

[20] P. E. Dodd et al., "SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1893–1903, Dec. 2001.

[21] Y. Morita et al., "Smallest V_{th} variability achieved by intrinsic silicon on thin BOX (SOTB) CMOS with single metal gate," in *Proc. Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2008, pp. 166–167.

[22] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura, "Local V_{th} variability and scalability in silicon-on-thin-box (SOTB) CMOS with small random-dopant fluctuation," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 835–845, Apr. 2010.

[23] T. Ishigaki, R. Tsuchiya, Y. Morita, N. Sugii, and S. Kimura, "Effects of device structure and back biasing on HCI and NBTI in silicon-on-thin-box (SOTB) CMOSFET," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1197–1204, Apr. 2011.

[24] J.-P. Noel et al., "Multi-V_T UTBB FDSOI device architectures for low-power CMOS circuit," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2473–2482, Aug. 2011.

[25] *Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress*, JEDEC Solid State Technology Association Standard JESD28, Rev. A, Dec. 2001.

[26] *A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress*, JEDEC Solid State Technology Association, Standard JESD60, Rev. A, Sep. 2004.

[27] P. Oldiges, R. Dennard, D. Heidel, B. Klaasen, F. Assaderaghi, and M. Ieong, "Theoretical determination of the temporal and spatial structure of α-particle induced electron-hole pair generation in silicon," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2575–2579, Dec. 2000.

[28] P. E. Dodd and F. W. Sexton, "Critical charge concepts for CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 1764–1771, Dec. 1995.

[29] N. Tam et al., "Multi-cell soft errors at the 16-nm FinFET technology node," in *Proc. IEEE Int. Rel. Phys. Symp.*, Monterey, CA, USA, Apr. 2015, Paper 4B.3.

[30] J. D. Black, P. E. Dodd, and K. M. Warren, "Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1836–1851, Jun. 2013.

[31] G. Tsiligiannis et al., "Dynamic test methods for COTS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3095–3102, Dec. 2014.

[32] H. Schöne et al., "Time-resolved ion beam induced charge collection (TRIBICC) in micro-electronics," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2544–2549, Dec. 1998.

[33] V. Ferlet-Cavrois et al., "Charge enhancement effect in NMOS bulk transistors induced by heavy ion irradiation-comparison with SOI," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3255–3262, Dec. 2004.

[34] V. Ferlet-Cavrois et al., "Direct measurement of transient pulses induced by laser and heavy ion irradiation in deca-nanometer devices," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2104–2113, Dec. 2005.

[35] D. Kobayashi et al., "Waveform observation of digital single-event transients employing monitoring transistor technique," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2872–2879, Dec. 2008.

[36] D. Kobayashi, M. Aimi, H. Saito, and K. Hirose, "Time-domain component analysis of heavy-ion-induced transient currents in fully-depleted SOI MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3372–3378, Dec. 2006.