Single Event Effects in 3-D NAND Flash Memory Cells With Replacement Gate Technology

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***Abstract*— We studied the heavy-ion single event effect (SEE) response of 3-D NAND flash memory cells with charge-trap (CT)-based replacement gate (RG) technology. Error cross sections, threshold voltage shifts, and underlying mechanisms are discussed. The behavior of RG cells is compared with previous generations of flash NAND memory cells with floating-gate (FG) architecture, both planar and 3-D. The cell array structure, the technology parameters, and the materials impacting radiation susceptibility of the different types of cells are discussed.**

***Index Terms*— Flash memory cells, nonvolatile memory, radiation effects, single event effects (SEEs).**

I. Introduction

FLASH memories have experienced a change of paradigm during the last few years, as planar devices were replaced by 3-D devices, in one of the first examples of successful 3-D integration in the semiconductor chip industry. Because of the introduction of the vertical dimension, the 3-D structure allows designers to relax the requirements on the cell feature size (reliability issues are exacerbated as the number of electrons used to store information decreases), but at the same time increasing the storage density [1], [2], [3].

Since the first commercial products in 2014, 3-D NAND flash memory has rapidly evolved, by increasing the number of layers (from 24 to 176 and beyond) and the number of bits per cell (up to 4 bits per cells). A 232-layer 3-D NAND device is currently in development and a roadmap out to 500-plus layers has been recently announced by one of the major manufacturers. Together with the use of CMOS under array (CuA) technology, which further optimizes the use of the silicon area by placing the control circuitry underneath the memory array [4], this has resulted in an increase of the areal bit density from 0.96 to more than 10 Gb/mm^2 [5].

An impressing amount of research was carried out during the last years on different solutions to realize 3-D flash memories, in order to achieve these results. Mainstream architectures use the vertical channel technology, where cells are located at the intersection of vertical pillars with horizontal planes, constituting the word lines. Concerning the storage element, two major solutions are available for 3-D NAND flash arrays: floating-gate (FG) [4] and charge trap (CT) cells [5], with different materials used for the storage electrode. In FG devices, the storage element is conductive, made of polysilicon and isolated from its neighbors by dielectric layers. This option makes it possible to use a gate-first manufacturing process.

In CT arrays, the storage element is no longer conductive but consists of a trap-rich dielectric material, typically silicon nitride (SiN), which makes it possible to store charge in discrete sites to represent bits of information. The 3-D NAND flash with CT cells is usually referred to as replacement gate (RG) or gate-last technology, due to fact that the control gate is manufactured by replacing a sacrificial oxide layer during the last steps of the cell manufacturing process. Most of the major vendors of 3-D NAND flash today use the RG architecture. One of the benefits of the RG technology is that it requires larger holes to be punched across the stack of alternating layers, making it easier to create taller pillars and therefore denser arrays.

The 3-D NAND flash devices have immediately attracted the attention of the space and high-reliability community, due to their higher density and potential for improved radiation sensitivity [6], [7], [8] with respect to planar flash devices [10], [11], [12], [13]. The 3-D structure of the memories is also attracting interest toward the possibility of using these devices as ionizing radiation detectors, e.g., single event effect (SEE) monitors [17], [18], not only with heavy ions but also with indirectly ionizing particles, such as high-energy protons [19].

Previous works have explored the SEE and total ionizing dose susceptibility of 3-D NAND cells, targeting specifically the FG structure [14], [15], [16]. In terms of SEE, one of the conclusions was that the 3-D structure takes the SEE sensitivity back two or three technology generations, with respect to planar devices, for memory arrays using the FG technology [14], [16]. Differences in the post-rad threshold voltage distributions compared to planar devices

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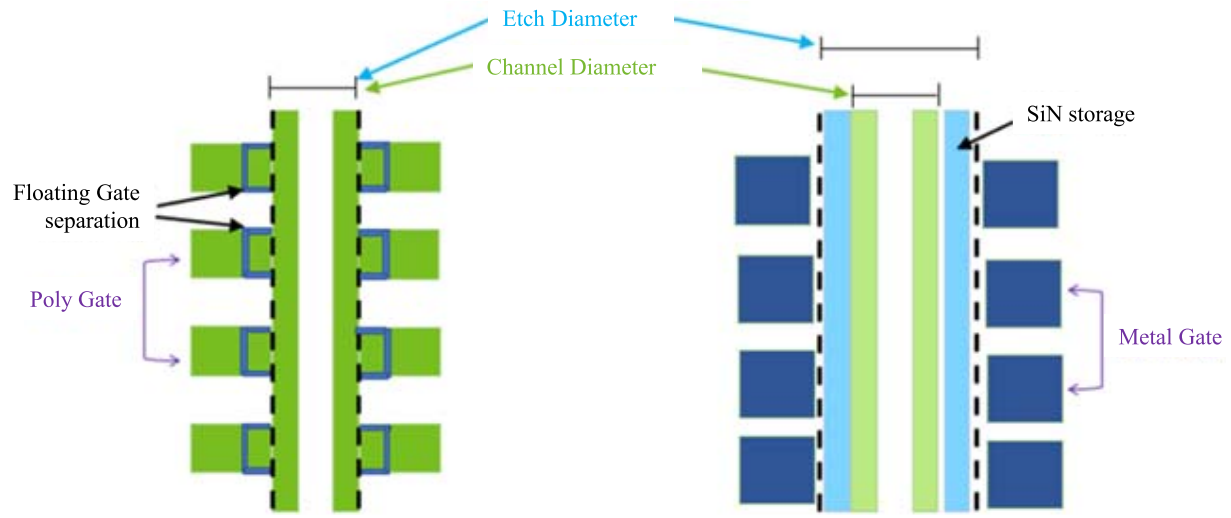

Fig. 1. Sketch of the vertical cross section of a 3-D NAND flash pillar with FG architecture (left) and RG architecture (right). Adapted from [20].

were identified and described, highlighting the presence of two peaks at high linear energy transfer (LET) values, corresponding to strikes in the tunnel and blocking oxides. Other works have explored the response of 3-D NAND flash commercial devices also using CT cells [6], [8], [9], but the lack of precise information on the architecture made it hard to decouple the response of the cell from the impact of the read-out scheme, placement of the reference voltages, and so on.

The purpose of this contribution is to explore the heavy-ion response of 3-D NAND RG devices, focusing on the CT cells. We will do this by analyzing changes in the threshold voltage due to heavy-ion strikes, thus leaving aside all the factors related to the peripheral circuitry. In the discussion, we will compare the new experimental RG results with previous data on 3-D and planar NAND with FG technology, pointing out the major differences between the two storage element solutions and their impact on the heavy-ion sensitivity.

This article is organized in the following way. Details of the studied devices, experimental setup, and irradiation are presented in Section II. Experimental results concerning cross section and threshold voltage shifts are described and discussed in Sections III and IV, respectively, highlighting similarities and differences between FG and RG architectures.

II. Devices Under Study and Experimental Details

The 3-D NAND flash test chips using CT RG technology provided by Micron Technology have been used in this work. They employ a gate-last cell with a SiN layer spanning the whole vertical pillar, band-engineered tunnel oxide, high-k blocking oxide, and tungsten wordlines [5].

Previous heavy-ion data on 3-D NAND FG devices were also collected on micrometer devices, which use a gate-first approach with a polysilicon storage element [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14].

A sketch illustrating the main structures of the pillars for the two types of 3-D NAND memory arrays is presented in Fig. 1. Both technologies use a gate-all-around (GAA) structure, with vertical channel (the green vertical elements in both left and right figure) and a storage element sandwiched between a tunnel oxide and a blocking oxide. The RG memories studied in this work (as well as the FG devices that are considered for comparison) are triple-level cell (TLC) devices, storing three bits in each cell, with eight different V_{th} (threshold voltage) levels, denoted as L0 (erased, lowest V_{th}) and L1–L7 (programmed, with progressively increasing V_{th}).

TABLE I
Details of the Heavy-Ion Beams Used in This Work

Facility	Ion species	Energy [MeV]	Surface LET in Si [MeVcm^2/mg]	Range in Si [μm]
HIF	C	131	1.3	269.3
	Ne	238	3.3	202
	Ar	353	9.9	114
	Cr	505	16.1	105.5
	Kr	769	32.4	94.2
	Xe	995	62.5	73.1
SIRAD	O	109	2.85	109
	Si	157	8.59	61.5
	Ni	220	28.4	33
	Ag	266	54.7	27.6

The 3-D NAND RG devices have been irradiated at the heavy-ion facility (HIF) in Louvain-la-Neuve, Belgium. The 3-D NAND FG samples have been irradiated with heavy ions at the SIlicon RADiation (SIRAD) line of the Legnaro National Laboratories (LNL) of Istituto Nazionale di Fisica Nucleare (INFN) in Legnaro, Padua, Italy. The details of the used heavy-ion beams are shown in Table I.

In all cases, the samples were irradiated unbiased, which is a relevant condition for nonvolatile memories (NVMs), especially when the cell behavior is under study. It is relevant to highlight that NVM cells are under bias only during erase/program/read and not in retention mode, even if the chip is powered on; yet, different electric fields are present in the cell oxides, depending on the program level and independent of bias conditions, even when no external bias is applied. All heavy-ion exposures were performed with the beam perpendicular to the die surface, at room temperature,

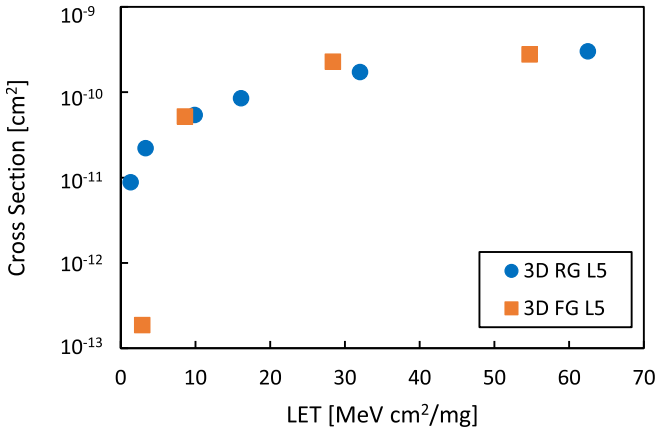

Fig. 2. Cross section (per cell) versus heavy-ion LET for SEE in 3-D RG NAND and 3-D FG NAND cells programmed to the same level (L5) before irradiation. The 2-σ Poisson error bars are smaller than the symbols.

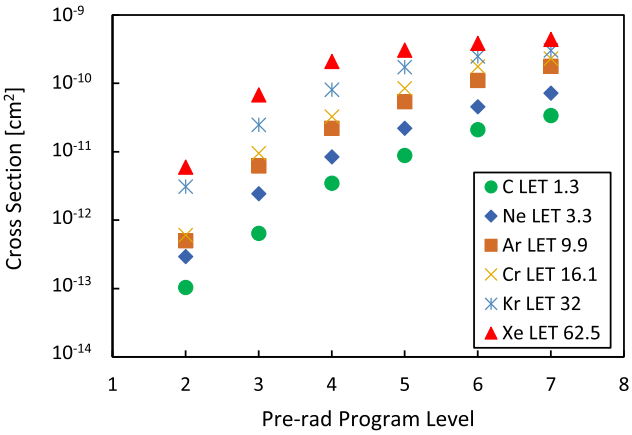

Fig. 3. Cross section (per cell) for heavy-ion-induced SEE in 3-D RG NAND cells that have been set to different program levels L2 to L7 before irradiation. The 2-σ Poisson error bars are smaller than the symbols.

in vacuum, and using particle fluences ranging from 10^7 to 3×10^7 ions/cm^2. It is worth highlighting that for all the beams used in this work, the range was high enough to cross the whole pillar, without significant LET variations, in both types of 3-D NAND flash memory arrays. Stopping and range of ions in matter (SRIM) simulations were performed, demonstrating that the LET change is negligible for cells located at the top and bottom of the pillar. In addition to irradiated devices, reference samples not exposed to heavy ions were considered, to account for possible effects not due to radiation.

III. Results

In order to compare the new results on RG devices with previous data in a meaningful way and understand the impact of heavy ions on the cells alone, we will first present cross-sectional data, not considering the number of errors, but instead the number of events leading to a threshold voltage shift above a certain value. This criterion corresponds to considering the number of cells that have lost more than a fixed number of electrons from the storage element (some hundreds). On the other hand, the number of errors depends not only on the cells but also on the read-out scheme. In fact, modern NAND flash devices feature several read-retry modes, making the use of errors even less suitable from the perspective of understanding the physical effects taking place on the cells. The cross section in the following is then calculated using the usual definition of events/fluence, where the number of events is equal to the number of cells with V_{th} below the set value.

Fig. 2 shows the heavy-ion SEE cross section calculated in this way for RG and FG devices (typical blocks are shown), using approximately the same initial V_{th} level, corresponding to program level L5. Remarkably, Fig. 2 shows that the cross sections at LET above 10 MeV·cm^2·mg^{-1} are pretty similar. At low LET, the Weibull curve falls less rapidly in the RG cells, signaling a lower threshold LET with respect to FG cells.

Fig. 3 shows the dependence of the cross section on the initial threshold voltage (program level). As in previous NAND flash devices, the higher the initial V_{th}, the larger the number

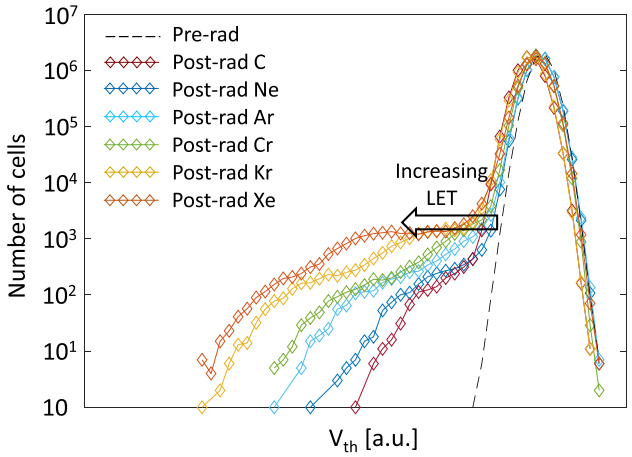

Fig. 4. Threshold voltage distributions before and after heavy-ion exposure for 3-D NAND cells with RG architecture programmed to the L5 level before irradiation. The delivered fluence was 1×10^7 ions/cm^2.

of events, but the trend is not linear and exhibits saturation at the higher program levels. The trend is consistent over the whole considered LET range.

In addition to cross sections, it is worth analyzing the impact of irradiation on the threshold voltage distributions and the shape of heavy-ion-induced tails.

Figs. 4 and 5 show the full V_{th} distributions before and after heavy-ion exposure for the RG and FG devices, respectively. As expected, the V_{th} shift increases with increasing LET. At high-LET values, RG memories do not clearly show the double peaks, which are instead evident in the FG [14]. At lower LET, the distribution shapes are similar in the two types of cell architectures. These V_{th} distributions will be explicitly compared in Section IV.

Fig. 6 shows a comparison of the average threshold voltage shift as a function of the ion LET in 3-D NAND RG cells, 3-D NAND FG cells, and two previous generations of planar NAND cells. The points at the same LET also have comparable values of the ion energy. 3-D NAND cells were programmed to the L5 level before ion exposure. The average shift in both 3-D FG and RG cells is smaller than that observed in 41 nm and comparable to that reported for 90-nm planar NAND flash.

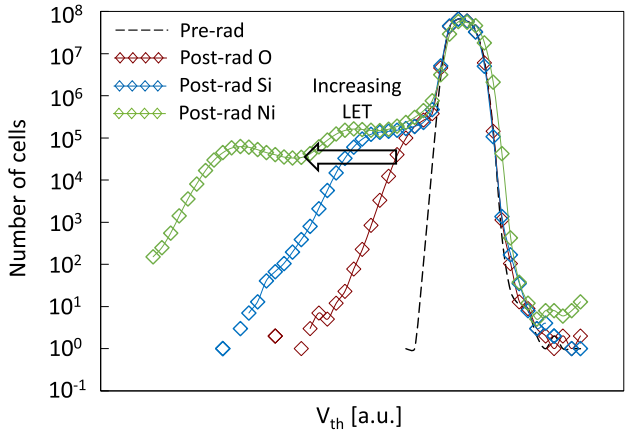

Fig. 5. Threshold voltage distributions before and after heavy-ion exposure for 3-D NAND cells with FG architecture programmed to the L5 level before irradiation. The delivered fluence was 3×10^7 ions/cm^2.

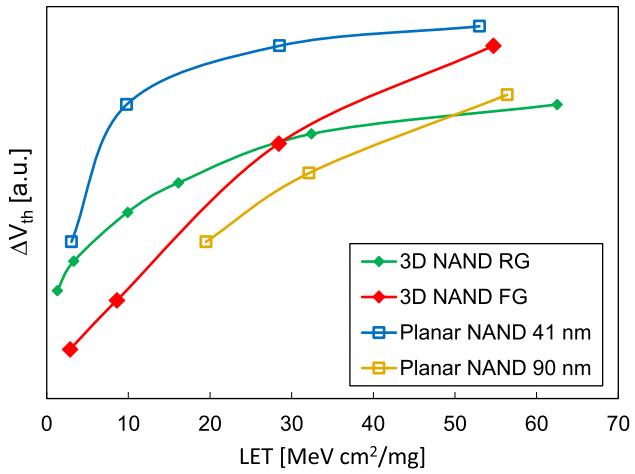

Fig. 6. Heavy-ion-induced threshold voltage shift versus LET in 3-D NAND cells with RG and FG architecture programmed to the L5 level before irradiation and exposed to high-LET ions. Average shifts are also reported for two previous generations of planar NAND flash memories.

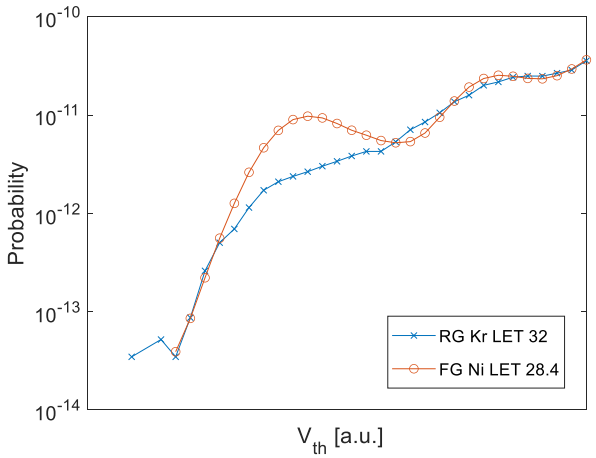

Fig. 7. Heavy-ion-induced threshold voltage tails in 3-D NAND cells with RG and FG architecture programmed to the L5 level before irradiation and exposed to high-LET ions.

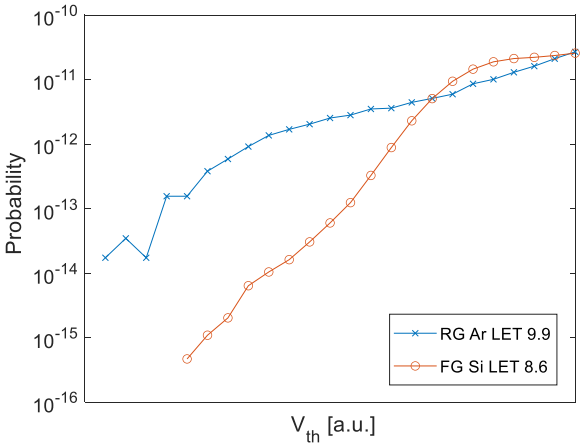

Fig. 8. Heavy-ion-induced threshold voltage tails in 3-D NAND cells with RG and FG architecture programmed to the L5 level before irradiation and exposed to medium-LET ions.

This confirms that, due to the 3-D structure (hence, the larger number of electrons used to store information in a memory cell), ion-induced SEE sensitivity is brought back to the levels it was for planar NAND belonging to several generations ago [12], [14].

Figs. 7–9 more closely compare the V_{th} distributions in RG and FG cells, focusing on ion-induced tails and highlighting the quantitative differences for LETs around 30 MeV·cm^2·mg^{-1} (see Fig. 7), 10 MeV·cm^2·mg^{-1} (see Fig. 8), and 3 MeV·cm^2·mg^{-1}(see Fig. 9). The range of threshold voltages shown in the x-axis of Figs. 7–9 is that of interest for heavy-ion-induced V_{th} tails. Again, the plots are referred to cells programmed to the L5 level before irradiation, for both RG and FG cells.

IV. Discussion

Although the two cell technologies are profoundly different, some parts of their heavy-ion response are remarkably similar. Indeed, we have shown in Section III that the saturation cross section (as previously defined) does not change appreciably in FG and RG cells, and it is in the order of some 10^{-10} cm^2 (per bit), corresponding to a circular area with a diameter of about 100 nm. Noticeably, the values in Fig. 2 are consistent with user mode cross sections previously published on 3-D NAND CT [6] and FG [7] cells.

We will now discuss the major differences between the two cell implementations and show how they can impact on the heavy-ion sensitivity.

Both architectures use a GAA structure, where an annular storage element is sandwiched between a tunnel oxide and a blocking dielectric layer. The RG CT technology uses a continuous layer for the storage elements, contrary to the FG technology, where the storage electrodes belonging to the same pillar are insulated (see Fig. 1). Indeed, given the conductive nature of FGs, adjacent cells in the same pillar need to be physically separated, i.e., mutually insulated. This is not needed for CT cells.

As a result, a heavy-ion strike can in principle affect also the region between adjacent cells (i.e., between the wordlines) in the CT architecture because the charge storing nitride layer is present also there. However, if we consider only the primary effect of heavy ions, which, as reported multiple times in the past, is the charge loss from the storage element

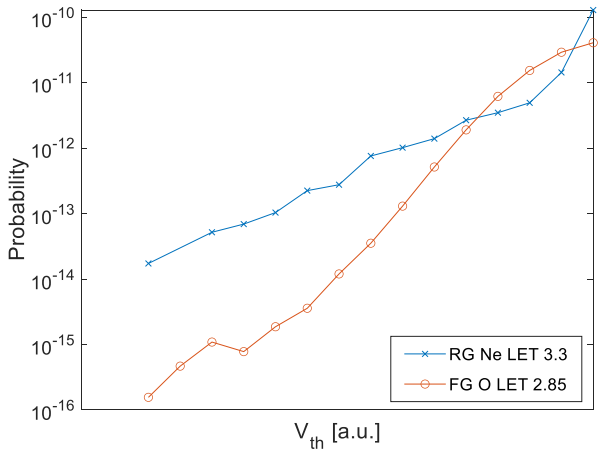

Fig. 9. Heavy-ion-induced threshold voltage tails in 3-D NAND cells with RG and FG architecture programmed to the L5 level before irradiation and exposed to low-LET ions.

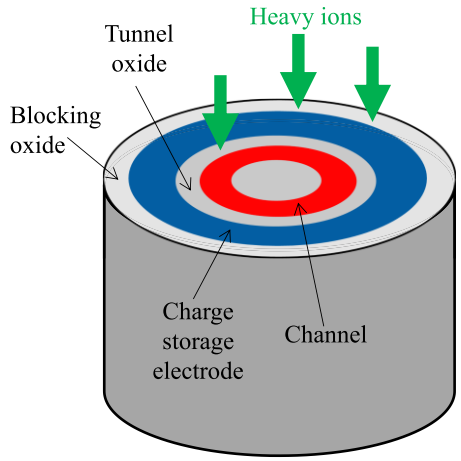

Fig. 10. Sketch of a 3-D NAND flash memory cell, mimicking the effect of heavy ions impinging at normal incidence with respect to the die surface. The figure is not to scale.

through the onset of a transient conductive path [14], no charge should be stored in the dielectric between the cells, and therefore, no charge should be removed. This is true unless charge migration occurred between the cells, which is an issue potentially affecting this type of CT architecture [5]. Radiation-induced charge trapping might take place, but this was shown not to be a factor in the past for planar CT-based memory cells [21].

The dielectric layers around the storage elements serve the same purposes (tunnel and blocking, respectively) in FG and CT cells, but they are optimized very differently. In particular, band engineering is used to improve the tunnel dielectric in CT cells, enhancing the erase performance. In short, this solution works by reducing the injection barrier when the erase voltage is applied and by keeping it high in retention mode [5]. High-k oxides with metal gates are used in CT cells as blocking oxides, to avoid back injection of electrons during erase, whereas an oxide–nitride–oxide (ONO) stack is used as tunnel oxide [5]. On the other hand, an ONO stack is typically used as the blocking dielectrics and SiO_2 for the tunnel dielectrics for FG cells.

Because of the different bandgaps, heavy-ion-induced charge generation (and consequently the current injected through the transient leakage path) in the layers surrounding the storage element is different for FG and CT cells. High-k oxides have a smaller bandgap, which results in a larger number of electron–hole pairs being generated by impinging heavy ions in the blocking oxide of CT cells.

The band-engineered tunnel layer in CT devices uses an ONO stack (i.e., qualitatively the same element used as the blocking oxide in FG) or a film with an engineered nitrogen profile [5]. A heavy-ion-induced transient path generated in such layers can be modeled as the series of multiple components, with more e–h pair generated in the nitride compared to the fully SiO_2 tunnel oxide in FG.

Thicknesses and electric fields in the oxides need also to be considered to model the impact of the heavy-ion strike. All things considered, no large differences in the heavy-ion-induced transient paths are expected.

A remarkable point is the thickness of the storage element that is smaller in the CT architecture, which causes the tunnel and blocking dielectrics to be closer together in the CT cells with respect to FG. The surrounding oxides together with the reduced thickness of the element used to store charge might well explain the observed difference in the shapes of the threshold voltage distributions, with two distinct peaks in the FG and a more gradual response in the CT at high LET (see Fig. 7). It is worth to recall that previous work explained the appearance of two distinct peaks in 3-D NAND FG cells with the fact that ions can hit the device on the different elements of the cell with different probabilities and different effects [14]. As highlighted in Fig. 10, particles impinging on the chip at normal incidence can hit the tunnel oxide, dielectric layer, storage element, or parts of them. At high LET in 3-D FG, two peaks appear (see Fig. 7), due to the different cross section and charge collection efficiency (proportional to the electric field) in the tunnel and blocking oxides. With the large separation in the FG cells, the blocking and tunnel layers can be hit separately by a heavy ion, something not possible (or much less likely) in the CT architecture. This might also be the reason why the charge loss is not so much reduced in CT devices, as one would expect because of the discrete trapping sites, assuming that the radiation-induced transient paths were similar. Indeed, an important difference between FG and CT is the discrete nature of the trapping sites in the storage layer of CT compared to the conducting FG, where the charge is stored on the surface. This should lead to a smaller charge loss in CT devices since the onset of a radiation-induced localized leakage path will not discharge the whole cell, but only a fraction of it. However, the fact that the heavy-ion track can affect to a large extent both the tunnel and the blocking layer at the same time in CT devices might offset this advantage, leading to a similar heavy-ion response.

Some considerations can be made also about the wordline and the channel materials, although these are not expected to impact significantly on the heavy-ion response. With scaling, research has been carried out to improve the channel material, moving away from polysilicon, which might cause a too high resistivity when pillars are very tall, but the tested memories

both use the most common polysilicon solution. Wordlines are made of polysilicon in FG and tungsten in CT. We do not expect this to have a significant impact on the threshold voltage shifts induced by heavy ions since the resistivity of the radiation-induced conductive path is basically determined only by the carrier concentration in the oxides surrounding the storage element and electric fields therein.

Finally, we have to note that this discussion is assuming that the electric fields are similar when using the same logic level in the two types of 3-D NAND flash arrays (namely, L5 program levels were compared in this work). This might not be necessarily the case and the different electric field (e.g., higher in the CT devices) might play a role in the response to ionizing radiation. The precise assessment of the electric field in the oxides is a complex issue that needs TCAD simulations and will be carried out in future work.

V. Conclusion

The response of 3-D NAND flash memory arrays with RG technology and CT cells has been experimentally measured and analyzed. The error cross section has been studied, considering the number of cells experiencing a threshold voltage shift larger than a given value. This method allowed a meaningful comparison with 3-D NAND cells using the FG technology, in order to understand the effects of radiation on the cells alone, without the impact of read-out protocols. The threshold LET is lower in RG cells compared to FG cells, but the cross section at medium and high LETs is comparable. The impact on threshold voltage distributions was also analyzed, studying the shape of ion-induced tails and threshold voltage shift absolute values. The reasons why the sensitivity stays at levels consistent with FG devices in spite of the presence of discrete trapping sites have been discussed, highlighting the differences between the two technologies, in particular, the materials and the role played by the reduced thickness of the storage layer in the CT architecture.

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