Neural-Network-Based Automated Synthesis of Transformer Matching Circuits for RF Amplifier Design

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***Abstract*— Rich experience and intuition play important roles in designing planar transformers (TFs) for contemporary radio frequency integrated circuits (RFICs). In general, RFIC designers have been heavily relying on multiple iterations of full electromagnetic (EM) simulations, which consumes much time and effort. Here, we propose an automated matching circuit synthesizer (AMCS) using neural networks (NNs). The proposed AMCS directly synthesizes a matching circuit combined with a TF throughout the entire design process, ranging from the desired performance to layout. In the AMCS, which is a "spec-to-layout" synthesizer, one NN returns physical parameters of matching circuits, and another NN estimates the electrical performance in two-port *S*-parameters from the desired impedances. Before the NNs are trained, input feature design is conducted to avoid the one-to-many problem, which cannot be well characterized with an inverse NN. This significantly reduces the time and effort for iterative circuit and EM simulations. The AMCS generated the matching circuit layouts for simple single-stage amplifiers operating at different frequencies up to 70 GHz or in different bandwidths of up to 32.5%. The estimated *S*-parameters of the amplifiers show good agreement with the EM simulation results.**

***Index Terms*— Automated synthesis, neural network (NN), radio frequency (RF) amplifiers, radio frequency integrated circuit (RFIC), transformer (TF).**

I. Introduction

PLANAR transformers (TFs) based on multilevel backend thick metallization technologies have been commonly used as impedance matching circuits (MCs) in contemporary millimeter-wave (mm-wave) CMOS circuits for a compact layout and broadband operation [1], [2], [3], [4], [5], [6], [7], [8]. However, the common equivalent models of TFs consisting of inductors, coupling factors, and parasitic capacitors and resistors are inaccurate at mm-wave or terahertz (THz) frequencies because of the distributed behavior of the parasitic elements [9]. Thus, characterizing TFs by electromagnetic (EM) simulations is a common method for mm- or THz-wave circuit design. Moreover, because of the inaccuracy of empirical or theorical models, multiple iterations between the initial guess in the equivalent circuit models and EM simulations are always required, which are very time-consuming and require experience-based knowledge.

There have been various efforts to develop automated circuit synthesis systems for digital as well as analog circuits. Genetic algorithms (GAs) have been used for topology selection and compact layouts in analog amplifiers [10], [11]. Power dissipation of an analog circuit was optimized with a GA [12]. A neural network (NN) with a rider optimization algorithm (ROA), RideNN, has been studied for fault diagnosis [13]. Moreover, a feedforward NN with a GA has been studied to make an automated synthesis system for operational amplifiers [14] in analog circuits.

Automated circuit synthesis techniques for radio frequency (RF) circuits have also been developed in order to mitigate iterative tasks such as model-order reduction [15]. A least-squares fitting algorithm has been studied to extract a spiral inductor's equivalent circuit [16], and analysis and simulation of inductors and TFs for integrated circuits (ASITIC) have been studied to design tunable inductors [17], [18]. In addition, a GA has been employed for optimizing the figure of merit (FoM) of low-noise amplifiers [19].

Machine-learning-based differential evolution has been suggested as a way to synthesize passive elements such as inductors and TFs at a single frequency [20]. Furthermore, under a smoothness assumption that similar design parameters have similar performance, general mm-wave integrated circuit (IC) synthesis based on differential evolution assisted by a Gaussian process model has been proposed to optimize inductors and TFs [21], [22]. A multilayer perceptron has been leveraged to predict the operation of square microstrip spiral inductors [23]. A knowledge-based NN with the concept of space mapping had been researched to synthesize microstrip bandpass filters [24].

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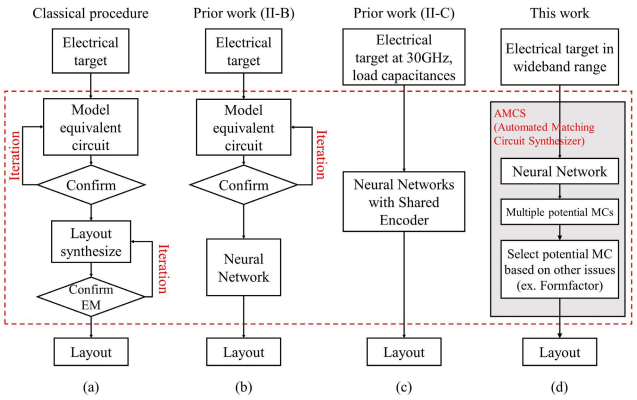

Fig. 1. Comparison of (a) classical design cycle for TFs, (b) prior work based on an equivalent circuit model, (c) prior work based on an NN with a shared encoder, and (d) proposed design cycle with the AMCS in this work.

Inverse modeling has been proposed to synthesize *LC* filters or microstrip filters [25], [26], [27] using an NN that takes electrical performance as input and layout as output. In order to synthesize TFs, inverse modeling has been employed to replace such iterative tasks [28], [29].

In this article, an NN-based automated matching circuit synthesizer (AMCS) is proposed. The AMCS suggests that MCs combined with a TF and shunt capacitors and thus have the potential to replace all the time-consuming processes in single-stage RF amplifier design (i.e., synthesize MCs). It determines the desired performance, such as output impedances in a wideband frequency range, and then directly returns TF layouts and shunt capacitors that satisfy the desired performance requirements without additional procedures. In the AMCS, two NN cores are trained. One generates multiple potential layouts that can match the given core transistors to 50 Ω, and the other returns the estimated performance of the auto-generated MCs. Then, the designer selects the most suitable layout based on the MCs' performance and addresses other issues that were not included in the NN such as the form factor, as shown in Fig. 1(d). The relationship between the target matching impedance and the MC layout is fundamentally a one-to-many problem and thus cannot be completely characterized by standard feedforward NNs [30]. In this work, an input feature design was conducted by utilizing the quality factor (Q-factor) and insertion loss (IL) of TFs as input features to relax the one-to-many problem. The MCs were generalized to consist of a TF and capacitors to match the input and output impedances of core transistors to an external 50-Ω source and load terminals. The key innovation introduced in this work is a direct MC synthesis method and a solution for the one-to-many problem for training NNs with the human-in-the-loop (HITL) concept. To demonstrate the effectiveness of these innovations, we present design examples of MCs for single-stage amplifiers operating at different frequencies up to 70 GHz or in different bandwidths of up to 32.5%.

Section II covers prior research on automated synthesis systems for RF circuit design and describes the purpose of this work. Section III describes the primary issue of an AMCS based on NNs and proposes the main idea for a solution and the structure of the AMCS. Section IV presents the basic information about NN training and the results. Section V discusses another NN that can predict MC characteristics. Design examples obtained with the AMCS at various frequencies and bandwidths are provided in Sections VI and VII, respectively. Section VIII discusses the limitations of the proposed AMCS and summarizes this article.

II. RFIC Design With TF Matching Circuits

Recently, TFs have been widely used as impedance MCs or signal baluns in CMOS RF circuits, in particular for those operating at mm-wave frequencies. TFs provide a compact layout and broadband operation. However, unlike capacitors, it is hard to directly synthesize TF layouts at high frequencies even with accurate material and dimension parameters due to the distributed nature of parasitic elements associated with TFs. This section briefly compares the design procedure between the classical and automated synthesis techniques, including the one proposed in this work for MCs, and presents the proposed AMCS.

A. Classic MC/TF Synthesis

In the classic RF circuit design process, for which a brief flowchart is shown in Fig. 1(a), designers first select matching impedance Γ_s and Γ_L from the characteristics of core TRs for the desired performance in, for instance, power, gain, or noise. To match the given source and load impedances to Γ_s and Γ_L, respectively, one may start to design the MCs with equivalent circuits, which is an iterative task. Once the equivalent circuit parameters are fixed, an initial MC layout should then be drawn based on the designers' experience. Due to the distributed parasitic elements, the equivalent circuit models cannot accurately represent nor estimate the actual characteristics of the TFs, and thus, for recent mm-wave radio frequency integrated circuits (RFICs), the layout is commonly verified by the EM simulation, which is also an iterative and time-consuming task. The iterative task between layout and EM simulation is continued until the EM simulation results satisfy the desired performance, as shown in Fig. 1(a). Due to the recent progress in high-performance computing hardware and accurate numerical simulators, the overall time consumed for the iterative task has been significantly reduced. However, the absence of a direct synthesis method for TFs fundamentally limits the degree of optimization and design throughput.

B. Automated TF Synthesis Techniques

There have been a few efforts to develop automated TF synthesizers for RF MCs. Munzer *et al.* [28] presented an NN-based synthesis technique that can address all design aspects, from the equivalent model parameters to the layout. Fig. 1(b) shows the design flow. As can be seen, the most time-consuming task between the layout and EM simulation can be avoided, but any inaccuracy of the equivalent model will be reflected in the final design.

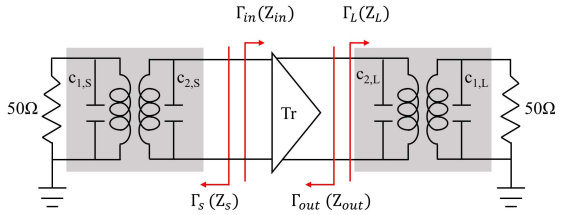

Fig. 2. Single-stage amplifier matching situation assumed in AMCS.

C. Direct Synthesis Techniques for MC Consisting of TF and Shunt Capacitors

In [29], further direct generation of TF layouts from the desired matching impedance was presented using a shared encoder composed of two NNs, as shown in Fig. 1(c). However, in that work, the design frequency was fixed to 30 GHz, and the capacitance value affecting the required transformation ratio of the TF has to be provided by the designer as an input parameter.

D. AMCS (Automated Matching Circuit Synthesizer)

The ultimate "spec-to-layout" design process with an AMCS would be the direct generation of the most optimum MC layout from the matching impedances Γ_s, and Γ_L that the designer selects for the desired performance in the target frequency band, as shown in Fig. 1(d). Here, our aim is to propose the ultimate "spec-to-layout" design tool using NNs.

III. AMCS Description

A. Primary Issue in Training NN (One-to-Many Problem)

The proposed AMCS using NNs can produce an MC layout. The auto-synthesized MC along with shunt capacitors will match the desired impedance Z_{in} or Z_{out} to 50 Ω. In this work, we aimed to design a simple single-stage amplifier whose input and output are matched by the AMCS, as shown in Fig. 2. Obviously, the desired impedances should be input parameters. One of the naïve ways to implement an AMCS is to train a regression NN so that it directly predicts MC layouts from an input of desired target impedances. However, since there must be many diverse possible layouts resulting in the same impedance, modeling such a one-to-many relationship by any type of regression is ambiguous and may only provide a rough generic answer that would never be desirable [31], [32], [33]. Fundamentally, designing a two-port network with single port impedance is a kind of one-to-many problem that even NNs cannot converge to an optimum and realistic solution. For instance, it is expected that the NN returns the optimum combination of a TF and, if necessary, capacitors for matching the given impedance Z_m to 50 Ω, as shown in Fig. 3(a). However, as shown in Fig. 3(b), the given constraint can also be satisfied with a TF whose two ports are isolated (or the mutual coupling factor = 0) and with a shunt element whose impedance is equal to Z_m. This is one radical example, but to realize the design scenario shown in Fig. 1(d), the one-to-many problem needs to be carefully dealt with.

In addition, for wideband circuit design, the MCs should match the desired impedance, which is commonly a function of frequency in the operating frequency range. Thus, to accommodate wideband operation, the NN should deal with the series of desired impedances $Z_m(f)$ (or $\Gamma_m(f)$ as a reflection coefficient) with respect to the frequency.

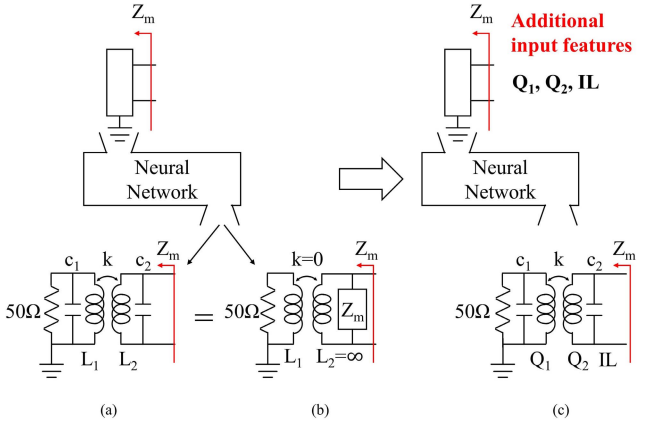

Fig. 3. Equivalent circuits of (a) MC that user desires, (b) MC unexpected from NN when input features are not designed, and (c) predicted MC from NN when input features are well designed.

B. Input Feature Design for Relaxing One-to-Many Problem

In the machine learning community, generative modeling has been introduced to overcome the limitation of regression in modeling one-to-many relationships [31], which are cumbersome to model, train, and use in practice. We take a different approach that, by tackling the design space of input features, is straightforward yet effective in relaxing the one-to-many relationship between MC layouts and impedances. We introduce domain-specific auxiliary constraints into inputs, which we call input feature design. Thereby, the desirable layout can be guided further by more specific inputs.

First, the one-to-many problem mainly arises from the limited information the designer can provide. It can be simply resolved if the full two-port parameters of the desired TF are provided. However, in general, estimating them is beyond the capabilities of even highly experienced designers. There are other electrical parameters that can be gauged by users and represent the full two-port characteristics, such as the Q-factors (Q_1 and Q_2) and IL of a TF [34]

$$Q_1(f) = \frac{\mathrm{Im}\left(Z_{\mathrm{TF},11}(f)\right)}{\mathrm{Re}\left(Z_{\mathrm{TF},11}(f)\right)} \tag{1}$$

$$Q_2(f) = \frac{\mathrm{Im}\left(Z_{\mathrm{TF},22}(f)\right)}{\mathrm{Re}\left(Z_{\mathrm{TF},22}(f)\right)} \tag{2}$$

and

$$\mathrm{IL}(f) = \frac{S_{\mathrm{TF},21}(f)}{S_{\mathrm{TF},12}(f)}\left(K(f) - \sqrt{K(f)^2 - 1}\right) \tag{3}$$

where $Z_{\mathrm{TF},ij}(f)$ represents the Z-parameters of TFs as a function of frequency. K is Rollett's stability factor defined as

$$K(f) = \frac{1 - \left|S_{\mathrm{TF},11}(f)\right|^2 - \left|S_{\mathrm{TF},22}(f)\right|^2 + |\Delta(f)|^2}{2\left|S_{\mathrm{TF},12}(f)S_{\mathrm{TF},21}(f)\right|} \tag{4}$$

$$\Delta(f) = S_{\mathrm{TF},11}(f)S_{\mathrm{TF},22}(f) - S_{\mathrm{TF},12}(f)S_{\mathrm{TF},21}(f). \tag{5}$$

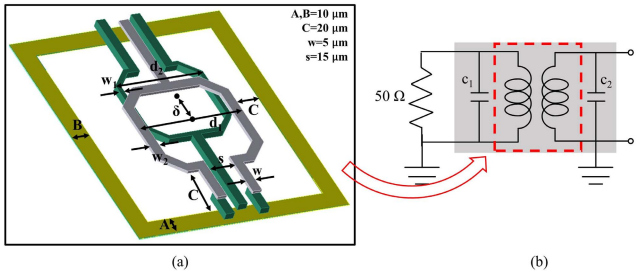

Fig. 4. Assumed (a) layout structure of TF and (b) MC in this work.

C. Inverse NN

As shown in Fig. 3(c), the NN for "spec-to-layout" synthesis, hereafter referred to as the "inverse" NN (INN), returns layout parameters of the MC from given input features [i.e., given features consist of the functions of frequency such as Q_1, Q_2, IL, and the desired impedances (Z_m)]. The MC assumed in this work consists of a TF and shunt capacitors, as shown in Fig. 4. The layout parameters are the TF layout parameters and the values of capacitive matching elements (c_1 and c_2), which are assumed, as shown in Fig. 4.

The input and output vectors of the INN, $\boldsymbol{x}$ and $\widehat{\boldsymbol{y}}_{\mathbf{MC}}$, are defined as follows:

$$\boldsymbol{x} = \left[\boldsymbol{f}, Z_m(\boldsymbol{f}), Q_{1,\min}, Q_{2,\min}, \mathrm{IL}_{\min}\right]^{\top} \tag{6}$$

$$\widehat{\boldsymbol{y}}_{\mathbf{MC}} = \left[\hat{d}_1, \hat{d}_2, \hat{w}_1, \hat{w}_2, \hat{\delta}, \hat{c}_1, \hat{c}_2\right]^{\top} \tag{7}$$

$$\widehat{\boldsymbol{y}}_{\mathbf{MC}} = \boldsymbol{INN}(\boldsymbol{x}). \tag{8}$$

To verify whether the designed input features relax the one-to-many problem and the training sets $\boldsymbol{x}$ and $\boldsymbol{y}_{\mathbf{MC}}$ are mapped one-to-one, as shown in Fig. 5(a), two additional reference input feature vectors, $\boldsymbol{x_{r1}} = [\boldsymbol{f}\ \mathbf{S_{MC}}(\boldsymbol{f})]$ and $\boldsymbol{x_{r2}} = [\boldsymbol{f}\ Z_m(\boldsymbol{f})]$, were prepared and used to train the INN. For the aforementioned reason in Section III-A, if the INN is designed with an input feature vector composed of only output impedances (Z_m), it would be a one-to-many system. As shown in Fig. 5(a), case (III) is a one-to-many system since the input feature vector ($\boldsymbol{x_{r2}}$) is only composed of output impedances. As can be seen in Fig. 5(b), $\boldsymbol{x_{r2}}$ leads to an NN converging with test error 2.154×10^{-2} larger than 10^{-4} (approximately equal to 1%) since $\boldsymbol{x_{r2}}$ only includes information about one port of the matching network, which means that it is a one-to-many problem. While the training result with $\boldsymbol{x_{r2}}$ does not converge well, the NN from $\boldsymbol{x_{r1}}$ [case (II)], including the full two-port S-parameters of the MC [$\mathbf{S_{MC}(f)}$], is expected to converge well. As can be seen in Fig. 5(b), the test error of training with $\boldsymbol{x}_{r1}$ [case (II)] was 3.730×10^{-4}, which is significantly lower than that in case (III), and this indicates that the one-to-many problem is relaxed well. On the other hand, the other input feature vector $\boldsymbol{x}$ [case (I)], which was designed in this work, consists of frequencies ($\boldsymbol{f}$), output impedances [$Z_m(\boldsymbol{f})$], Q-factors, and IL. The proposed one results in a 3.033×10^{-5} test error, which is also significantly better than that for $\boldsymbol{x_{r2}}$ [case (III)], 2.154×10^{-2}. The results indicate that the proposed input feature design effectively solves the one-to-many problem even with fewer input features. The NN has a simple multilayer

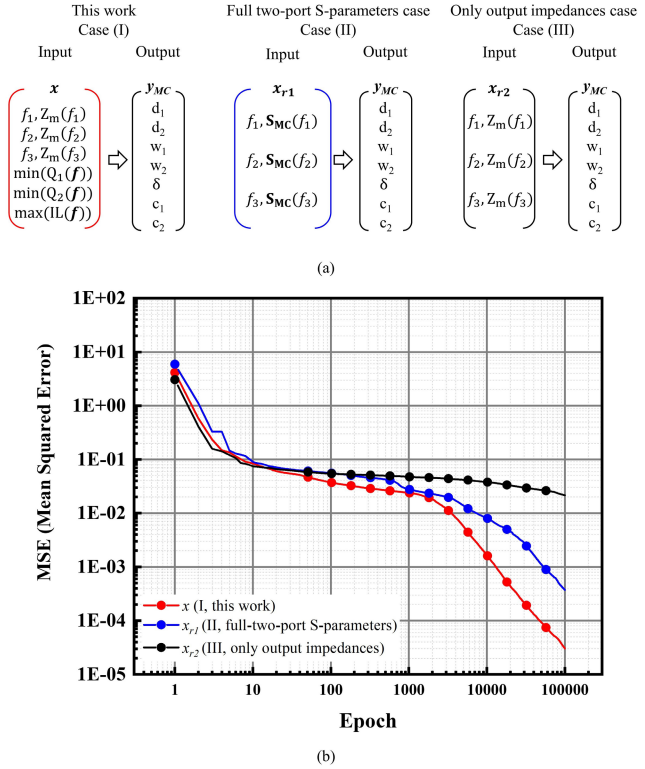

Fig. 5. Comparison among input feature case of (a) input and output vectors of INN. (b) Test error of INN [red: designed features in this work, blue: full two-port S-parameters, and black: only output impedances (Z_m)].

perceptron structure, which is set to 100×8, for all three input feature vectors, $\boldsymbol{x}$, $\boldsymbol{x_{r1}}$, and $\boldsymbol{x_{r2}}$.

It should be noted that, in general, designers do not seek specific values of Q_1, Q_2, and IL but can provide them as constraints. For instance, to achieve the target performance, they may guess that Q_1 should be at least greater than 9 based on their experience. There must be numerous potential circuits that satisfy the condition, and thus, this is still a one-to-many problem. However, unlike the two-port parameters, this problem can be dealt with by using an HITL architecture, in which the user makes the final decision among potential candidates.

Several studies have shown that NNs can solve a problem with constraints by using, for instance, a constraint violation penalty concept [35]. However, Q_1, Q_2, and IL of TFs in the MC cannot be simply judged with a single standard; the designer may comprehensively look at various performance parameters such as gain, return loss, or bandwidth and finally select a matching network from various possible ones, even if Q_1, Q_2, or IL is slightly worse than expected one. To deal with this particular problem, we employed the concept of HITL in this work [36], where the user makes the final decision. Definitions of input and output variables and a brief algorithm of an AMCS consisting of two NNs are shown in Fig. 6 and Algorithm 1.

The overall flowchart of the AMCS is given as follows.

1) The user enters three target frequencies ($\boldsymbol{f}$), three desired impedances [$Z_m^{\star}(\boldsymbol{f})$], and minimum and

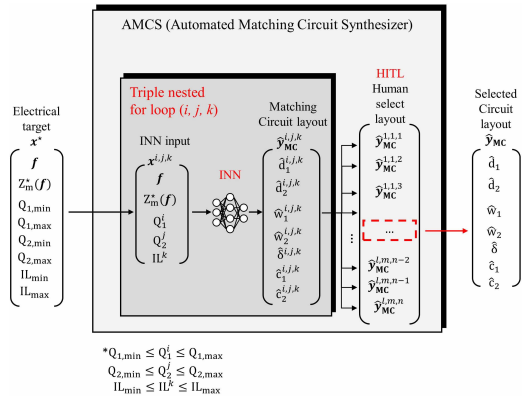

Fig. 6. Structure of AMCS.

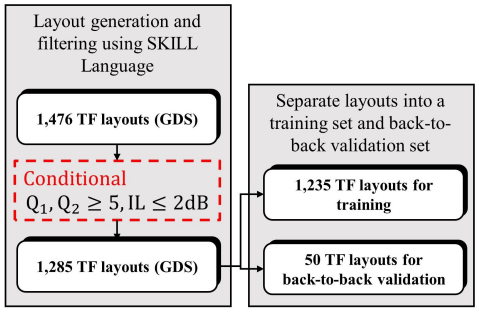

Fig. 7. Preparation and separation of TF dataset.

Variables

$\boldsymbol{f} := [f_1, f_2, f_3]$, design frequencies
$Z_m^*(\boldsymbol{f})$:= desired impedances at each frequency
$Q_{1,min}Q_{1,max}$:= Min, Max constraint of primary turn'Q factor
$Q_{2,min}, Q_{2,max}$:= Min, Max constraint of secondary turn'Q factor
IL_{min}, LL_{max} := Min, Max constraint of IL
$\boldsymbol{x}$:= input vector of INN
$\hat{\boldsymbol{y}}_{\mathbf{MC}}$:= predicted structure parameters of MC
MClist := List of candidates of MC

Algorihtm 1 Pseudo Code of AMCS

Input: $\boldsymbol{f}, Z_m^*(\boldsymbol{f}), Q_{1,\,min}, Q_{1,\,max}, Q_{2,\,min}, Q_{2,\,max}, IL_{min}, IL_{max}$
Output: **MClist**
define: **FoM**
count = 1
$Q_1 = [Q_{1,min}, Q_{1,min}+1, \ldots, Q_{1,max}]$
$Q_2 = [Q_{2,min}, Q_{2,min}+1, \ldots, Q_{2,max}]$
$IL = [IL_{min}, IL_{min}+1, IL_{min}+2, \ldots, IL_{max}]$
for $i = 1$: **do**
  for $j = 1$: m **do**
    for $k = 1$: n **do**
      $\boldsymbol{x} \leftarrow [\boldsymbol{f} Z_m^*(\boldsymbol{f}) Q_1(i) Q_2(j)\, IL(k)]$
      $\hat{\boldsymbol{y}}_{\mathbf{MC}} := [\hat{d}_1\ \hat{d}_2\ \hat{w}_1\ \hat{w}_2\ \hat{\delta}\ \hat{c}_1\ \hat{c}_2] \leftarrow \boldsymbol{INN}(\boldsymbol{x})$
      MClist(count)$\leftarrow \hat{\boldsymbol{y}}_{\mathbf{MC}}$
      count $\leftarrow$ count +1
    end for
  end for
end for
Sort MClist according to **FoM**
Return MClist

maximum acceptable bounds of Q-factors ($Q_{1,min}$, $Q_{1,max}$, $Q_{2,min}$, $Q_{2,max}$) and IL (IL_{min}, IL_{max}).

2) The AMCS iterates the INN for various potential combinations of Q_1, Q_2, and IL that satisfy the limits specified by the user. MC layout parameters from the INN are saved along with the user-defined FoM.
3) The AMCS lists the outputs in terms of, for instance, the FoM, and the user selects one of the top candidates, which is an implementation of HITL in this work.

IV. Inverse NN Training

A. Learning Data Preparation

In this work, the TF in the MC was assumed to have a simple 1:1 octagonal shape [Fig. 4(a)]. First, layout samples [graphic design system (GDS)] for training were prepared by using SKILL language and PCELL. EM simulations were conducted, using shell script, at up to 100 GHz for various TF layouts whose dimensions were swept as follows: diameters (d_1, d_2) from 70 to 210 μm in 20-μm steps, widths (w_1, w_2) from 5 to 10 μm in 2.5-μm steps, and offsets between primary and secondary TFs (δ) from 0% to 30% of bigger diameters in 10% steps. Fixed parameters were the widths of the guard ground ring (A, B), 10 μm; the spacing from the ground (C) to the edge of TFs, 20 μm; the spacing between differential feeding lines, 15 μm; and the width of the feeding lines, 5 μm. d_2 was forced to be in the range of 70%–130% of d_1. Then, 1476 TF samples were prepared, and samples that had poor performance, namely, a Q-factor lower than 5 and IL bigger than 2, were excluded. Finally, a total of 1285 samples were prepared, and 50 of them were used as back-to-back validation test samples, as shown in Fig. 7.

To train the INN to return the MC structure parameters, such as the layout parameters of the TF and values of shunt capacitors, as shown in Fig. 4, simple circuit simulations were conducted with the S-parameters and capacitors of the TF samples in the range of [0, c_{max}], where c_{max} is defined as

$$c_{1,max} = \frac{1}{(2\pi f)^2 L_1} \tag{9}$$

$$c_{2,max} = \frac{1}{(2\pi f)^2 L_2} \tag{10}$$

where L_1 and L_2 are inductances of the TF's primary and secondary turn, respectively, which are defined as

$$L_1 = \frac{\mathrm{Im}(Z_{TF,11})}{2\pi f} \tag{11}$$

$$L_2 = \frac{\mathrm{Im}(Z_{TF,22})}{2\pi f}. \tag{12}$$

A brief flowchart of data preparation for the INN is shown in Fig. 8. The detailed pseudocode and notation of data preparation are described in Fig. 9 and Algorithm 2. From the circuit simulation, output impedances $[Z_m(\boldsymbol{f})]$ of all possible MCs were extracted. Finally, 79 625 pairs of input and output vectors $(\boldsymbol{x}, \boldsymbol{y}_{\mathbf{MC}})$ were extracted from the EM and circuit simulations for the supervised learning of the INN. GDS generation took 1.1 s for each TF layout, so, totally, it took about 27 min. The EM simulation took about 25 s for each TF layout, so, totally, it took 10 h on a Linux server (AMD

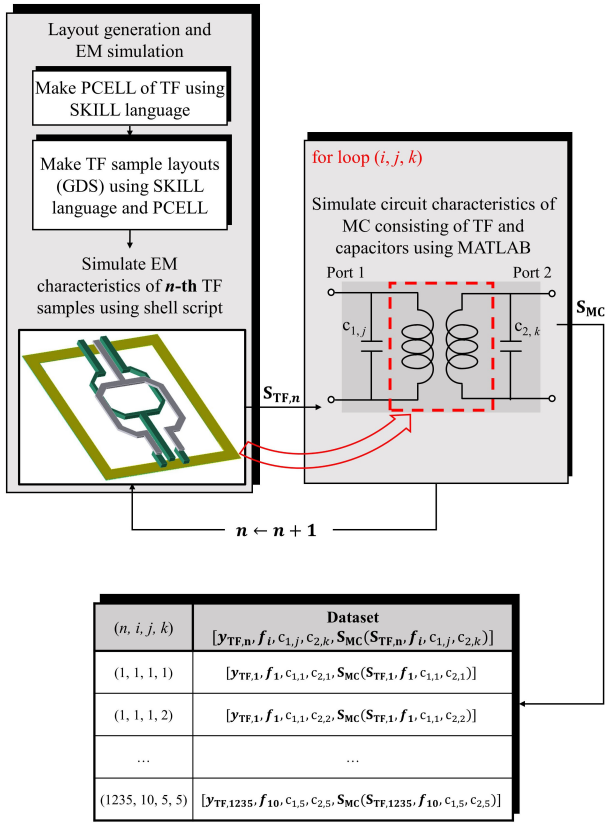

Fig. 8. Flowchart of data preparation for INN learning.

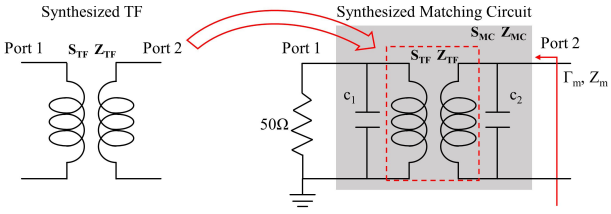

Fig. 9. Assumed MC in this work.

EPYC 7601 32-Core processor, 512-GB RAM, CentOS Linux 7.9.2009). In this work, we used MATLAB, Cadence Virtuoso, and the EMX 3-D solver.

In machine learning, it should be verified whether the input vectors of a dataset sufficiently cover the desired design space. Since, as shown in Fig. 10(a), the key role of the AMCS is to generate an MC satisfying the designer's requirements, the training set should include as wide a range of potential input parameters as possible, in particular Z_m. Fig. 10(b) shows Z_m at 60 GHz. As can be seen, Z_m in the training set widely covers the inductive impedance region in the Smith chart suitable for matching TR-based amplifiers, whose input and output are capacitive.

For training the INN, we used a multilayer perceptron structure, the mean squared error (mse) with the "percent" option in MATLAB [37] as an error function, the sigmoid function as the activation function, and the scaled conjugate gradient (SCG) algorithm [38]. The training was stopped when the epochs reached 100 000, and the NN model with the lowest

Variables

$\boldsymbol{f} := [f_1, f_2, f_3]$, frequencies
$\mathbf{S}_{\mathbf{TF},n}(f)$:= 2-port S-parameters of $n-$thTF $\mathbf{S}_{\mathbf{MC}}(\mathbf{S}_{\mathbf{TF},n}, \boldsymbol{f}_i, c_{1,j}, c_{2,k})$:= 2-port S- parameters of MC composed of n − th TF and shunt capacitors at frequency $\boldsymbol{f}_i$
$c_{1,j}, c_{2,k}$:= primary, secondary shunt capacitances of MC

Algorihtm 2 Pseudocode of for loop in Fig. 8

Input: $\mathbf{S}_{\mathbf{TF},n}$, $\boldsymbol{y}_{\mathbf{TF},n}$
Output: **Dataset**
count $= 1$
for i $= 1 : 10$ **do**
$\boldsymbol{f}_i = [2 \quad 6 \quad 10] + [10 \quad 10 \quad 10] * (i - 1)$
$Z_{TF,11}(\boldsymbol{f}_i) = 50 \times \frac{1+S_{TF,11}(\boldsymbol{f}_i)}{1-S_{TF,11}(\boldsymbol{f}_i)}$
$Z_{TF,22}(\boldsymbol{f}_i) = 50 \times \frac{1+S_{TF,22}(\boldsymbol{f}_i)}{1-S_{TF,22}(\boldsymbol{f}_i)}$
$L_1(\boldsymbol{f}_i) = \frac{\mathrm{Im}(Z_{TF,11}(\boldsymbol{f}_i))}{2\pi \boldsymbol{f}_i}$
$L_2(\boldsymbol{f}_i) = \frac{\mathrm{Im}(Z_{TF,22}(\boldsymbol{f}_i))}{2\pi \boldsymbol{f}_i}$
$c_{1,\max} = \max\left(\frac{1}{(2\pi \boldsymbol{f}_i)^2 \times L_1(\boldsymbol{f}_i)}\right)$
$c_{2,\max} = \max\left(\frac{1}{(2\pi \boldsymbol{f}_i)^2 \times L_2(\boldsymbol{f}_i)}\right)$
$c_1 = [0 \ 1 \ 2 \ 3 \ 4] \times \frac{c_{1,\max}}{4}$
$c_2 = [0 \ 1 \ 2 \ 3 \ 4] \times \frac{c_{1,\max}}{4}$
for j $= 1 : 5$ **do**
for k $= 1 : 5$ **do**
$\mathbf{S}_{\mathbf{MC}} \leftarrow \boldsymbol{CircuitSimulation}(\mathbf{S}_{\mathbf{TF},n}(\boldsymbol{f}_i), \boldsymbol{f}_i, c_{1,j}, c_{2,k})$
Dataset (count) $\leftarrow [\boldsymbol{y}_{\mathbf{TE},n}, \boldsymbol{f}_i, c_{1,j}, c_{2,k}, \mathbf{S}_{\mathbf{MC}}]$
count $\leftarrow$ count $+1$
end for
end for
end for
Return Dataset

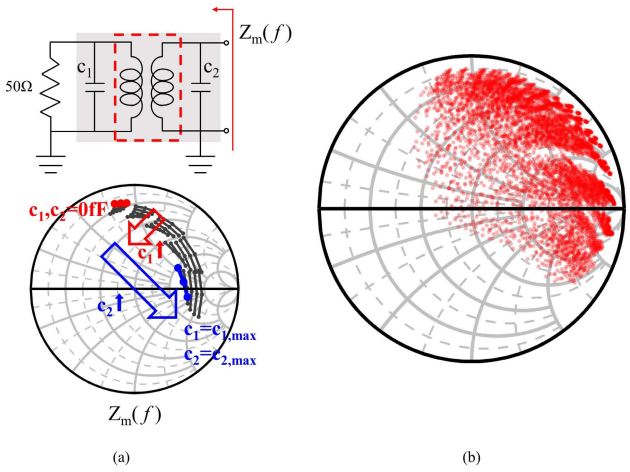

Fig. 10. MC output impedance (Z_m). (a) Variation depending on c_1 and c_2 and (b) training set at 60 GHz.

validation error according to standard practice in machine learning was selected [39].

The training results for various numbers of hidden layer node and layer combinations ($n \times m$) in the INN are shown in Fig. 11. We independently swept the number of hidden layers from 1 to 9 and the number of nodes as 10, 20, 30, 50, 100, and 200. As can be seen in Fig. 11(a), the test error

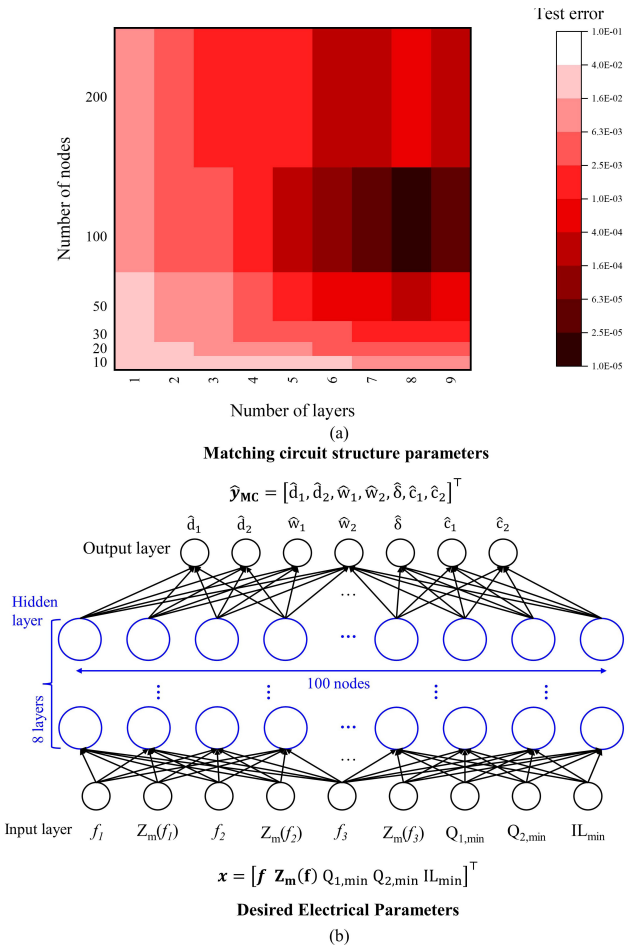

Fig. 11. INN's (a) test errors according to the number of layers and nodes and (b) layer structure that has the lowest validation error.

is significantly reduced as the number of nodes increases. In addition, as the number of layers increases, the test error is reduced to 2.262×10^{-5} for eight layers and 100 nodes at 100 000 epochs. Finally, the 100×8 NN in Fig. 11(b) was selected for the INN. Training for the 100×8 INN took 7 h on a PC (MATLAB code in Intel i5-7500, RAM 16 GB, SDD, NVIDA GeForce RTX 2080 Ti).

V. Forward Neural Network

A. Forward Neural Network

In the AMCS procedure, the designer must, in general, verify whether the MC works properly by full EM simulation, which is a time-consuming task. In the AMCS, another network, a forward neural network (FNN), is deployed to estimate the full two-port S-parameters ($\mathbf{S_{TF}}$) and Q-factors (Q_1, Q_2) at the target frequency with the TF's layout from the INN. The input and output vectors for the FNN in this work were intuitively designed by mapping the TF geometry to the S-parameters ("layout-to-spec") as follows:

$$\boldsymbol{y}_{\mathbf{TF}} = [f, d_1, d_2, w_1, w_2, \delta]^{\top} \tag{13}$$

$$\hat{\boldsymbol{x}} = \left[\hat{\boldsymbol{S}}_{\mathbf{TF}}(f), \hat{Q}_{\mathrm{TF},1}(f), \hat{Q}_{\mathrm{TF},2}(f)\right]^{\top} \tag{14}$$

$$\hat{\boldsymbol{x}} = \boldsymbol{FNN}(\boldsymbol{y}_{\mathbf{TF}}). \tag{15}$$

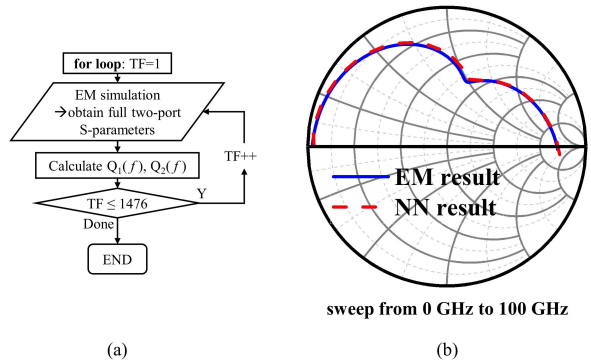

Fig. 12. FNN's (a) flowchart of data preparation and (b) comparison with EM simulation.

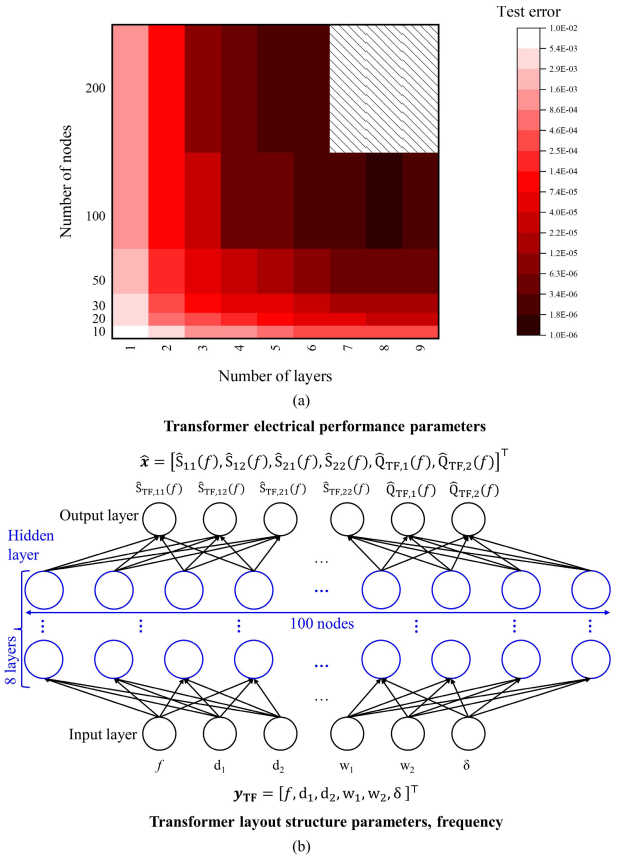

Fig. 13. FNN's (a) test error according to layer structure (hatched area could not be determined due to memory limits) and (b) layer structure that has the lowest validation error.

The whole procedure of the training set preparation for the FNN, shown in Fig. 12(a), is almost identical to that for the INN. The FNN dataset shared the GDS and EM simulation results from the INN dataset. It took 5 min to calculate the Q-factor and IL. It should be noted that, unlike the INN, FNN mapping from the TF layout to S-parameters is a many-to-one problem, in which an NN can be effectively modeled. The FNN was trained with 295 200 pairs of input and output vectors by using the SCG algorithm with the mse and sigmoid function. Also, the training was stopped when the epochs reached 50 000. Training for the 100×8 FNN took 15 h

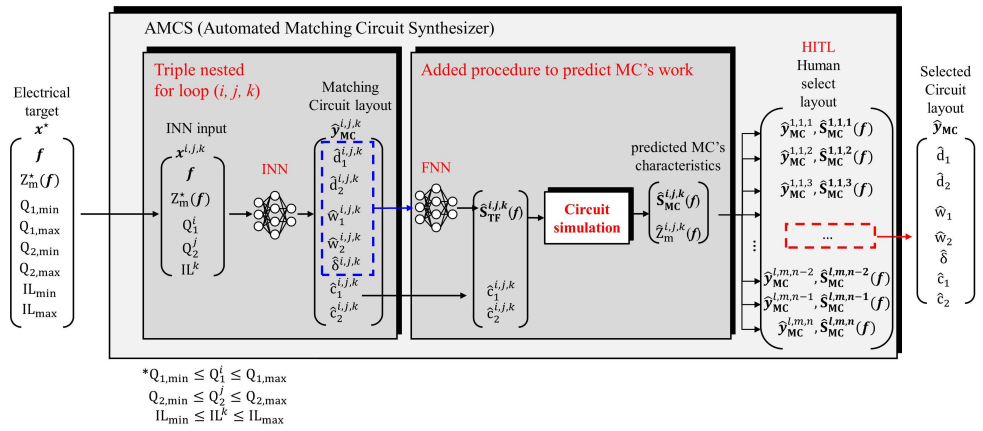

Fig. 14. Structure of AMCS combined with FNN which can predict MC's operation.

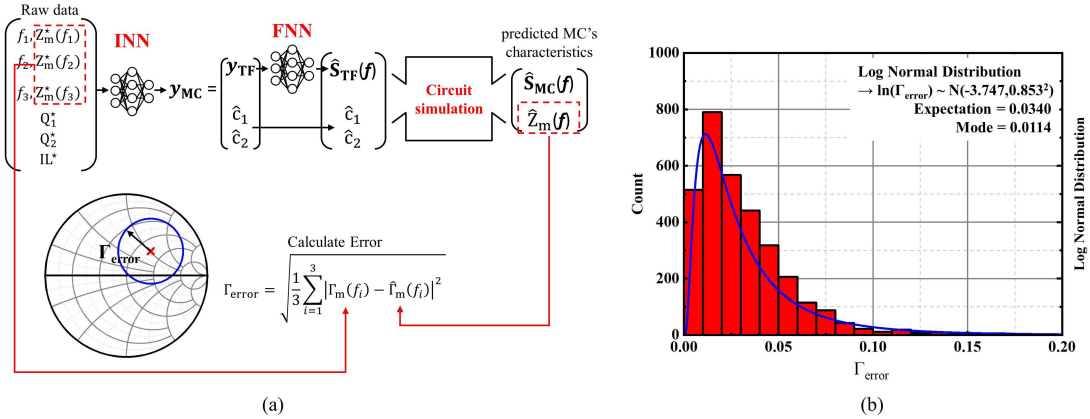

Fig. 15. (a) Back-to-back validation procedure. (b) Histogram of Γ_{error} calculated from the back-to-back validation.

on the same PC as that used for the INN. The FNN predicts TF operation very accurately, as shown in Fig. 12(b).

The hyperparameters $n \times m$ of the FNN were also varied, the same as they were in the INN. As shown in Fig. 13(a), the 100×8 NN in Fig. 13(b), which was chosen for accurate S-parameter estimation in this work, exhibited the minimum test error of 1.541×10^{-6}.

The FNN took around 0.1 s and the EM simulation took around 25 s for each TF sample, although the FNN was slightly less accurate than the EM simulation. Therefore, by using the FNN, users can predict much faster whether an MC will work in a wider frequency range and select one based on more detailed performance characteristics such as bandwidth. This work ultimately proposes a design procedure that can also predict the MC operation, as shown in Fig. 14.

In this work, to examine how close the matching impedances of the auto-synthesized matching network are to those the user inputs, we defined the FoM as the root mean square of the difference between desired impedances $[\Gamma_m^\star(\boldsymbol{f})]$ and predicted impedances $[\hat{\Gamma}_m(\boldsymbol{f})]$

$$\text{FoM} = \Delta\Gamma_m := \sqrt{\frac{1}{3}\sum_{i=1}^{3}\left|\Gamma_m^\star(f_i) - \hat{\Gamma}_m(f_i)\right|^2}. \quad (16)$$

B. Back-to-Back Validation

Fig. 15(a) shows the detailed procedure for the back-to-back validation. To verify the accuracy of the AMCS, we prepared

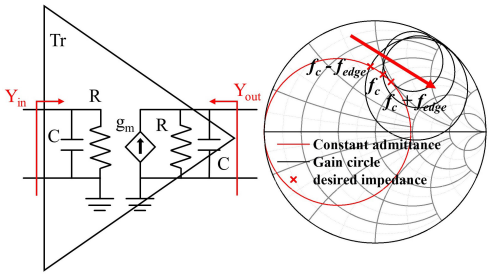

Fig. 16. Method to select matching impedances (Z_m).

test MC samples consisting of a test TF sample and two shunt capacitors (c_1, c_2) and, finally, extracted a total of 3200 back-to-back validation sets comprising impedances at three frequencies from the test MC samples. The back-to-back validation sets were then input to the AMCS, and the estimated impedance $\hat{Z}_m(\boldsymbol{f})$ was calculated from $\hat{\mathbf{S}}_{\mathbf{MC}}(\boldsymbol{f})$. To verify the accuracy of the AMCS, we compared output impedances from the EM simulation with output impedances predicted by the AMCS. The comparison was made with the function of error in the reflection coefficient domain as follows:

$$\Gamma_{\text{error}} = \sqrt{\frac{1}{3}\sum_{i=1}^{3}\left|\Gamma_m(f_i) - \hat{\Gamma}_m(f_i)\right|^2}. \quad (17)$$

The error distribution Γ_{error} shown in Fig. 15(b) was fit to the log-normal distribution, and the expectation was 0.0340.

TABLE I
TEN MC LAYOUT CANDIDATES PROPOSED BY AMCS IN DESIGN EXAMPLE 1 40-GHz CASE

MC	PRIMARY				SECONDARY				δ [μm]	Γ_{error}
	d_1 [μm]	w_1 [μm]	c_1 [fF]	Q_1	d_2 [μm]	w_2 [μm]	c_2 [fF]	Q_2		
1	149.835	5.001	15.840	17.851	114.902	9.979	2.522	16.549	9.146	0.0312
2	175.522	10.005	38.577	11.381	119.934	5.018	2.898	19.240	31.201	0.0335
3	163.797	7.506	22.495	14.844	123.470	9.887	5.793	18.506	8.685	0.0339
4	167.788	7.503	62.083	15.168	107.680	10.007	2.579	18.541	39.065	0.0442
5	180.569	10.005	70.842	7.730	132.646	4.978	2.954	14.544	29.165	0.0463
6	171.691	7.505	41.085	14.717	109.359	10.056	1.289	18.065	36.632	0.0494
7	188.043	10.002	72.387	10.956	132.121	9.859	2.982	17.771	17.039	0.0569
8	179.572	10.005	25.538	12.646	115.197	8.171	0.143	19.703	39.433	0.0576
9	176.957	10.003	65.689	12.934	113.208	9.883	0.313	18.868	35.435	0.0581
10	179.630	10.005	44.108	14.430	114.770	5.936	0.490	20.071	26.165	0.0613

VI. DESIGN EXAMPLE 1: OPERATING FREQUENCY

The AMCS was verified by designing MCs for a simple one-stage amplifier required to offer 10% fractional bandwidth at 28, 40, 60, and 70 GHz. A common-source differential core cell was assumed in this work. To improve the isolation characteristics, core TRs were neutralized with cross-coupled capacitors to enable a unilateral MC design. In general, selecting input and/or output impedances to be matched with MCs determines the overall performance of amplifiers, in particular for power and low-noise purposes. In this work, as shown in Fig. 16, the target impedances were selected by the following procedure: 1) assuming the input and output impedance of TRs can be equivalently modeled with a shunt resistor and capacitor, plot constant gain circles at the edge and center frequencies of the target bandwidth, and 2) find three intersection points between the gain circles and admittance circles in the Smith chart and use them as target impedances. The minimum and maximum bounds of Q were set to 4 and 30, and those of IL were set to 0.5 and 2 dB, respectively, so that the AMCS could evaluate almost all possible circuit combinations generated by the INN.

Table I lists the best ten sets of auto-generated MC structure parameters, including the TF layout generated for 40-GHz output matching. The ten candidates provide output impedances close to desired ones overall with little deviation in Γ_{error} but with different TFs and capacitors. In this work, for instance, we selected MC #3 because it consisted of a TF with high Q_1 and Q_2. Depending upon purposes, the user may choose another MC with small capacitance.

Fig. 17 shows the characteristics of the auto-generated MCs for 28, 40, 60, and 70 GHz from the FNN along with full-EM simulators for direct comparison. As can be seen in Fig. 17, the target impedances at all frequencies except 28 GHz, at which the target impedances are located in the region of $\Gamma > 0.94$, are well matched with the MCs auto-generated with the AMCS. S-parameters estimated by the FNN well agree with those from the EM simulation of the auto-generated layouts. Fig. 18 shows the operations of amplifiers that were matched by the AMCS. As can be seen in Fig. 18, the amplifiers were well matched through S_{11} and S_{22}'s magnitude below -10 dB at the design frequencies.

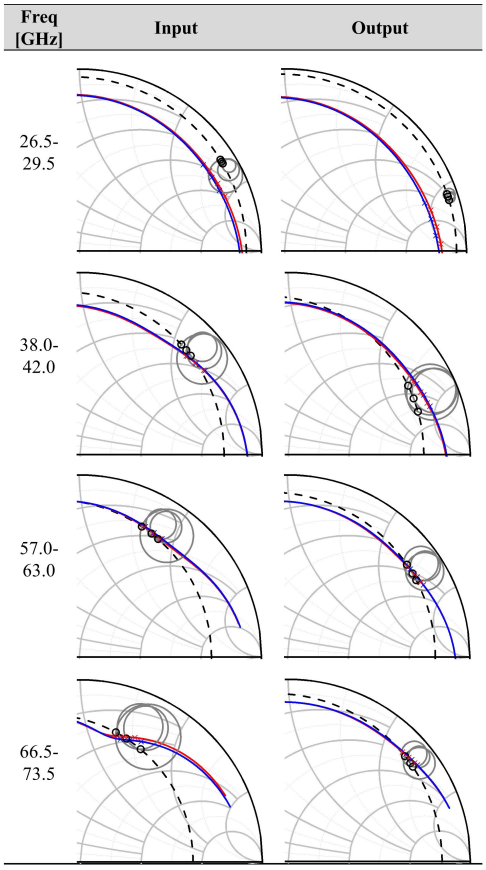

Fig. 17. Smith charts of proposed MCs. Gray line: gain circles of each frequency. Dashed line: constant admittance circle. Black dots: selected matching impedances. Red: impedances predicted by AMCS. Blue line: those calculated by EM simulation of MC.

As shown in Table II, the bandwidth characteristics well net the target. However, gain performance was lower than the target. This is because the desired impedances were in the high-Γ region and thus could not be matched with lossy TF elements, as seen in the 28-GHz case, because of the IL of the MC itself, i.e., from 1 to 1.5 dB per MC. Table III and Fig. 19 summarize the MC structure parameters for each case.

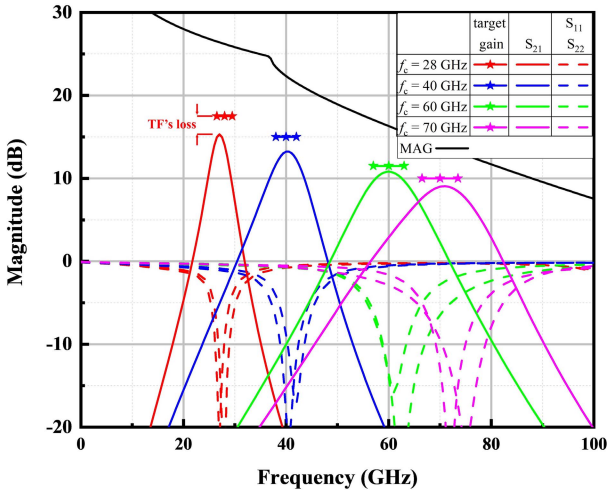

Fig. 18. EM simulated *S*-parameters of MCs generated by AMCS according to the operating frequency. Line with star: target gain. Colored solid lines: S_{21}. Colored dashed lines: S_{11} and S_{22}. Black solid line: maximum available gain.

TABLE II
CHARACTERISTICS OF AMPLIFIERS MATCHED BY AMCS

Target 1-dB BW [GHz]	1-dB BW [GHz]	% BW	Target gain [dB]	1-dB gain [dB]
26.5-29.5	26.17-27.86	6.26	17.5	14.30
38.0-42.0	38.47-42.04	8.79	15.0	12.23
57.0-63.0	57.20-62.84	9.40	11.5	9.80
66.5-73.5	67.29-74.24	9.79	10.0	8.05

TABLE III
PROPOSED MC LAYOUTS AT EACH FREQUENCY

Input port							
FREQ [GHz]	PRIMARY			SECONDARY			δ
	d_1	w_1	c_1	d_2	w_2	c_2	
28	232.1	10.0	70.0	147.5	10.0	40.9	42.5
40	173.1	7.5	68.0	136.6	9.9	21.0	3.1
60	87.8	5.0	42.5	66.2	10.0	11.9	2.9
70	66.5	5.0	64.2	52.0	5.5	16.3	11.6
Output port							
FREQ [GHz]	PRIMARY			SECONDARY			δ
	d_1	w_1	c_1	d_2	w_2	c_2	
28	242.2	10.0	87.7	158.8	9.9	56.0	38.3
40	155.9	5.0	58.4	120.3	10.0	29.5	9.0
60	122.1	5.0	28.6	91.3	9.7	12.2	20.7
70	118.2	5.0	15.4	86.3	10.0	3.5	17.1

It should be noted that the AMCS's "spec-to-layout" synthesis procedure from impedance input to layout generation took around 10 min at each frequency with a PC (MATLAB code in Intel i5-7500, RAM 16 GB, SDD, NVIDA GeForce RTX 2080 Ti).

VII. DESIGN EXAMPLE 2: BANDWIDTHS

The second example is the design of MCs for 40-GHz amplifiers operating in various bandwidths of 10%, 20%, 25%, and 37.5%. To maintain in-band flat gain, constant gain circles were used to determine the target impedances.

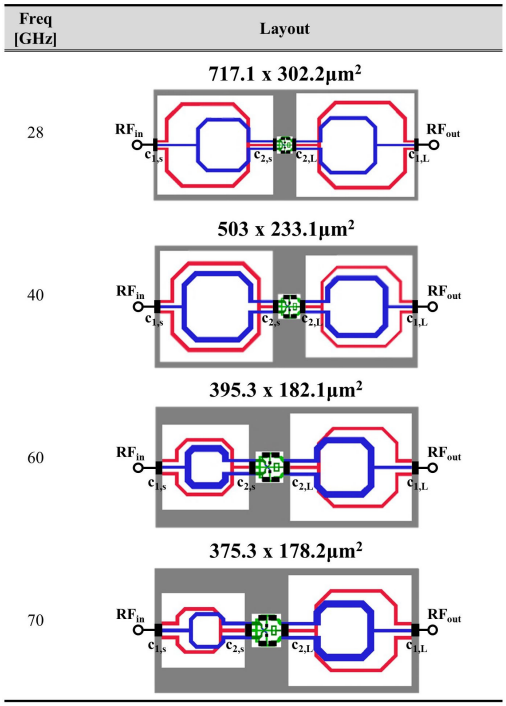

Fig. 19. Layouts of all matched amplifiers depending on frequencies.

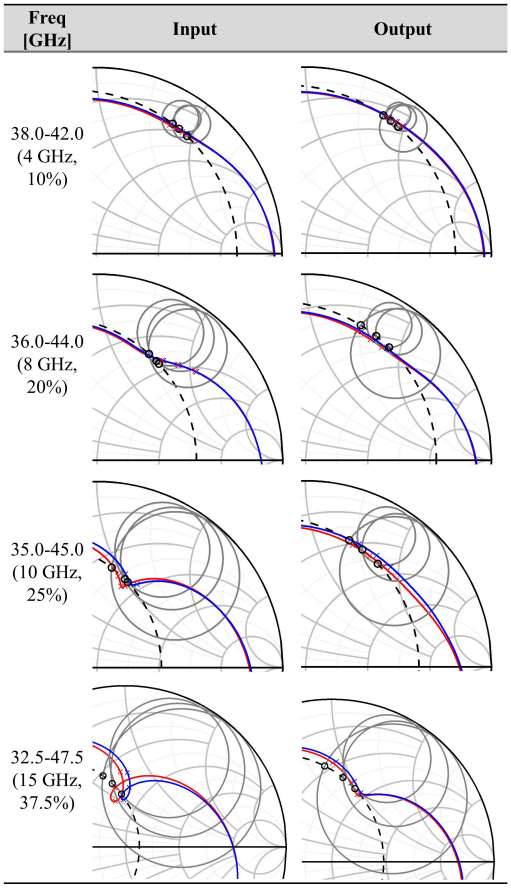

Fig. 20. Smith charts of the proposed MCs. Gray line: gain circles of each frequency. Dashed line: constant admittance circle. Black dots: selected matching impedances. Red line: impedances predicted by AMCS. Blue line: those calculated by EM simulation of MC.

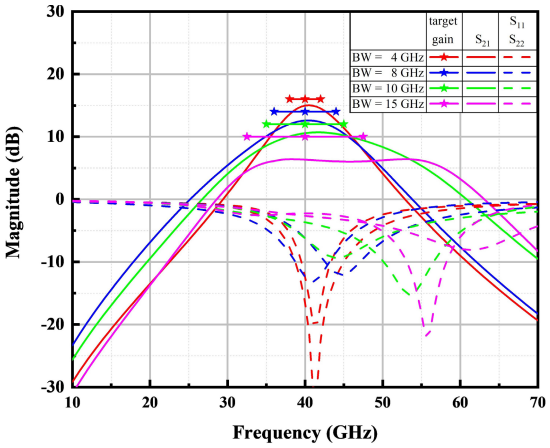

Fig. 21. EM simulated S-parameters of MCs generated by AMCS according to bandwidth. Line with star: target gain. Colored solid lines: S_{21}. Colored dash lines: S_{11} and S_{22}. Black solid line: maximum available gain.

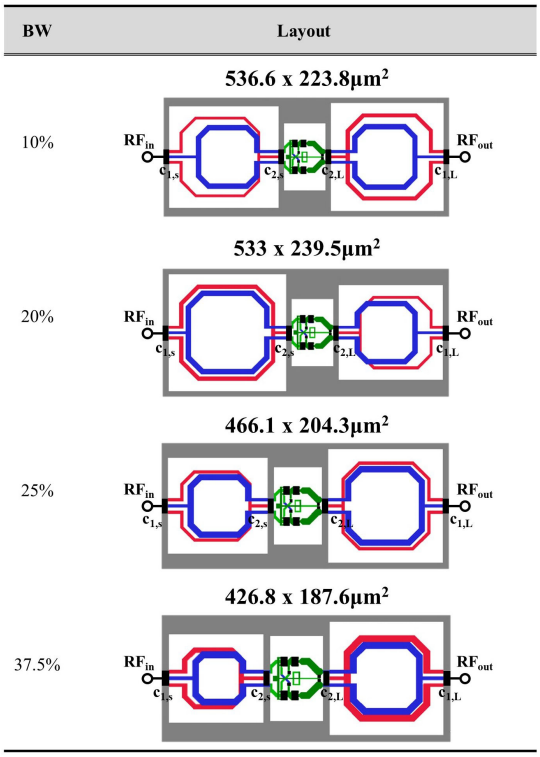

Fig. 22. Layouts of all matched amplifiers depending on each bandwidth.

Fig. 20 shows the matching impedances of the designed MCs and the S-parameters of the amplifiers from the FNN along with those from full-EM simulators for direct comparison. As can be seen in Fig. 20, the target impedances at all frequencies are well matched with the auto-generated MCs. S-parameters estimated by the FNN show good agreement with those from the EM simulation. As shown in Fig. 21, the amplifiers were well matched through S_{11} and S_{22}'s magnitude under -10 dB at the design frequencies. Table IV summarizes the target and performance results for all cases. Table V and Fig. 22 summarize the MC structure parameters for each case.

TABLE IV
CHARACTERISTICS OF AMPLIFIERS MATCHED BY AMCS

Target 1-dB BW [GHz]	1-dB BW [GHz]	% BW	Target Gain [dB]	1-dB Gain [dB]	GBP
38.0-42.0	38.43-42.63	10.4	16.0	14.0	132.8
36.0-44.0	37.19-43.55	15.4	14.0	11.6	116.5
35.0-45.0	37.12-46.71	23.1	12.0	9.70	112.8
32.5-47.5	33.89-57.11	34.7	10.0	5.40	57.6

TABLE V
PROPOSED MC LAYOUTS DEPENDING ON EACH BANDWIDTH

Input port							
BW [%]	PRIMARY			SECONDARY			δ
	d_1	w_1	c_1	d_2	w_2	c_2	
10	151.5	5.0	33.4	120.3	10.0	6.5	14.6
20	179.3	7.5	61.7	156.2	9.9	19.1	0.7
25	116.1	5.1	75.2	103.4	9.9	25.7	5.9
37.5	91.0	7.6	122.7	79.9	9.8	55.3	9.1
Output port							
BW [%]	PRIMARY			SECONDARY			δ
	d_1	w_1	c_1	d_2	w_2	c_2	
10	163.8	7.5	22.5	123.5	9.9	5.8	8.7
20	137.0	5.0	19.0	118.3	8.9	9.8	17.9
25	144.3	5.1	5.1	129.3	9.7	10.5	1.7
37.5	127.6	10.0	41.5	107.6	9.9	20.7	0.9

TABLE VI
COMPARISON BETWEEN STATE OF THE ARTS OF AUTOMATED TF SYNTHESIZERS

Work	Form of synthesis	Design object	Synthesis time	Demo	Frequency range
Liu [20], 2011	Direct	TF	2.3 h to synthesize a TF	Freq at 60 GHz	-
Liu [21], 2014	Direct	TF with transmission line	42 h to synthesize two-stage amplifier	Freq at 60 GHz	-
Munzer [28], 2020	Indirect	TF	-	-	-
Er [29], 2021	Direct	TF with shunt capacitors (Require capacitances)	-	Frequency at 30 GHz	Single frequency (30 GHz)
This Work	Direct	TF with shunt capacitors	10 min to synthesize one-stage amplifier	Freq upon 70 GHz BW upon 37.5%	Wideband (in 0-100 GHz)

VIII. CONCLUSION AND DISCUSSION

In this article, an NN-based AMCS was presented to synthesize TF layouts for impedance MCs satisfying the desired impedance. Input features were carefully designed to avoid the one-to-many problem, which would be underfit by NNs. Instead of full two-port S-parameters of MCs, which cannot be provided by designers, we suggested input features such as the

Q-factors and IL of TFs for use as constraint factors. The proposed features effectively represent the full two-port characteristics of the desired MC and facilitate one-to-one mapping. The concept of HITL to deal with the Q-factors and IL in the proposed AMCS gives us additional freedom to design MCs; the AMCS returns multiple MCs and allows users to select one of them depending upon their purposes in a handy way. With the proposed AMCS, we designed simple single-stage amplifiers operating at different frequencies up to 70 GHz or in different bandwidths up to 32.5%. The estimated S-parameters of the amplifiers showed good agreement with the EM simulation results. As can be seen in Table VI, the AMCS provides a faster and more efficient way to synthesize MCs with TFs. The proposed NN-based AMCS can dramatically reduce design time by eliminating various time-consuming and iterative tasks and can enhance the accuracy of the high-frequency circuit design by offering a "spec-to-layout" procedure.

Finally, it is worth noting the limitations of the current approach, which need to be overcome for fully automated RF circuit design.

1) The proposed AMCS currently matches core transistors only to 50 Ω. In order to generate interstage matching for arbitrary impedance, training datasets should be prepared for all possible impedance combinations for a given TF. Though it will not cause the one-to-many problem, training error must highly depend on the coverage of the impedance to be matched in the Smith chart.

2) In this method, the designer should select the target output impedances at target frequencies, which dominate the amplifier's performance. If a user selects unachievable output impedances, the AMCS may return wrong TF layouts that do not provide good enough RF performance. Another loop for the various possible impedances based on the HITL concept would be a simple way to avoid this, but additional cost function design and input impedance selection routines will be required for reducing computing time.

3) The AMCS can only generate 1:1 TFs that are predefined with various parameters. Since there must be multiple possible layouts for given impedances, training NNs for arbitrary-shape TF generation will suffer from the one-to-many problem. This is one of the most importance open research problems for the NN-based RFIC design.

4) Currently, EM simulation based on the accurate process parameters would be the most efficient and simplest way to prepare the training datasets; it would rarely be possible to prepare several thousand samples for measurement. However, to implement a more generalized AMCS supporting the functionalities mentioned above, several ten or even several hundred times more EM simulations need to be run (i.e., 1476 simulations in the current work). From this point of view, efficient data sampling algorithms should be intensively investigated as well [40].

Despite the limitations, this work clearly showed that the concept of input feature design and HITL is effective for automated RFIC design.

REFERENCES

[1] K. Kim, K. Lee, S. Cho, G. Shin, and H. J. Song, "A 28–34-GHz stacked-FET power amplifier in 28-nm FD-SOI with adaptive back-gate control for improving linearity," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 52–55, 2021, doi: 10.1109/LSSC.2021.3054885.

[2] K. Kim *et al.*, "A 50-Gb/s compact RadCom E-band transmitter with phase-controlled push–push quadrupler and stacked-FET power amplifier," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 150–153, 2021, doi: 10.1109/LSSC.2021.3108486.

[3] K. Lee, K. Kim, G. Shin, and H. J. Song, "65.6–75.2-GHz phase-controlled push–push frequency quadrupler with 8.3% DC-to-RF efficiency in 40-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 579–582, Jun. 2021, doi: 10.1109/LMWC.2021.3068179.

[4] G. Shin, K. Kim, K. Lee, H.-H. Jeong, and H.-J. Song, "An E-band 21-dB variable-gain amplifier with 0.5-V supply in 40-nm CMOS," *Electronics*, vol. 10, no. 7, p. 804, Mar. 2021, doi: 10.3390/electronics10070804.

[5] S. Hu, F. Wang, and H. Wang, "2.1 A 28 GHz/37 GHz/39 GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 32–33, doi: 10.1109/ISSCC.2017.7870246.

[6] K. Okada *et al.*, "20.3 A 64-QAM 60 GHz CMOS transceiver with 4-channel bonding," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 346–347, doi: 10.1109/ISSCC.2014.6757463.

[7] W. Shin, S. Callender, S. Pellerano, and C. Hull, "A compact 75 GHz LNA with 20 dB gain and 4 dB noise figure in 22 nm FinFET CMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 284–287, doi: 10.1109/RFIC.2018.8429036.

[8] S. Callender, S. Pellerano, and C. Hull, "A compact 75 GHz PA with 26.3% PAE and 24 GHz bandwidth in 22 nm FinFET CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 224–227, doi: 10.1109/RFIC.2018.8428993.

[9] C. Wang, H. Liao, Y. Xiong, C. Li, R. Huang, and Y. Wang, "A physics-based equivalent-circuit model for on-chip symmetric transformers with accurate substrate modeling," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 4, pp. 980–990, Apr. 2009, doi: 10.1109/TMTT.2009.2014479.

[10] J. D. Lohn and S. P. Colombano, "A circuit representation technique for automated circuit design," *IEEE Trans. Evol. Comput.*, vol. 3, no. 3, pp. 205–219, Sep. 1999, doi: 10.1109/4235.788491.

[11] T. Sripramong and C. Toumazou, "The invention of CMOS amplifiers using genetic programming and current-flow analysis," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 21, no. 11, pp. 1237–1252, Nov. 2002, doi: 10.1109/TCAD.2002.804109.

[12] K. Usami *et al.*, "Automated low-power technique exploiting multiple supply voltages applied to a media processor," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 463–472, Mar. 1998, doi: 10.1109/4.661212.

[13] D. Binu and B. S. Kariyappa, "RideNN: A new rider optimization algorithm-based neural network for fault diagnosis in analog circuits," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 1, pp. 2–26, Jan. 2019, doi: 10.1109/TIM.2018.2836058.

[14] G. Wolfe and R. Vemuri, "Extraction and use of neural network models in automated synthesis of operational amplifiers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 198–212, Feb. 2003, doi: 10.1109/TCAD.2002.806600.

[15] R. A. Rutenbar, G. G. E. Gielen, and J. Roychowdhury, "Hierarchical modeling, optimization, and synthesis for system-level analog and RF designs," *Proc. IEEE*, vol. 95, no. 3, pp. 640–669, Mar. 2007, doi: 10.1109/JPROC.2006.889371.

[16] A. C. Watson, D. Melendy, P. Francis, K. Hwang, and A. Weisshaar, "A comprehensive compact-modeling methodology for spiral inductors in silicon-based RFICs," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 3, pp. 849–857, Mar. 2004, doi: 10.1109/TMTT.2004.823594.

[17] N. Wainstein, T. Tsabari, Y. Goldin, E. Yalon, and S. Kvatinsky, "A dual-band CMOS low-noise amplifier using memristor-based tunable inductors," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, Jul. 2019, pp. 290–295, doi: 10.1109/ISVLSI.2019.00060.

[18] A. M. Niknejad, "Modeling of passive elements with ASITIC," in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp. Dig. Papers*, 2002, pp. 303–306, doi: 10.1109/RFIC.2002.1012054.

[19] A. Papadimitriou and M. Bucher, "Optimization of RF low noise amplifier design using analytical model and genetic computation," in *Proc. 24th Int. Conf. "Mixed Design Integr. Circuits Syst. (MIXDES)*, Jun. 2017, pp. 302–307, doi: 10.23919/MIXDES.2017.8005220.

[20] B. Liu, D. Zhao, P. Reynaert, and G. Gielen, "Synthesis of integrated passive components for high-frequency RF ICs based on evolutionary computation and machine learning techniques," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 10, pp. 1458–1468, Oct. 2010, doi: 10.1109/TCAD.2011.2162067.

[21] B. Liu, D. Zhao, P. Reynaert, and G. G. E. Gielen, "GASPAD: A general and efficient mm-wave integrated circuit synthesis method based on surrogate model assisted evolutionary algorithm," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 2, pp. 169–182, Feb. 2014, doi: 10.1109/TCAD.2013.2284109.

[22] R. Martins *et al.*, "Two-step RF IC block synthesis with preoptimized inductors and full layout generation in-the-loop," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 38, no. 6, pp. 989–1002, Jun. 2019, doi: 10.1109/TCAD.2018.2834394.

[23] G. L. Creech, B. J. Paul, C. D. Lesniak, T. J. Jenkins, and M. C. Calcatera, "Artificial neural networks for fast and accurate EM-CAD of microwave circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 5, pp. 794–802, May 1997, doi: 10.1109/22.575602.

[24] W. Na, F. Feng, C. Zhang, and Q. Zhang, "A unified automated parametric modeling algorithm using knowledge-based neural network and l_1 optimization," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 3, pp. 729–745, 2017, doi: 10.1109/TMTT.2016.2630059.

[25] C. Zhang, J. Jin, W. Na, Q. J. Zhang, and M. Yu, "Multivalued neural network inverse modeling and applications to microwave filters," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 8, pp. 3781–3797, Aug. 2018, doi: 10.1109/TMTT.2018.2841889.

[26] M. Ohira, A. Yamashita, Z. Ma, and X. Wang, "Automated microstrip bandpass filter design using feedforward and inverse models of neural network," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Nov. 2018, pp. 1292–1294, doi: 10.23919/APMC.2018.8617627.

[27] H. Kabir, Y. Wang, M. Yu, and Q.-J. Zhang, "Neural network inverse modeling and applications to microwave filter design," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 4, pp. 867–879, Apr. 2008, doi: 10.1109/TMTT.2008.919078.

[28] D. Munzer *et al.*, "Residual network based direct synthesis of EM structures: A study on one-to-one transformers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 143–146, doi: 10.1109/RFIC49505.2020.9218278.

[29] S. Er *et al.*, "Deep learning assisted end-to-end synthesis of mm-wave passive networks with 3D EM structures: A study on a transformer-based matching network," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 66–69, doi: 10.1109/IMS19712.2021.9575030.

[30] C. Tang and R. R. Salakhutdinov, "Learning stochastic feedforward neural networks," in *Proc. Adv. Neural Inf. Process. Syst.*, 2013, pp. 503–538.

[31] K. P. Murphy, *Probabilistic Machine Learning: An Introduction*. Cambridge, MA, USA: MIT Press, 2022.

[32] L. Wang, A. Schwing, and S. Lazebnik, "Diverse and accurate image description using a variational auto-encoder with an additive Gaussian encoding space," in *Proc. Adv. Neural Inf. Process. Syst.*, vol. 30, 2017, pp. 1–11.

[33] K. Sohn, H. Lee, and X. Yan, "Learning structured output representation using deep conditional generative models," in *Proc. Adv. Neural Inf. Process. Syst.*, vol. 28, 2015, pp. 1–9.

[34] R. Bajwa and M. K. Yapici, "Integrated on-chip transformers: Recent progress in the design, layout, modeling and fabrication," *Sensors*, vol. 19, no. 16, p. 3535, Aug. 2019, doi: 10.3390/s19163535.

[35] P. P. Chu, "A neural network for solving optimization problems with linear equality constraints," in *Proc. Int. Joint Conf. Neural Netw. (IJCNN)*, vol. 2, Jun. 1992, pp. 272–277, doi: 10.1109/IJCNN.1992.226996.

[36] D. Honeycutt, M. Nourani, and E. Ragan, "Soliciting human-in-the-loop user feedback for interactive machine learning reduces user trust and impressions of model accuracy," in *Proc. AAAI Conf. Hum. Comput. Crowdsourcing*, Jan. 2020, vol. 8, no. 1, pp. 63–72. [Online]. Available: https://ojs.aaai.org/index.php/HCOMP/article/view/7464

[37] MathWorks. *MATLAB MSE*. Accessed: May 7, 2022. [Online]. Available: https://mathworks.com/help/deeplearning/ref/mse.html

[38] M. Møller, "A scaled conjugate gradient algorithm for fast supervised learning," *Neural Netw.*, vol. 6, no. 4, pp. 525–533, 1990, doi: 10.1016/S0893-6080(05)80056-5.

[39] F. Girosi, M. Jones, and T. Poggio, "Regularization theory and neural networks architectures," *Neural Comput.*, vol. 7, no. 2, pp. 219–269, Mar. 1995, doi: 10.1162/neco.1995.7.2.219.

[40] Z. Zhang, Q. S. Cheng, H. Chen, and F. Jiang, "An efficient hybrid sampling method for neural network-based microwave component modeling and optimization," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 7, pp. 625–628, Jul. 2020, doi: 10.1109/LMWC.2020.2995858.

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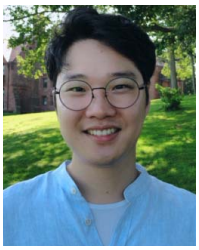

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