Analysis of mm-Wave Multi-Stage Rectifier and Implementation

Yun Fang, *Member, IEEE*, Wei Hong, *Fellow, IEEE*, and Hao Gao, *Member, IEEE*

***Abstract*— In the mm-wave frequency band, the rectifier's sensitivity is the bottleneck of a wireless-powered IoT transponder's distance. At a meter's distance, the received power is weak, and transistors in a front end of a wireless power receiver operate in the weak inversion region. This article presents a mathematical analysis of the mm-wave multi-stage rectifier in the low-power region. A design methodology of a 57–64-GHz fully integrated eight-stage rectifier with a bulk-drain connection in 40-nm CMOS technology is presented. Parasitic effects on a multi-stage rectifier are analyzed. Based on the analysis, an intrinsic threshold voltage modulation is applied to improve the sensitivity. A tree-type power splitter is also proposed for the RF power signal's phase balance. With this method, the RF signal arrives at each stage with an equal phase, and its suppression at the output is improved by 16 dB. This mm-wave rectifier achieves −7.1-dBm input sensitivity at 57 GHz with 1-V dc output voltage. The overall sensitivity from 57 to 64 GHz is better than −4.5 dBm. Compared to other mm-wave silicon-based rectifier state of the arts, the proposed mm-wave rectifier achieves better sensitivity while maintaining a compact size.**

***Index Terms*— CMOS, mm-wave, rectenna, rectifier, sensitivity, wireless power receiver.**

I. Introduction

SINCE the mm-wave frequency band was introduced into commercial wireless communication, the IoT transponder function at mm-wave frequencies has received much attention for its potential massive deployment combined with cloud computing and AI technology. In these scenarios, low cost and small size are crucial requirements for the transponder. The conventional solution is mostly battery-operated. The battery limits the transponder's size, and its replacement adds significant maintenance costs for the massive deployment. IoT transponders with the wireless power function would be an attractive solution for their unique advantage of maintenance-free usage.

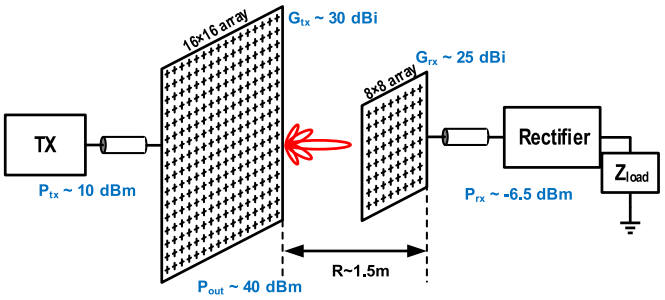

Fig. 1. Concept illustration of an mm-wave WPT system with its link budget estimation at 60-GHz ISM band for a 1.5-m wireless transfer distance.

In such an mm-wave wirelessly powered IoT transponder, the transponder works in a sequential architecture [1]: the energy is temporarily stored and then consumed. Compared to a duplex system, such as an RFID system, it can provide more instant energy. In this architecture, a rectifier's sensitivity dominates the communication distance instead of its efficiency. At 60 GHz, in the order of 6 × 6 cm^2 size, a power transmitter could integrate with a 16 × 16-element slot array antenna of 30-dBi gain [2]. A compact IoT transponder could also integrate with an 8 × 8-element array of 25-dBi gain, which is in the order of a quarter-sized smart card. The rectifier's sensitivity requirement could be derived from a regulated 10-dBm output power of a 60-GHz power transmitter [3] and half-room-height (1.5-m) transfer distance, as shown in Fig. 1. According to the Friis transmission equation, the free-space path loss at the 60-GHz band with a 1.5-m distance is 71.5 dB. Furthermore, the 60-GHz band is characterized by high levels of atmospheric energy absorption. The maximum oxygen absorption is 10–15 dB/km [4], resulting extra 0.015–0.025-dB loss in this system. In this combination, a rectifier with −6.6-dBm sensitivity is crucial for a 1.5-m distance indoor application.

At mm-wave frequency bands, a rectifier could be implemented by Schottky diodes with high efficiency due to its low turn-on voltage [5], [6], [7], [8], [9]. However, the Schottky diode has a compatibility issue with deep submicrometer silicon-based technology in a fully integrated on-chip wireless power receiver solution. A rectifier based on diode-connected transistors is an on-chip integration solution in deep submicrometer silicon technology. To overcome the limited output

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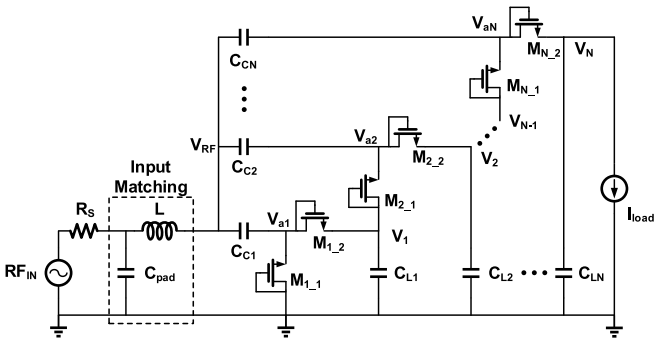

Fig. 2. mm-wave N-stage rectifier based on the Dickson multiplier structure.

voltage from a one-stage rectifier, Dickson voltage multipliers are proposed in [10] and are widely used in [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], and [27]. The architecture is shown in Fig. 2. However, the threshold voltage in a diode-connected transistor still limits the rectifiers' sensitivity: the transistor would only conduct a strong current when the voltage swing is larger than the threshold voltage.

In history, several techniques have been proposed to overcome the threshold voltage limitation in the Dickson voltage multipliers. They could be classified into three categories.

1) The first category is the equivalent threshold voltage reduction technique. It could be achieved by shifting the threshold voltage by introducing a gate-bias voltage [13], [14] or modulating the threshold voltage by a bulk-bias (BB) voltage [15], [16]. Those rectifiers' bottleneck is the requirement of extra bias voltages. Therefore, an internal-threshold canceling (ITC) rectifier in [17], [18], [19], [20], [21], and [22] is applied to solve this issue.
2) The second category is the inductor peaking (LP) technique. The gate voltage swing is boosted by inserting an inductor in-between the gate and source [23], [24], [25], [26]. However, the voltage phase difference between gate–source and drain–source generates a reverse leakage current, limiting a rectifier's performance.
3) The third category is the technique combination of threshold voltage reduction and gate voltage boosting [27]. It could be achieved by inserting an in-phase passive voltage multiplier (IPVM), and an ITC bias scheme to boost the forward current while minimizing the reverse-leakage current. However, it has a complex control scheme, and the separation of bias and booster would have the bottleneck of a starting issue.

Furthermore, some other topologies have been explored in [28], [29], [30], and [31]. He and Zhao [28] proposed an mm-wave switching rectifier, extracting the dc signal from the drain of a switching transistor by mixing the RF signal and its phase-shifted replica. Weissman *et al.* [29], Shaulov *et al.* [30], and Vroede *et al.* [31] employed a differential Colpitts VCO along with an on-chip antenna to realize RF-to-dc conversion. However, the switching rectifier and the Colpitts VCO-based rectifier show limited sensitivity.

In this article, we propose a compact and robust mm-wave multi-stage rectifier with a bulk-drain connection. This intrinsic threshold voltage modulation improves the sensitivity without introducing extra bias voltages. Compared to inductor-peaking and IPVM rectifiers, this mm-wave multi-stage rectifier is much more compact and allows broadband operation. The proposed mm-wave rectifier works at the low input power range, and transistors operate in the weak-inversion region at the front-end circuits. In this region, the ac-to-dc analysis proposed in [10] and the analysis in [32] are no longer applicable to this rectifier. A detailed analysis of a multi-stage rectifier in a weak input power with bulk-drain connected transistors is also presented.

This article is organized as follows. Section II presents the bulk-drain connection transistor and N-stage rectifier modeling with steady-state analysis in a low voltage swing situation. Section III describes the design methodology of an eight-stage mm-wave rectifier in CMOS technology. The measurement results are discussed in Section IV. The conclusions are drawn in Section V.

II. MM-WAVE RECTIFIER WITH BULK-DRAIN CONNECTED TRANSISTORS

The sensitivity of an mm-wave rectifier in CMOS technology is limited by the transistor's threshold voltage. The 1-V sensitivity [23] is in the range of −3–1 dBm at 45, 60, and 24 GHz [1], [11], [12]. The threshold voltage can be modulated through a bulk voltage by taking advantage of the deep N-well in the bulk CMOS technology or SOI technology. This threshold modulation technique can improve a rectifier's 1-V sensitivity to −5 dBm at 60 GHz [15]. However, the external bias voltage limits its application in an on-chip wireless power receiver. Therefore, an mm-wave rectifier with bulk-drain connected transistors is proposed. In this method, the bulk voltage is directly connected to the input RF node. With an increased input signal, the threshold voltage can be reduced with the input voltage amplitude. As shown in Fig. 3, under the same input power level and load conditions, the bulk-drain connection rectifier improves sensitivity and efficiency by 22% and 58%, respectively. Few studies report this low input power region. In this section, an analysis with a mathematical model is provided for an mm-wave bulk-drain connection rectifier for sensitivity optimization.

The cross-view of a bulk-drain connected transistor is shown in Fig. 4(a). In a deep submicrometer technology, the deep N-well option enables the bulk to be biased separately instead of connected to the lowest voltage. In this bulk-drain connection, the gate, the drain, and the bulk of an n-type transistor are connected together as the input port. The source is the output port. Since the bulk and gate are connected to the same voltage potential, an n-type transistor with a bulk-drain connection has three effective parasitic diodes and two effective parasitic capacitors. Those parasitic diodes are the diode between bulk and source D_{BS}, the diode between bulk and N-well D_{ISO}, and the diode between N-well and P-substrate D_{WELL}. Those effective parasitic capacitors are C_{GS} and C_{BS}. In this bulk-drain connection, D_{ISO} and D_{WELL}

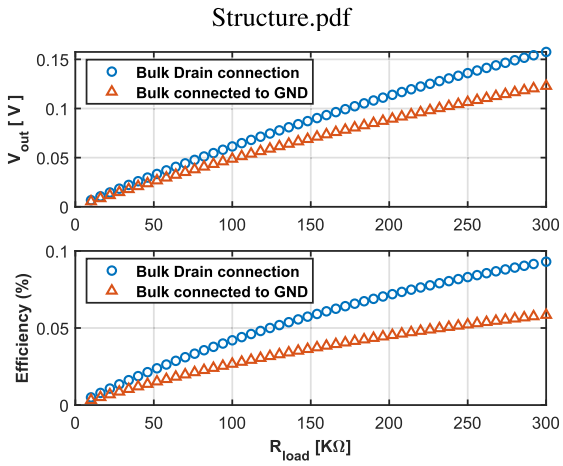

Fig. 3. Simulated output voltage and efficiency of rectifiers with different bulk connections.

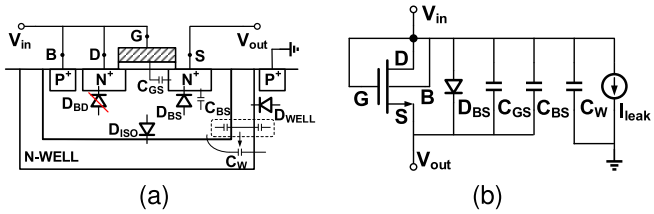

Fig. 4. (a) Cross view and (b) equivalent circuit of an n-type transistor with bulk-drain connection in a deep N-well technology.

are in series and creating a path between node V_{in} and ground. Those two diodes are always reverse-biased, restraining the leakage current to its reverse saturation current, and it is irrelevant to V_{in}'s phase. The two parasitic capacitors are in series and are modeled as C_W: between bulk and N-well, and between N-well and P-substrate. Therefore, the equivalent circuit of the bulk-drain connection n-type transistor is shown in Fig. 4(b). The bulk-drain connection n-type transistor has a parallel diode D_{BS}, two parallel capacitors C_{GS} and C_{BS}, along with a parasite capacitor C_W, and a leakage current I_{leak} between V_{in} and ground.

A. Steady-State Analysis

In the rectifier, each identical stage consists of two bulk-drain connected transistors in a series-cascade way. The sinusoidal RF signal V_{RF} is ac-coupled to each stage's series node. The loading capacitors are large enough to store the charge without generating significant ripples.

Before a steady state, it is assumed that all the coupling and loading capacitors have no charges. When $V_{\text{RF}} < 0$, forward-biased M_{i_1} charges C_{Ci}. When $V_{\text{RF}} > 0$, M_{i_2} charges C_{Li} and generates the dc voltage. The same mechanism is repeated in every subsequent stage, and the rectifier eventually offers a stable output dc voltage and load current. In the steady state, every transistor's forward and reverse current is the same. The current is transported to the load current one by one. With identical capacitors, the output-to-input dc boost voltage will be the same. The series node V_{ai} in each stage will be charged

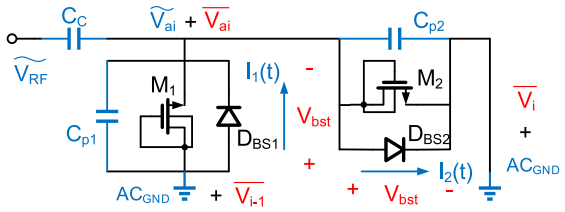

Fig. 5. AC and ac-to-dc analysis of the ith-stage rectifier.

to a dc voltage level to keep the same forward-bias voltage and the same conduction angle for each transistor.

Since the voltage and the current waveform are the same for each stage in the steady stage, it would be convenient to analyze only one stage and multiply its boost voltage with the stage number, N, to get the final dc output voltage. The ac and dc equivalent circuit for the ith-stage rectifier is shown in Fig. 5. The ac portion of voltage at each node is indicated with blue color, while the dc portion is indicated with red color. The ac-to-dc conversion is provided by the unbalanced charging current of nonlinear devices, so the charge contributed by any linear device is zero in one input RF signal's period. In this way, the analysis of the ith-stage rectifier is divided into two parts: ac analysis to determine the amplitude of $\widetilde{V_{\text{ai}}}$ and ac-to-dc analysis to determine the boost voltage V_{bst}.

Because of the loading capacitors, the dc input and output ports have extremely small ac portion voltages. In this consideration, they are simplified as ac ground. Therefore, $\widetilde{V_{\text{ai}}}$ can be calculated by the voltage division of C_c and the sum of C_{p1} and C_{p2}. In the single-stage rectifier, $M_{1,2}$ and their parasitic diode $D_{\text{BS1,2}}$ are turned on alternatively in the negative and positive half periods, respectively. Since C_{BS} is the parasitic capacitor of D_{BS}, it will be shorted when D_{BS} is turned on. Thus, the effective C_{BS} would only be counted once in every input period, while parasitic capacitors C_{GS} and C_W in both transistors are always effective

$$\widetilde{V_{\text{ai}}} = \frac{C_c}{C_c + C_{\text{par}}} \widetilde{V_{\text{RF}}} \tag{1}$$

where $C_{\text{par}} = C_{p1} + C_{p2} = 2(C_{\text{GS}} + C_W) + C_{\text{BS}}$.

In ac-to-dc analysis, $\widetilde{V_{\text{ai}}}$ and dc voltage differential V_{bst} are used to generate the unbalanced current $I_1(t)$ or $I_2(t)$. Because M_1 and M_2, and coupling and loading capacitors are in the same size, the unbalanced current and the boost voltage are the same. For simplicity, the following analysis will be carried out with a one-transistor rectifier.

B. Analysis of One-MOS Rectifier

Fig. 6(a) shows the ac-to-dc conversion model of a single bulk-drain connected transistor, and Fig. 6(b) shows the ac portion $\widetilde{V_a}$, dc boost voltage V_{bst}, and the total current through the n-type transistor with its parasitic diode. The leakage current generated by D_{ISO} and D_{WELL} is neglected for simplicity considering the extremely small current contribution.

Since the RF input signal is not large enough to turn on a transistor, the bulk-drain connected transistor is assumed to work at the weak-inversion region during the whole

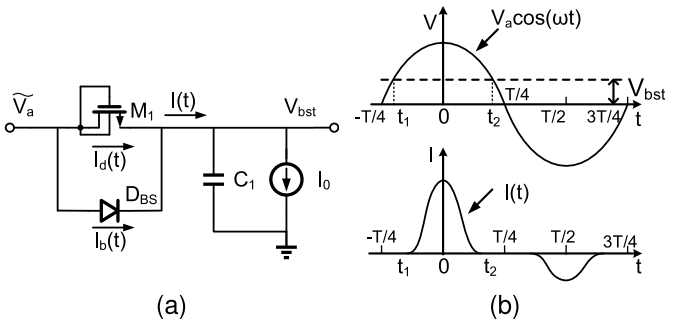

Fig. 6. (a) AC-to-dc conversion model of a bulk-drain connected transistor and (b) its voltage and current waveform.

period. The transistor is forward-biased during $[t_1, t_2]$ and reverse-biased during the rest of the period. The subthreshold current in this region can be expressed as [33]

$$I_{\text{dsub}} = I_{s0}\left(1 - \exp\left(-\frac{V_{\text{ds}}}{v_t}\right)\right)\exp\left(\frac{V_{\text{gs}} - V_{\text{th}} - V_{\text{OFF}}}{nv_t}\right) \quad (2)$$

$$I_{s0} = \mu_0 \frac{W}{L}\sqrt{\frac{q\varepsilon_{\text{si}}N_{\text{ch}}}{2\phi_s}}v_t^2 \quad (3)$$

where v_t is the thermal voltage, n is the subthreshold swing parameter, V_{OFF} is the subthreshold region offset voltage, V_{th} is the threshold voltage of the transistor, μ_0 is the mobility, q is the electron charge, ε_{si} is the silicon permittivity, N_{ch} is the doping concentration in the channel, and ϕ_s is the surface potential.

Given the transistor in bulk-drain connection, the varied bulk–source voltage introduces varied threshold voltage V_{th}. Thus, the body effect should be considered in this analysis, expressed as

$$V_{\text{th}} = V_{\text{th0}} + K_1\left(\sqrt{\phi_s - V_{\text{bs}}} - \sqrt{\phi_s}\right) - K_2 V_{\text{bs}} \quad (4)$$

where V_{th0} is the threshold voltage when $V_{\text{bs}} = 0$, K_1 and K_2 are first- and second-order body effect coefficients, respectively. Given that V_{bs} is quite small, the threshold voltage V_{th} can be linearized as

$$\begin{aligned} V_{\text{th}} &= V_{\text{th0}} - \left(\frac{K_1}{2\sqrt{\phi_s}} + K_2\right)V_{\text{bs}} \\ &\approx V_{\text{th0}} - kV_{\text{bs}}. \end{aligned} \quad (5)$$

Therefore, I_{dsub} can be further expressed as

$$I_{\text{dsub}} = I'_{s0}\left(1 - \exp\left(-\frac{V_{\text{ds}}}{v_t}\right)\right)\exp\left(\frac{(1+k)V_{\text{ds}}}{nv_t}\right) \quad (6)$$

where

$$I'_{s0} = \mu_0 \frac{W}{L}\sqrt{\frac{q\varepsilon_{\text{si}}N_{\text{ch}}}{2\phi_s}}v_t^2 \exp\left(-\frac{V_{\text{th0}} + V_{\text{OFF}}}{nv_t}\right). \quad (7)$$

Assuming that the current model of the parasitic diode D_{BS} is a resistance-free diode without current limiting feature because of small ac voltage, I_{bs} can be expressed as

$$I_{\text{bs}} = I_{\text{sbs}}\left(\exp\left(\frac{V_{\text{bs}}}{NV_{\text{tm}}}\right) - 1\right) \quad (8)$$

where $NV_{\text{tm}} = N_{\text{J}}v_t$; N_{J} is the junction emission coefficient.

For the load capacitor, the charging current is formed by the forward current of the bulk-drain connected transistor and parasitic diode. The discharging current consists of load current I_{load} and the reverse current from the nonlinear devices. In the steady state, the input charge Q_{in} equals the output charge Q_{out}, and it can be expressed as

$$Q_{\text{in}} = \int_{t_1}^{t_2} |I_{\text{dsub}}(t) + I_{\text{bs}}(t)|dt \quad (9)$$

$$Q_{\text{out}} = I_{\text{load}}T + \int_{t_2}^{T+t_1} |I_{\text{dsub}}(t) + I_{\text{bs}}(t)|dt. \quad (10)$$

Because the above equations contain a term $\exp(\cos\omega t)$, which has no Riemann integral function, the input signal $V_a \cos\omega t$ is simplified as its first two terms of the Taylor series expansion $V_a(1 - \omega^2 t^2/2)$. This approximation can only be used in $[t_1, t_2]$ to calculate Q_{in}. Thus, $|t_{1,2}|$ can be simplified as

$$|t_{1,2}| = \sqrt{2(V_a - V_{\text{bst}})/V_a}/\omega. \quad (11)$$

The input charge contributed by the subthreshold current Q_{d1} is expressed as

$$\begin{aligned} Q_{d1} = I_{s1}\,\text{erf}&\left(\sqrt{\frac{(1+k)V_a}{2nv_t}}\omega t_2\right) \\ &- I_{s2}\,\text{erf}\left(\sqrt{\frac{(1+k-n)V_a}{2nv_t}}\omega t_2\right) \end{aligned} \quad (12)$$

where

$$I_{s1} = \frac{I'_{s0}\exp\left[(1+k)(V_a - V_{\text{bst}})/nv_t\right]}{\omega\sqrt{(1+k)V_a/2\pi nv_t}} \quad (13)$$

$$I_{s2} = \frac{I'_{s0}\exp\left[(1+k-n)(V_a - V_{\text{bst}})/nv_t\right]}{\omega\sqrt{(1+k-n)V_a/2\pi nv_t}}. \quad (14)$$

The input charge contributed by the forward-biased diode current Q_{b1} is expressed as

$$Q_{b1} = -2I_{\text{sbs}}t_2 + I'_{\text{sbs}}\,\text{erf}(\sqrt{V_a/2N_{\text{tm}}}\omega t_2) \quad (15)$$

where

$$I'_{\text{sbs}} = \frac{I_{\text{sbs}}}{\omega}\sqrt{\frac{2\pi N_{\text{tm}}}{V_a}}\exp\left(\frac{V_a - V_{\text{bst}}}{N_{\text{tm}}}\right). \quad (16)$$

When the transistor is reverse-biased, the transistor leakage current I_{dlk} is the subthreshold current with $V_{\text{gs}} = 0$. Due to its small value, it would be unnecessary to calculate it without any approximation. Here, I_{dlk} is approximated as a sinusoidal wave

$$I_{\text{dlk}} = \begin{cases} |I_{\text{dlkp}}|\cos\omega'(t - t_s), & \dfrac{T}{2} - \dfrac{\pi}{2\omega'} \le t \le \dfrac{T}{2} + \dfrac{\pi}{2\omega'} \\ 0, & t < \dfrac{T}{2} - \dfrac{\pi}{2\omega'},\ t > \dfrac{T}{2} + \dfrac{\pi}{2\omega'} \end{cases} \quad (17)$$

where $\omega' = 3\pi/(T - 2t_2)$ and $t_s = (T + 4t_2)/6$

$$I_{\text{dlkp}} = I'_{s0}\left(1 - \exp\left(\frac{V_a + V_{\text{bst}}}{v_t}\right)\right)\exp\left(-\frac{k(V_a + V_{\text{bst}})}{nv_t}\right). \quad (18)$$

Thus, the output charge contributed by MOSFET leakage current $Q_{\rm dlk}$ is

$$Q_{\rm dlk} = 2(T - 2t_2)|I_{\rm dlkp}|/3\pi. \tag{19}$$

The output charge contributed by $D_{\rm BS}$ reverse current $Q_{\rm blk}$ is

$$Q_{\rm blk} = I_{\rm sbs}(T - 2t_2). \tag{20}$$

A further approximation is with $Q_{\rm in} = Q_{\rm out}$. Assuming that $V_a > 6\upsilon_t$ and $V_{\rm bst}$ is small enough to ensure that $V_a - V_{\rm bst} > 6\upsilon_t$, (12), (15), (19), and (20) can be simplified as

$$Q_{d1} \approx \frac{I'_{s0}}{\omega}\sqrt{\frac{2\pi n\upsilon_t}{(1+k)V_a}}\exp\frac{(1+k)(V_a - V_{\rm bst})}{n\upsilon_t} \tag{21}$$

$$Q_{b1} \approx \frac{I_{\rm sbs}}{\omega}\sqrt{\frac{2\pi NV_{\rm tm}}{V_a}}\exp\frac{V_a - V_{\rm bst}}{NV_{\rm tm}} \tag{22}$$

$$Q_{\rm dlk} \approx \frac{4I'_{s0}}{3\omega}\left(\pi - \sqrt{\frac{2(V_a - V_{\rm bst})}{V_a}}\right) \times \exp\frac{(n-k)(V_a + V_{\rm bst})}{n\upsilon_t} \tag{23}$$

$$Q_{\rm blk} \approx \frac{2I_{\rm sbs}}{\omega}\left(\pi - \sqrt{\frac{2(V_a - V_{\rm bst})}{V_a}}\right). \tag{24}$$

The output dc voltage is the root of the charge balance equation

$$Q_{d1} + Q_{b1} = Q_{d2} + Q_{b2} + 2\pi I_{\rm load}/\omega. \tag{25}$$

To validate this analysis, a multi-stage rectifier is designed and implemented with 40-nm CMOS technology. The simulation comparison to the mathematical model is performed with different load resistances and input amplitudes at 55 GHz. In SPICE simulations, the transistors and MoM capacitors are based on the foundry-provided PDK RF model. The transistor's $V_{\rm th0}$ is 435 mV. When the rectifier is working in a high sensitivity range, the transistors are in the weak inversion region. Because the input impedance of an eight-stage rectifier is $8–46.8j\Omega$, the -8-, -7-, and -6-dBm input power are transferred to 290, 330, and 370 mV in the voltage domain.

Fig. 7 shows the output voltage of the eight-stage rectifier with different input voltage amplitudes $\widetilde{V_{\rm RF}}$. Fig. 8 shows the output voltage of three rectifiers with input voltage amplitude $\widetilde{V_{\rm RF}} = 370$ mV. The rectifiers' stage numbers are 2, 4, and 8, respectively. Compared to the PDK model, the output voltages calculated by the mathematical model are getting larger when the input voltage increases. The deviation is coming from the forward-biased parasitic diode $D_{\rm BS}$. It is usually recommended to be reverse-biased for an active transistor operation. However, in an mm-wave rectifier, it is forward-biased periodically to deliver more current to the load and achieve better sensitivity. However, the forward-biased current in the model file is facing the modeling limitation from the PDK recommended region.

As shown in Fig. 8, the output voltages calculated by the mathematical model are also getting larger with the increase in the stage number. This deviation comes from the decreased ac portion amplitude V_a. According to (1), V_a is determined by

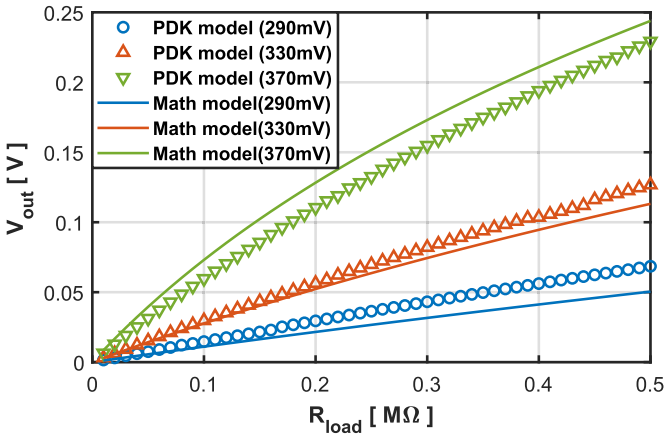

Fig. 7. Comparison of the mathematical model in this work to the PDK model: eight-stage rectifier output voltage with different load resistances and input amplitudes.

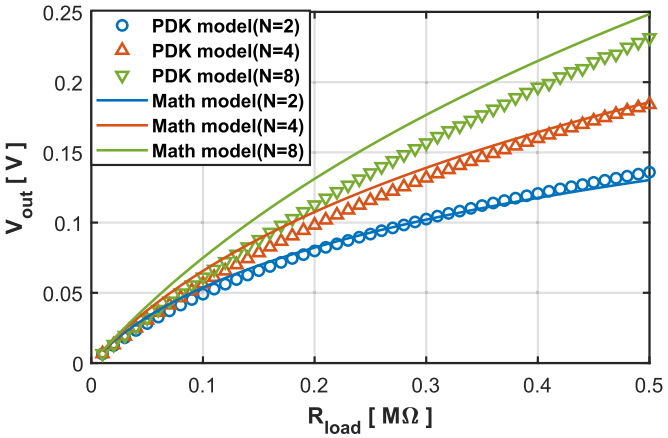

Fig. 8. Comparison of the mathematical model in this work to the PDK model: output voltage of multi-stage rectifiers with different load resistances and stage numbers.

the voltage-depended $C_{\rm par}$. The mathematical model assumes that each stage has the same $C_{\rm par}$, hence the same V_a. However, the parasitic capacitance contributor C_W is not the same in each transistor. For the parasitic capacitor $C_{\rm GS}$ or $C_{\rm BS}$, the voltages on them are always $\widetilde{V_{\rm ai}}$ together with one boost voltage $V_{\rm bst}$. However, C_W is the overall capacitance between the bulk and N-well, and between N-well and P-substrate. Its voltage is $\widetilde{V_{\rm ai}}$ together with N times $V_{\rm bst}$, depending on the stage number. Because of the different C_W capacitances, a decreased $\widetilde{V_{\rm ai}}$ is observed. Therefore, the deviation becomes larger when more stages are used.

C. Power Consumption and Efficiency of N-Stage Rectifier

The power consumption of the one-stage rectifier is the sum of leakage power consumption and nonlinear device power consumption. The nonlinear power consumption is contributed by bulk-drain connected transistors and parasite diodes in forward- and reverse-biased regions

$$P_{\rm loss} = 2(P_{\rm leak} + P_{d1} + P_{b1} + P_{b2} + P_{d2}) \tag{26}$$

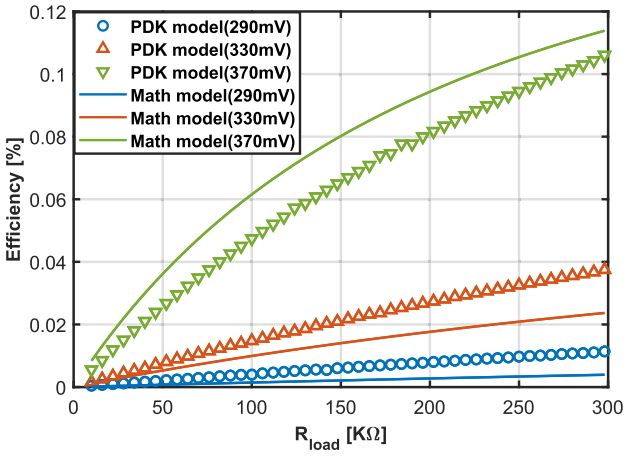

Fig. 9. Theoretical and simulated efficiencies of an eight-stage rectifier with different load resistances and input amplitudes.

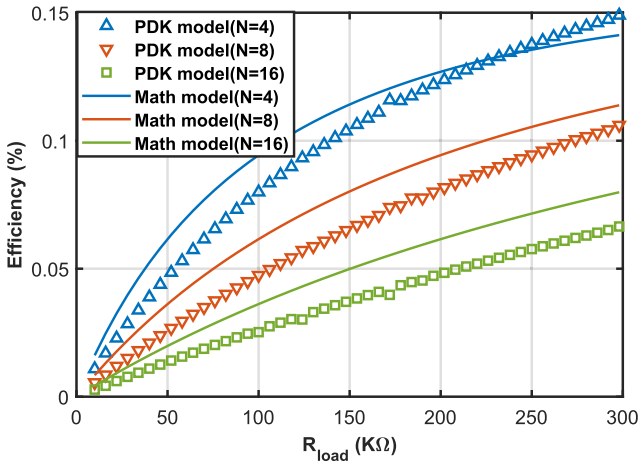

Fig. 10. Theoretical and simulated total efficiencies of multi-stage rectifiers with different load resistances and stage numbers.

where P_{leak} is the power consumption of the leakage current source I_{leak}, and P_{d1} and P_{b1} are the power consumption of bulk-drain connected transistor and parasite diode in forward-biased region, respectively, while P_{d2} and P_{b2} are those in reverse-biased region. The approximation of those components is listed as

$$P_{\text{leak}} = 2V_a I_{\text{leak}}/\pi \tag{27}$$

$$P_{d1} \approx I'_{s0}\sqrt{\frac{n\upsilon_t}{2\pi(1+k)V_a}}(V_a - V_{\text{bst}})\exp\frac{(1+k)(V_a - V_{\text{bst}})}{n\upsilon_t} \tag{28}$$

$$P_{b1} \approx I_{\text{sbs}}\sqrt{\frac{NV_{\text{tm}}}{2\pi V_a}}\left(V_a - V_{\text{bst}} - \frac{NV_{\text{tm}}}{2}\right)\exp\frac{V_a - V_{\text{bst}}}{NV_{\text{tm}}} \tag{29}$$

$$P_{d2} \approx \frac{4I'_{s0}}{3\pi}\left(1 - \frac{2t_2}{T}\right)(V_a + V_{\text{bst}})\exp\frac{(n-k)(V_a + V_{\text{bst}})}{n\upsilon_t} \tag{30}$$

$$P_{b2} \approx I_{\text{sbs}}V_{\text{bst}}\left(1 - \frac{2t_2}{T}\right) + I_{\text{sbs}}V_a\sin(\omega t_2)/\pi. \tag{31}$$

Therefore, the efficiency of the N-stage rectifier can now be expressed as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + NP_{\text{loss}}}. \tag{32}$$

Fig. 9 shows the efficiency of the eight-stage rectifier with different input voltage amplitudes V_{in}, i.e., 290, 330, and 370 mV. Fig. 10 shows the total efficiency of four-, eight-, and 16-stage rectifiers with input voltage amplitude $\widetilde{V_{\text{RF}}} = 370$ mV. Since the rectifier is working in the weak inversion region, the efficiency in all different scenarios is quite limited. With the increase in the stage number, the efficiency dropping can be observed. Therefore, rectifiers with fewer stage numbers are better when the maximum-efficiency strategy is adopted.

III. Rectifier Implementation

A. Stage Number Optimization of N-Stage Rectifier

According to the rectifier mathematical analysis and modeling, a rectifier with more stages would have an advantage on the output voltage under the same input amplitude and load condition. However, the measurement of mm-wave rectifiers is based on power. High-stage rectifiers suffer from a lower input amplitude because of their decreased input impedance. Therefore, the optimal stage number should be found to achieve the best sensitivity.

For each stage, the input impedance is mainly contributed by the input capacitor C_c. From the RF input port, each stage is connected in parallel in an N-stage rectifier. Therefore, its input impedance $Z_{\text{in}}(n)$ can be expressed as

$$Z_{\text{in}}(n) = Z_{\text{in}}(1)/n \tag{33}$$

where $Z_{\text{in}}(1)$ is the input impedance of a one-stage rectifier. With an input power P_{in}, the N-stage rectifier's input amplitude V_{RF} is derived as

$$V_{\text{RF}}(n) = \sqrt{2P_{\text{in}}Z_{\text{in}}(1)/n}. \tag{34}$$

Fig. 11(a) shows the simulated input impedance and the input amplitude of different rectifiers with the same input power. Taking the input impedance and input amplitude with a fixed power level into consideration, the eight-stage rectifier shows the best sensitivity, as shown in Fig. 11(b). Therefore, the matching network is designed for the eight-stage bulk-drain connection rectifier.

B. Matching Network of N-Stage Rectifier

An eight-stage mm-wave rectifier is implemented with bulk-drain connected transistors. Different RF power levels will influence the transistor's working region. Therefore, the parasitic capacitance and the input impedance vary between the weak inversion region and the strong inversion region [34]. In this work, the input matching network is done with an input power of -6 to -4 dBm for the high-sensitivity application.

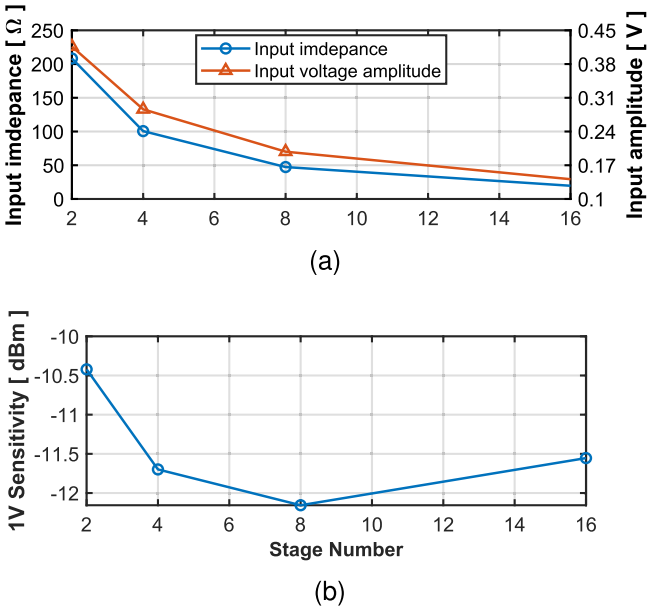

Fig. 11. (a) Input impedance and input amplitude with the same input power. (b) 1-V sensitivity of multi-stage rectifiers with different stage numbers.

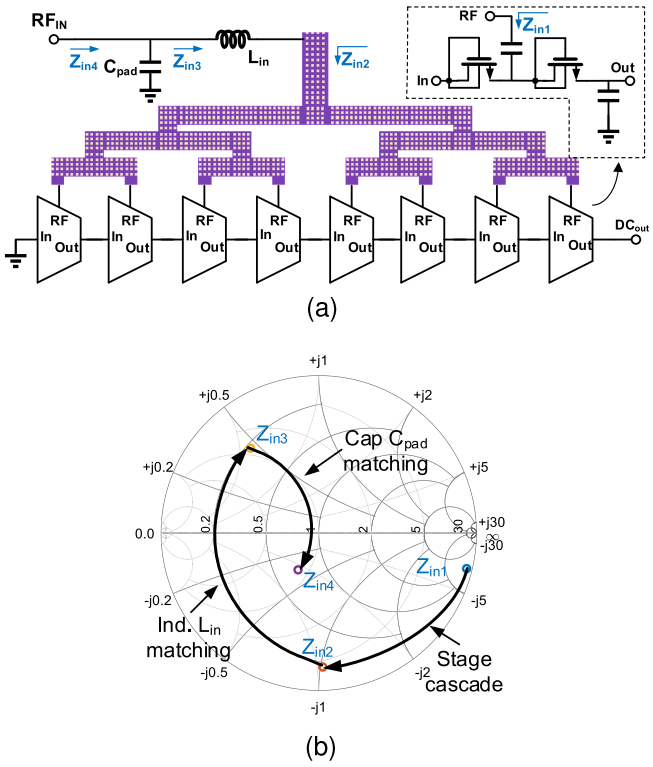

Fig. 12. (a) Proposed eight-stage mm-wave rectifier with bulk-drain connected transistors, an input matching network, and a TTPS. (b) Input matching illustration in the Smith chart.

A series inductor L_{in} is used as the input matching network. Also, a tree-type power splitter (TTPS) is inserted in-between the input matching inductor and the coupling capacitors, as shown in Fig. 12. By cascading one-stage rectifier, the input impedance Z_{in1} is transformed to Z_{in2}. Considering the PAD parasite capacitor C_{pad}, the mm-wave rectifier shows a well-matched 50-Ω impedance with an input matching network.

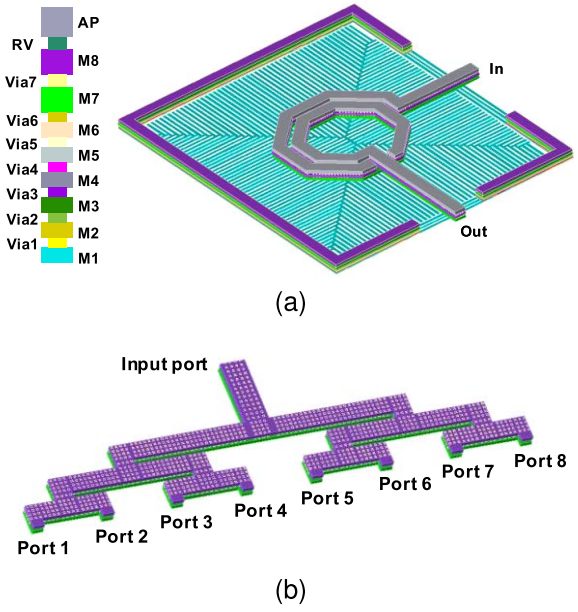

Fig. 13. 3-D model of the input matching inductor and the TTPS. (a) 3-D model of the input matching inductor with meshed ground shielding. (b) 3-D model of the TTPS with input and output ports for each stage.

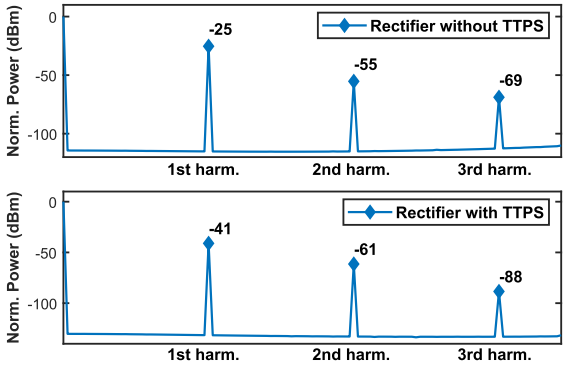

Fig. 14. Comparison on SSR for a rectifier with and without the TTPS.

Fig. 13 shows the 3-D models of the input matching inductor and the TTPS. The TTPS feeds the input RF signal to each stage with the same phase. Therefore, there is only one transistor charging/discharging the load capacitor. Otherwise, some capacitors will be charged by two transistors causing higher voltage while the others with lower voltage by discharging. The overcharge/discharge state will pass from the first stage to the last one, introducing the final output's ac component. In the wireless power receiver, a rectifier is a power supply. The high-frequency ac component at the dc output introduces distortion for the load. The signal suppression ratio (SSR) is defined as the ratio between RF leakage power and dc power. Fig. 14 shows a comparison of a rectifier with the TTPS and without TTPS. By introducing an equal phase at each stage's input, the rectifier with TTPS improves the suppression by 16 dB.

IV. Measurement Results

The chip is fabricated in 40-nm CMOS technology. The die area, including the input matching inductor, is 0.2 × 0.12 mm^2. The die micrograph and the measurement setup

TABLE I
SILICON-BASED MM-WAVE RECTIFIER PERFORMANCE COMPARISON TABLE

Reference		Technology [nm]	Freq. Band [GHz]	Topology	Stage	Area [mm^2]	Freq. [GHz]	Vout [V]	Sensitivity [dBm]	Sensitivity FoM* [dB]
[12]	APWC 2018	130-nm BiCMOS	24	Dickson	1	0.09	24	1	-3	30.60
[1]	JSSC 2010	90-nm CMOS	45	Dickson	10	N/A	45	1	1	32.06
[11]	A-SSCC 2012	65-nm CMOS	60	Dickson	1	0.066	60	1	1	34.56
[15]	MWCL 2016	65-nm bulk CMOS	50–60	Dickson BB	3	0.0153	60	1	-5	40.56
[16]	MWCL 2021	22-nm FDSOI	61	Dickson BB	2	N/A	61	1	1	31.61
[25]	JSSC 2015	65-nm CMOS	24	Dickson LP	6	N/A	24	0.9	-10.5	37.19
[23]	RFIC 2013	65-nm CMOS	62	Dickson LP	1	0.182	62	1	-4	39.85
[24]	RFIC 2013	65-nm CMOS	70–72	Dickson LP	3	N/A	71	1	5	32.03
[20]	T-MTT 2014	65-nm bulk CMOS	24/35/60	Dickson ITC	1	N/A	35	1	2	28.88
[19]	RFIC 2013	40-nm bulk CMOS	60	Dickson ITC	1	N/A	60	1	6	29.59
[22]	SSCL 2021	40-nm bulk CMOS	38/60	Dickson ITC	3	0.026	40/60	1	-7.8/-6.6	39.8/42.2
[21]	RFID 2020	22-nm FDSOI	61	Dickson ITC	3	2.4	61	0.4	-3	30.75
[27]	T-MTT 2014	65-nm bulk CMOS	46–56	Dickson IPVM+ITC	7	0.148	53	1.2	-7	43.07
[28]	T-MTT 2019	65-nm CMOS	91/94	Switched	N/A	0.0875	94	0.64	16	19.59
[29]	EuMC 2013	90-nm CMOS	95–99	Inverted VCO	N/A	0.15	91	0.8	11.4	25.84
This Work		40-nm bulk CMOS	57–64	Dickson BDC	8	0.024	57	1	-7.1	42.22

* sFoM = 20log(f_{req}[GHz])+20log(V_{out}[V])-P_{in}[dBm]

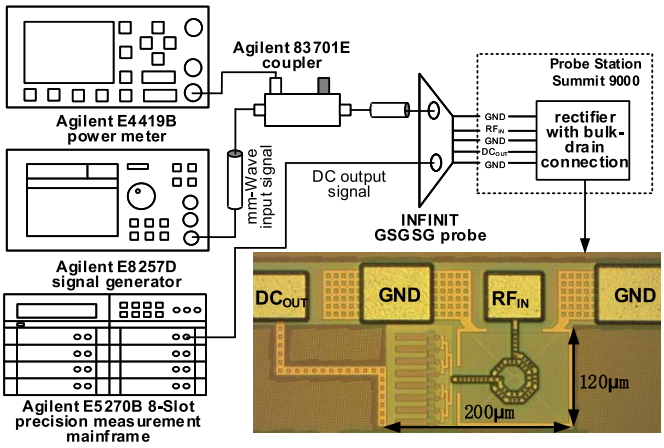

Fig. 15. Die micrograph and measurement setup.

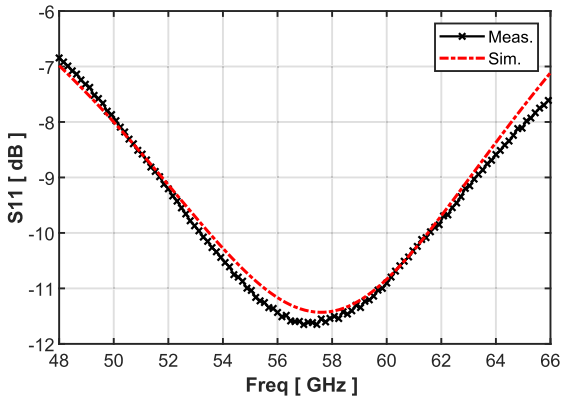

Fig. 16. Measured S_{11} of the rectifier and comparison to the simulated result.

are shown in Fig. 15. The chip is measured with on-wafer RF probes with the input signal provided by an Agilent E8257D signal generator. The input power is measured by an Agilent E4419B power meter through a directional coupler (Agilent 83701E). The optimal load current for the rectifier efficiency is accurately controlled by the Agilent E5270B precision measurement mainframe. The S-parameters of this rectifier are measured with the Agilent N5247A PNX-X network analyzer. As shown in Fig. 16, the measured small-signal input matching S_{11} of the rectifier is -11.6 dB at 57 GHz and less than -7 dB from 48 to 66 GHz. Simulation results also predict that the center frequency of S_{11} is at 57 GHz. To explore the output dc voltage versus input RF power characteristic of this rectifier, different input powers from -15 to -2 dBm have been fed to this rectifier. The measurement results are presented in Fig. 17. With -2-dBm input power, this rectifier can provide more than 3-V output voltage at 57 and 60 GHz, while the output voltage is near 2 V at 64 GHz. A comparison of the measured outputs to the proposed mathematical model is also shown in Fig. 17. From this comparison, the mathematical modeling's effectiveness in this article is also verified. With the input power increased, the forward-biasing current of the parasitic diode D_{BS} results in a larger output voltage. Fig. 18 summarized this rectifier's measured sensitivity for 1-V output voltage over 56–67 GHz, covering the whole 60-GHz ISM band. The rectifier achieves a peak sensitivity of -7.1 dBm at 57 GHz. Over the entire 60-GHz ISM band, this mm-wave rectifier can provide more than 1-V output voltage with an input power of -4.5 dBm. This sensitivity corresponds to a 1.5-m power transfer requirement at 57 GHz and

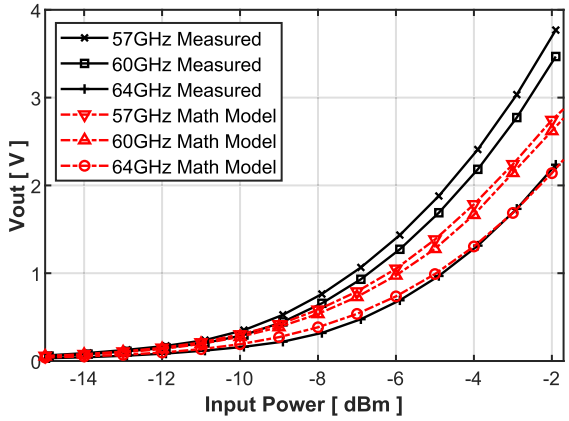

Fig. 17. Measured characteristic of the dc output voltage versus input RF power and comparison to the mathematical model in this work.

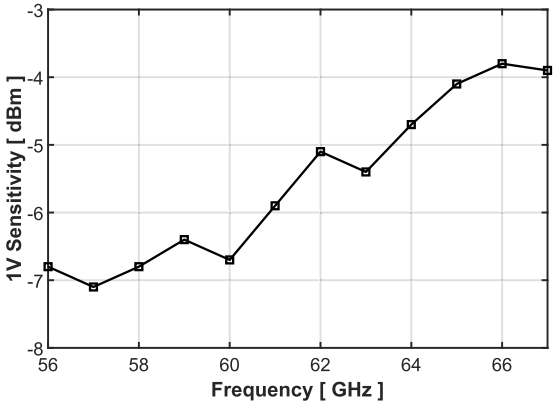

Fig. 18. Measured characteristic of rectifier sensitivity for 1-V dc output voltage with input RF signal frequency.

a 1-m wireless power transfer distance requirement over the entire 60-GHz ISM band.

Table I shows the performance summary and a comparison of the proposed eight-stage mm-wave rectifier with bulk-drain connection to other state-of-the-art mm-wave rectifiers in silicon-based technologies. A sensitivity Figure of Merit (sFoM) is defined in (35) for comparing with other mm-wave rectifiers in terms of sensitivity. In (35), F_{req} is the rectifier working frequency, V_{out} is the measured output sensitivity voltage, and P_{in} is the input power according to the sensitivity voltage. This work achieves a sensitivity FoM of 42.22 dB

$$\text{sFoM} = 20\log(F_{\text{req}}[\text{GHz}]) + 20\log(V_{\text{out}}[V]) - P_{\text{in}}[\text{dBm}]. \tag{35}$$

V. Conclusion

In an mm-wave wireless communication network, the IoT transponder function at mm-wave frequencies has the advantage of potential massive deployment combined with cloud computing and AI technology. In these scenarios, low cost and small size are crucial requirements for the transponder. IoT transponders with wireless power functions would be an attractive solution for their unique advantage of maintenance-free usage. However, the sensitivity of the rectifier is the limiting factor for the wireless power transfer distance. In a high sensitivity situation, the transistor works below the threshold voltage. This article presents a mathematical model and analysis of a multi-stage mm-wave rectifier in the weak inversion region. The intrinsic threshold voltage modulation can improve the sensitivity of the multi-stage rectifier. This work achieves −7.1-dBm input sensitivity at 57 GHz with 1-V dc output voltage. Over the entire 60-GHz ISM band, this mm-wave rectifier provides more than 1-V output voltage with an input power at −4.5 dBm. This sensitivity corresponds to a 1.5-m power transfer requirement at 57 GHz and a 1-m wireless power transfer distance requirement over the entire 60-GHz ISM band. Compared to other works, the proposed rectifier achieves better sensitivity while maintaining a compact size, suitable for the mm-wave wireless powered transponder in a middle-distance application.

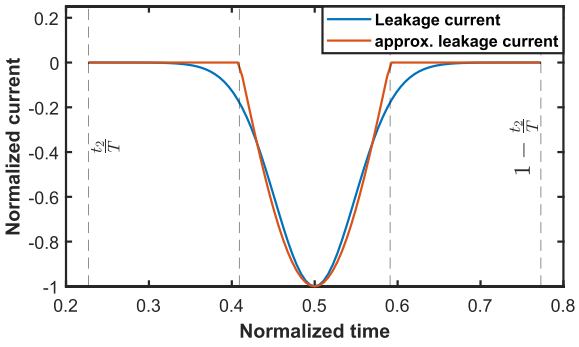

Fig. 19. Normalized leakage current and the approximated sinusoidal leakage current with $V_a = 350$ mV and $V_{\text{bst}} = 50$ mV.

Appendix
Input and Output Charge Approximation

By solving (11) and (12), the input charge contributed by the subthreshold current Q_{d1} can be expressed as

$$Q_{d1} = I_{s1}\,\text{erf}\left(\sqrt{\frac{(1+k)(V_a - V_{\text{bst}})}{n v_t}}\right) - I_{s2}\,\text{erf}\left(\sqrt{\frac{(1+k-n)(V_a - V_{\text{bst}})}{n v_t}}\right). \tag{A1}$$

Assuming that $(V_a - V_{\text{bst}}) > n v_t$ and $1+k-n > 1$, the inputs of both the erf function are greater than 1, so their outputs can be approximated as 1. Therefore, Q_{d1} can be further simplified with (13) and (14)

$$Q_{d1} = \frac{I'_{s0}}{\omega}\sqrt{\frac{2\pi n v_t}{V_a}}\exp\left(\frac{(1+k)(V_a - V_{\text{bst}})}{n v_t}\right) \times \left(\frac{1}{\sqrt{1+k}} - \frac{1}{\sqrt{1+k-n}}\exp\left(-\frac{V_a - V_{\text{bst}}}{v_t}\right)\right). \tag{A2}$$

By neglecting the much smaller term $\exp(-(V_a - V_{\text{bst}})/v_t)$, Q_{d1} is finally simplified as (21). This approximation method

is also applicable to the input charge contributed by the forward-biased diode current Q_{b1}.

This work employed a sinusoidal wave with the amplitude as the maximum leakage current to approximate the bulk-connected transistor leakage current. Due to the exponential dependence of voltage, the effective period is not the duration when the transistor is reverse-biased, as shown in Fig. 6(b). A numerical approximation is made. Fig. 19 shows the normalized leakage current and the approximated leakage current, assuming that $V_a = 500$ mV and $V_{\text{bst}} = 100$ mV.

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