

A Wideband *E/W*-Band Low-Noise Amplifier MMIC in a 70-nm Gate-Length GaN HEMT Technology

Fabian Thome¹, Peter Brückner¹, Stefano Leone¹, and Rüdiger Quay¹, *Senior Member, IEEE*

Abstract—This article reports on a gallium-nitride (GaN) low-noise amplifier (LNA) monolithic microwave integrated circuit (MMIC) with a 3-dB gain bandwidth (BW) from 63 to 101 GHz. The MMIC is fabricated in the Fraunhofer IAF 70-nm GaN-on-silicon-carbide (SiC) high-electron-mobility transistor (HEMT) technology. The four-stage common-source LNA exhibits an average noise figure (NF) of 3 dB for a measured frequency range from 75 to 101 GHz. The MMIC reaches a minimum NF of 2.8 dB at an operating frequency of 83 GHz. A mapping of two 100-mm wafers shows an excellent homogeneity with an 86% yield and an average NF of 3–3.3 dB. At 100 GHz, the LNA obtains output-referred 1-dB compression and third-order intercept points of 12.1 and 14.4 dBm, respectively. Furthermore, comprehensive investigations of the bias dependence of all measured performance parameters provide an insight into the presented device and LNA. To the best of the authors' knowledge, this MMIC demonstrates the lowest NF among GaN LNAs at *E/W*-band frequencies.

Index Terms—*E*-band, gallium nitride (GaN), high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), silicon carbide (SiC), *W*-band.

I. INTRODUCTION

DUE to a high band gap, gallium nitride (GaN) has been widely used for high power amplifiers (PAs) for frequencies as high as 200 GHz. Even though also other circuit topologies have been reported, the generation of RF power is still the dominating topic and main driver for GaN high-electron-mobility transistor (HEMT) technologies. However, low-noise amplifiers (LNAs) can as well benefit from the outstanding robustness and ability to operate GaN HEMTs with higher supply voltages than other transistor technologies allow. Technology developments and the gate-length scaling

of GaN HEMTs provided, over the years, a promising combination of performance parameters, such as the transition frequency (f_T) and the minimum noise figure (NF_{\min}) with still considerably high breakdown voltages compared to other technologies. Thereby, LNA and PA applications benefit, at least up to some extent, from the same target to optimize GaN HEMTs for a steep increase of the transconductance (g_m) in the turn-on region when plotting g_m versus the drain current (I_d). A corresponding figure of merit for low-noise devices is known as $g_m/\sqrt{I_d}$. For PAs, a low quiescent I_d reduces the quiescent dissipated power ($P_{dc,q}$) and consequently the drain efficiency can be increased. In general, LNAs benefit from a low quiescent I_d as well since the channel-related noise power of a transistor is reduced. A high g_m corresponds to a high RF gain which can suppress the impact of the output-related noise power even further [1].

At the same time, GaN HEMTs provide RF output power (P_{out}) densities that are at least a magnitude higher than dedicated InGaAs-based low-noise technologies and still factors compared to, e.g., pHEMT technologies. High output power is shown, for instance, in wideband PA monolithic microwave integrated circuits (MMICs) with a P_{out} of 34.6 dBm (75–100 GHz) demonstrated with a 0.14- μm GaN technology [2] and 22.5 dBm (68–110 GHz) realized with a 50-nm InGaAs mHEMT technology [3]. Both references exhibit state-of-the-art performance compared within the corresponding class of technology but highlight at the same time the benefit of GaN technologies for large-signal performance characteristics. However, it is not only the increased power levels of GaN technologies, most likely leading to an increased dynamic range in systems, which should be considered. Several, especially wideband, applications, such as sensing or imaging, still require the lowest possible noise figures (NFs) to obtain a sensitive receiver performance. This makes modern GaN technologies attractive candidates for highly linear high-frequency low-noise receiver applications and a strong competitor for established technologies.

Fig. 1 shows an overview of state-of-the-art GaN LNA MMICs in the *W*-band frequency range (75–110 GHz). Best GaN-on-silicon-carbide (SiC) results report NFs of less than 4 dB, at least for some part of the band [4], [5]. This compares very good to other technologies, such as CMOS with an NF of 3.7–4.5 dB from 67 to 79 GHz [6] and pHEMT with an average NF of 3.8 dB from 90 to 100 GHz [7].

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The authors are with the Fraunhofer IAF, Fraunhofer Institute for Applied Solid State Physics, 79108 Freiburg im Breisgau, Germany (e-mail: fabian.thome@iaf.fraunhofer.de).

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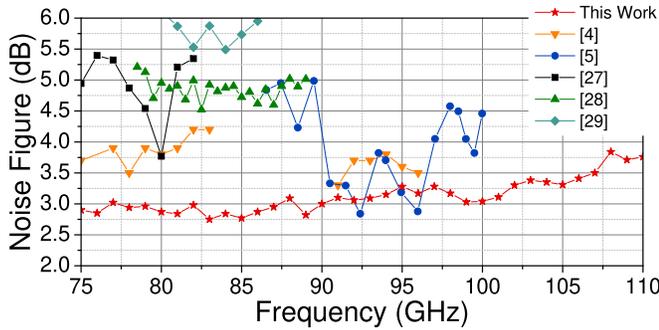


Fig. 1. Comparison of state-of-the-art GaN LNAs in the 75–110-GHz frequency range.

However, the absolute state of the art over all semiconductor technologies is still demonstrated by InGaAs-based HEMTs with an average NF over the entire W -band of 1.9 dB [8], [9]. When thinking about system applications, one might also consider other circuit topologies, e.g., distributed amplifiers, that have reported in W -band an appealing combination of an average NF of 3.6 dB and an output-referred 1-dB compression point ($OP_{1\text{dB}}$) in the range of 7.4–8.4 dBm.

In this work, we demonstrate a GaN LNA MMIC fabricated in a 70-nm gate-length HEMT technology. The design targets an NF as low as 3 dB and an operating frequency that covers the E -band satellite communication bands (71–76 GHz and 81–86 GHz) and the radar bands from 92 to 100 GHz. The article is organized as follows. Section II summarizes key features of the utilized in-house GaN HEMT technology. Section III describes the device selection and the design of the presented LNA. The on-wafer measured small- and large-signal performance is presented in Section IV. An extensive set of measurement results provides an insight into the used GaN device and a better understanding of performance tradeoffs, e.g., versus bias. Section V summarizes the results and compares them to the state of the art.

II. 70-nm GaN-ON-SiC HEMT TECHNOLOGY

The presented work is based on the Fraunhofer IAF 70-nm gate-length GaN HEMT technology. The epitaxial layers are grown in-house by metal-organic chemical vapor deposition (MOCVD) on 100-mm semi-insulating 4H-SiC substrates. The AlGaIn/GaN heterostructure includes a thin aluminum-nitride (AlN) interlayer for reducing the sheet resistance and improving the confinement of the 2-D electron gas (2DEG). The ohmic contact resistance as well as the source and drain access resistances are reduced by silicon implantation. Furthermore, the transistor layout is optimized so that, especially, the source resistance is reduced. This is important for increasing the extrinsic g_m and by that the extrinsic f_T which is also a crucial parameter for low-noise operation (further discussed in Section III-A). The T-gates are defined by electron-beam (e-beam) lithography and feature several gate lengths. In this work, T-gates with a gate length of 70 and 100 nm are used. The parasitic capacitance of the gates is reduced by an optimized deposition of the metal-insulator-metal (MIM) silicon nitride.

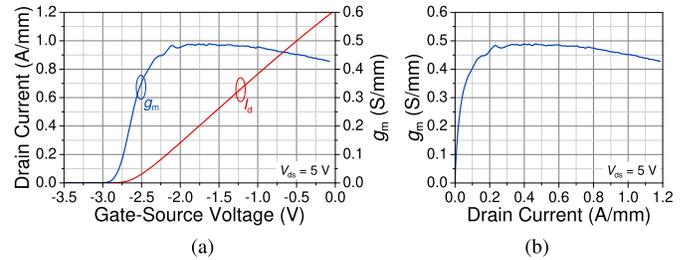


Fig. 2. Transfer characteristic of a 70-nm gate-length GaN HEMT with a gate width of $2 \times 30 \mu\text{m}$. (a) Normalized I_d and dc g_m versus V_{gs} for a V_{ds} of 5 V. (b) Same data as in (a) are shown, however, g_m is plotted versus I_d .

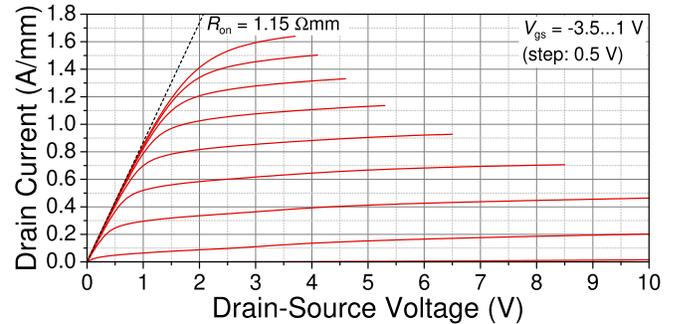


Fig. 3. DC output characteristic of a 70-nm gate-length GaN HEMT with a gate width of $2 \times 30 \mu\text{m}$.

The technology features two gold-based interconnection metallization layers. The plated top metal is done in an air-bridge technology. In addition, 50- Ω/sq NiCr thin-film resistors (TFRs) are available. After finishing the front-side process, a full back-side process including wafer thinning to a thickness of 75 μm , through-substrate vias, and back-side metallization follows [10].

In Fig. 2, the dc transfer characteristic of a HEMT with a gate length of 70 nm is given. Fig. 2(a) shows g_m and I_d versus the gate-source voltage (V_{gs}) of a $2 \times 30 \mu\text{m}$ transistor for a drain-source voltage (V_{ds}) of 5 V. In Fig. 2(b), g_m is plotted versus I_d . For an I_d of approximately 400 mA/mm, a peak g_m of 490 mS/mm is achieved. g_m exceeds 400 mS/mm, which is more than 80% of peak g_m , for an I_d of 100 mA/mm and stays above this value up to at least 1.2 A/mm. In Fig. 3, the dc output characteristic of a $2 \times 30 \mu\text{m}$ transistor is given. The ON-resistance (R_{ON}) exhibits a value of 1.15 $\Omega \cdot \text{mm}$. The gate-drain breakdown voltage (with a gate current of 1 mA/mm as stop criterion) is approximately 30 V.

Fig. 4 shows the gain characteristics of a 70-nm gate-length GaN HEMT with a gate width of $4 \times 30 \mu\text{m}$. The corresponding S-parameters are measured with an Anritsu VectorStar vector network analyzer (VNA) setup from 1 to 225 GHz. The device is biased with a V_{ds} of 5 V and an I_d of 300 mA/mm. For this bias condition, an extrapolated f_T and maximum-oscillation frequency (f_{max}) of 145 and 296 GHz are achieved, respectively. The VNA is calibrated with dedicated on-wafer calibration standards using a line-reflect-reflect-match (LRRM) algorithm. The calibration standards are designed so that the reference planes of the measurement are on the wafer. This allows to have the reference plane of

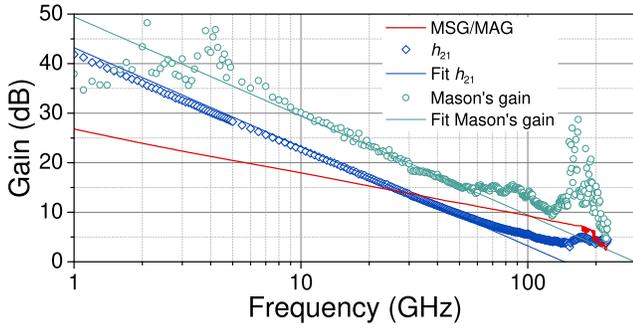


Fig. 4. Measured extrinsic MSG/MAG, h_{21} , and Mason's unilateral gain of a 70-nm gate-length GaN HEMT with a gate width of $4 \times 30 \mu\text{m}$. The transistor is biased with a V_{ds} of 5 V and an I_d of 300 mA/mm. For the extrapolated extrinsic f_T and f_{max} , curves are fit to the measured h_{21} and Mason's gain at a frequency range from 10 to 50 GHz and extrapolated with a constant slope of -20 dB.

the measurement directly at the reference plane of the device under test (DUT). Consequently, the RF pad is not included in the measured data. The standards use the same grounded coplanar waveguide (CPWG) as the measured DUTs. The ground-to-ground spacing of the CPWG is $50 \mu\text{m}$. The line standard consists of a zero-length through (reference planes of both ports on top of each other). The open and short standards are open and shorted $50\text{-}\Omega$ transmission lines, respectively. For the match standard, a model is used that is based on an EM simulation (done with CST Microwave Studio) and verified against measurements with a multiline through-reflect-line calibration. The model that is used for the calibration accounts for dc resistance variations of the dedicated TFR of the measured match standard.

Fig. 5 shows contour plots of the extracted f_T and f_{max} over bias. A maximum f_T is achieved for a V_{ds} of 5 V and an I_d of 300 mA/mm. Furthermore, the V_{ds} for an optimum f_T at each I_d is approximately 5 V. For an I_d of more than 125 mA/mm, the improvement of f_T starts to saturate. This observation is in line with the g_m versus I_d characteristic where for an I_d of more than 100 mA/mm, g_m exceeds 80% of its maximum value. A maximum f_{max} of 380 GHz is achieved by increasing V_{ds} and I_d to 10 V and 400 mA/mm, respectively.

III. LNA DESIGN

This part describes in Section III-A the device selection for an optimal LNA MMIC design, which is then explained in Section III-B.

A. Device Considerations

As is known from the low-noise theory, e.g., as given in [1] and [11], a major goal is to optimize a transistor and its operation so that it provides highest possible gain at lowest possible bias, especially low drain current. This can be observed from the minimum noise temperature (T_{min}) of an intrinsic HEMT [1]

$$T_{min} \approx 2 \frac{f}{f_T} \sqrt{g_{ds} T_d r_{gs} T_g} \quad (1)$$

where T_d is the drain noise temperature related to the small-signal output conductance (g_{ds}) and T_g is the gate noise

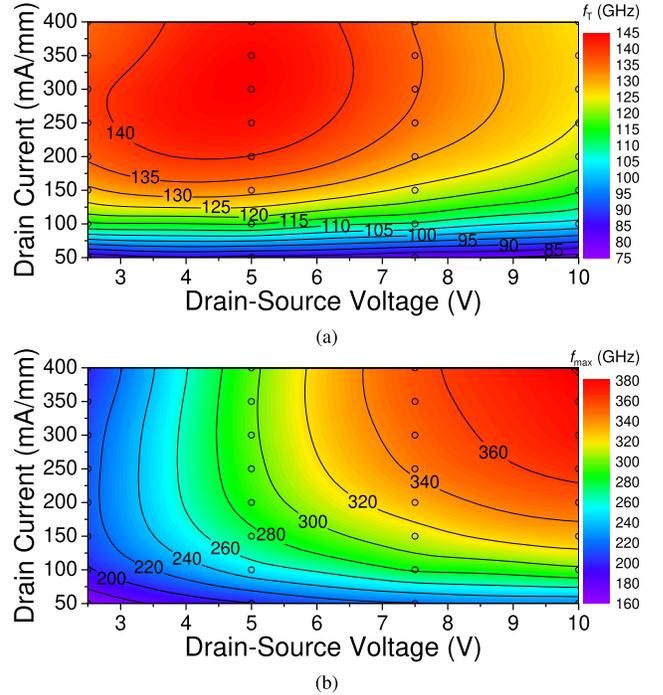


Fig. 5. Contour plot of the extrapolated extrinsic (a) f_T and (b) f_{max} versus bias of a 70-nm gate-length GaN HEMT with a gate width of $4 \times 30 \mu\text{m}$. The circles denote the bias point where the corresponding S-parameters have been measured (up to frequencies of 225 GHz).

temperature related to the intrinsic gate-source resistance (r_{gs}). T_g is considered as temperature equal to the ambient temperature of the device. T_d is still modeled as thermal noise, but describing the channel noise as the temperature of $r_{ds} = 1/g_{ds}$ independent and, in general, much higher than the corresponding lattice temperature. By that, (1) illustrates the tradeoff between f_T and T_d since both parameters depend on the bias and increase with I_d . Correlating this to the f_T contour, as shown in Fig. 5(a), the noise-optimum V_{ds} is at approximately 5 V. The noise-optimum I_d is expected at about 200 mA/mm since, up to 200 mA/mm, f_T is strongly improving, whereas f_T is flattening for a further current increase. Thus, for the design of the LNA, the bias of the noise-relevant HEMTs is a V_{ds} of 5 V and an I_d of 200 mA/mm. The importance of (the extrinsic) f_T further emphasizes the benefit of a transistor layout optimization with a reduced source resistance.

In this work, the small-signal HEMT model is based on a compact scalable model approach as described in [12] including a Pospieszalski noise model [1]. The small-signal model is fit to measured S-parameters up to 225 GHz and features a scalability over a wide range of device sizes and bias point. The noise model is extracted upon on-wafer noise parameter measurements from 8 to 50 GHz. Fig. 6 shows the simulated NF_{min} of a $4 \times 15 \mu\text{m}$ HEMT, as used in Section III-B, for a V_{ds} of 5 V and an I_d of 100, 200, and 300 mA/mm. It strengthens the conclusion on 200 mA/mm being optimal for noise. For a V_{ds} of 5 V and an I_d of 200 mA/mm, T_d is approximately 2300 K and the simulated f_T and f_{max} of a $4 \times 15 \mu\text{m}$ HEMT are 108 and 350 GHz, respectively.

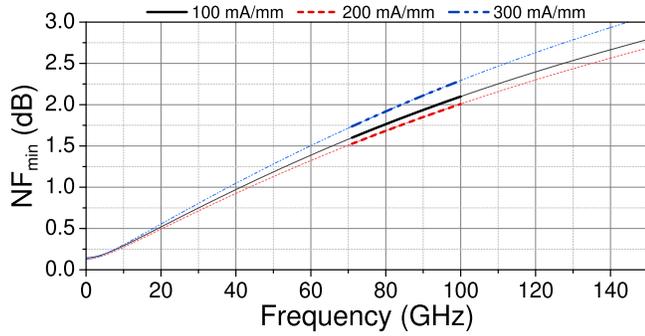


Fig. 6. Simulated NF_{\min} of a $4 \times 15 \mu\text{m}$ HEMT in common-source configuration and different drain currents. V_{ds} is 5 V. The intended design frequency range (71–100 GHz) is highlighted by bold lines.

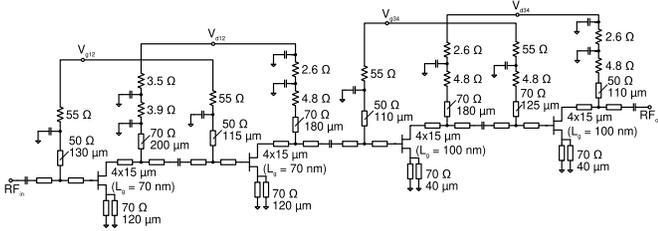


Fig. 7. Simplified schematic of the presented four-stage LNA MMIC.

B. MMIC Design

The LNA MMIC in this work is based on a four-stage topology with common-source HEMTs in all stages. The circuit is designed in a CPWG environment. The design targets best achievable noise performance. The large-signal performance of the LNA is simulated with a preliminary large-signal model and is demonstrated together with the measured results in Section IV-B. Fig. 7 illustrates a simplified schematic including values of the most relevant matching components. Even though, the LNA design comprises no specific tradeoffs to enhance the large-signal performance, e.g., by matching the output of the LNA for a maximum P_{out} , the amplifier makes use of the technology feature to have transistors with a gate length of 70 and 100 nm on the same MMIC. The first two (most noise-relevant) stages utilize 70-nm gate-length HEMTs, whereas the latter two stages contain 100-nm gate-length HEMTs. Since the 70-nm gate-length HEMTs provide a higher f_T for the same bias condition, the first two stages utilize HEMTs with the shorter gate length. The 100-nm gate-length HEMTs provide, in general, slightly higher breakdown voltages, which makes them more favorable for the latter two stages. Furthermore, the first and latter two stages are designed with different initial bias conditions. The first two stages are biased for optimum noise performance. Based on the investigations of Sections II and III-A, the corresponding bias is $V_{d12} = 5 \text{ V}$ and $I_{d12} = 200 \text{ mA/mm}$. The latter two stages are designed with a drain voltage of $V_{d34} = 7.5 \text{ V}$.

The gate width is chosen so that a good input noise and power matching of the first stage is achievable with as few required components in the input matching network as possible. Thus, a four-finger HEMT with a total gate width of $60 \mu\text{m}$ is used. In combination with an inductive source degeneration (two $120\text{-}\mu\text{m}$ -long transmission lines in parallel),

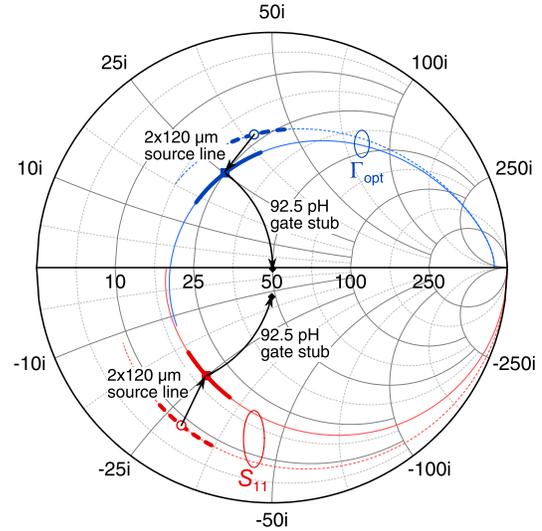


Fig. 8. Simulated S_{11} and Γ_{opt} of a 70-nm gate-length GaN HEMT with a gate width of $4 \times 15 \mu\text{m}$ for a frequency range from 0.1 to 150 GHz. The HEMT is biased with 5 V and 200 mA/mm. The dashed lines depict the curves for a HEMT in common-source configuration. For the solid lines, the HEMT includes symmetric source lines with two $120\text{-}\mu\text{m}$ -long transmission lines in parallel. The intended frequency range (71–100 GHz) is highlighted by bold lines. The black arrows illustrate, as an example, an optimum noise matching for an operating frequency of 85 GHz.

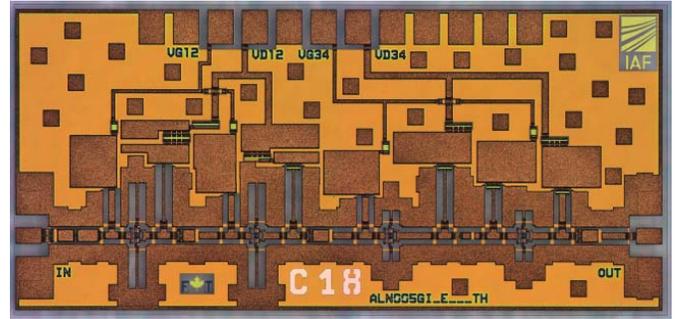


Fig. 9. Chip photograph of the fabricated LNA MMIC with a total size of $2 \times 1 \text{ mm}^2$.

the input matching can be realized with an RF-shorted gate stub. Based on simulated data, Fig. 8 exemplifies this matching procedure. The dashed lines show the input reflection coefficient (S_{11}) and the source reflection coefficient for optimum noise matching (Γ_{opt}) of a $4 \times 15 \mu\text{m}$ HEMT in common-source configuration for frequencies from 0.1 to 150 GHz. The solid lines indicate S_{11} and Γ_{opt} of the same transistor with two source lines (length $120 \mu\text{m}$) connected in parallel. By this, S_{11} and Γ_{opt} of a mid-band frequency, e.g., 85 GHz, are approximately on the circle for a constant conductance of $1/50 \text{ S}$. With an inductive gate stub, S_{11} and Γ_{opt} can be then turned close to the $50\text{-}\Omega$ point. For a wideband input matching and frequency response, the gate stubs are connected as close as possible to the gate of the HEMTs.

The HEMTs in all stages use the same gate width of $4 \times 15 \mu\text{m}$ including an inductive source degeneration in all stages. In the latter stages, the inductive source degeneration is used for an improved wideband frequency response. The interstage matching networks match the output of each stage directly to the input of the subsequent stage. Except for the first

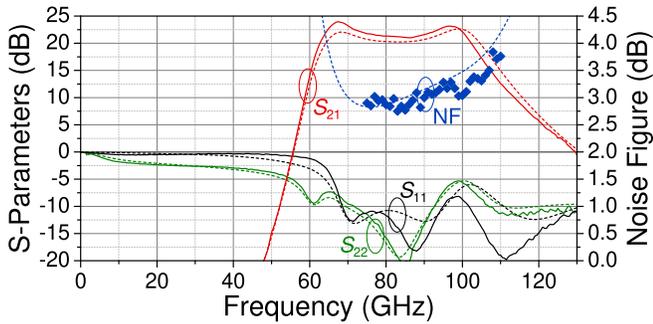


Fig. 10. Measured (solid lines) and simulated (dashed lines) S-parameters of the presented LNA MMIC. The measured NF is shown by blue symbols. The LNA is bias for optimum noise performance ($V_{d12} = 5$ V; $V_{d34} = 7.5$ V; $I_d = 200$ mA/mm).

stage, all stages use a $4.8\text{-}\Omega$ resistor in the drain path before the first shunt capacitor to ensure stability even in case of process variations. For noise reasons, this is avoided in the first stage. Nevertheless, based on Rollet's stability factor, the LNA exhibits unconditional stability. The gate and drain voltages of the first and second stage and the third and fourth stage, respectively, are connected together on the MMIC. Before combining the gate voltages, $55\text{-}\Omega$ resistors are connected in series. A chip photograph of the fabricated LNA MMIC is shown in Fig. 9.

IV. MEASUREMENT RESULTS

The LNA is characterized on wafer with different setups. Unless not otherwise stated, the MMIC is biased for noise-optimized conditions ($V_{d12} = 5$ V; $V_{d34} = 7.5$ V; $I_d = 200$ mA/mm). The mentioned drain-source voltages refer to the HEMT stage. For calculating $P_{dc,q}$, the total supply voltage including the small voltage drop of the series resistors in the drain path is considered. Consequently, $P_{dc,q}$ of the MMIC is 307 mW. For large-signal measurements, the dc-pad voltage is fixed. For all setups, the data are calibrated to the RF probe tips. The S-parameter and NF measurements are reported in Section IV-A. The large-signal results in Section IV-B include single-tone and intermodulation measurements. A large set of measured data including the investigation of the bias dependence of various parameters will give an insight of the tradeoffs between different small- and large-signal characteristics.

A. Small-Signal Measurements

The S-parameters are measured with an Anritsu VectorStar VNA setup. The RF probe-tip calibration is done with an LRRM algorithm and a FormFactor impedance standard substrate. The measured S-parameters are shown in Fig. 10 for noise-optimized bias conditions. The measured 3-dB gain bandwidth (BW) is from 63 to 101 GHz and exhibits more than 21 dB of S_{21} . A maximum S_{21} of 24 dB is achieved at 67 GHz. The measured group delay for the 3-dB gain BW is within 36–81 ps (see Fig. 11). Rollet's stability factor is given in Fig. 12. The K -factor is above 3 for the entire frequency range. The simulated data show very good agreement with the experiment. The measured S_{21} is by about 1.5 dB higher than

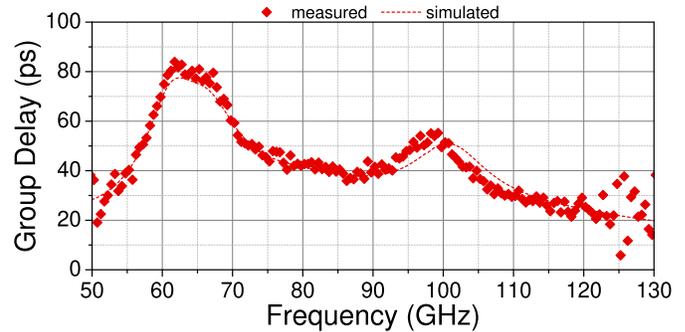


Fig. 11. Measured (symbols) and simulated (dashed lines) group delay of the presented LNA MMIC. The LNA is bias with $V_{d12} = 5$ V, $V_{d34} = 7.5$ V, and $I_d = 200$ mA/mm.

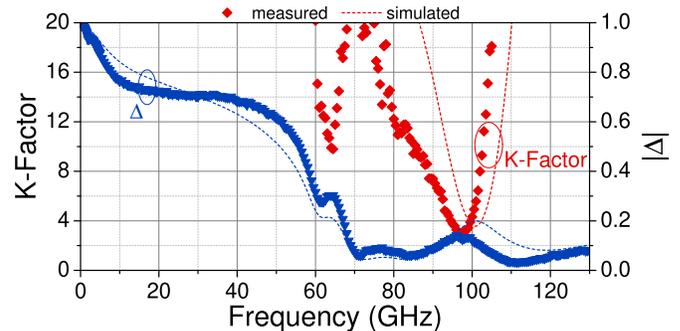


Fig. 12. Measured (symbols) and simulated (dashed lines) Rollet's stability factor (K -factor and $|\Delta|$) of the presented LNA MMIC. The LNA is bias with $V_{d12} = 5$ V, $V_{d34} = 7.5$ V, and $I_d = 200$ mA/mm.

simulated, which is most likely due to slight improvements of the dedicated wafer run. However, this is still below a 0.5-dB deviation per stage.

The NF is characterized by an ELVA-1 WR-10 waveguide noise diode and a Keysight NF analyzer. After the DUT, the signal is down-converted to an intermediate frequency of 99 MHz with a commercially-available waveguide mixer module and a Keysight signal generator including a frequency extension module. The down-converter limits the lower band edge of the setup to 75 GHz. A simplified block diagram of the noise measurement setup is illustrated in Fig. 13. The noise measurements are corrected for the contribution of the down-converter by a previous on-wafer calibration step. The measured NF is as well illustrated in Fig. 10 and exhibits an average value of 3 dB (75–101 GHz). With 2.8 dB, a minimal NF is achieved in the frequency range from 83 to 85 GHz. Even above the 3-dB gain BW, for frequencies of up to 110 GHz, the NF stays below 3.8 dB. Changing V_{d34} between a voltage of 5 and 10 V has no observable impact on the NF.

In order to further investigate the bias dependence of the small-signal performance, the bias of the first two (most noise-relevant) stages is varied over a wide supply range. Corresponding contour plots of the measured average S_{21} and NF are shown in Figs. 14 and 15, respectively. The measured data are in line with the observations, especially, of g_m and f_T in Fig. 2(b) and 5(a), respectively. Below an I_d of 100 mA/mm, S_{21} drops. Above 100 mA/mm, only minor changes can be

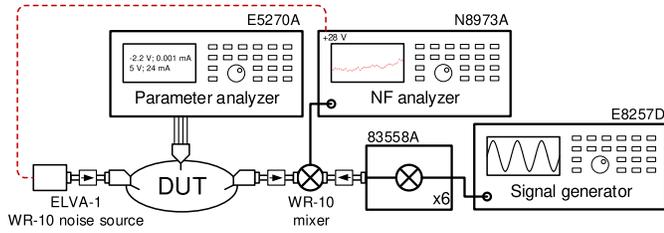


Fig. 13. Simplified block diagram of the on-wafer noise measurement setup.

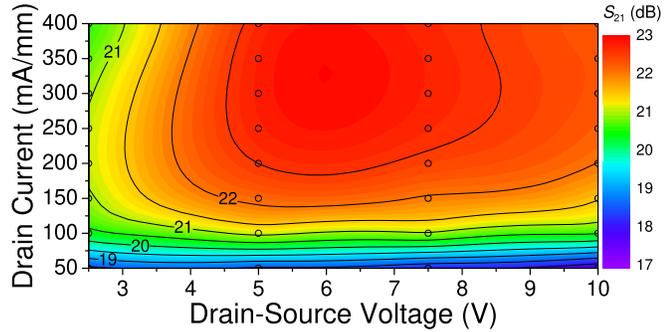


Fig. 14. Contour plot of the measured S_{21} versus V_{d12} and I_{d12} of the presented LNA MMIC. The circles denote the bias points where S_{21} is measured and averaged over the 3-dB BW (63–101 GHz). The bias of the later two stages is kept constant at $V_{d34} = 7.5$ V and $I_{d34} = 200$ mA/mm.

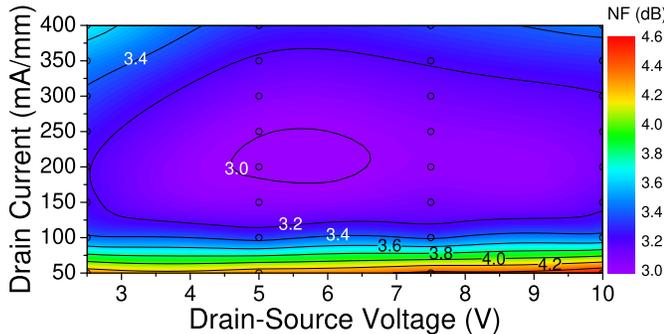


Fig. 15. Contour plot of the measured NF versus V_{d12} and I_{d12} of the presented LNA MMIC. The circles denote the bias points where the NF is measured and averaged from 75 to 101 GHz. The bias of the later two stages is kept constant at $V_{d34} = 7.5$ V and $I_{d34} = 200$ mA/mm.

observed. The voltage dependence is, in general, considerably small. For a V_{d12} of more than 3–3.5 V, S_{21} remains within a variation of approximately 1 dB. Consequently, the NF variation exhibits a small bias sensitivity with an average value of still better than 3.2 dB over a wide bias range.

Fig. 16 shows the average NFs of a wafer mapping of two wafers including 33 cells of the 37 available cells on each wafer. The measurements exhibit an excellent homogeneity with an NF variation of only 0.2–0.3 dB for more than 86% of the cells available on a wafer.

B. Large-Signal Measurements

The single-tone continuous-wave (CW) power measurements are done with a Keysight signal generator including a frequency extension module (83558A), which can provide signals in a frequency range from 75 to 110 GHz.

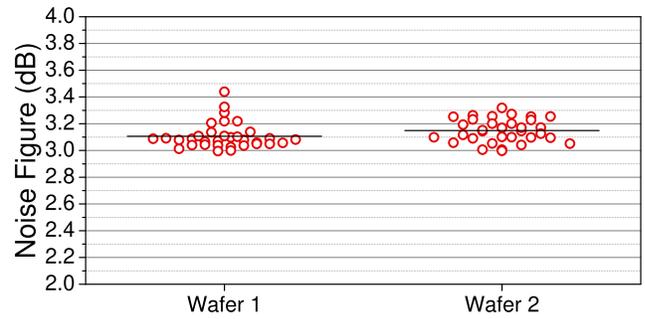


Fig. 16. Mapping of two wafers of the measured NF including 33 cells of 37 cells on each wafer. Each data point represents the average NF of an LNA MMIC (averaged from 75 to 101 GHz). All amplifiers are biased for standard noise-optimized conditions ($V_{d12} = 5$ V; $V_{d34} = 7.5$ V; $I_d = 200$ mA/mm).

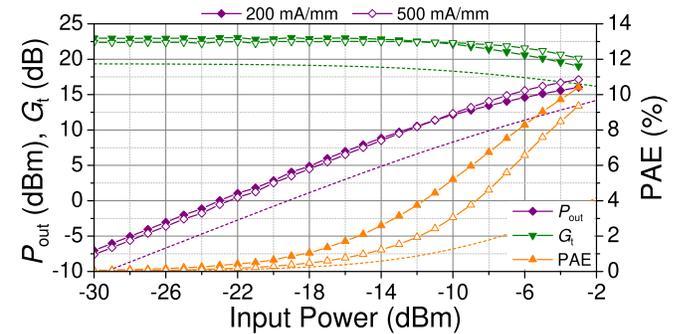


Fig. 17. Measured P_{out} , G_t , and PAE versus P_{in} at an operating frequency of 100 GHz for (closed symbols) the standard noise-optimized bias and (open symbols) an increased quiescent I_d for the latter two stages of 500 mA/mm. OP_{1dB} is 12.1 and 16.2 dBm, respectively, indicating that the large-signal output matching is improved for an increased I_d in the output stage. The bias dependence of OP_{1dB} is further investigated by varying the bias of the latter two (most power-relevant) stages (V_{d34} and I_{d34}) in a range from 2.5 to 10 V and 50 to 600 mA/mm, respectively. The corresponding contour plot is depicted in Fig. 18. OP_{1dB} exhibits maximum values of more than 16 dBm for an I_{d34} of approximately 500 mA/mm and a V_{d34} in the range of 7.5–10 V. As it can be also observed for the dependence of small-signal characteristics on I_{d12} , OP_{1dB} drops in a similar way for an I_{d34} of below 100–150 mA/mm. In a noise-optimized drain-current region (approx. <250 mA/mm), almost no voltage dependence of OP_{1dB} can be observed.

The input power (P_{in}) is controlled by a motorized WR-10 waveguide attenuator. P_{out} is measured by a Keysight power meter (N1913A) and a WR-10 waveguide sensor (W8486A).

Fig. 17 shows a P_{in} sweep at an operating frequency of 100 GHz for (closed symbols) the standard noise-optimized bias and (open symbols) an increased quiescent I_d for the latter two stages of 500 mA/mm. OP_{1dB} is 12.1 and 16.2 dBm, respectively, indicating that the large-signal output matching is improved for an increased I_d in the output stage. The bias dependence of OP_{1dB} is further investigated by varying the bias of the latter two (most power-relevant) stages (V_{d34} and I_{d34}) in a range from 2.5 to 10 V and 50 to 600 mA/mm, respectively. The corresponding contour plot is depicted in Fig. 18. OP_{1dB} exhibits maximum values of more than 16 dBm for an I_{d34} of approximately 500 mA/mm and a V_{d34} in the range of 7.5–10 V. As it can be also observed for the dependence of small-signal characteristics on I_{d12} , OP_{1dB} drops in a similar way for an I_{d34} of below 100–150 mA/mm. In a noise-optimized drain-current region (approx. <250 mA/mm), almost no voltage dependence of OP_{1dB} can be observed.

The IMD of the LNA MMIC is characterized with a setup that is illustrated in Fig. 19. It is based on two Keysight signal generators with two connected frequency extension modules. The two signals are combined with a 10-dB WR-10 directional waveguide coupler. The through path is attenuated by an

TABLE I
OVERVIEW OF STATE-OF-THE-ART E/W-BAND LNA MMICS

Reference	Technology	BW (GHz)	S_{21} (dB)	$P_{dc,q}$ (mW)	FOM ₁ (GHz)	FOM ₂ (GHz)	IP ₁ dB (dBm)	IIP3 (dBm)	NF (dB)
Other Technologies									
[8]	35-nm InGaAs mHEMT	75–110	24–28	40.8	n/a	n/a	n/a	n/a	1.6–2.2 (av 1.9)
[9]	50-nm InGaAs mHEMT	75–108	27–32	30.3	n/a	n/a	n/a	n/a	1.6–2.6 (av 1.9)
[13]	100-nm InP HEMT	80–100	30	33	n/a	n/a	n/a	n/a	1.6–2.6 (av 1.9)
[14]	20-nm InGaAs MOSHEMT	75–100	15–20	69.7	n/a	n/a	n/a	n/a	2.3–3.2 (av 2.8)
[15]	100-nm pHEMT	71–86	20–22.4	262.5	0.38	n/a	–10	n/a	2.7–4.3
[16] [*]	35-nm InGaAs mHEMT	75–110	12.9–13.6	346	0.57	n/a	–4–2	n/a	3.5–5 (av 3.6)
[7]	100-nm pHEMT	90–100	12–13	30	n/a	n/a	n/a	n/a	av 3.8
[17]	100-nm pHEMT	68–86	21.5–23.5	360	0.4	2.8	–7; –6.3 [‡]	0.3; 1.4 [‡]	3.7–4.3
[6]	22-nm FinFET	67–79	17–20	10.8	0.24	n/a	–22.8 [†]	n/a	3.7–4.5
[18]	0.13- μ m SiGe BiCMOS	72.5–84	18.3–21.3	52	0.26	n/a	–14.5 [§]	n/a	4.5–5.5
[19]	0.12- μ m SiGe BiCMOS	84–100	10–13	8.1	n/a	5.8	n/a	–5.4 [♣]	3.3–6.7 (av 5.5)
[20]	SiGe BiCMOS	75–105	13.5–16.4	5.1	n/a	n/a	n/a	n/a	4.1–6
[21]	32-nm CMOS SOI	76–108	4.2–7.2	5.2	1.22	n/a	–12 ^Υ	n/a	4.3–6.7 [◊]
[22]	28-nm FDSOI	53–117	12–17.7	38.2	0.34	n/a	–13.3–10.3 [#]	n/a	5–6 [#]
[23]	65-nm CMOS	84.9–107	19.1–22.1	42	0.48	n/a	–14.8–13.2	n/a	4.9–7.4
[24]	22-nm FDSOI	77–108	15.2–18.2	16	0.09	n/a	–22.8 [‡]	n/a	5.8–6.6
[25]	28-nm CMOS	68.1–96.4	26.6–29.6	31.3	0.07	n/a	–28.1–23	n/a	6.4–8.2
[26]	0.18- μ m SiGe BiCMOS	70–97	16–19	8.1	0.003	n/a	–35 [◊]	n/a	8.6–11.8
GaN Technologies									
[4]	90-nm GaN-on-SiC HEMT	75–83 91–96	15.5–16.1 18–19.1	200	n/a	n/a	n/a	n/a	3.5–4.2 3.3–3.8
[5]	100-nm GaN-on-SiC HEMT	86–98	>20	128	n/a	n/a	n/a	n/a	2.9–5
[27]	120-nm GaN-on-SiC HEMT	80	20.4	n/a	n/a	n/a	n/a	n/a	3.8
[28]	100-nm GaN-on-Si HEMT	78.5–89	14.5–17	190	0.33	n/a	–11–7	n/a	4.5–5.2
[29]	100-nm GaN-on-SiC HEMT	84	25	800	0.15	n/a	–6.7	n/a	5.6
[30]	100-nm GaN-on-SiC HEMT	106.5–113.5	28.4–31.4	2400	0.01	n/a	–23–13 [∇]	n/a	≈7.6 [∇]
This work	70-nm GaN-on-SiC HEMT	63–101	21–24	307	0.41	0.74	–16–10 [*]	–8.1–7.4 [*]	2.8–3.3 (av 3) [*]

^{*} Distributed amplifier topology (circuit operates from 1 to 330 GHz). | [†] 73.5 GHz. | [‡] 71 and 86 GHz. | [§] 77 GHz. | [♣] 91 GHz. | ^Υ 95 GHz. | [◊] 91–97 GHz. | [#] 75–105 GHz. | [‡] 92 GHz. | [◊] 80 GHz. | [∇] Different dc bias. | ^{*} Measurement setup limits data to >75 GHz.

$$\text{FOM}_1 = S_{21} [1] \cdot \text{IP}_1 \text{ dB} [\text{mW}] \cdot f [\text{GHz}] / ((\text{NF} [1] - 1) \cdot P_{dc,q} [\text{mW}]). \quad \text{FOM}_2 = S_{21} [1] \cdot \text{IIP3} [\text{mW}] \cdot f [\text{GHz}] / ((\text{NF} [1] - 1) \cdot P_{dc,q} [\text{mW}]).$$

additional 10-dB WR-10 waveguide attenuator before the coupler so that both signals provide approximately the same power at the output of the directional coupler. Fine-tuning of the power levels is done by a user flatness in the signal generator. After the coupler, a motorized WR-10 waveguide attenuator follows, which is used to control the power level during the IMD measurements simultaneously for both input signals. The motorized attenuator is connected to the RF input probe tip. The power levels of the signal generators are calibrated to the input probe tip so that for each attenuator setting both test frequencies provide at each frequency the same power. At the output of the setup, a Keysight spectrum analyzer with an external WR-10 waveguide mixer measures the output signals of the DUT. The two fundamental tones are separated by 10 MHz around the center frequency.

Fig. 20(a) shows the measured P_{out} of the fundamental signals and the third-order products versus P_{in} at a center frequency of 100 GHz (offset frequency: 10 MHz). The dashed lines are fitting curves with a constant slope for the fundamental signal and the third-order product of 10 and 30 dB, respectively. The extrapolation of the fit curves exhibit an output-referred third-order intercept point (OIP3) of 14.4 dBm. Fig. 20(b) shows measured and simulated results for frequencies from 75 to 105 GHz. The OIP3 is in the range of 13–14.4 dBm (from 75 to 100 GHz). The input-referred third-order intercept point (IIP3) is in the range of –8.1 to –7.4 dBm. Fig. 20(b) shows as well OP_{1dB}, the input power at the 1-dB compression point (IP_{1dB}), and P_{out} at the 4-dB compression point (OP_{4dB}) that are in the ranges from 4.5 to 12.1, –16 to –10, and 9.1 to 16 dBm, respectively.

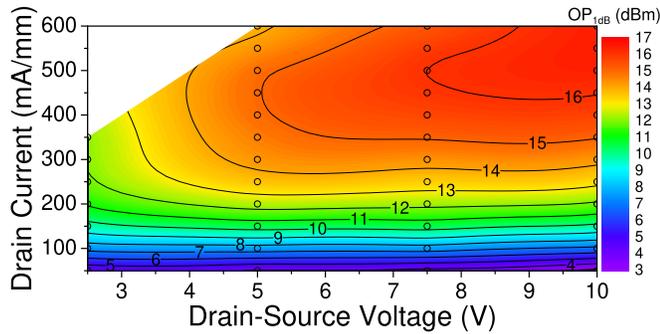


Fig. 18. Contour plot of the measured OP_{1dB} at 100 GHz as a function of the bias of the later two stages. The bias of the first two stages is kept constant at $V_{d12} = 5$ V and $I_{d12} = 200$ mA/mm.

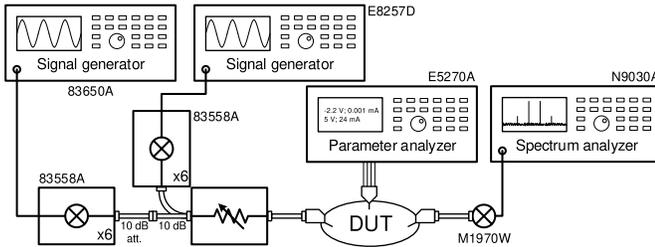


Fig. 19. Simplified block diagram of the on-wafer IMD measurement setup.

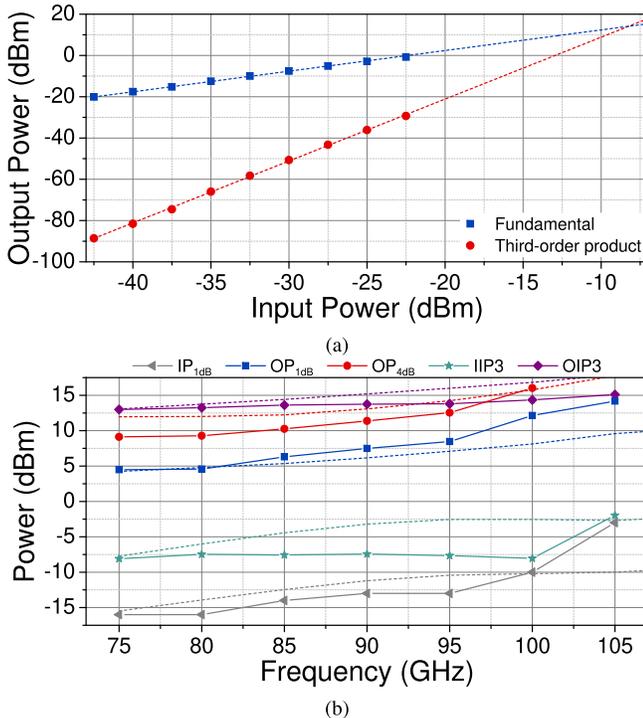


Fig. 20. (a) Measured P_{out} of the fundamental and the third-order product versus P_{in} at a center frequency of 100 GHz. The dashed lines are fit curves with slopes of 10 and 30 dB for the fundamental frequency and the third-order product, respectively. (b) Measured and simulated IP_{1dB} , OP_{1dB} , OP_{4dB} , $IIP3$, and $OIP3$ versus operating frequency. The LNA is biased with standard noise-optimized bias ($V_{d12} = 5$ V; $V_{d34} = 7.5$ V; $I_d = 200$ mA/mm). Dashed lines indicated the simulated data.

The bias dependence of the IMD characteristic is summarized in Fig. 21. In a similar way as for the dc characteristic, $OIP3$ improves for increasing drain currents below

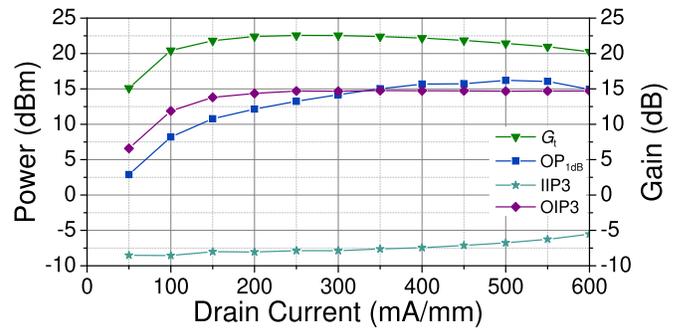


Fig. 21. Measured $IIP3$, $OIP3$, OP_{1dB} , and the $IP3$ corresponding G_t versus drain current at a center frequency of 100 GHz. The LNA is biased with standard supply voltages ($V_{d12} = 5$ V; $V_{d34} = 7.5$ V).

200 mA/mm and remains then almost constant with a value of 14.7 dBm. For currents of up to 300 mA/mm, G_t increase in a similar way as $OIP3$ so that $IIP3$ is without major variations at approximately -8 dBm. For larger currents, G_t decreases and $IIP3$ increases in a symmetric manner. The shown OP_{1dB} curve is based on the same data that are used for Fig. 18 and represent a cut through the contour at a V_{d34} of 7.5 V. As discussed before, due to an improved large-signal output matching for an I_{d34} of 500 mA/mm, OP_{1dB} increases for currents of up to 500 mA/mm.

V. DISCUSSION AND CONCLUSION

As a conclusion of the measured dc, small-signal, and large-signal performance, one can summarize that g_m -related parameters, such as S_{21} , NF, and $OIP3$, follow the behavior which is already given by the g_m curve itself. Thus, the optimum V_{d12} and I_{d12} is 5 V and 200 mA/mm, respectively. On the one hand, this provides the best noise performance and, on the other hand, S_{21} and $IP3$ are almost at its optimum so that no major improvement, e.g., by increase V_{d12} or I_{d12} is achieved. Since the output large-signal matching, of course, considerably relies on the supply voltage and quiescent current of the output stage, parameters, such as OP_{1dB} , depend on the bias of the output stage. However, due to high gain in the first two stages, the bias of the output stages can be adjusted for optimum output performance, e.g., OP_{1dB} , without affecting other performance parameters such as NF or $IP3$. The comparison of P_{1dB} and $IP3$ highlights the importance of IMD measurements of LNAs for, e.g., wideband receiver applications. Depending on the design of the output matching of an LNA, small- or large-signal, P_{1dB} can be improved with only minor impact on $IP3$. It is the authors' belief that the importance of linearity consideration, such as IMD, applies especially to GaN LNAs since linearity is a major promise of GaN technologies.

In summary, this article demonstrates a 63–101-GHz GaN LNA MMIC with a measured minimum NF of 2.8 dB and an average value of 3 dB (75–101 GHz). In addition, the measured $IP3$ and P_{1dB} demonstrate promising linearity data. As shown in Table I, the demonstrated noise performance narrows the gap to dedicated low-noise InGaAs HEMT technologies considerably to now less than a factor of two in noise

temperature (T_e) difference; [8], [9] average T_e : 159 K versus this work average T_e : 289 K. Furthermore, the achieved NF outperforms pHEMT, silicon-based, and other GaN HEMT technologies. By that, the presented LNA demonstrates an appealing performance for a multitude of applications in the area of highly-linear low-noise receiver systems.

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Fabian Thome received the Dipl.-Ing. degree in electrical engineering and information technologies from the Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2011, and the Ph.D. degree in the field of semiconductor devices and wireless communication from the University of Freiburg, Freiburg im Breisgau, Germany, in 2020.

In 2010, he joined the Fraunhofer Institute for Applied Solid State Physics (Fraunhofer IAF), Freiburg im Breisgau, where he has been a Research Scientist and a Project Manager since 2012. His current research interests include the development of InGaAs and gallium-nitride (GaN) high-electron-mobility transistor (HEMT) technologies as well as the design and characterization of linear and nonlinear semiconductor devices and monolithic microwave integrated circuits from the microwave to submillimeter-wave frequency range for applications in radio astronomy, wireless communications, quantum computing, and measurement equipment.



Peter Brückner received the Dipl.-Ing. degree in electrical engineering and the Ph.D. degree in the field of gallium-nitride (GaN)-epitaxy and free-standing GaN-substrates from Ulm University, Ulm, Germany, in 2004 and 2008, respectively.

Afterward, he joined the Institute of Optoelectronics, Ulm University, as a Member of Scientific Staff. From 2008 to 2010, he was a Development Engineer with United Monolithic Semiconductors, Ulm, for GaN high-electron-mobility transistor (HEMT) technologies. He joined the Fraunhofer Institute for

Applied Solid State Physics, Freiburg im Breisgau, Germany, in 2011, as the Responsible Group-Manager for plasma etching, where he also is in charge of the development for short gate-length GaN-on-silicon-carbide (SiC) technologies.



Stefano Leone was born in Catania, Italy, in 1978. He received the B.Sc. and M.Sc. degrees in industrial chemistry from the University of Catania, Catania, in 2000 and 2002, respectively, and the Ph.D. degree in semiconductor materials from the University of Linköping, Linköping, Sweden, in 2010.

He has 17 years of experience in the epitaxial growth of wide bandgap semiconductors by having worked in different industries in Italy, USA, and Germany. Since 2017, he has been leading the Group of the Epitaxial Growth of Nitride Semiconductors,

Fraunhofer Institute for Applied Solid State Physics (Fraunhofer IAF), Freiburg im Breisgau, Germany.



Rüdiger Quay (Senior Member, IEEE) received the Diploma degree in physics from Rheinisch-Westfälische Technische Hochschule (RWTH), Aachen, Germany, in 1997, and the Ph.D. degree (Hons.) in technical sciences, the second Diploma degree in economics, and the Venia Legendi (Habilitation) degree in microelectronics from the Technische Universität Wien, Vienna, Austria, in 2001, 2003, and 2009, respectively.

In 2001, he joined the Fraunhofer Institute of Applied Solid-State Physics (Fraunhofer IAF), Freiburg im Breisgau, Germany, in various positions. He is currently the Deputy Director of Fraunhofer IAF, where he is responsible for the business fields. Since 2020, he has been a Fritz-Hüttinger Professor with the Institute for sustainable systems, Albert-Ludwig University, Freiburg im Breisgau. He has authored or coauthored more than 300 refereed publications, three monographs, and contributions to two further.