61.5% Efficiency and 3.6 kW/m^2 Power Handling Rectenna Circuit Demonstration for Radiative Millimeter Wave Wireless Power Transmission

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***Abstract*— A new GaN Nano-Schottky diode rectifier is introduced with capacitance per unit gate width of 381 fF/mm, and series resistance is 0.45 Ω·mm leading to transition frequency (f_T) of 928 GHz. The associated forward current is 1.8 A/mm with breakdown voltage of 30 V. The new device was modeled and an on-wafer voltage doubler rectenna circuit was designed and fabricated on GaN/SiC wafers. A *W*-band small and large signal characterization was performed to highlight the integrated rectenna performance. An RF-dc efficiency of 61.5% was measured at 95 GHz with associated input power density of 3.61 kW/m^2. The latter represents a 15.7% increase in efficiency over the state-of-the-art *W*-band rectenna circuit. The input power handling has also increased by a factor of 1.5 and 9.5 from reported GaAs and CMOS-based rectenna circuits at 94 GHz. The result highlights key improvements in the rectenna metrics for wireless power beaming demonstrations of the future.**

***Index Terms*— Active denial system (ADS), diodes, directed energy systems, GaN transistors, high power rectifier, microwave monolithic integrated circuits (MMICs), millimeter wave (mm-Wave) systems, radiative wireless power, rectifiers, sub-mm-Wave circuits, *W*-band, wireless power beaming, wireless power transmission.**

I. Introduction

WIRELESS power transmission at far-field can provide key capability for power-starved systems such as Internet of Things (IoT), unattended sensors, and autonomous systems that could include unmanned aerial and ground vehicles (UAVs and UGVs). Key to the realization of such capabilities is the compactness of the power-absorbing receiver together with its associated high-power density to provide adequate energy per unit volume. In order to realize such capability, all aspects of the wireless power system would need to be optimized including the modality of its operation such as RF, millimeter wave (mm-Wave), and optical regimes for the specific application of use. mm-Wave wireless power provides a focused energy beam which can be directed to far-field, reducing the path-loss substantially compared with RF and microwave modalities. In addition, the availability of transmitter technologies that are capable of 100 kW of radiated mobile power allows for the substantial converted power at the receiver. Intermediate force protection (IFP) system such as Silent Guardian [1] as shown in Fig. 1 provide dual-use capability for mm-Wave wireless power transfer to low size, weight, and power (SWAP) assets while under protection duties. These types of transmitters are mobile and can be deployed as needed to project wireless power at ranges exceeding a kilometer. Larger output power mm-Wave transmitters can also be built to enable stationary power transfers to remote locations as desired.

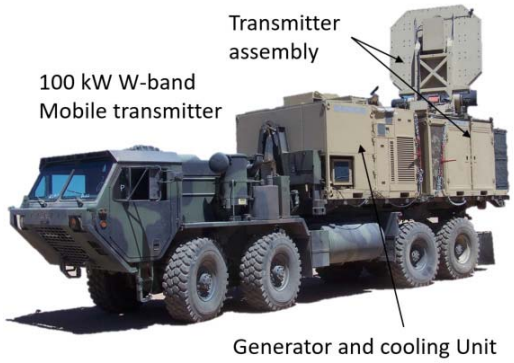

Fig. 1. 100 kW-directed energy mm-Wave transmitter is shown designed for nonlethal operations. It provides a high-power mobile source for mm-Wave wireless power transmission.

The mm-Wave output power density at range can vary from 1 to 40 W/cm^2 which will require the rectenna receiver to operate at high-power regime in order to take advantage of such exceptional power densities. The higher the power capability of the rectenna receiver, the more compact and higher will be the received power to weight-volume ratio (W/kg·m^3). The focus of this article is to highlight the development of the high-power mm-Wave rectifier and rectenna circuit technology relating to the applications discussed. The article will focus on the high-power rectenna receiver technology with Section II describing the receiver architecture and its quality factors followed by description of a new high-power rectifier technology called GaN nano-Schottky diodes (NSDs) [2] and include the design, fabrication, and characterization of an integrated monolithic rectenna circuit in Sections III–VI.

II. Rectenna Receiver Architecture and Metrics

Fig. 2 represents the block diagram of the rectenna receiver comprising of its major components each of which require high-quality factor in order to ensure high performance of the receiver. Assuming the rectenna receiver is placed in the

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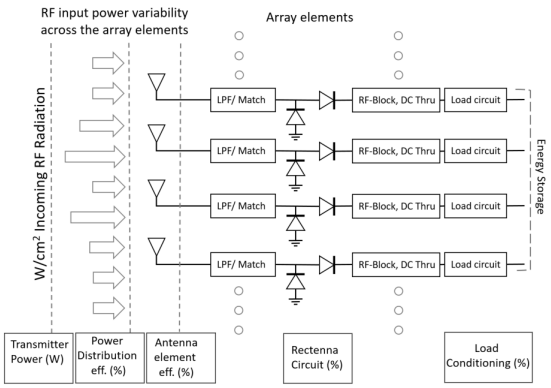

Fig. 2. Block diagram representation of the wireless power transmission receiver system highlighting all the key components of the system that will influence the overall efficiency of the receiver.

far-field of the antenna a plane wave with a certain power density will radiate the array. In the mm-Wave case, the power density is in multiple W/cm^2 pending distance from the transmitter. The first-quality factor would be how uniformly the rectenna receiver array elements are fed, which will be related to how well the receiver is aligned to the transmitter. This will result in power density variation across the elements of the array, which at high power could be a major factor is overall conversion efficiency. The latter is called power-distribution efficiency, which for static transmitter and receiver could be optimized to be very high. However, for dynamic transmitter–receiver array setup, the efficiency will change temporally and will depend on how quickly the pointing and tracking are performed. At mm-Wave, the wavelength on wafer is small, which will allow for a viable integrated rectenna circuit fabrication approach. However, integrated antennas are generally not as efficient as substrate-less antennas, and for this reason the antenna efficiency is separated from the rectenna circuit as a separate quality factor in the block diagram shown in Fig. 1. Typical efficiencies at mm-Wave could be as high as 85% using waveguides, air-filled micromachined geometries, or lower loss substrates such as quartz or liquid crystal polymers (LCPs) circuits [3]–[5]. The rectenna circuit includes the input low-pass-filter (LPF) and matching network, the rectifier diode topology which could be single or multiple diodes in close vicinity and RF short-circuit and the output matching network with a dc feed-thru. The thin-film capacitors generally required for the circuit operation need to be integrated closely to the rest of the components. At mm-Wave, this is in the range of 100 μm for highest efficiency performance. These tolerances would be hard to achieve using independent devices and assemble them on a separate substrate much like the microwave assembly. As a result, an all integrated microwave monolithic integrated circuit (MMIC) is usually chosen for mm-Wave frequency range, which is also highlighted by many publications [6], [7]. The rectenna circuit efficiency is generally the most important quality factor in the receiver. It provides RF-dc conversion using signal conditioning by suppressing any harmonics except a dc output. The rectifier technology in-turn would need to be optimized for frequency of operation and power handling. An important note for high-power regime operation is the high conversion efficiency at high input power levels. This is a hard task to accomplish, where the combined achievement of both metrics is architecturally limited and is highlighted in the next few sections. Furthermore, a comparison of the published mm-Wave rectenna circuit efficiency and input power handling compared with the latest results is discussed in Section IV. Another key component of the rectenna receiver is the load presented to the rectenna circuit. Considering the diode rectifier is the two-terminal device, its input and output are not isolated from each other unlike a three terminal transistor and hence the output load effects the input impedance match for the desired operation. As a result, the load presented to the rectenna circuit has an optimal value by which the peak conversion efficiency occurs for every input power level settings to the circuit. If the transmitter and receiver are on mobile platforms the power density across the receiver rectenna array will vary and the optimum load for peak efficiency will need to change accordingly. The load adjustment is at dc and can be controlled using a load conditioning circuit [8]. The output energy from the rectenna receiver can then be used directly or stored in a battery pending the overall system operational need.

The following sections focus on the development of the high-power rectenna circuit based on a new GaN-based nano-Schottky rectifier diode. A high-power rectenna design and characterization and its comparison with the other published W-band rectenna circuits are also highlighted.

III. GaN Nano-Schottky Rectifier

The high-power regime for the wireless power energy transfer requires a high-power handing rectifier diode in order to handle the high incoming radiation at W/cm^2 input power levels. The current device technologies used for the wireless power rectification are GaAs and CMOS-based rectifiers operating at high frequency range [9], [10]. The key to high efficiency RF-dc rectification is the high switching speed of the diode (high cutoff frequency) which entails a low-series resistance and low-associated capacitance. For high-power operation high forward current handling and reverse breakdown, voltage is required. GaAs planar air bridged diodes have been effectively used in the mm-Wave and beyond for many years as frequency multipliers and mixers [11]. They enjoy high cutoff frequency ($>$1 THz) and the breakdown voltage in 4–8 V pending design of the epitaxial layers for the operational frequency. They are tailored for high frequency operation with a planar air-bridged layout architecture to reduce parasitic components to the diode structure. In recent times, the silicon advanced CMOS high-density transistor node processes have been used for various demonstrations of integrated rectenna circuits with embedded rectifiers, highlighting efficiency of 38% at 94 GHz [12], [24]. Although the advanced node silicon CMOS process offers high switching speed, however, the breakdown voltage for the technology is somewhat limited based on the material characteristics and not suited for high-power operation. Rectenna circuits have been designed in a variety of technologies at mm-Wave frequency range. These range from GaAs to Si CMOS and recently GaN through advanced scaling of its parameters to reach the high switching speed requirements [13]. For high-power operation

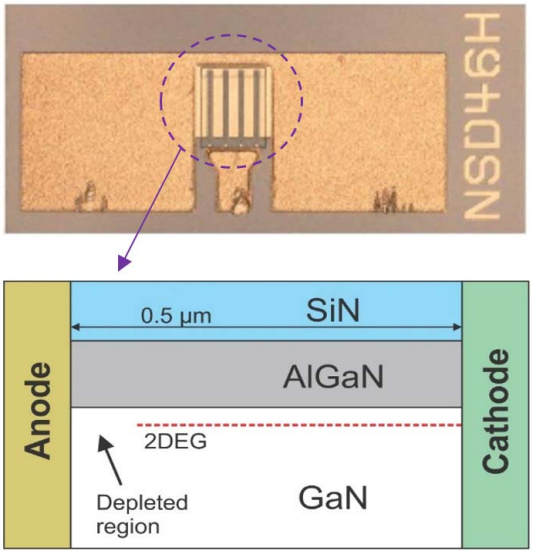

Fig. 3. Technology cross section of the NSD. The anode metal contacts laterally with a 2DEG formed in an AlGaN/GaN HEMT structure. The cathode is made of a regrown n^+GaN on the 2DEG.

regime a high breakdown voltage is required, moving the choice of the technology into the GaN device technology much like transistor-based power amplifier integrated circuits with high output power density. Various GaN Schottky diodes have been developed, highlighting the improvement of the output rectified power, and however, the higher frequency of operation has been limited by the device design and its fabrication process limiting the overall efficiency [14], [15].

Fig. 3 illustrates a technology cross section of the NSD. The epitaxial structure consists of an AlGaN–GaN HEMT structure where a 2-D electron gas (2DEG) is formed near the AlGaN–GaN interface. The sheet electron density and the mobility of the 2DEG are 1.2×10^{13} cm^{-2} and 1600 cm^2/V·s, respectively. The 2DEG is confined in the GaN channel layer within a few nanometers below the interface, enabling a nano-scale Schottky contact between the anode metal and the 2DEG. The small Schottky contact area and a lateral depletion length of the 2DEG determine the junction capacitance (C_j). The cathode ohmic contact is formed by an n^+GaN layer regrown on the 2DEG. The low-contact resistance (=0.1 Ω·mm) and the low-sheet resistance of the 2DEG (=330 Ω/sq.) contribute to a low-series resistance (R_s) of the diode. The distance between the anode and the cathode is 0.5 μm.

IV. Device Characterization and Modeling

The rectifier diodes fabricated have a rectangular T-Gate structure [NSD-rectangular shaped (NSDR)], which is fed from an air-bridged beam connected to the anode contact as shown in Fig. 3. The diode rectifiers were fabricated with total gate width of 10 μm as the default value for all variations 1, 2, 3, and 4 of gate fingers. Each device type was measured at dc using dc device monitors across the wafer. The RF probable devices were also characterized from 1 to 50 GHz following the use of on-wafer calibration standards. Fig. 4 represents the dc I–V of each GaN NSD device type for forward and

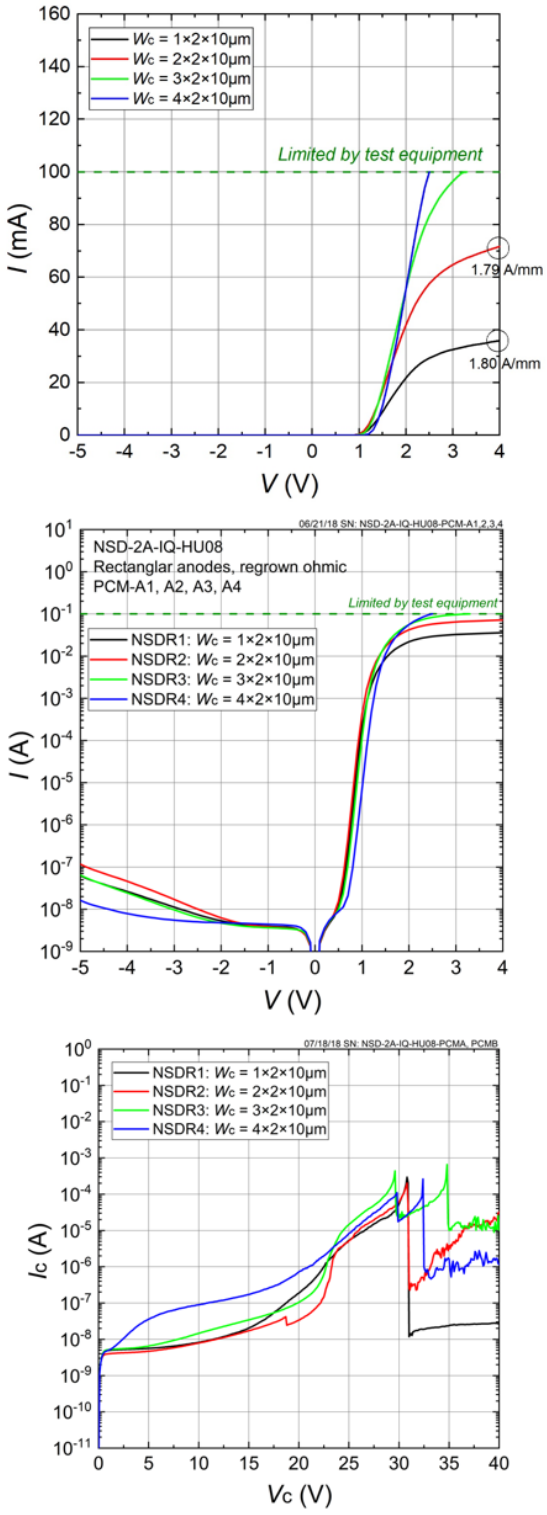

Fig. 4. GaN NSDs measured dc characteristics shown for various device peripheries. The performance of the NSDs is scalable with device sizes highlighting 1.8 A/mm and a breakdown voltage of 30 V. The device is ideally suited for high-power wireless power system demonstrations.

reverse bias characteristics of a fabricated diode. The turn-on voltage defined at 10 mA/mm is 1.0 V, the diode ideality factor (n) is 1.6, and the maximum current density is 1.8 A/mm at a forward bias of 4 V. The forward current handling is a key requirement for high-power rectification operation. The

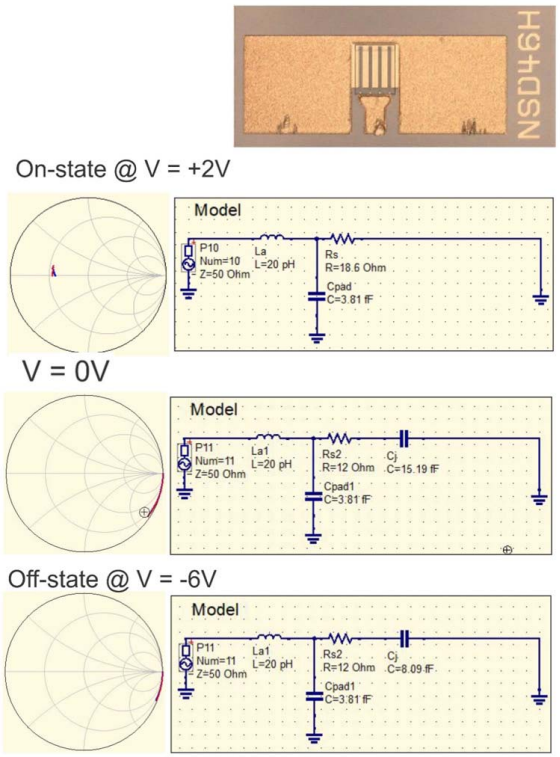

Fig. 5. GaN NSD equivalent circuit model under various bias conditions. The modeled versus measured is shown on the Smith chart representation. The zero bias (0 V) equivalent circuit model components are used to develop a model in active denial system (ADS) for design of the rectenna circuit.

high degree of scalability between various device sizes is also shown resulting from careful device geometry layout and high yield fabrication process. The measured reverse bias characteristics shown in Fig. 4 shows a similar breakdown voltage threshold for the device types of >30 V. This indicates an averaged breakdown field of 133 V/μm which is key contributor to the high-power operation of the rectifier.

The RF characterization of the various diode types following a careful calibration of the on-wafer measurements was used to develop a bias-dependent model for the GaN nano-Schottky rectifier diode. Fig. 5 represents the equivalent circuit model of the diode at $+2$, 0, and -6 V together with model and measured data. The mapping of the measured and modeled data represents the accuracy of the diode deembedding and the scaling of the diode rectifier technology. At zero bias, the diode is represented by the zero bias capacitance of 15.19 fF for the 2 μm $\times$ 2 μm $\times$ 10 μm in series with the series resistance of 12 Ω. At 2 V forward bias the dynamic diode resistance is smaller in impedance than the diode capacitance with the value of 6.6 Ω (18.6–12 Ω). At -6 V the reverse bias capacitance is steadily reduced from the zero bias capacitance value by a factor of 1.9 as expected from a reverse biased diode device. The inductance of 20 pH and a pad capacitance of 3.81 fF is also added to the model and are considered parasitic elements for the one-port coplanar waveguide (CPW) probed structure. The latter will not be included in the diode model when used in the circuit since the diode pads will be integrated with the associated transmission lines of the circuit. Fig. 6 represents the diode capacitance versus reverse bias plot together with

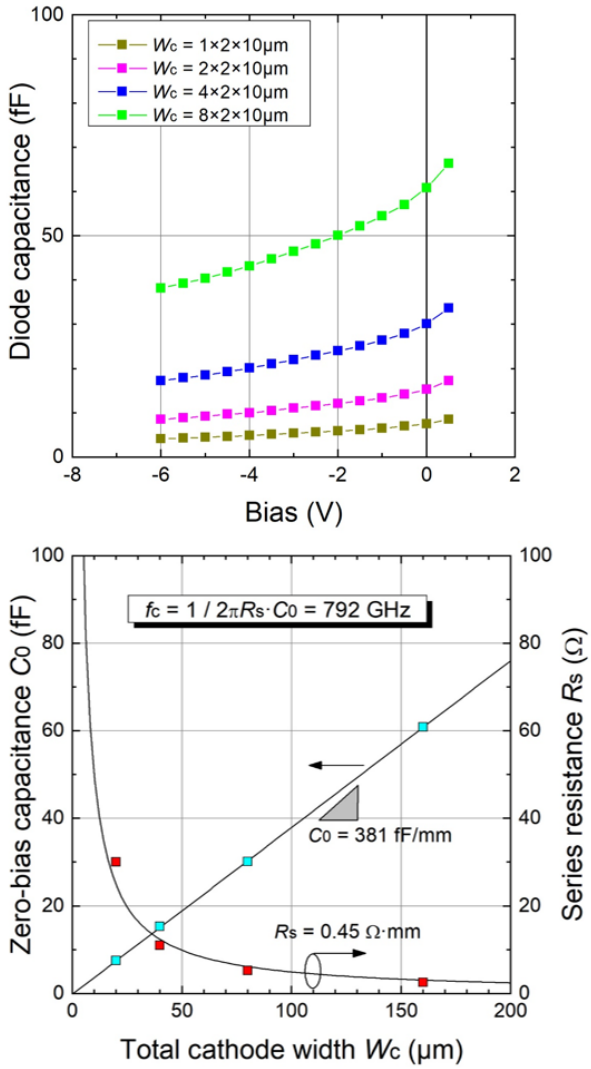

Fig. 6. Diode model elements such as the junction capacitance and series resistance as a function of bias and size are shown. The linear scaling of size versus 381 fF/mm of capacitance and 0.45 Ω·mm of resistance indicate high degree of fabrication uniformity.

a plot of zero bias capacitance and series resistance versus various gate widths. The C_{ON}/C_{OFF} ratio is 1.8 which highlights the low parasitic capacitance of the diode

The bias dependency of the capacitance is seen for all devices and somewhat limited by the parasitic element of the probe pads. The cutoff frequency of the diodes is stated as the inverse product of its zero bias capacitance and series resistance. The rectangular diodes show a cutoff frequency of 928 GHz. The lower plot highlights the scalability of the diode data as the size of the diodes varied and the capacitance per unit gate width fits a linear line while the resistance is exponential, which is expected. The capacitance per unit gate width is 381 fF/mm for the rectifier diode types while the series resistance is 0.45 Ω·mm, respectively.

V. Rectenna Circuit

The GaN NSD rectifier diode was used to design a variety of the rectenna circuits for performance evaluation of the developed technology. The rectenna circuit (circuit#4) shown

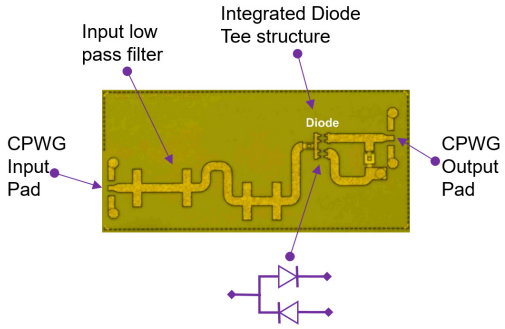

Fig. 7. GaN nano-Schottky rectenna MMIC integrated with a voltage doubler diode topology, input LPF, and dc circuitry measuring 2.1 mm × 0.75 mm. The GaN MMIC is fabricated on GaN/SiC wafers with the MMIC having a final thickness of 50 μm with substrate vias for low-inductance ground on the bottom side of the MMIC.

in Fig. 7 was one fabricated as an integrated circuit directly on the GaN/SiC wafer. The circuit includes an input LPF using a double-stub matching network designed for roll off at 96 GHz which prevents any higher harmonics power generated by the rectifier to be radiated out of the input port. Similarly a large integrated thin-film capacitor is connected through a substrate via as a low-loss RF short circuit allowing only dc to be extracted at output port. The rectifier topology used for circuit 4 is a voltage doubler arrangement using two 2 μm × 2 μm × 10 μm rectifiers as described in the previous section. An integrated thin-film capacitor of value 350 fF was also used for the voltage doubler for charging and discharging operation during forward and reverse operation RF input swing across the rectifier diodes. All components of the circuit were tightly coupled in a single integrated circuit to avoid any interconnect losses and impedance mismatch more acute at *W*-band frequency range compared with RF frequencies. Although an integrated antenna could have been added to complete the rectenna circuit, it was decided to omit the on-wafer antenna since a higher efficiency off-wafer can then be used. Additionally, using a ground-signal-ground (GSG) probe allows for careful characterization of the circuits through on-wafer probing and calibration. The fabrication and characterization processes mirrored mm-Wave integrated circuit methodology to be able to validate the performance through careful analysis through reference plans of the ports. Although, the output-port should have no *W*-band power content and only dc output power should be measured, an output port was created to validate its performance.

Multiple wafers were fabricated through the front-side process and thinned to 50 μm before the circuits were separated into individual die for characterization. The circuits were selected and small signal *S*-parameters were measured following a probe-tip calibration process. The output port of 50 Ω probe was used as the load for the circuit for this characterization process which is sufficient for validation of the input and output match before the large signal rectenna characterization. The *S*-parameter data for three independent circuits were measured and shown in Fig. 8 in blue, green, and red lines in both rectangular plot as well as the Smith-chart representation. The highest return-loss is at design frequency of 93 GHz, representing the highest efficiency by maximizing

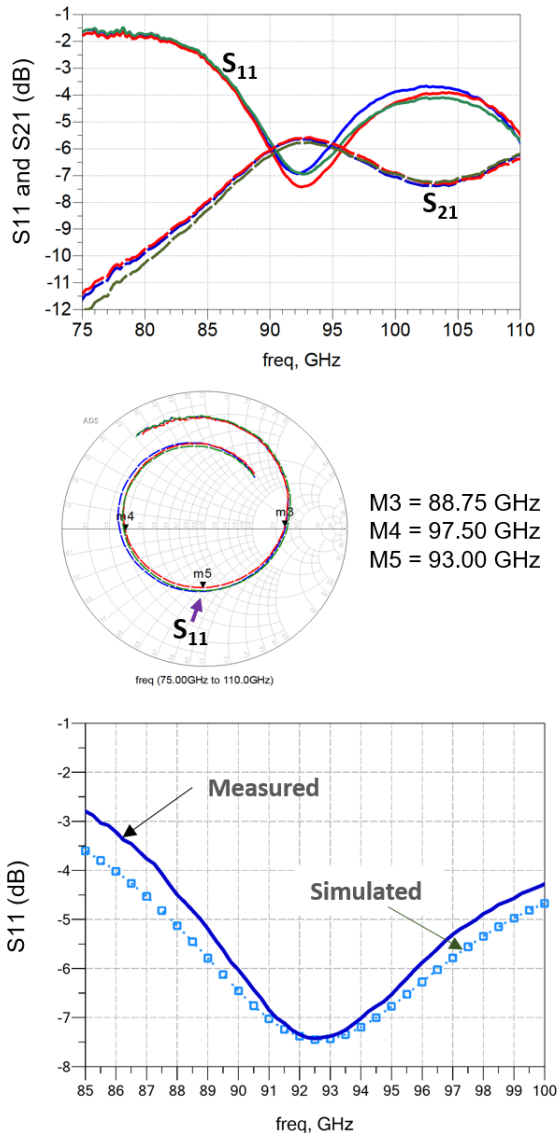

Fig. 8. Small signal characterization data for three independent circuits measured shown in red-blue and green lines highlighting impedance match at 93 GHz with high degree of RF rejection into port 2 (the dc port) as intended per rectenna performance requirements. The lower plot represents the return loss measured for the circuit versus an EM simulated plot of the circuit with all associated components. The close correlation between the measured versus simulated highlights the accuracy of the device model and passive circuits fabricated on wafer.

the absorbed power by the circuit. As a comparison, the measured data were compared with the simulated circuit in which an electromagnetic (EM) simulation was performed to capture all associated passive components in the circuit and couple it to the diode electrical model. The rectangular plot at the bottom of Fig. 8 represents the close comparison between the measured versus simulated results of the circuit, highlighting the accuracy of the diode model and circuit component extraction.

VI. Large Signal Rectenna Circuit Characterization

As discussed in the previous section, the antenna was omitted from circuit#8 to enable on-wafer probing both for

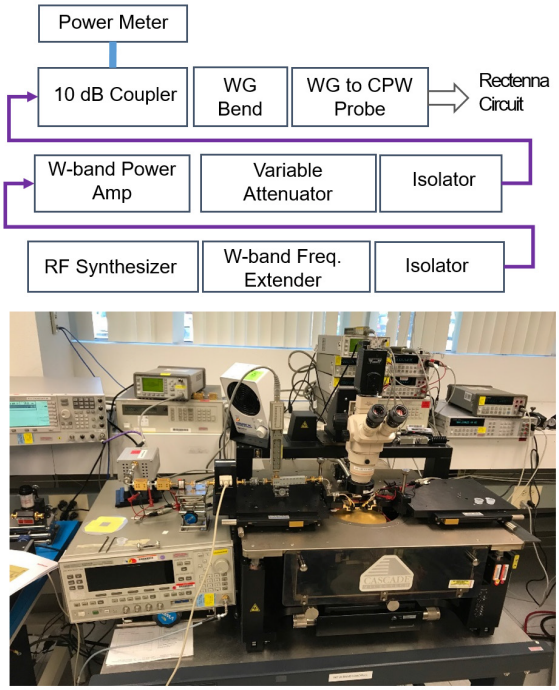

Fig. 9. Large signal block diagram and photograph of the setup for characterizing the rectenna circuit under the highest probed power at 95 GHz. The system is well calibrated to define the exact power that has been absorbed by the rectenna circuit by measuring the reflected power at each incident power level.

small and large signal analysis. In order to characterize the rectenna circuit, a large signal characterization setup was configured and shown both in block diagram and pictorial view of Fig. 9. An RF synthesizer and a W-band frequency extender were used to generate small signal frequency of choice serving as an input for the power amplifier. The frequency range of the power amplifier is between 92 and 95 GHz, and it was decided to set the measurement frequency at 93 GHz which also corresponds to the transmitter frequency for future radiative power transmission demonstrations. The amplifiers use the same high-power MMICs as in [23] and are capable of 1.2 W of saturated power. An electronically controlled variable attenuator is used to control the power incident on the rectenna circuit. This is as opposed to controlling the output power of the amplifier through bias control which would not be a linear power for the rectenna circuit measurements. A 10-dB coupler was also inserted in the path to measure the reflected power from the rectenna circuit and hence, define the power absorbed by the rectenna circuit. A WR10 rectangular waveguide bend completes the measurement setup connecting to the waveguide to CPW probe tip for on-wafer contact to the MMIC rectenna. A pictorial view of the measurement setup is shown in the inset of Fig. 7 capable of probing a variety of circuit types by using micromanipulators of an on-wafer probe station. Each component was separately measured on a network analyzer at W-band frequency range and its loss was noted. In addition, a waveguide short circuit was placed at the waveguide CPW probe and power was measured at the power meter port to further validate the loss of the chain (offset value) at each attenuator settings. Fig. 10 represents the plot of the attenuator setting versus measured power at the

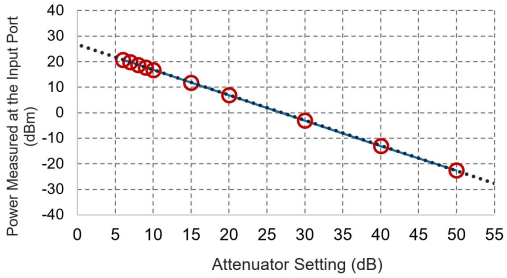

Fig. 10. Input power measured as a function of attenuator setting highlighting a linear line for a controlled incident power into the rectenna circuit. Nonlinear line would indicate internal reflections between the source and the various waveguide components adding uncertainty in the large signal measurements of the rectenna circuit.

probe port with the amplifiers set to 30 dBm. The measured results show a linear relationship of the power measured as a function of the attenuator setting, indicating the amplifier is not being affected by any reflections through the chain. The latter is important for accurate high-power measurement of the rectenna circuit allowing for the offset value (loss of all components) to be the similar across all attenuator settings. The offset value 4.78 dB was measured with minor variation of $<5\%$ across the attenuator settings of 50–10 dB.

The calibration was carried out at 93 GHz with the input probe delivering the W-band power and the output probe dc power measured across a 240-Ω load resistor. The latter was found to be the optimal load for circuit#8 for the highest RF-dc conversion efficiency. The measurements of the circuit#8 rectenna MMIC was performed using the attenuator setting which correlates to a specific transmission power as described above and in order to define the power at the rectenna port-1 a transmission offset value of -4.78 dB was used sure to all the components between the attenuator and the rectenna port-1. For reflected power, the offset is larger due to the 10 dB coupler and the double path through the input port, and it was measured to be -12.71 dB. Using these offset values, a set of measurements were carried out using attenuator setting of 30–0 dB which represents the highest to the lowest power level of -8 to 22 dBm, respectively. Port-2 measurements included the dc measurements which included the voltage and current measurements across a 240 Ω resistor using a high-resolution digital multimeter.

Fig. 11 represents the dc voltage versus current generated from the circuit for each input power level. The circuit topology used is a voltage doubler which provides a higher voltage than the shunted rectifier topology which in this case is 1.1 V at 4.6 mA. The data measured fall on a linear line indicating the diode rectifier is being driven in forward and reverse direction by the incoming RF signal and have not reached the maximum limits of forward current and reverse breakdown voltage. The lower plot highlights the latter in detail where the dc power generated by the circuit is shown as a function of input power absorbed by the circuit. A fit curve is also included to highlight what trajectory is expected for higher input power. For example, at 20 dBm input power a 100 mW of dc power can be generated representing an input power density of 2.5 W/mm of gate width which is comparable with

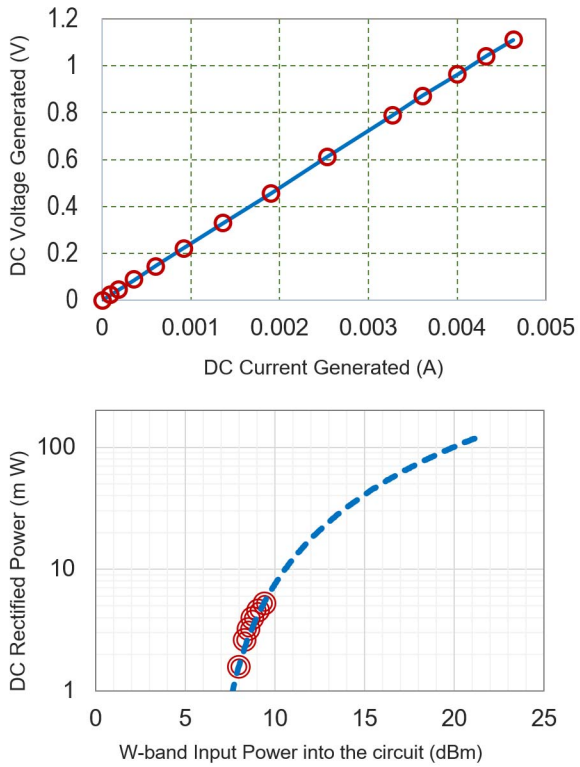

Fig. 11. GaN nano-Schottky rectenna MMIC dc voltage versus current measured under large signal 93 GHz drive. Each data point indicates an input power level incident on the rectenna circuit. The lower plot highlights the dc power generated by the rectenna circuit versus incident power. The dotted line represents the higher power level trajectory if more power was available on the test system.

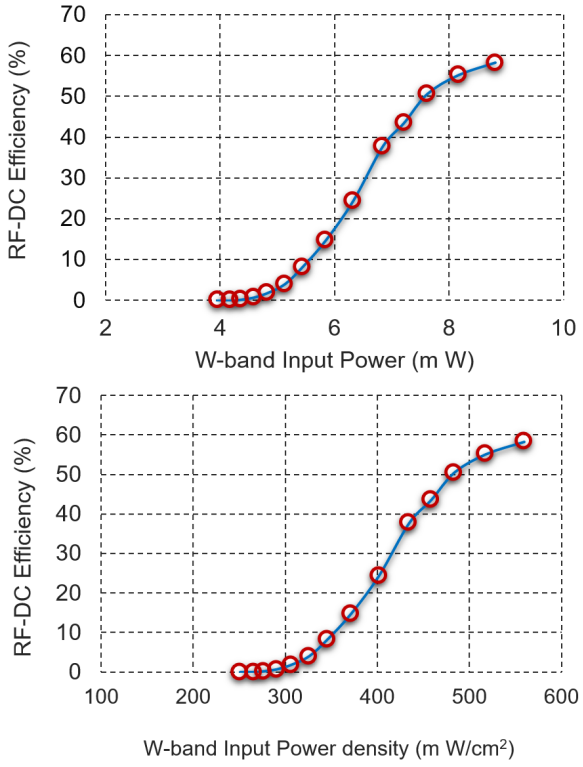

Fig. 12. Plots of RF-dc efficiency at 93 GHz are shown versus input power level and the power density. The GaN nano-Schottky rectenna circuit represents an outstanding input power handling at high degree of efficiency.

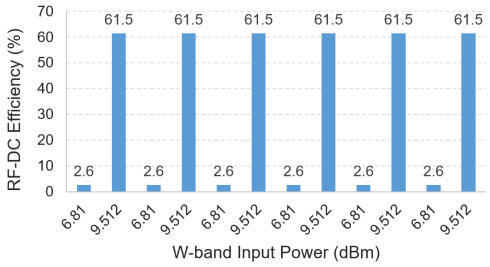

Fig. 13. Plot of efficiency versus 6.81 and 9.512-dBm input power cycles to highlight the performance uniformity and repeatability of the GaN nano-Schottky rectenna.

the HEMT transistor power handling at W-band frequency range [16]. In order to increase the input power further, a larger amplifier is needed to be inserted in the test setup or transition into a quasi-optical setup using a far-field measurement.

Fig. 12 represents the conversion efficiency plots for the measurements as a function of W-band input power absorbed by the circuit and the power density (power absorbed per unit area of the MMIC). The data represent the highest efficiency rectenna circuit reported at W-band frequency range. It can be seen that the efficiency has not peaked completely and with more input power even higher value can be achieved. The input power density can also be calculated where the ratio of the input power versus area of the circuit#4 MMIC is used to highlight input power handling capability. The value of 0.560 W/cm^2 indicates the highest power handling of W-band rectifier to date. Similarly, to the above with more input power higher efficiency can be expected. Key enabling criteria for the circuit is the rectifier switching speed, its high forward current and large breakdown voltage enable the high conversion efficiency and power handling. The latter is a key enabler in a radiative power transmission scenario as high incident power together with high associated efficiency result in a high dc power extraction per unit area of the rectenna receiver.

Another key attribute of the newly developed GaN nano-Schottky rectenna is its inherent robustness of GaN/SiC material system. The 2° rectifier diode is similar to the HEMT structure, which has shown record reliability and output power in amplifier MMICs at W-band frequency range [5]. As an early trial of the robustness, a new circuit #8 MMIC was tested by switching the high input power ON and OFF and recording the conversion efficiency. The results are shown in Fig. 13 where the bar-plot of the efficiency versus input power level into the circuit is shown through five switching cycles. A conversion efficiency of 61.5% was recorded during the high input power of 9.512 dBm and in the low power or OFF-state 2.6% at 6.81 dBm. It can be seen that the rectifier diode in circuit #8 performs consistently as it is presented with rapid high-power switching input levels. This represents a high-power capability of the device technology at 2.5 W/mm of gate width that highlights its great potential as the device size is increased from 0.04 to 1 mm and beyond for high-power rectenna array demonstrations.

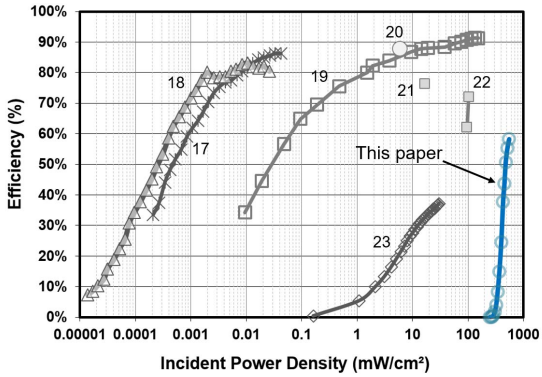

Fig. 14. Plot of RF-dc efficiency versus incident power density of selected published rectenna circuits at various frequency ranges compared with the rectenna reported in this article (blue). It can be seen that the GaN nano-Schottky provides not only very high efficiency compared with other *W*-band published data but also the highest power density compared to all frequency rectenna circuits.

TABLE I

COMPARATIVE PERFORMANCE OF VARIOUS PUBLISHED RECTENNA CIRCUITS AT 94–95 GHz. IT CAN BE SEEN THAT THE GaN NANO-SCHOTTKY PROVIDES THE HIGHEST EFFICIENCY OF >60% TOGETHER WITH ULTRAHIGH POWER DENSITY OF 3.6 kW/m^2

Reference	9	24	25	26	27	This WORK
Rectifier Tech.	GaAs Diode	0.13µm CMOS Sch Diode	65nm CMOS	GaAs Diode	40nm CMOS	GaN nano Schottky
Architecture	Ant + Diode Chip	Integ MMIC with Ant	Integ MMIC with Ant	Ant + Diode Chip	MMIC no-Ant.	MMIC no-Ant.
Tx Source Type	Klystron	Network Analyzer	Soild State Power Amp	Soild State Power Amp	Network Analyzer	Soild State Power Amp
Tx Power (W)	100	0.1	0.14	0.4	0.063	0.09
Rectenna DC Power (mW)	0.65	0.9	0.1	39	0.029	5.7
Efficiency (%)	32.3	37	10	38	45.8	61.5
Element Area (mm2)	5.62	2.9	0.48	18	0.0756	1.58
Power Handling (kW/m^2)	0.17	0.31	0.038	2.38	0.38	3.61

VII. COMPARISON TO THE STATE-OF-THE-ART

In order to analyze the rectenna performance reported in this article two separate comparisons with the state-of-the-art rectenna circuits are presented. The first comparison focuses on a selected high-performing rectenna circuits across the frequency range and the second focuses the comparison directly at *W*-band frequency range. These are shown in Fig. 14 and Table I, respectively. Since 1960s, there have been numerous wireless power beaming demonstrations and associated rectenna performance metrics that have defined the overall efficiency of these demonstrations. Fig. 14 represents the plot of efficiency versus incident power density for various rectenna circuits from MHz to 94 GHz. The latter is certainly not an exhaustive list, but a selective high-performing demonstrations. Brown [19] rectenna performance at 2.45 GHz with an efficiency of 91.4% is certainly a highlight representing a peak power handling of 100 mW/cm^2. Ogawa *et al.* [17] and Sun *et al.* [18] represent the energy harvesting approach with the lowest power handling required appropriately per application need. It can also be seen as the frequency of operation of various rectenna circuits increases the overall efficiency and power handling is reduced. This is mainly due to the higher switching speeds (f_T) required for the rectifier diode as the frequency of operation increases together with parasitic loading of the rectenna circuit. In addition, for higher frequency of operation, lower diode sizes are required (lower junction capacitance) for improved overall efficiency. These generally lead to lower input power handling relating to forward current capability of the particular diode junction size during the RF input cycle. The GaN nano-Schottky rectenna circuit result is also shown providing the highest reported efficiency at *W*-band together with the highest incident power density/handling of 3.61 kW/cm^2. It is also important to note the power handling value was limited by the test bench and is expected to be higher for the circuit. It is our intention to build larger anode periphery devices and validate the latter experimentally. While the comparison to all frequency range rectenna circuits is important for evaluation of the new technology and the circuit performance, its direct comparison with latest published *W*-band circuits of various technologies will also provide a reference for its impact on wireless power beaming demonstrations. Table I represents the latest published *W*-band rectenna circuit performance metrics compared with the GaN-nano-Schottky rectenna circuit. Si CMOS circuits provide very high switching speeds, but fall short on the power handling due to the lower inherent breakdown voltage and current carrying capability of the diode rectifier. However, CMOS presents high degree of integration and can provide substantial advantage for lower power arrays due to many layers of interconnects and the capability of integrating the power conditioning circuits. GaAs diodes being a predominant mm-Wave and sub-mm-Wave device technology also provide great switching speeds and moderate breakdown voltage and hence improvement over the silicon CMOS-based rectenna metrics. The GaN nano-Schottky rectenna circuits reported in this work provide the highest measured RF-dc efficiency of 61.5% and incident power handling of 3.61 kW/m^2. The power handling is defined by the ratio of the dc power measured and the area MMIC for direct comparison with the published results as stated in Table I. The result is an improvement of 1.5× in power handling over GaAs and 9.5× over CMOS rectenna circuits while improving the efficiency by 15.7% over the highest previously reported *W*-band rectenna circuits. It is our belief that the GaN nano-Schottky represents the next-generation technology for the demonstrations of high-power wireless power beaming to come, and it is our intention to integrate similar rectenna circuits in systems and report their result in the near future.

VIII. CONCLUSION

A new technology of GaN nano-Schottky rectifier is introduced, in which a rectifier model is developed following a series of fabrication results of various size diodes. The model is then used to design a voltage–doubler on-wafer rectenna circuit. Small and large signal characterizations of

the fabricated GaN nano-Schottky rectenna circuit at W-band frequency range have resulted in the highest recorded RF-dc efficiency of 61.5% at input power handling of 3.6 kW/m^2 at 95 GHz. The result represents a 15.7% improvement in efficiency compared with the highest reported efficiency of a W-band rectenna and a factor of 1.5× and 9.5× improvement over GaAs and CMOS rectenna circuits at this range. The future work will focus on increasing the rectenna power density as the output power of the transmitters increase in the millimeter range for the highest overall wireless power delivery. Higher frequency of operation beyond 100 GHz is also of interest as the beamwidth further narrows for improved overall efficiency. However, the latter will depend on the high-power sub-mm-Wave transmitter development, which will require improvements in solid-state power amplifiers in the sub-mm-Wave range.

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