

Design of a Cost-Efficient Monostatic Radar Sensor With Antenna on Chip and Lens in Package

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Abstract—This work presents a *D*-band monostatic radar system operating from 144.6 to 161 GHz, which is placed inside a 3-D-printed low-cost case with a built-in lens to boost the antenna (ANT) directivity. The monolithic microwave integrated circuit (MMIC) is manufactured in a 130-nm BiCMOS process and includes a compact transceiver architecture consisting of an oscillator, a diode-based mixer, and an on-chip antenna. The implemented topology allows to significantly improve the signal-to-noise ratio and features a built-in self-test (BIST) structure with the possibility to provide on-chip antenna characterization using power sensors in combination with a directional coupler. Housed inside the robust printed package, the MMIC has only dc and baseband frequency connections, which offers ease of handling and poses the low-cost potential for a variety of applications. The complete transceiver chip consumes only 84.7 mA from a 3.3-V supply and its size is 1964 μm \times 1448 μm . Together with the package the sensor measures a size of 42.2 mm \times 42.2 mm \times 45.7 mm.

Index Terms—BiCMOS, diode, mixer, SiGe, transceiver.

I. INTRODUCTION

THE ambitious development of new technologies over the years led to processes with steadily increasing maximum frequencies fulfilling demands of the industry [1]. Despite several benefits of increasing the operation frequencies, such as smaller areas, nonallocated bands, and new fields of application, there are also challenges to it. In particular, the losses of chip-to-board connections increase in the mm-wave range. Consequently, on-chip antennas (ANTs) became more and more popular recently [2], [3]. On the one hand, they allow to directly radiate the signal from the chip and on the other hand, they even shrink with increased frequency, as they scale with the wavelength. The latter is the reason why on-chip antennas are considered more at high frequencies. Due to the fact that they are quite large at low frequencies, they would consume a huge area which directly relates to costs.

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In terms of area consumption, monostatic transceivers are attractive, as they use only one antenna for transmitting and receiving. Hence, the compact diode-based transceiver topology introduced in [4], which improves the signal-to-noise-ratio by omitting a coupler and its associated losses [5], [6], is extended by built-in self-test (BIST) circuits and an on-chip antenna to enable an innovative cost-efficient sensor solution with monitoring options for production test. The integrated BIST circuits provide good test coverage without the need for millimeter-wave probes and test equipment. The output power available from the oscillator, as well as the antenna connections and matching, can be evaluated using the on-chip BIST readings.

As the metal stack in the standard CMOS and BiCMOS technologies has normally a quite small spacing between top metal and substrate, on-chip antenna designs tend to be inefficient. The low resistivity and high dielectric constant of the silicon substrate make it challenging to achieve a good performance. The work presented in [7] addresses this issue by using a thinned-down substrate and placing the chip on a gold-finished opening on a printed circuit board (PCB) that forms the backside reflector of a dipole-antenna. Furthermore, substrate wave cancellation mitigates antenna losses as described in [8]. Other approaches to increase the antenna performance are to use hybrid antennas [9] or artificial dielectric layer superstrates [10]. Despite increasing the performance, all these methods introduce additional steps to the manufacturing process and require further components aside from the chip, adding to cost. Hence, the on-chip antenna in this work is an inset feed patch that solely uses the standard metal stack of the provided technology. As it is crucial to get a good estimate of the power delivered to the antenna to account for the gain and its return loss, time-consuming electromagnetic (EM)-simulations of connections between the antenna and the circuit, as well as an additional area for antenna test structures are necessary to achieve an optimized antenna design. Here, a simple BIST structure in the transceiver path is provided, which allows to measure the matching of the on-chip antenna, and the power delivered to it, directly on the die using power sensors together with a directional coupler. There are several works in the literature that show how to observe the output power of circuits with such sensors and also how to determine the matching [11]–[14]. Here, a power sensor is used to perform a return loss measurement on-chip using a directional coupler. To the best of the authors' knowledge, this is the first time that such

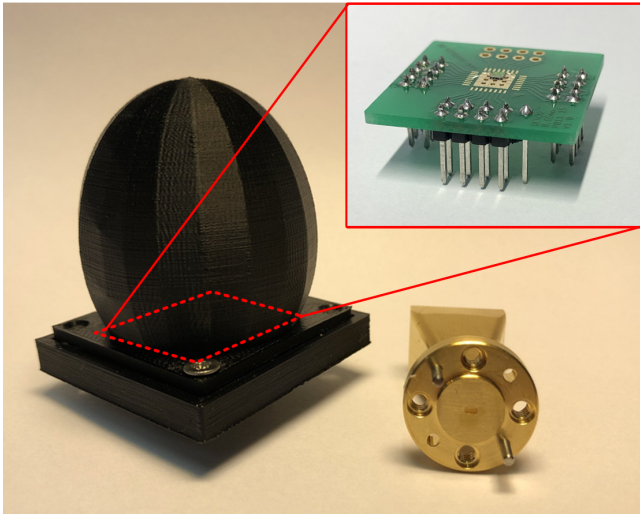


Fig. 1. Photograph of the realized monostatic transceiver system. The MMIC is bonded on an adapter board and placed inside the 3-D-printed package, which includes and aligns the lens on top of the die. The WR-06 waveguide horn is placed for scale.

a BIST structure is implemented together with an on-chip antenna in this frequency range. Thus, it is possible to monitor the output power and the impact of process variations without using RF probes during the production phase, while taking advantage of the information provided by the structure already in the design phase.

In addition to the on-chip antenna and the BIST structure, a 3-D-printed case for the monolithic microwave integrated circuit (MMIC) is presented that features an integrated lens, which allows to increase the directivity of the antenna and thereby extends its operation in terms of range. As the die possesses only low-frequency connections, it can be bonded onto a low-cost FR4 adapter board that is placed inside the case, leading to the robust and cost-efficient sensor shown in Fig. 1. Possible applications for such a system include, for example, motion sensors or ground speed detection e.g., antilock brake systems [15]–[17].

The article is organized as follows. In Section II, the transceiver MMIC with its different building blocks is explained, while Section III describes the simulation and measurement results of those. Section IV gives an overview of the transceiver implementation into a radar demonstrator and the respective measurement results of the sensor are presented in Section V. Finally, in Section VI, the results are summarized.

II. TRANSCEIVER MMIC

The block diagram of the transceiver chip is shown in Fig. 2 and the circuit is realized in a 130 nm BiCMOS technology [18], which offers HBTs with f_t and f_{max} of 250 and 370 GHz. The process features four thin copper layers for routing and two thick copper layers for passives. The topmost metal is aluminum and is usually used for pads or fuses. In this work, the aluminum layer is also used to implement the antennas, as this allows to maximize the distance between radiating patch and ground plane, which is realized in the lowest metal layer.

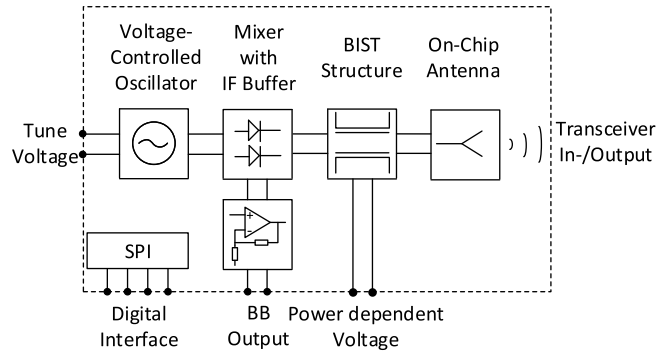


Fig. 2. Block diagram of the realized monostatic transceiver system.

In this monostatic implementation, a transfer mixer connected in series between the signal source and the antenna is used. As the mixer is realized with a single diode, a large fraction of the voltage-controlled oscillator (VCO) signal is coupled via the mixer diode to the antenna. At the same time, the VCO acts as a local oscillator (LO) signal for mixing the received signal from the antenna to the baseband. The fundamental VCO is designed to deliver a high output power, as amplifiers and doublers for high frequencies would lead to a larger power and area consumption. Thus, choosing this VCO leads to low power and compact design. Additionally, a BIST structure consisting of a directional coupler with power sensors is placed between the mixer and the antenna to enable power and return loss measurements. Here, the benefit is that the power delivered to the antenna and its return loss can be measured with the patch as load. Furthermore, a digital interface can be used to control the different blocks.

Compared to state-of-the-art monostatic transceiver implementations, the proposed diode-based mixer topology allows to increase the signal-to-noise ratio (SNR)

$$\text{SNR} = \frac{P_T G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_0 B F_n}. \quad (1)$$

Here, P_T is the transmit power, G the gain which is similar in receive and transmit direction for a monostatic implementation, λ the wavelength, σ the radar cross section, R the range, k the Boltzmann's constant, T_0 the temperature, B the noise bandwidth, and F_n the noise figure. The impact on the SNR by the topology is explained in Fig. 3, which shows a conventional monostatic transceiver implementation [19] and the proposed one using a diode-based mixer. The insertion loss introduced by the rat race coupler in the conventional approach decreases the output power at the antenna and also the power that is delivered from the antenna to the mixer. Thus, the insertion loss between port power amplifier (PA) and ANT decreases P_T , and the losses occurring from port ANT to RF_{mix} increase F_n , leading to a degradation of SNR. In addition, the coupler has limited isolation, which restricts the output power of the system. Otherwise, the transmitter leakage could impair the receiver performance. The innovative diode-based implementation operates without a coupler and can therefore forgo the splitting of the signal into two equal parts, as well as the associated insertion loss. Here, the signal

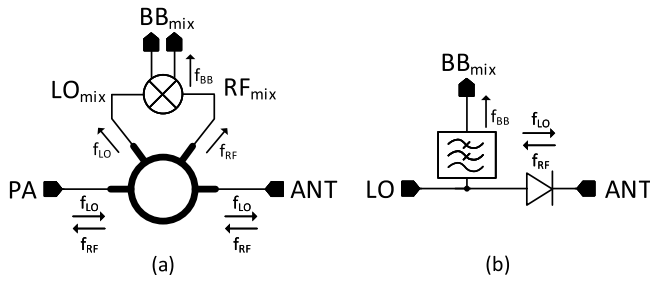


Fig. 3. Monostatic transceiver implementations. (a) Rat race coupler with mixer (conventional). (b) Diode-based mixer (proposed) [4].

travels through the diode-connected transistor which poses a sufficiently low impedance, so just a small insertion loss occurs. Furthermore, there are no limitations on the output power with this approach. The diode-based implementation also has a simple design and allows to save space, as mixer and coupler area are reduced to a single transistor.

In the following, each component of the realized transceiver is briefly described:

A. Voltage Controlled Oscillator

The fundamental VCO in Fig. 4(a) can be derived from a common-collector Colpitts topology. The base of transistors Q_1 and Q_2 is coupled via a transformer consisting of L_1 and L_2 which also provides the bias voltage. This voltage is created by diode connections to the supply and not shown here to improve readability. The current mirror supplying $I_{\text{bias}1}$ is not shown for the same reason. Transmission line TL_1 serves to isolate the current mirror from the emitter of Q_1 . TL_2 and TL_3 together form the output matching and allow to extract the fundamental frequency. The lines TL_4 and TL_5 are placed to further increase the impedance of the varactors to ground, additionally to R_1 and R_2 . Capacitors C_1 and C_2 are placed as dc blocks.

The two oscillator cores that are formed by the base-coupled cascode stage lock together at a fixed frequency leading to a high output power design. The varactors controlled by $V_{\text{tune}1}$ and $V_{\text{tune}2}$ allow fine respective coarse tuning of the output frequency. The circuit draws 70 mA from 3.3 V voltage supply. Furthermore, the tail current can be controlled by the digital interface allowing power control.

B. Mixer With BB Buffer

In Fig. 4(b) the diode-based mixer is shown together with an BB Buffer. Here, the base-emitter diode of transistor Q_3 is used to mix the LO and RF signal, while enabling the LO signal to pass to the RF port with a small insertion loss. The contact configuration of Q_3 is BEBC to provide a small base resistance and minimize the insertion loss. Furthermore, an additional diode-connected transistor Q_4 is placed in the mixer to adjust the BB common-mode voltage to the input of the buffer. This transistor is similar in size and contact configuration to Q_3 . Transmission line TL_6 transforms the RF short circuit caused by C_2 to an open so that the LO signal

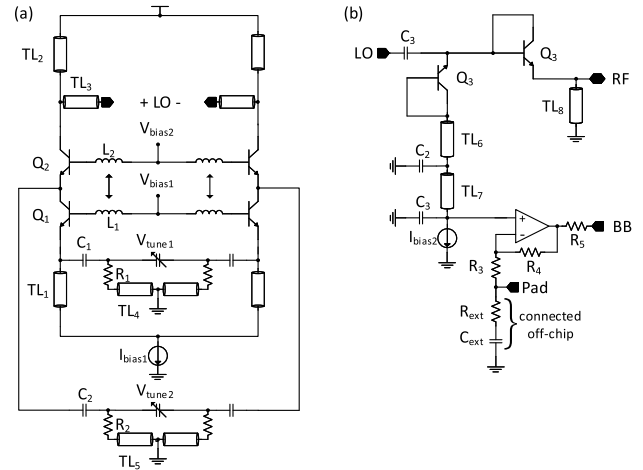


Fig. 4. Simplified schematics. (a) Base-coupled VCO. (b) Diode-based mixer. For readability only one half of the differential circuit is shown after the VCO.

travels ideally only to Q_3 . TL_7 and C_3 decouple the BB signal even more from the transceive path. At the RF port, TL_8 also transforms the short circuit to an open and provides a path to ground for a DC current that is applied by the current source $I_{\text{bias}2}$ to bias the diode. $I_{\text{bias}2}$ is realized with a current mirror, whose reference current can be controlled via serial peripheral interface (SPI), and allows to slightly control the tradeoff between noise figure and conversion gain. Capacitor C_3 is inserted for AC coupling.

The BB signal is fed to the positive input of the buffer stage, which is connected as noninverting operational amplifier. Here, the ratio between resistors R_3 and R_4 allows to set the gain, which can be modified by an external resistor R_{ext} that is connected to a pad. This allows to adjust the circuit after manufacturing and is also necessary as the AC coupling capacitor C_{ext} is too large to be implemented on the chip. The resistor R_5 is inserted to desensitize the output against connected measurement equipment, e.g., capacitances of long cables.

C. BIST Circuit

The BIST circuit is based on the power sensor depicted in Fig. 5. Here, a diode-based detector together with a directional coupler similar to [20] serves to sense the power in the transceiver path. The schematic of the diode detector is shown in Fig. 5(a). The detector uses the nonlinearity of the diode-connected transistor Q_1 which is operated in the square-law region, so an output voltage proportional to the power is observed. The signal path is connected to the emitter of the diode, which leads to a higher sensitivity as the influence of large collector parasitics is removed. After the diode, the signal passes an RC low pass filter and is extracted at the emitter follower Q_2 . Resistance R_4 is placed at the base of Q_2 to suppress possible negative resistances for long lines after the emitter follower, which could lead to instability. Transistors Q_1 and Q_2 are biased with current mirrors, which are shown here as current source $I_{\text{bias}1}$, respectively, $I_{\text{bias}2}$ for readability. Resistors R_2 and R_5 are inserted to decouple the capacitance of the current source, leading to increased sensitivity for

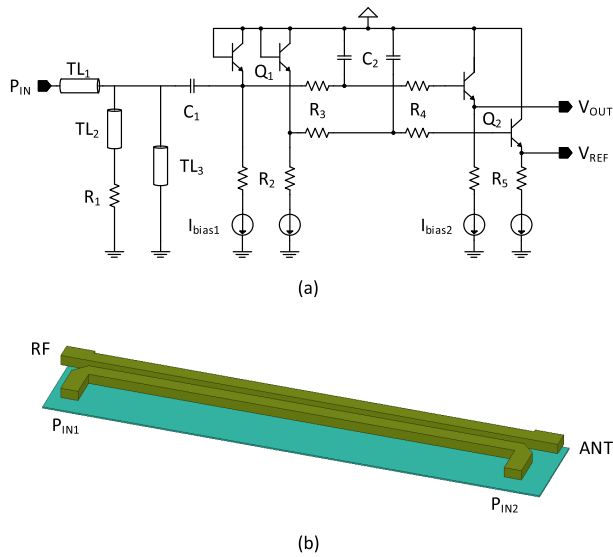


Fig. 5. BIST structure based on a power sensor consisting of (a) diode detector and (b) directional coupler.

the detector and better stability for the emitter follower. The matching network consisting of TL_2 , TL_3 , and R_1 is placed at the input to match the coupler impedance to the capacitive behavior of the detector diode and to adjust the range of operation for the detector. Here, R_1 is a tradeoff between losses in the matching network and bandwidth, while also desensitizing the circuit against process variations. Transmission line TL_1 can be varied to enable flexibility in the positioning of the power detector, while C_1 is inserted as AC coupling. Except for the input matching the same signal path is placed again and provides a reference voltage. Hence, it is necessary to place the elements in close vicinity in the layout to keep the influence of process variation or thermal effects to a minimum. The circuit consumes 0.36 mA from a 3.3 V supply.

The directional coupler depicted in 5(b) is used to acquire the signal traveling to the antenna and the reflected signal. It is realized in a thick top metal of the technology and uses a metal two layers below as reference ground plane. Two detectors are connected to the coupler, where the detector at P_{IN1} senses the power coming from the RF port and P_{IN2} the power coming from the ANT port. The detector circuits deliver a voltage proportional to the power in each direction. While the detector diodes work in the square-law region, no correction factor is necessary, because the voltage scales linear with the power as shown in [21]. This allows one to calculate the return loss

$$RL = 10 \log \left(\frac{V_{rev}}{V_{fwd}} \right). \quad (2)$$

Here, V_{rev} represents the voltage equivalent to the reflected power and V_{fwd} the accepted power by the antenna. They are the voltage difference between V_{OUT} and V_{REF} acquired at the respective power sensor. Furthermore, the two voltage levels can be used to determine the absolute power that is transmitted, as well as the power that is received by the antenna.

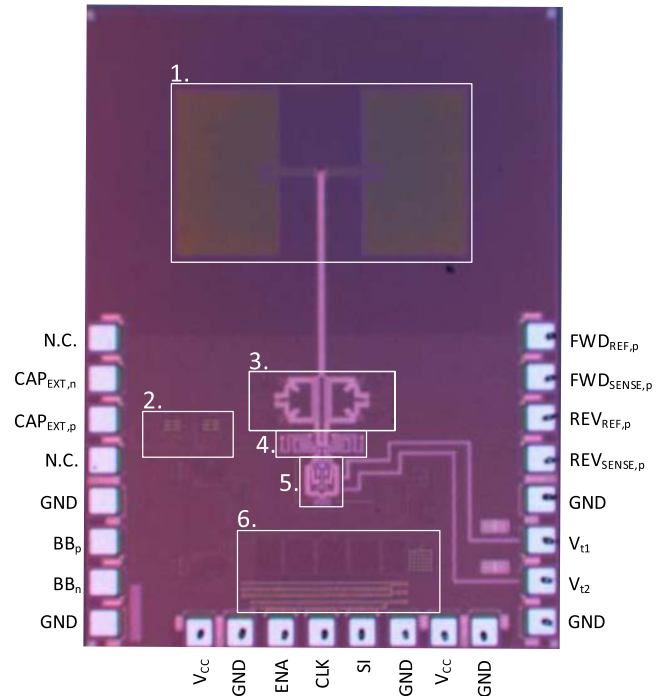


Fig. 6. Chip photograph of monostatic transceiver ($1964 \mu\text{m} \times 1448 \mu\text{m}$) with (1) antenna, (2) BB buffers, (3) BIST structures, (4) transfer-mixers, (5) fundamental VCO, and (6) SPI interface.

D. Antenna

Fig. 6 shows the on-chip antenna which is arranged in a 2×1 array formation to increase the antenna gain. Each antenna is fed with one part of the differential signal. At first, only one inset feed patch has been designed and optimized using the 3-D simulator HFSS from Ansys. The top metal of the technology which is aluminum serves as the material for the patch, while the lowest metal which consists of copper is used for the ground plane. As the antenna substrate height is quite small due to the metal stack height, no additional mitigation measures for surface waves were taken. To achieve repeatable antenna performance, fill structures are used to satisfy the density rules for chip fabrication. This leads to small metal rectangles of different sizes in the layers between top and bottom, resulting in an increased effective permittivity. Consequently, the wavelength decreases according to

$$\lambda = \frac{c_0}{\sqrt{\mu_r \epsilon_r} f}. \quad (3)$$

Here, λ is the wavelength, c_0 the speed of light, μ_r the effective permeability, ϵ_r the effective permittivity, and f the frequency. For the used patch that scales with the wavelength, the size can be reduced as it scales with the antenna area. The associated decrease in the gain can be mitigated by array structures and the smaller form factor of the antenna allows better realization of placement and routing. To account for the change in effective permittivity, the parallel-plate capacitor formula

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad (4)$$

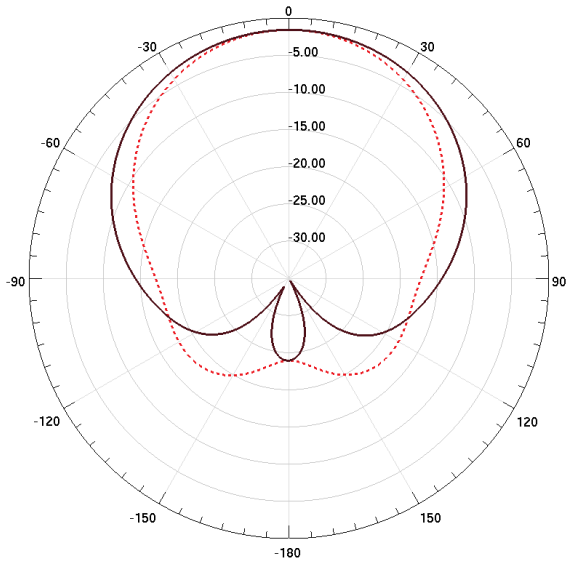


Fig. 7. Simulated radiation pattern of the antenna array at 152 GHz with E -plane (dashed) and H -plane (solid).

is used, where C is the capacitance, A the area of the antenna and d its distance to the ground plane. After comparing the simulation results of two $100 \mu\text{m}^2$ areas, one with filling structures and one without, ϵ_r is extracted. The resulting value from EM-simulation differs with $\epsilon_r = 7.2$ (including fill structures), from the specified one for the technology $\epsilon_r = 4.2$ (without fill structures) [22]. Fig. 7 shows the simulated radiation pattern of the realized antenna array. At 152 GHz it reaches a peak gain of -1.25 dBi with an efficiency of 12.3%.

E. Transceiver

The complete manufactured transceiver die is depicted in Fig. 6. On the left side of the chip the external capacitors to the ground are connected at the pad $\text{CAP}_{\text{EXT},p}$, respectively, $\text{CAP}_{\text{EXT},n}$, with the possibility to insert a series resistance to change the gain of the BB buffer on the chip. The BB frequency can be extracted on the same side at the BB_p and BB_n pads, where the indices p and n solely denote the left and right path between VCO and antenna. Due to the same phase, those two signals cannot be used differentially. On the bottom side of the chip, the SPI connection pads for enable (ENA), clock (CLK), and slave input (SI) are located, as well as two V_{CC} pads to apply and measure the supply voltage at the same time for on-wafer characterization, while providing a lower resistance when it is supplied in the demonstrator via a low dropout regulator (LDO). On the right side, the forward and reverse voltage of the power detectors for the right half of the circuit can be measured at $\text{FWD}_{\text{REF},p}$ and $\text{FWD}_{\text{SENSE},p}$, respectively, $\text{REV}_{\text{REF},p}$ and $\text{REV}_{\text{SENSE},p}$. Also the tuning voltage for the VCO is applied at this side via V_{11} and V_{12} . As the high-frequency signal is transmitted and received by the on-chip antenna, no high-frequency connections are necessary for the pads. To verify the concept of the BIST structure, two transceivers with different

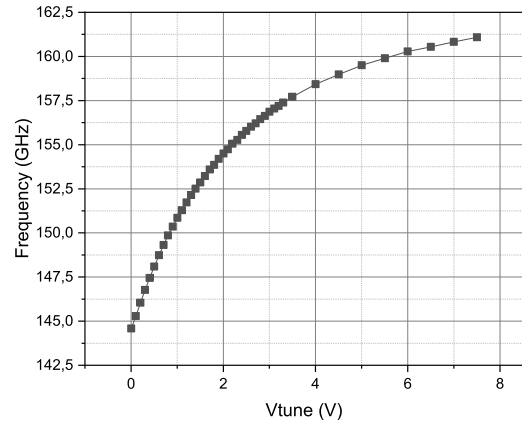


Fig. 8. Measured output frequency versus tuning voltage with fine and coarse voltage connected.

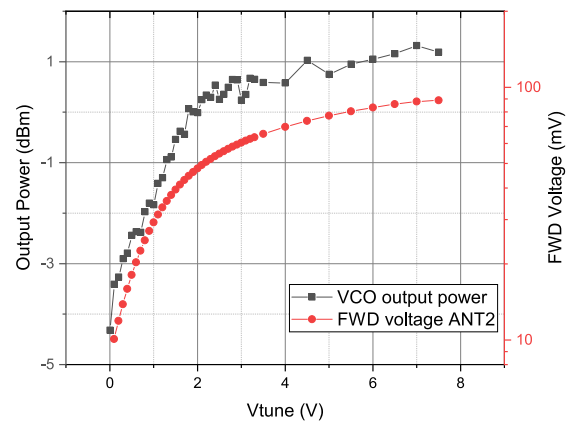


Fig. 9. Measured output power of VCO and forward detector voltage of transceiver with second antenna design (ANT2) versus tuning voltage with fine and coarse voltage connected.

antenna dimensions are implemented. The two antennas will be denoted as ANT1 and ANT2, and are shown in Fig. 15.

III. SIMULATION AND MEASUREMENT RESULTS

The VCO is characterized as a stand-alone chip which allows one to measure the output power that is delivered to the antenna, and is implemented unchanged in the transceiver. All values are measured on-wafer using ground-signal-ground (GSG) Infinity waveguide probes to contact the chip at one differential output while terminating the other with 50Ω . Fig. 8 shows the tuning characteristic of the VCO for different supply voltages, which is measured using a harmonic mixer from OML together with a Keysight N9010A EXA signal analyzer. The inputs for fine and coarse tuning are connected to each other for this measurement and the voltage is swept from 0 to 7.5 V. This leads to a tuning range of 10.7% ranging from 144.6 to 161 GHz for a 3.3 V supply. The corresponding output power can be seen in Fig. 9 and is acquired using a VDI Erickson PM5 power meter. Its peak is 1.3 dBm for a tuning voltage of 7 V corresponding to a frequency of 160.8 GHz. This corresponds to a total differential output power of 4.3 dBm. For tuning voltages lower than 2 V the output power decreases, due to the decrease in the quality

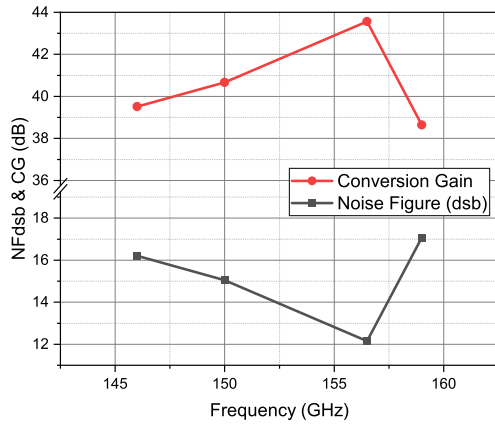


Fig. 10. Measured conversion gain and double-sideband noise figure of the diode-based mixer at a BB frequency of 700 kHz.

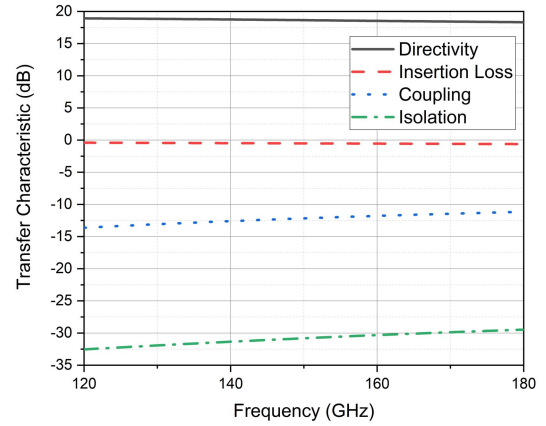


Fig. 12. Simulated transfer characteristic of the directional coupler.

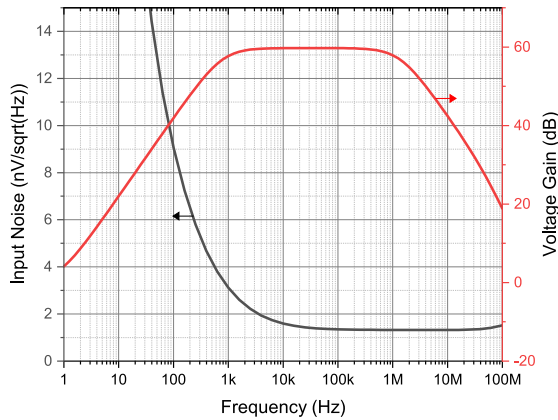


Fig. 11. Simulated input noise and voltage gain of the BB buffer with $R_3 = 20 \Omega$, $R_4 = 20 \text{ k}\Omega$, $R_5 = 100 \Omega$, $R_{\text{ext}} = 0 \Omega$ and $C_{\text{ext}} = 10 \mu\text{F}$ [see Fig. 4(b)].

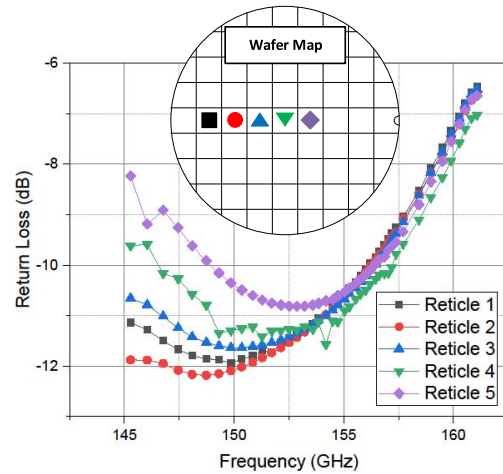


Fig. 13. Measured variation of the return loss measured on different reticles of the wafer for the second antenna design.

factor of the varactor. This is uncritical for the determination of the return loss, as the power sensor has a high dynamic range. Fig. 9 shows also the forward voltage of the detector on the transceiver with the second antenna design (ANT2) that relates to the power which is passed to the antenna. As expected the voltage characteristics follow the measured power.

In Fig. 10, the noise figure and the conversion gain of the mixer are shown. The BB frequency of 700 kHz is chosen here due to spurious signals around 1 MHz caused by the measurement environment. Measured noise figure and conversion gain already include the influence of the operational amplifier, which is connected as a noninverting amplifier with a gain of 60 dB and has a 10 μF capacitance off-chip to provide an AC ground for its negative input. The simulated values for the BB buffer can be seen in Fig. 11. Noise figure and conversion gain of the mixer with this BB buffer are determined using the Y-factor method. For the measurement, a version of the chip without antenna is characterized on the wafer using a GSG *D*-band waveguide probe in combination with a VDI-730 SGX *D*-band extender and an ELVA-1 ISSN-06 noise source. The BB signal is evaluated using an E5052 signal

source analyzer from Keysight and the necessary external capacitor is connected via a probe tip.

In Fig. 12, the simulated values for directivity, insertion loss, coupling, and isolation of the directional coupler, that is used in the BIST structure, are shown. To evaluate the return loss of the antenna, the VCO of the transceiver is fed with a voltage ranging from 0 to 7.5 V at its tuning ports, that are connected to each other. Then the directional coupler is used to provide the signals for the power sensor. The voltages V_{rev} and V_{fwd} of the sensor are measured using voltmeters. The return loss of the on-chip antennas in Fig. 13 is based on the measured V_{rev} and V_{fwd} of the power sensor and calculated as given in (1). Here, the values of the second antenna design for different reticles on the wafer are shown. The shift between the different plots is due to the process variation and is primarily caused by the fluctuation of the distance between the top aluminum layer and the lowest copper layer, which acts as ground. Additionally, a change in color of the patches on the wafer can be observed under the microscope due to the variation of the passivation thickness, visualizing the process variation.

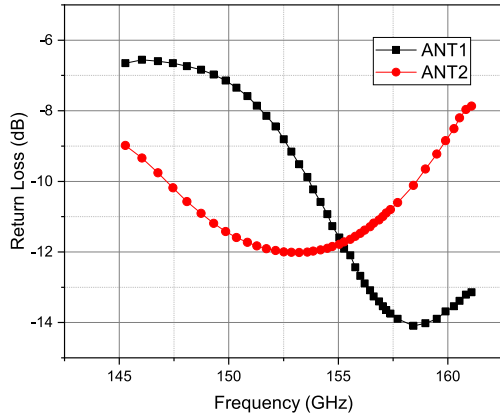


Fig. 14. Return loss of the antennas calculated from measured power sensor voltages for two designs with different antenna size.

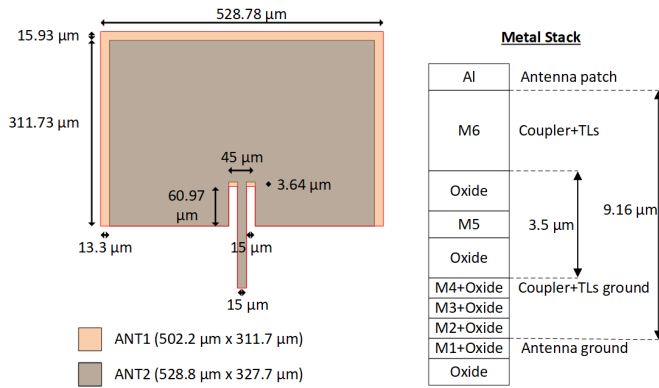


Fig. 15. Differences in dimensions of a single inset-fed patch of the on-chip antennas and simplified metal stack of the used technology.

A return loss comparison of the first (ANT1) and the second (ANT2) antenna design is shown in Fig. 14. The input matching of ANT1 is centered at 158.4 GHz and of ANT2 at 153.2 GHz according to the power sensor. This difference in frequencies aligns with the dimensions given in Fig. 15. As the length of the patch scales with the wavelength, the larger antenna is centered at a lower frequency.

IV. IMPLEMENTATION OF THE TRANSCEIVER SYSTEM

A. System Overview

To demonstrate the operation of the designed monostatic transceiver, a simple demonstrator using a microcontroller (μC) is realized. The block diagram of the demonstrator is shown in Fig. 16. Here, a commercially available development board is used and its LDO provides the power for all blocks. The board also features a USB to universal asynchronous receiver transmitter (UART) converter, which allows to program the microcontroller and at the same time to readback information from it. The μC is used to send the necessary SPI commands to the MMIC and to perform a fast Fourier transform (FFT) on the BB signal, allowing to determine the frequency and thus to evaluate the Doppler effect, giving the velocity of the detected target. The result can then be shown on a display that features a plot of the velocity together with

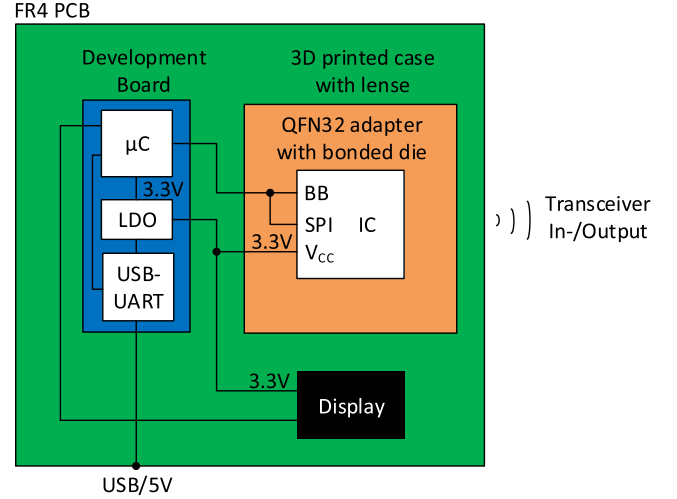


Fig. 16. Block diagram of the monostatic transceiver demonstrator.

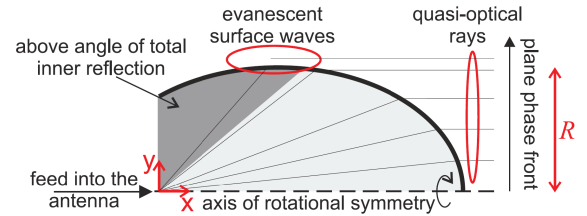


Fig. 17. Ellipsoid lens outline [23].

signal information at the top and the spectrum that is covered by the FFT at the bottom. As the MMIC that delivers the BB signal only has low-frequency connections, it is bonded on an adapter board. Afterward, this adapter board is placed in a 3-D-printed case, that features an integrated lens to focus the transmitted and received power from the on-chip antenna.

B. Case With Lens

An ellipsoid lens is embedded in the package to increase directivity and therefore range. The design is based on [23], where the following equation is used:

$$1 = \left(\frac{x - R/\sqrt{\epsilon_r - 1}}{R/\sqrt{1 - 1/\epsilon_r}} \right)^2 + \left(\frac{y}{R} \right)^2. \quad (5)$$

Here, x and y denote position in a coordinate system, R is the radius around the axis of rotation, and ϵ_r the relative permittivity. The resulting outline of the antenna can be seen in Fig. 17. As the package is fabricated using a 3-D-printer, the filament is characterized regarding its permittivity and loss tangent, because the lens is directly embedded and consequently printed as well. Thus, a sample of the used acrylonitrile butadiene styrene (ABS) is used for various measurements leading to the values given in Table I. Relative permittivity and loss tangent have a flat characteristic over the frequency and small deviations can be explained by the different measurement setups that are used depending on the frequency range. The permittivity and loss tangent values are then used to create an HFSS model of the ellipsoid lens, which is then excited with an open-ended rectangular waveguide to

TABLE I
MEASURED VALUES FOR RELATIVE PERMITTIVITY AND LOSS TANGENT AT DIFFERENT FREQUENCIES

| Frequency | Relative permittivity ϵ_r | Loss tangent $\tan \delta$ |
|-----------|---------------------------------------|-------------------------------|
| 1 kHz | 2.49 | 0.0019 |
| 10 kHz | 2.47 | 0.0036 |
| 100 kHz | 2.46 | 0.0039 |
| 1 MHz | 2.45 | 0.0039 |
| 10 MHz | 2.43 | 0.0039 |
| 100 MHz | 2.42 | 0.0039 |
| 1 GHz | 2.40 | 0.0040 |
| 10 GHz | 2.39 | 0.0040 |
| 100 GHz | 2.38 | 0.0038 |

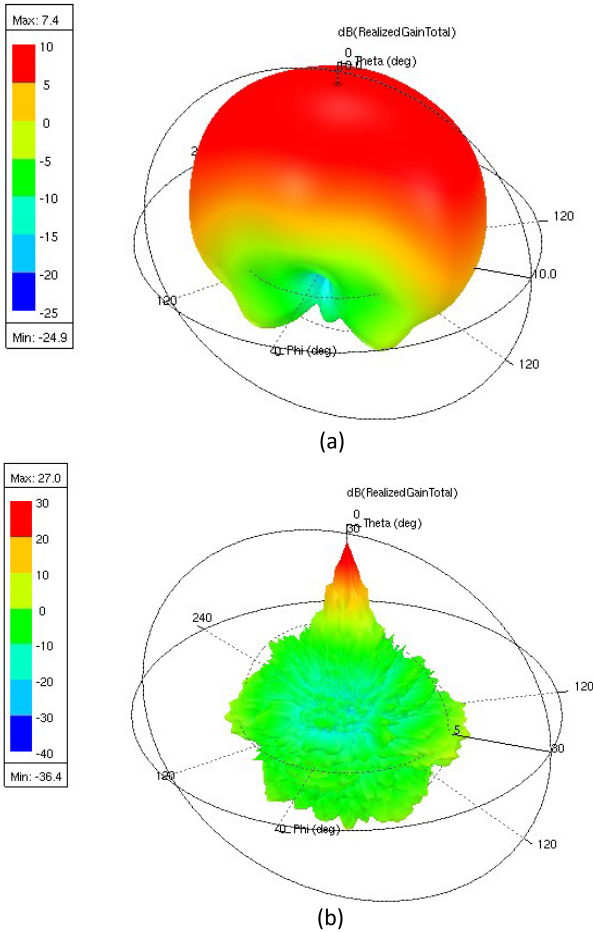


Fig. 18. Simulated antenna at 150 GHz for a WR6 open-ended rectangular waveguide as (a) stand-alone structure and (b) embedded in package.

verify its functionality. The waveguide is used here instead of the on-chip antenna, as it provides a similar antenna pattern, but has a less complicated mesh, leading to reduced simulation times. As the antenna pattern of the waveguide and the antenna are similar, with both having a broad radiation angle, this simplification can be made here. To evaluate the influence of the increased directivity by the package with embedded lens, the open-ended waveguide is excited with a TE_{10} mode and its antenna pattern is simulated stand-alone, as well as inside the package, where the chip would be located. The simulated results and the geometries can be seen in Fig. 18 and show that

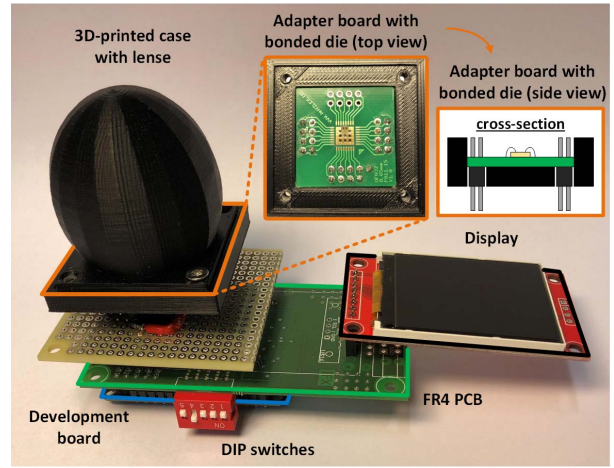


Fig. 19. Photograph of the realized demonstrator. The different parts are all connected via pin headers.

at a frequency of 150 GHz the peak antenna gain is increased by 19.6 dB, due to a directivity improvement of 25 dB. The values used for the ellipsoid are $x = 44.3$ mm, $y = 15.8$ mm and $R = 20.1$ mm. The setup for the EM-simulation is similar to the cross section shown in Fig. 19, except it uses an open-ended waveguide instead of the on-chip antenna. The 3-D-printed case also protects the bondwires and its frame acts as a spacer between PCB and the top, thus ensuring the correct distance to the lens. Furthermore, this setup also allows for low-cost bondwire packages in high volume production.

C. Demonstrator

A photograph of the realized sensor system is shown in Fig. 19 and uses pin headers to combine the different parts. The development board is plugged into the FR4 board, which serves to connect its respective pins with the transceiver in the package and features two operational amplifiers, as well as a multiplexer. Via 5 DIP switches which are also placed on the board, it is possible to control the baseband gain by switch 1 and 2, leading to different feedback resistors for the amplifiers and resulting in four possibilities to increase the BB signal even further by 10, 25, 40, or 56 dB. By switch 3 it is possible to toggle between two bandwidths for observation of the BB signal by setting the sampling frequency to 2048 or 5120 Hz, while switch 4 sets the number of samples to 512 or 1024. Switch 5 allows to choose between the two SAR analog-to-digital converters (ADCs) on the microcontroller from which each is connected to one BB output of the MMIC. This simple architecture allows rapid prototyping of case implementations together with possible lenses and also the quick change of bonded chips.

Furthermore, a display can be plugged in that shows an instantaneous evaluation of the detected signal, as depicted in Fig. 20. In the upper half, on the left side the speed of the detected target, the average power over all signals and the scaling factor used for plotting are shown, while on the right side the FFT bin of the detected signal and the ratio between signal and average power are listed. Below those six values, a plot indicating the change in frequency is shown. In the lower half, an instantaneous spectrum based on the

TABLE II
COMPARISON OF SiGe MONOSTATIC TRANSCEIVER CIRCUITS WITH ON-CHIP ANTENNA

| Reference | Technology (f_T/f_{max}) (GHz) | Freq. (GHz) | P_{TX} (dBm) | NF_{DSB} (dB) | CG (dB) | G_{ANT} (dBi) | Antenna | P_{DC} (W) | Area (mm ²) |
|-----------|---------------------------------------|----------------|-------------------|--------------------|------------|--------------------|---------------------|-----------------|----------------------------|
| [24] | SiGe 130 nm (230/280) | 122 | 3.6* | 11.5 (1MHz) | 13 | 6 | patch + resonator | 0.9 | 5.72 |
| [5] | SiGe 130 nm (300/500) | 154 | 3 | 20 (1MHz) | 2 | - | patch + DRA | - | 1.9 |
| [25] | SiGe 130 nm (300/500) | 169 | 3** | 15.5 (1MHz) | 19 | 5 | folded-dipole + LBE | 0.87 | 5.4 |
| [3] | SiGe 130 nm (250/370) | 224 | -2.1** | 22.6 (23kHz) | 38.4 | -0.2+35*** | patch | - | - |
| This work | SiGe 130 nm (250/370) | 157 | 3.7* | 12.1 (700kHz) | 43.5 | -1.3+19.6*** | patch | 0.28 | 2.84 |

*at probe **radiated ***with lens

DRA: dielectric resonator antenna

LBE: localized backside etch

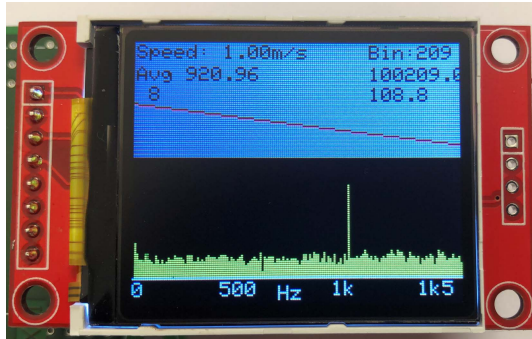


Fig. 20. Example for an evaluation on the microcontroller shown on the display of the demonstrator.

calculated FFT is drawn. The example evaluation displayed here assumes an operating frequency of 157 GHz, as well as a BB frequency that increases repeatedly from 1 Hz up to 1045 kHz, resulting in a sawtooth plot. The respective velocity is determined according to

$$v_{target} = \frac{f_{BB}}{2f_{osc}} c_0 \text{ [m/s]}. \quad (6)$$

Here, f_{BB} is the baseband frequency given by the mixer, f_{osc} the operating frequency of the VCO and c_0 the speed of light. As 1024 samples and a sampling frequency of 5120 Hz are used, FFT bin 209 corresponds to 1045 Hz, respectively, a velocity of 1 m/s.

Combined with the possibility to evaluate the return loss and the power of the antenna with the BIST structure, this demonstrator allows to quickly optimize the whole system.

V. SENSOR EVALUATION

The sensor is evaluated using the measurement setup shown in Fig. 21. Here, a target placed on the plate of a 3-D-printer is moved along the z -direction, while the sensor is placed at the top facing downward and is operated as a Doppler radar with a fixed oscillation frequency of 157 GHz. The programming of the printer is done by G-code, a computerized numerical control (CNC) programming language that allows to set the velocity of the step motors that move the plate. For the measurement depicted in Fig. 22 a value between 1000 and 1700, which denotes the movement speed in mm/min, is passed to the printer. The comparison of

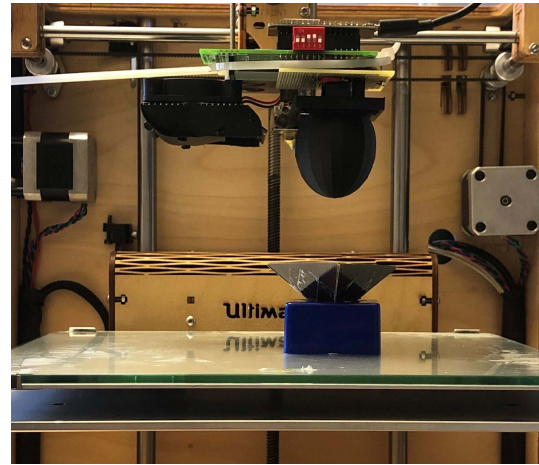


Fig. 21. Setup used for demonstrator evaluation.

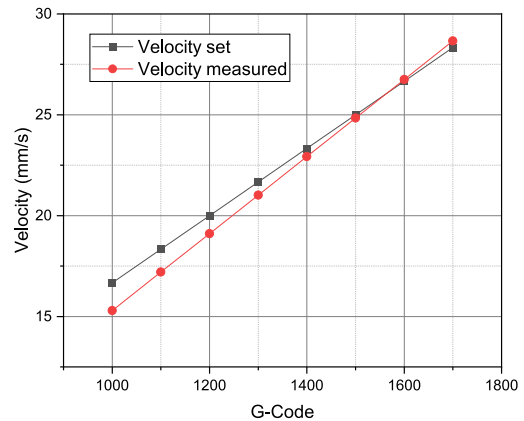


Fig. 22. Comparison between measured and set velocity.

the adjusted and measured velocity shows a small offset in the detected movement. This deviation from the set velocity can be explained by the FFT that is performed on the microcontroller. To detect the slow movements of the plate, the sample frequency is set to 2048 Hz with 1024 samples, which leads to a bin width of 2 Hz. The minimum velocity difference that can be determined therefore is 1.91 mm/s. Thus, the resolution is only limited by the evaluation of the microcontroller. Consequently, the measured velocity is always a multiple of the 1.91 mm/s and therefore evaluates to one of the two adjacent values to the set velocity.

VI. CONCLUSION

This article has presented a compact monostatic radar transceiver that enables low-cost system implementations despite high-frequency operation. The introduced demonstrator shows the ease in handling of the topology and exhibits the possibility to overcome challenges posed by lossy on-chip antennas with a cost-efficient package. Compared to the monostatic transceivers introduced in Table II, this work performs favorably in terms of noise figure, power consumption, and area, due to its innovative architecture. Even with the on-chip antenna that has a gain of -1.25 dBi, the chip transmits sufficient power for close-range operation, which can be extended up to several meters by using the package with an integrated lens. The packaging concept is a simple and appealing alternative, compared to the other low-cost options like surface-mountable packages with flip-chip or embedded wafer level ball grid array packages [26], [27].

As the chip topology scales with the wavelength, the area consumption shrinks with increasing frequency. Thus, also implementations in future processes can benefit from the introduced design, enabling compact transceivers at much higher frequencies.

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