# A SiGe-Chip-Based *D*-Band FMCW-Radar Sensor With 53-GHz Tuning Range for High Resolution Measurements in Industrial Applications

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***Abstract*— The article presents a monostatic *D*-band frequency-modulated continuous-wave (FMCW) radar based on a fully integrated monostatic single-channel silicon-germanium (SiGe) transceiver (TRX) chip. The chip is fabricated in Infineon's bipolar-complementary metal–oxide–semiconductor (BiCMOS) production technology B11HFC which offers heterojunction bipolar transistors (HBTs) with an $f_T/f_{max}$ of 250 GHz/370 GHz. The monolithic microwave integrated circuits (MMICs) output signal is coupled by a fully differential substrate integrated waveguide (SIW) based coupling network. The output power at the WR-6.5 antenna flange is more than −10 dBm over a bandwidth of 37.5 GHz. For a sweep within a single-loop phase-locked loop (PLL) circuit from 174.5 to 121.5 GHz, a spatial resolution of almost 3 mm with a metallic plate as the target is achieved. The radar provides a small form factor of 2 × 4 × 5 cm$^3$ and low power consumption of 2.2 W at 5 V. Finally, the capabilities of the sensor for non-destructive testing (NDT) are demonstrated using a millimeter scanner. With radar imaging, it was possible to measure the orientation of the fiber layers up to a depth of 7.03 mm.**

***Index Terms*— *D*-band, frequency-modulated continuous-wave (FMCW), frequency synthesis, millimeter-Waves (mm-Waves), monolithic microwave integrated circuits (MMICs), radar systems, radar imaging, SiGe bipolar ICs, substrate integrated waveguide (SIW), ultra-wideband.**

## I. Introduction

HIGH precision radar sensors have become increasingly important measurement systems for industrial purposes such as tank level probing radar [1], tube extrusion, or rolling mills [2] because of their applicability in harsh environments such as dust and steam. With the advances of modern silicon-germanium (SiGe):C technologies millimeter-wave systems are developed at a higher absolute frequency while maintaining also high relative bandwidth for such applications. They offer excellent stability, precision, and spatial resolution in a compact form factor [3], [4].

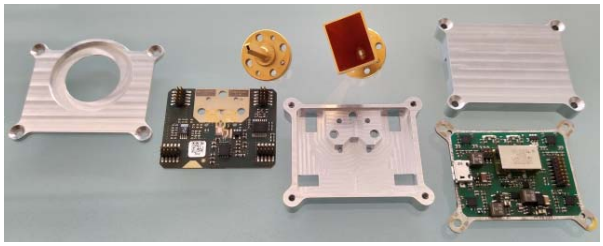

Fig. 1. Photograph of disassembled *D*-band radar consisting of separate front-end (left) and back-end (right) board and three aluminum housing parts.

Besides a carefully designed monolithic microwave integrated circuit (MMIC) at the center of the system, efficient signal radiation is also essential for excellent performance. Even at 240 GHz [5] on-chip antennas require a large part of the total chip space, which increases even more toward lower frequencies. Thus, conventional off-chip antennas become increasingly advantageous. However, microstrip line-based components on printed circuit boards (PCBs) have a high insertion loss. The substrate integrated waveguide (SIW) [6] is a low-cost, low insertion loss, and easy to integrate equivalent of the standard waveguide and thus a good solution to couple MMIC and antenna in millimeter-wave radar [7], [8] or for reference distribution and board interconnection [9] in multiple input multiple output (MIMO) radar.

In addition to conventional ranging applications, 3-D radar imaging for non-destructive testing (NDT) has been getting more attention in a large variety of applications [10]–[15]. The investigation of fiber composite materials has shown to be challenging here, because of reflections inside the profiled material and the high demand of range resolution for layer separation. As this material is used under high mechanical stress, such as wind turbines or in the aerospace sector, even small defects may lead to severe damages. Hence, the use of reliable techniques is of great importance and results in a demand for technical solutions.

Recently, we published our first radar prototype (see Fig. 1, Table I) for industrial applications in the *D*-band based on a SiGe:C MMIC [16]. With a focus on system-level and

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TABLE I
TECHNICAL SPECIFICATIONS OF mm-WAVE RADAR SENSOR

| Radar sensor type | PLL-stabilized D-band FMCW |
|---|---|
| Stabilized frequency range | 121.5 GHz to 174.5 GHz |
| FMCW ramp width | 53 GHz (35.8 %) |
| Phase noise (in-loop)* | -73 dBc/Hz @ 10 kHz |
| Phase noise* | -93 dBc/Hz @ 1 MHz |
| Output power* | -6.9 dBm @ WR-6.5 Flange |
| Antenna port | monostatic – WR-6.5 |
| MMIC / Sensor DC power | 340 mW / 2.2 W |

* measured at the center frequency

the passive millimeter-wave (mm-Wave) front-end on PCB, in this conference publication, we showed the overall excellent performance of the system in terms of range resolution due to the relative frequency tuning range (rFTR) of 35.8%. For a chirp within a single-loop PLL circuit from 174.5 GHz down to 121.5 GHz, a spatial resolution of 5.4 mm at a distance of 0.6 m was achieved. We showed that this can be further improved to 4.6 mm by waveguide dispersion compensation. Key features to achieve those results are a wideband signal generation on-chip and the efficient wideband signal transmission toward an off-chip waveguide antenna. We have shown the design and measurement results of a fully differential MMIC-to-rectangular waveguide (RWG) interface in SIW that we developed for that purpose. This article is an extended version in which we present some already published results of the *D*-band radar for a proper explanation. Additional results are added here. In particular, the novelty of the content regarding circuit design, which is backed by on-wafer measurement results, should be noted. Additionally, we present improved system results in terms of range-resolution, mainly because of a radar calibration that we performed here. The sensor's stability is evaluated over a wide temperature range of −30 °C to 70 °C. Examples for industrial applications, which are the process control in plastic tube extrusion and a 3-D radar imaging for NDT, are presented here. Even though the applications are not limited to those purposes, they show the potential of such technology in industrial applications.

The following content of this article is organized into four parts. In Section II, an overview of the system concept and its realization is given. Section III focuses on the design of the integrated transceiver MMIC. Finally, the system is characterized in Section IV and its potential in industrial applications such as in a 3-D imaging radar is shown (see Section V).

## II. SYSTEM REALIZATION

### A. System Overview

Consider Fig. 2, which shows a simplified block diagram of the presented monostatic FMCW radar in combination with a dielectric target. It consists of three main building blocks, which are the MMIC, the front-end PCB, and the back-end PCB of the radar. The MMIC is designed in the automotive-qualified production technology B11HFC by Infineon Technologies AG [18], which is a 130-nm BiCMOS SiGe:C technology with an $f_T/f_{max}$ of 250 GHz/370 GHz, respectively. It integrates a wideband fundamental Colpitts–Clapp voltage-controlled oscillator (VCO) with

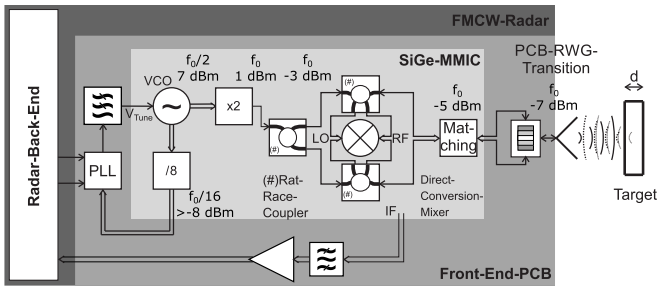


Fig. 2. Block diagram of the monostatic ultra-wideband transceiver chip stabilized in a single-loop PLL circuit in an FMCW radar system. (Taken from [17].)

a center frequency at 75 GHz [19] with a push-push frequency doubler similar to [20] and [21] at the output in the *D*-band. The single-ended frequency-doubled signal is transmitted to the differential matching network and a direct down-conversion Gilbert-cell type mixer by a local oscillator (LO)- transmitter (TX)-receiver (RX) distribution network based on three rat-race couplers. Additionally, a static divide-by-8 chain for stabilization with a commercial off-the-shelf (COTS) PLL-circuit and a temperature sensor are integrated.

The monostatic design has the benefits of a reduced board complexity and lower manufacturing costs since only a single radio frequency (RF)-interface is required. In addition, due to the identical phase center of the TX and RX channels, they can be placed in the focal point of a single dielectric lens antenna. In bi-static radar systems with a shared lens, squinting may occur because at least one feed point will not be in the focal point. The required wideband waveguide transition is directly milled into the PCB. This gives the system high flexibility. The waveguide transition and the coupling network are realized in SIW for high performance and low manufacturing costs. The PCB and MMIC are connected by bond wires. A bond wire and pad compensation network is included on-chip.

Besides the SiGe MMIC, on the front-end, the PLL circuit with an active loop filter is included. For ramp generation, the ADF4169 fractional-N frequency synthesizer with a reference frequency at 100 MHz coming from the ultralow-noise CVSS-945 reference crystal oscillator on the back-end is used. The loop filter is designed as an active filter of fourth order with a LT6202 ultralow noise operational amplifier (Op-Amp). Loop bandwidth and phase margin are carefully designed to stabilize the single loop PLL, which accompanies a high loop gain variation (35.5 to 1.9 GHz/V), over the entire band. At the center frequency of 150 GHz, the loop bandwidth is 355 kHz with a phase margin of 62°, which changes to 87 kHz and 47° at 175 GHz, or 1.1 MHz and 43.5° at 125 GHz, respectively. The fully differential received intermediate frequency (IF)-signal is amplified and bandpass filtered on the front-end PCB by a design based on an LT6203 dual-channel Op-Amp and transmitted to the back-end. The realization of the front-end is shown in Fig. 3. The power supply, digital signal processing, and triggering of the fractional ramp-sweeps are done with a radar-back-end [20] board to complete the realization of a compact ultra-wideband sensor. On the back-end, an anti-aliasing filter (AAF) of eighth order with a corner frequency of 400 kHz is included.

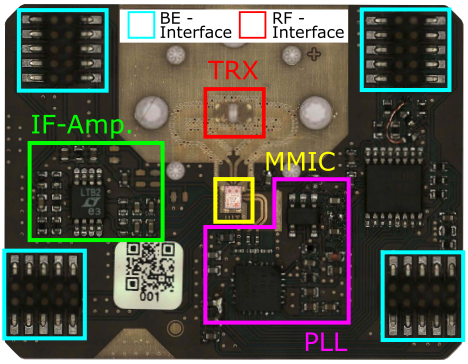


Fig. 3. Photograph of realized front-end (total dimension of 40 × 31 mm$^2$). On the board are the transceiver MMIC, the waveguide transition, PLL with active loop filter, and a first IF amplification stage included. Marked in red is the waveguide interface to the antennas and in blue are the four connectors for the back-end.

TABLE II
SUMMARY OF POWER CONSUMPTION

| | | |
|---|---|---|
| Front-end | | ≈ 550 mW |
| Radar MMIC | FHR | ≈ 340 mW |
| PLL | ADF4169 | ≈ 115 mW |
| Loop Filter | LT6202 | ≈ 45 mW |
| IF-Amp | LT6203 | ≈ 50 mW |
| Back-end | | ≈ 1500 mW |
| ADC | LTC2378 | ≈ 70 mW |
| PGA | HMC960 | ≈ 300 mW |
| AAF | LTC6362 | ≈ 50 mW |
| MCU | STM32F4 | ≈ 400 mW |
| USB PHY | SMSC3300 | ≈ 270 mW |
| VCXO | CVSS-945 | ≈ 400 mW |
| Total | | ≈ 2.2 W |

Consequently, the maximum detection distance is 6.8 m with ramp parameters of 53-GHz tuning range and 6-ms modulation duration.

Other radar systems using this back-end and similar system architecture at 80 GHz [22]–[24], 94 GHz [7], 240 GHz [5], [25], and a harmonic radar at 61 GHz/122 GHz [17] center frequency have been presented so far. The back-end contains the radar control features and power supply, such as the microcontroller (MCU), universal serial bus (USB) interface, direct current (dc)-dc converters, low-dropout (LDO) regulators, low phase noise (PN) reference oscillator (VCXO) for the MCU, and the PLL, AAF with a programmable gain amplifier (PGA), and an analog-to-digital converter (ADCs) for intermediate frequency (IF)-signal sampling. The complete radar system is powered by a single USB port and is consuming 440 mA at 5 V in total. The individual power consumption (excluding the dissipated power in LDO's, DCDC converters, and passive filters) is summarized in Table II. Without the flanged WR-6.5 standard gain horn, which is used for measurements presented here, the total dimension of the system is only 2 × 4 × 5 cm$^3$.

### *B. Front-End Design*

The front-end has been fabricated on a Rogers RT/duroid 5880. The die can be placed inside an open cavity milled from the topside on the 1-mm-thick copper plane for sufficient heat transfer. As a standardized antenna interface the *D*-band WR-6.5 waveguide is used, which is directly milled into the thick metal cladding from the top side.

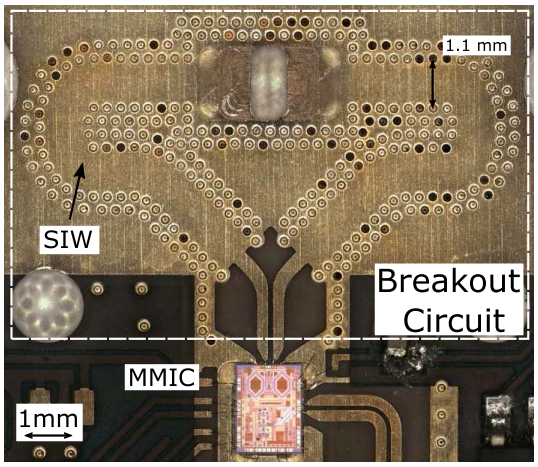


Fig. 4. Detailed view of the *D*-band radar RF-output. This includes a differential MMIC-to-PCB interface via bond wires, a transition from differential microstrip line to two separate SIW with a length of 9 mm, and a differential SIW-to-RWG transition. A WR-6.5 interface is milled into the thick metal cladding as a standardized antenna flange. (Taken from [17].)

In Fig. 4, all passive mm-Wave components on the PCB are shown. These are a transition from differential microstrip lines to two separate SIW and a waveguide transition. The differential microstrip line port is directly connected to the bond wire pads on PCB and the single-ended ports are coupling into a SIW with a cutoff frequency equivalent to the *D*-band waveguide of $f_c \approx 91$ GHz. Besides the low insertion loss even in the *D*-band, the waveguides block the fundamental leakage of the radar MMIC due to their inherent cutoff frequency. As SIW-to-RWG interface a differential adaption of [26] with a center frequency of 150 GHz for *D*-band coupling is used. It is based on a multi-section impedance transformer by milling waveguide sections of different heights and thus impedance into the thick metal cladding. For the system presented here, in contrast to previous radar systems at 80 GHz [24] or 94 GHz [7] center frequency with single-ended waveguide transitions as presented in [27] a fully differential transition is used here. The previous designs are fabricated on an identical substrate and feature a single-ended SIW interface on the PCB level. Even though they cover a sufficient bandwidth for ultra-wideband mm-Wave front-ends the major drawback is the necessity of a coupler with its frequency dependency and loss. The coupler transforms the differential microstrip line, which connects the MMIC and PCB to a single-ended topology to couple the signal into a SIW. Especially at higher frequencies a rat-race coupler or $\lambda/2$-Balun in the *D*-band is impractical due to the wide microstrip lines in comparison to the radius of such couplers on this substrate. With the fully differential design, which is discussed in [16] in more detail, the single-ended to differential conversion is not required anymore.

## III. CIRCUIT DESIGN

This circuit design chapter is divided into three parts and elaborates in detail the *D*-band SiGe-MMIC that is already presented in Fig. 2. The first part thoroughly describes the

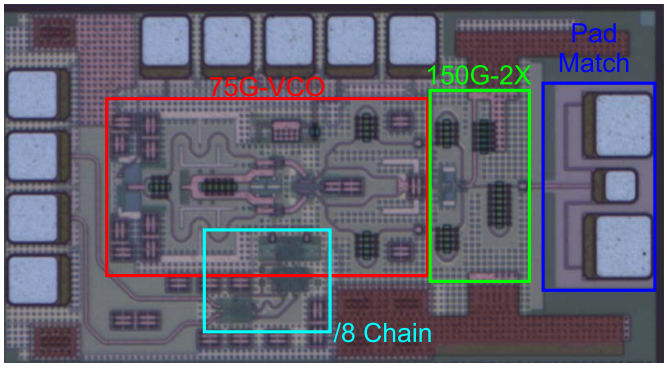


Fig. 5. Micrograph of the signal generation breakout chip with highlighted building blocks and a size of 1060 × 570 $\mu$m$^2$.

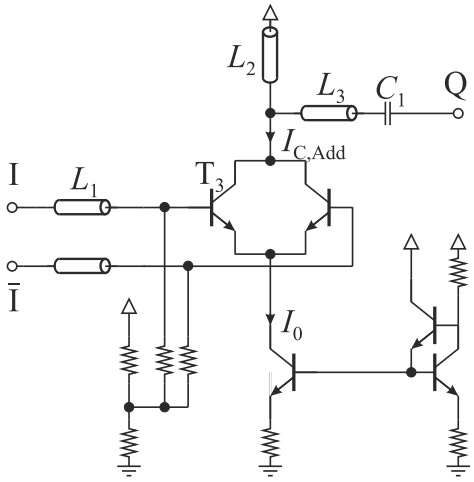


Fig. 6. Detailed schematic of the push–pull frequency doubler with biasing circuits.

signal generation of the transceiver MMIC, which is shown on the left half in the block diagram of Fig. 2 with the VCO, the frequency doubler, and the static divide-by-8 chain. This is backed up by on-wafer measurements done on a breakout chip with just these components for verification of this most critical part. The remaining components of the block diagram are given in the second part with the description of the whole transceiver MMIC. The last and closing part of this section gives a small comparison between improvements due to technology and conceptual change to the sensor in [20].

### A. Ultra-Wideband D-Band Signal Generation

The micrograph of the realized breakout chip for verification of the signal generation at *D*-band is shown in Fig. 5. Its size is 1060 × 570 $\mu$m$^2$ and is mainly defined by the pad frame needed for on-wafer characterization. The concept of the ultra-wideband 75-GHz VCO in the red rectangle of Fig. 5 is based on the Colpitts–Clapp topology that was first described in [28] with a realization in Infineons predecessor SiGe:C technology B7HF200. The realization of the here used *E*-band VCO is much more than just a copy of [28] which offered a rFTR of 30%.

The first results of this combination of the *E*-band VCO with its divider chain have already been published in [19] along with a *W*-band VCO with both demonstrating the capability of being continuously tunable over a whole waveguide frequency band. Due to the already published results in [19] and [24] the VCO and prescaler design will not be overly discussed here. Additionally to the increased tuning range from 30% to about 40%, the phase noise performance at 1-MHz offset was increased from −97 to about −99 dBc/Hz while operating at a reduced voltage supply of 3.3 instead of 5 V. This is an incredible feat considering the critical collector-base voltage of the oscillating transistors which has a beneficial effect on phase noise as well as tuning range.

A secondary impact from the new design that can be fully attributed to the technology change is the first frequency divider stage. This stage could now be realized with a static frequency divider with inductive peaking instead of a dynamic divider design with a regenerative divider topology. And due to the reduced supply voltage of 3.3 V, the efficiency of the first static divider stage is the same while gaining the stability and reliability that static dividers are known for.

The total power consumption of the chip shown in Fig. 5 is 89 mA from a 3.3-V supply. With 65 mA being consumed by the VCO and the divide-by-8 chain. This results in a total current consumption of 24 mA by the frequency doubler with its detailed schematic given in Fig. 6. The doubler topology is loosely inspired by the first comprehensively described balanced SiGe realizations from [29]. These implementations were highly tuned for efficiency at the $K_u$- and $K_a$-band, and hence are operated in class-B. While the balanced topology discussed here is biased and operated in class-AB with the $\beta$-helper current mirror topology supplying the core current $I_0$.

The output current $I_{C,\text{add}}$ can be represented as a train of rectified current pulses for the positive as well as the negative input half-wave to the differential pair $T_3$ due to shorting of both collectors. To increase the harmonic content, especially of the second harmonic, the peak values of these current pulses have to be maximized. This can be achieved by maximizing the input voltage level to the transistors of the doubler by entering large-signal operation to use much of the exponential relation between Collector-current $I_C$ and Base-emitter-voltage $V_{BE}$ of the HBTs.

Since there is no need to obey matching to 50 Ω (or differential 100 Ω) between the VCO and the doubler this additional degree of freedom was used to increase the input drive level to the doubler with the only cost being additional computational time in simulations for the optimizations. The output network of the VCO consisting of a microstrip transmission line and a metal-insulator-metal (MIM)-capacitor in series, which also offered the needed ac-coupling between the doubler and the VCO, and the input network of the doubler formed by the microstrip line $L_1$, have been optimized together. The output network of the doubler formed by the transmission lines $L_2$ and $L_3$ together with the MIM-capacitor $C_1$ have been optimized in the same simulations, to maximize the second harmonic content at the single-ended output $Q$ of the doubler. The optimal input impedance of the doubler, which was found in simulations at center frequency, is $Z_{\text{IN,Doub@75 GHz}} = 26.5\ \Omega$. This is nearly one-fourth of the

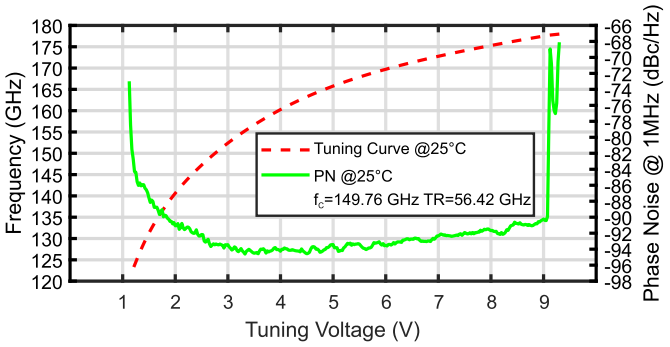


Fig. 7. Frequency and phase noise at 1-MHz offset of the breakout chip versus tuning voltage.

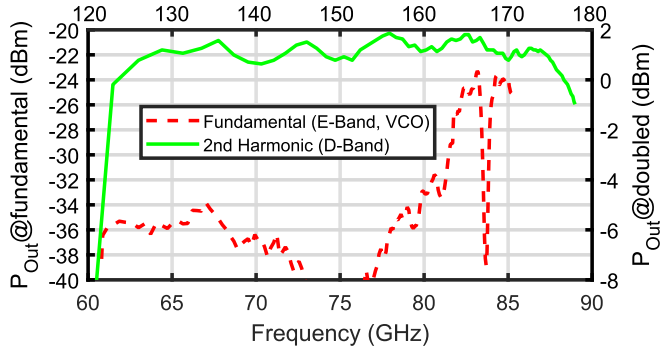


Fig. 8. Measured output power at the fundamental frequency of the VCO and at the intended doubled frequency.

differential load impedance of 100 Ω the VCO in [19] was optimized for.

The first two results of this jointly optimized signal generation block are shown with the measured tuning curve and phase noise in Fig. 7. From the measured tuning characteristic of the signal generation breakout circuit, a center frequency $f_C$ of 149.76 GHz with an absolute tuning range (TR) of 56.42 GHz can be observed. This correlates to an rFTR of 37.7%. Compared to the results presented in [19] for the standalone *E*-band VCO a reduction of 2.4% in rFTR is measured. This can be attributed to the intended mismatch for maximization of the second harmonic content between the VCO and the frequency doubler. The mismatch results in an unfavorable load impedance of the VCO which reduces the tuning range. Comparing the phase noise performance on the other hand a minimum of −94 dBc/Hz can be observed. This is 1 dB better than the mere frequency translation from −99 dBc/Hz at the fundamental frequency of 75 GHz to −93 dBc/Hz at the doubled frequency would suggest. This example shows the ever-present tradeoff between key performance indicators that every circuit designer has to face.

The next results with the measured output power of the fundamental signal of the VCO as well as the intended second harmonic are shown in Fig. 8. Considering the intended second harmonic output power, a very flat response can be seen. The small periodic ripple on the measured output power can be explained by the used *D*-band waveguide probe. Taking this into account, an output level of around 1 dBm is obtained with a variation of only 2 dB over the whole frequency tuning range, when neglecting the leftmost measured point where

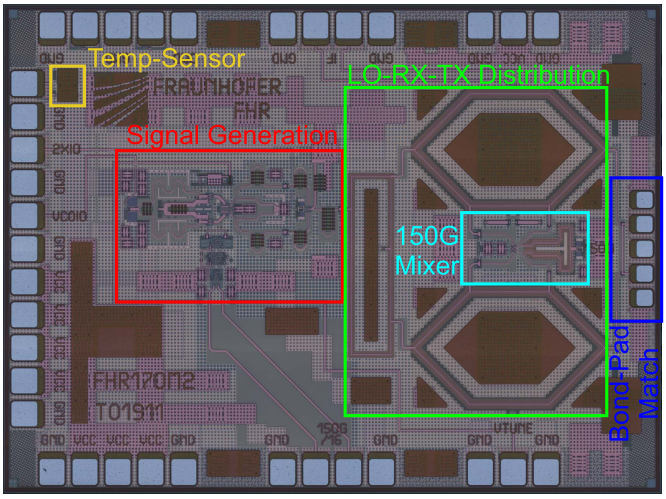


Fig. 9. Micrograph of the *D*-band transceiver chip with highlighted building blocks and a size of 1964 × 1448 $\mu m^2$.

the VCO turns off. For the measurement of the fundamental signal, the Rohde & Schwarz FSW85 spectrum analyzer in combination with a 0.8-mm coaxial probe was used to directly measure the output of the breakout circuit from Fig. 5 at the fundamental frequency. The spectrum analyzer offers a maximum direct input frequency of 85 GHz limiting the shown measurement to 85 GHz. In the measurable range, a minimum suppression of the fundamental signal of 25 dB and a suppression of more than 30 dB can be observed for frequencies below 81 GHz.

### *B. D-Band Transceiver MMIC*

For the full functionality given in the block diagram of Fig. 2 additional components to the previously discussed signal generation circuit components had to be developed and integrated into the SiGe transceiver MMIC. In Fig. 9 the chip micrograph with a size of 2.85 $mm^2$ with its highlighted circuit blocks is shown. In addition to the critical signal generation block, the needed LO-RX-TX distribution network, and the direct-down conversion mixer, a temperature sensor was also integrated onto the transceiver MMIC for functional safety purposes. The total current consumption of the transceiver MMIC is 103 with 89 mA consumed by the signal generation block (VCO, frequency divider, and frequency doubler), 12 mA by the down-conversion mixer, and an additional 2 mA by the temperature sensor.

Due to the high yield, reliability, and high level of integration possible in SiGe technologies most SiGe MMIC as well as this transceiver MMIC feature a differential topology with their many benefits. Here, the main drawback of the chosen doubler topology with its single-ended output is that it has to be converted to a differential signal again. For this purpose, one of the three rat-race or couplers from the LO-TX-RX distribution network is used directly at the output of the doubler as a balun. This rectangular rat-race coupler, which can be seen in the green rectangle of Fig. 9 in direct vicinity to the red signal generation rectangle, is fed by the doubler. One output is connected to the upper hexagonal rat-race coupler. The 180° phase-shifted output is connected

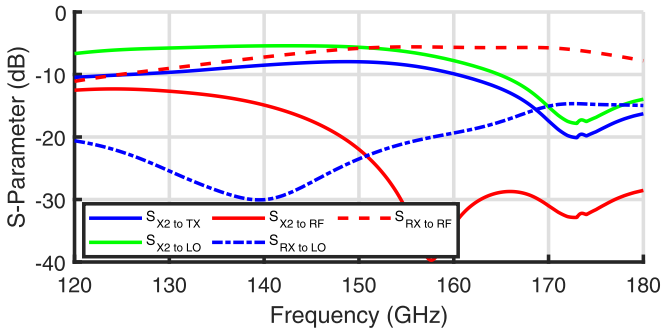


Fig. 10. S-Parameter simulation of coupling network on MMIC and bond wire interface to PCB.

to the lower hexagonal rat race. The common-mode port is unused and terminated by a 50-Ω TaN-resistor on-chip.

Both hexagonal rat race couplers are used as splitters dividing the now differential signal from the signal synthesis block into the LO signal for the mixer and the TX signal while the isolated port is connected to the RX port of the mixer. Seen from the input–output interface into the differential rat-race couplers the received signal is split into the RX signal for the mixer while the LO input of the mixer is now at the isolated port of the rat-race couplers. One drawback of this chosen topology or mainly of the chosen monostatic approach is of course the loss in receive input level of 3 dB due to this splitting. This directly degrades the noise figure (NF) of the RX by at least 3 dB, but this is still a very smart approach when a monostatic interface is necessary.

All rat race couplers are implemented with microstrip transmission lines with a characteristic impedance of $\sqrt{2} \times 50\ \Omega$. They are designed straightforward with six $(\lambda/4)$ transmission lines at 150 GHz. Both types, the rectangular and hexagonal, are verified by simulations with the 2.5-D EM simulator Sonnet. The simulated losses of the stand-alone rat-race couplers are around 1 dB. The simulated results of the entire distribution network are shown in Fig. 10. The differential ports that are connected to the mixer on the TRX MMIC are terminated with 100 Ω in this simulation. At the center frequency, the insertion loss from the doubler-output to LO-input is 5.6 and 8 dB to the PCB. While the isolation from the doubler-output to RF-input of the mixer is better than 20 dB above 148 GHz, it decreases to 12 dB at 120 GHz. Considering the 2-dBm output power of the frequency doubler from Fig. 8, the mixer had to be designed for an RF-input level of $-10$ dBm without severe degradation of its NF. In a monostatic design, a high input compression point is required anyway due to reflections of the transmitted signal in the coupling network toward the antenna (e.g., bond-compensation network, passive couplers on PCB, or antenna in-/output).

Fig. 11 shows the detailed schematic of the down-conversion mixer that directly converts the RF signal to the IF signal. Due to the intended FMCW operation of the radar, the IF frequency can be sampled directly by an ADC and the impact of flicker noise on the systems signal-to-noise ratio (SNR) is negligible. The chosen architecture shares similarities with the classic Gilbert-Cell [30] but at the RF input the differential pair is omitted due to the limited

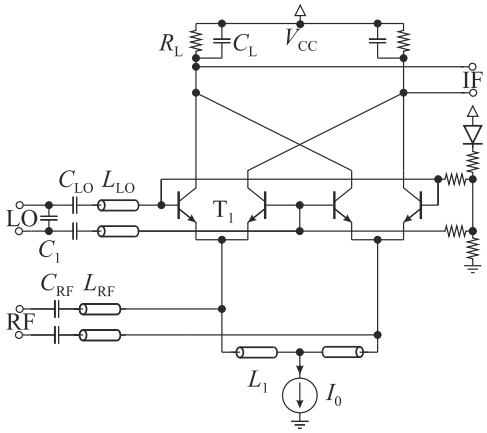


Fig. 11. Detailed schematic of the $D$-band down-conversion mixer, which shares the same current mirror topology as the doubler circuit.

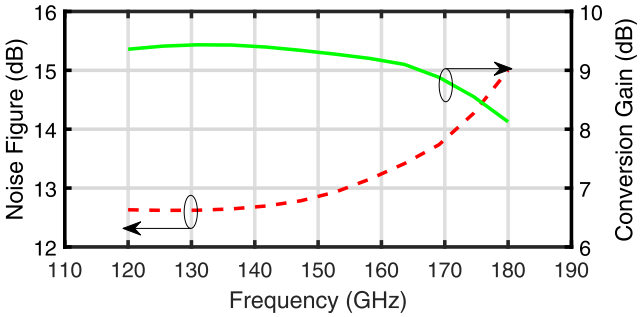


Fig. 12. Simulated results for conversion gain and single-sideband NF of the standalone $D$-band mixer from 120 to 180 GHz at an IF of 1 MHz.

maximum available gain at the chosen operating frequency of the available HBTs. Only the switching quad that is needed for the frequency translation by applying a large LO signal at the bases is implemented and optimized here.

Both inputs, LO and RF, are matched with passive networks by using the available MIM-capacitors ($C_1$, $C_{\mathrm{LO}}$ $C_{\mathrm{RF}}$) from the technology and microstrip transmission lines ($L_{\mathrm{LO}}$, $L_{\mathrm{RF}}$). Since no input differential pair is used, additional decoupling of the core current source $I_0$ has to be applied. This is realized with transmission lines $L_1$, which have nearly a length of $(\lambda/4)$. The core current $I_0$ of 10 mA is supplied by the same $\beta$-helper current mirror topology as the doubler uses in Fig. 6. At the output, the first filtering with a low-pass $RC$-filter is used as an on-chip load of the mixer cell.

The simulated performance of the designed D-Band mixer is given in Fig. 12. The conversion gain of the mixer is quite flat over the simulated frequency range from 120 to 180 GHz with a variation of less than 2 dB and a maximum gain of about 9.4 dB. The single-sideband NF ($\mathrm{NF_{SSB}}$) shows a higher variation especially for frequencies above 150 GHz but the variation stays below 2.5 dB with a minimum NF of about 12.6 dB. Especially, when compared to a more classic Gilbert-cell realization at half the operating frequency in the same SiGe technology [24] with an NF of about 10 dB at mid-band these results prove to be quite good. This is mainly achieved by omitting the input differential pair.

The last open part on the MMIC is the integrated temperature sensor. The temperature sensor itself is not a temperature

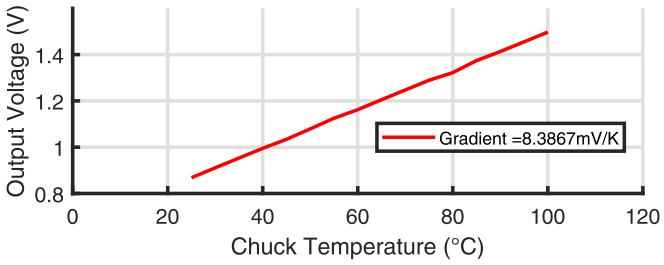


Fig. 13. Measured temperature dependence of the used Brokaw-cell as a temperature sensor.

sensor per se but a Brokaw bandgap reference cell [31]. The main intention of this voltage reference is the use as an integrated low-dropout regulator for future digital control circuitry that can be integrated due to the BiCMOS nature of the used SiGe technology but needs a supply voltage of 1.2 V. Since the Brokaw-cell generates a proportional to absolute temperature (PTAT) voltage to compensate the temperature behavior of $V_{\mathrm{BE}}$ it can also be used to sense the on-chip temperature. The total power consumption of the cell is about 2 with 1 mA alone by loading the 1.2-V reference output with a 1.2-kΩ resistor on-chip for stabilization.

Fig. 13 shows the measured temperature behavior of the temperature sensor on the transceiver MMIC. The output voltage at the output pad of the sensor is amplified and shifted on-chip to a more suitable output level for sampling with a simple ADC from a COTS MCU yielding a gradient of roughly 8.4 mV/K in a temperature range from 25 °C to 100 °C.

### *C. Comparison of Technology and Conceptual Impacts*

The presented MMIC in [20] manufactured in Infineon's B7HF200 technology is quite similar to the one presented in this work but in a slower or older technology. This gives an opportunity to shortly analyze improvements that can be gained from a technology change and a conceptual change. The main design criteria and methodology in this work is to achieve the same level of performance as [20] without the offset mixing concept with two PLLs at a lower supply voltage of 3.3 instead of 5 V.

The HBTs used in the B7HF200 technology offer transit frequencies $f_{\mathrm{T}}$ of up to 170 GHz and a maximum oscillation frequency $f_{\mathrm{max}}$ of up to 250 GHz. The B11HFC technology that is used here offers a $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 250 GHz/370 GHz. This relates to a nearly 50% faster technology from $f_{\mathrm{T}}/f_{\mathrm{max}}$ point of view. Just considering the VCO and doubler part of both works, the technology benefit is directly translated into a power consumption reduction to 62% ($\mathrm{P_{dc,VCODoub,B11HFC}} =$ 208 mW, $\mathrm{P_{dc,VCODoub,B7HF200}} =$ 338 mW). The main reason for this is the conceptual change from a 5-V supply within B7HF200 to a 3.3-V supply within B11HFC. Even with this reduction, the same output power and phase noise levels have been achieved while the rFTR has been increased from 31.9% to 37.7%.

Comparing the prescaler stages from [20] to this work, the technology change allowed for a conceptual change from a regenerative miller divider topology to a more reliable static divider topology at the same level of efficiency and frequency.

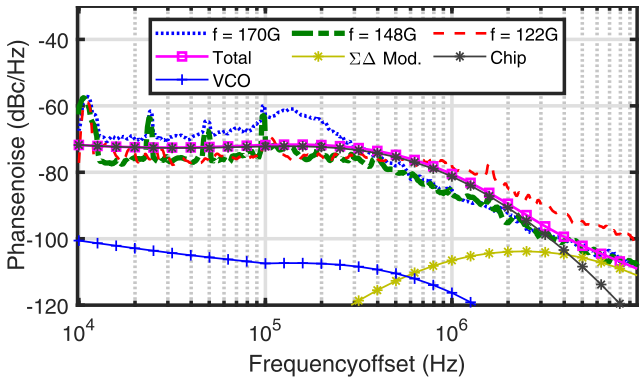


Fig. 14. Measurement results of the radar system's PLL-stabilized phase noise at the WR-6.5-WG-flange for different frequencies in comparison to simulation results (solid lines) at 148 GHz.

As a last short comparison, the down-conversion mixer is worthy to note. At 62% power consumption (B7HF200 65 mW; B11HFC 40 mW) compared to [20] the maximum single-sideband NF is decreased from 19.3 dB to below 15 dB at 180 GHz. In part, the reduction can be explained by the smaller base resistances from the faster technology but the main part can be explained by the conceptual change by omitting the input differential pair from the classic Gilbert-Cell topology.

## IV. System Measurement Results

In this section, the system is characterized by multiple measurements. First, results of the signal source taken with laboratory equipment are shown. Then, the quality of the IF-signal characterizing the entire system is shown.

### *A. TX Signal*

In Fig. 14, the measured phase noise of the PLL-stabilized VCO at different frequencies and the simulation results at the center frequency are shown. The phase noise is measured with a WR-6.5 harmonic mixer flanged to the systems antenna interface. At a center frequency of 148 GHz and at the lower end of the stabilizable region at 122 GHz, the in-loop phase noise is below −73 dBc/Hz. Toward the upper end at 170 GHz the minimum increases to −60 dBc/Hz at around 13-kHz offset frequency because of the high loop-gain variation. The simulated phase noise at 148 GHz is slightly higher than the measurement but overall coincides well with the measurement results. As can be seen from the noise contributions, the phase frequency detector (PFD) noise of the PLL-Chip is dominating the noise floor within the loop bandwidth. The phase-noise contribution from the VCO is negligible. For an application with better phase noise requirements, a design with an improved PLL IC should be considered.

Next, the output power at different stages of the transmitter, and the insertion loss of the coupling networks on PCB and MMIC are shown in Fig. 15. The power measured at the WR-6.5 waveguide flange $\mathrm{P_{Meas.RWG}}$ ranges from −6.6 to −9.6 dBm within a frequency range of 127.5 to 165 GHz. When compared to the constant measured output power of the frequency doubler on-chip $\mathrm{P_{Meas.X2}}$ (cf. Fig. 8), at a center frequency of 148 GHz, the coupling LO-TX-RX distribution

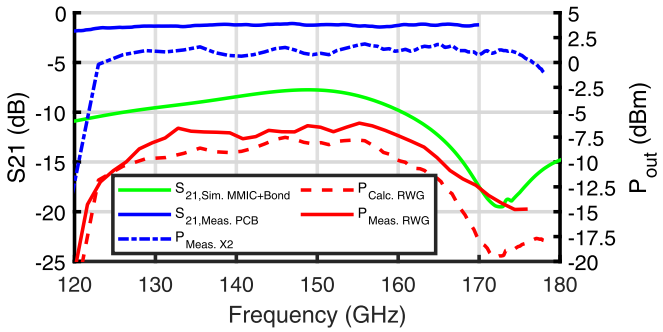


Fig. 15. Output power of the system measured at the WR-6.5 flange and insertion loss of coupling network on PCB $S_{21,Meas.PCB}$ (see Fig. 4) and MMIC+bond wire $S_{21,Est.MMIC+Bond}$.

network reduces the output power by 7.5 dB. The coupling toward the LO-input is contributing 3 dB and is consequently inevitable. As expected the output power is lower toward the tuning range limits but especially at the upper end a fairly wide stabilizable frequency range with a low output power of only −15 dBm is measured. The bandwidth of the fully differential MMIC-to-RWG interface on PCB $S_{21,Meas.PCB}$ (see the area marked as breakout circuit in Fig. 4) is exceeding the tuning range sufficiently and cannot be the reason here. Within the frequency range of 120 to 170 GHz the insertion loss is 1.9 to 1.1 dB and varies only by 0.2 dB in the output power referred 3-dB bandwidth of the sensor (from [16]). As can be seen in the figure, the reduction of output power at the upper end of the frequency range can be explained by the frequency dependency of the coupling network on MMIC and the bond wires $S_{21,Sim.MMIC+Bond}$. It consists of the rat-race coupler, the LO-RX-TX distribution network, the bond wire and pad, and the corresponding matching network. The calculated output power

$$P_{Calc.RWG} = P_{Meas.X2} + S_{21,Sim.MMIC+Bond} + S_{21,Meas.PCB} \quad (1)$$

is around 1–2 dB lower than measured, but besides that matches well to the measured results. This means that the loss contributions in the simulation are modeled too pessimistic.

For high accuracy measurements with a high range resolution not only the bandwidth but also the ramp linearity is an important figure of merit [32], [33]. Especially in a single-loop PLL, the high loop gain variation may degrade the radar performance substantially. These frequency errors are dependent on the ramp slope. In Fig. 16 the measurement results of down-ramps with 6- and 1-ms modulation duration are shown. The ramp is measured with 25 GS/s with the Tektronix DPO77002SX oscilloscope and P77BRWSR differential probe at the differential microstrip line that connects the divide-by-8 output of the radar MMIC (which corresponds to a divide-by-16 ratio when referred to the radar RF signal) and the RF input of the PLL-chip. The sampled time signal is processed to the frequency-domain to represent the ramp-frequency vs. ramp-time. A moving averaging with a window of 60 $\mu$s for the 6-ms ramp and a 10-$\mu$s window for the 1-ms ramp is applied to suppress high-frequency noise. When compared to an ideal ramp, it becomes clear that the frequency error for the slower 6-ms ramp is less. Here, after a settling time of

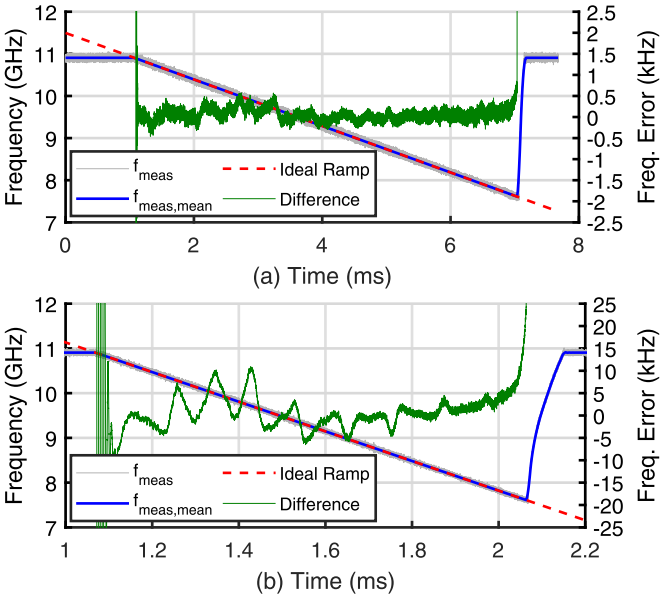


Fig. 16. Frequency of FMCW down-ramp measured at the divide-by-16 output for a ramp duration of (a) 6 ms and (b) 1 ms with 53-GHz tuning range (≈ 3.31 GHz at the divider output). The frequency error is determined by the difference to an ideal ramp with corresponding slope. The RMS error is 137 Hz for the 0.552 GHz/ms and 3.254 kHz for the 3.31-GHz/ms ramp.

30 $\mu$s, the frequency error is less than 0.5 kHz. The peak overshoot is 15 kHz. The RMS error is 137 Hz when the first and last 1% of the chirp is excluded. With the 1-ms ramp, the system achieves a frequency error of less than 11 kHz after a settling time of 53 $\mu$s and a peak overshoot of 534 kHz. The RMS error is 3.254 kHz, with 5% excluded at start and end. These results are comparable with automotive radar systems that use dual-loop architectures for loop gain linearization [34] and therefore enable high precision measurements with high range resolution as will be shown in Section IV-B.

### *B. IF Signal*

Overall, the discussed characteristics influence the quality of the sensors' frequency response as can be seen in Fig. 17(a). Here the time-domain representation of a single down-ramp from 174.5 to 121.5 GHz in 6 ms is shown. A 20-dBi standard gain horn is used as an antenna and the radar target is a metallic plate at a distance of 0.6 m. One can observe a reduction of amplitude toward the frequency limits with significant reduction at higher frequencies. This coincides with the system's output power. The oscillation corresponding to the radar target is superimposed by low-frequency components of which the strongest contribution results from antenna mismatch.

In Fig. 17(b) the corresponding frequency-domain representation of the signal re-normalized to 0 dB is shown. The dynamic range is more than 70 dB for this configuration. For sidelobe level reduction, a Tukey window function ($\alpha = 0.25$) is used. The comparison [see Fig. 17(c)] of the peaks for different ramp slopes shows only a small influence on the position and −6-dB width. Relative to the measurement at 6 ms, the peak for a duration of 1 ms is shifted by 244 $\mu$m, and for a duration of 16 ms by 217 $\mu$m in this setup. The smallest achievable range resolution of a FMCW radar, with

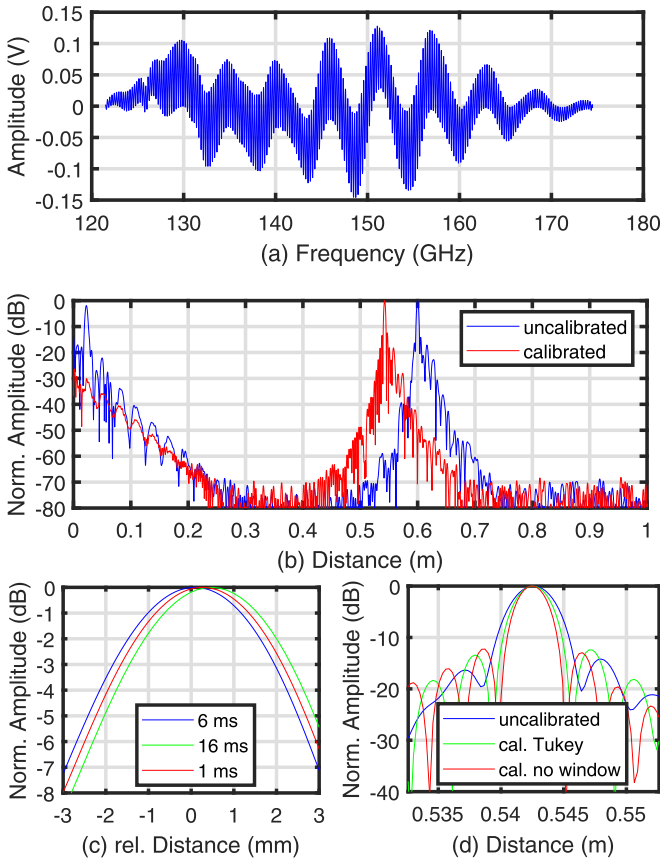


Fig. 17. (a) Uncalibrated IF signal with metallic plate positioned at a distance of around 0.6 m for a down-chirp of 53-GHz bandwidth in 6 ms. (b) Corresponding uncalibrated and calibrated frequency-domain representation. For decreased sidelobe level a Tukey window ($\alpha = 0.25$) is applied. (c) Comparison of peak for different ramp durations relative to 6-ms ramp. (d) Comparison of peak with a ramp duration 6 ms for calibrated and uncalibrated measurement.

a modulation bandwidth BW that is given by

$$\Delta R = \frac{c_0}{2 \cdot \mathrm{BW}} \cdot 1.38. \tag{2}$$

Harris [35], is 3.9 mm. With a ramp duration of 6 ms, the uncalibrated system achieves a resolution of 5.428 mm as a result of amplitude taper, waveguide dispersion in SIW and RWG, and ramp nonlinearity. The resolution changes by less than 10 $\mu$m (5.427 mm at 1 ms and 5.421 mm at 16 ms), which shows that the ramps are sufficient linear and not the dominating factor that impacts the reduction in range resolution. In [17] we have shown that the resolution of this system can be further increased to 4.6 mm by analytically compensating waveguide dispersion by the complex transfer function. As shown in Fig. 17(b) and (d), with a calibration [15] that characterizes the frontend, the resolution is improved to 3.84 mm. Without the window function, the radar achieves a resolution of 3.264 mm. The calibration factor was measured in a different measurement setup after re-assembling the system, which also shows the robustness of this method. The range is calibrated toward the tip of the standard waveguide horn. This results in a shift of the measured distance since in the uncalibrated measurement the time delay of the entire frontend is included. We note that this

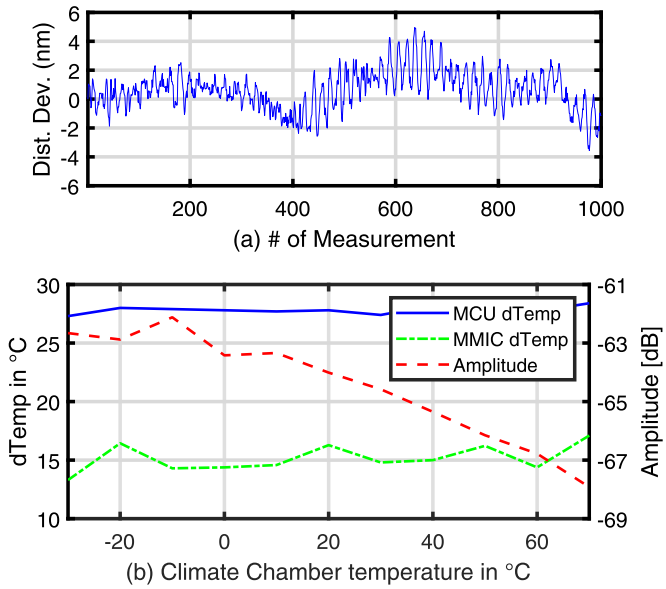


Fig. 18. (a) Distance deviation of the system over 1000 measurements to the same target at room temperature and measured distance at −30 °C, 20 °C, and 70 °C. (b) Measured temperature difference of sensor on MMIC and MCU to temperature in climate chamber and influence on amplitude.

is crucial for imaging purposes (cf. Section V-B). In addition, the strong reflection of antenna mismatch is shifted to negative distances and hence not shown in the graph. In Fig. 18(a), the measured range of 1000 consecutive measurements at an ambient temperature of 20 °C with a pulse repetition frequency of 100 Hz is shown. The distance deviation lies within an excellent range of only 8.5 nm. The standard deviation is only 1.36 nm. In industrial applications, the stability over temperature is also of importance. Thus, the radar performance over temperature is evaluated in a climate chamber over the temperature range from −30 °C to +70 °C. For highly accurate measurements over a wide temperature range, the dependency of the measurement setup or the system needs to be compensated. The measured results on MMIC and in MCU are shown in Fig. 18(b). The temperatures have a constant offset with a mean value of 15.2 °C on MMIC and 27.8 °C in MCU when compared to the climate chamber temperature. The amplitude decreases by 5.3 dB from −30 °C to 70 °C. In contrast to previous measurements, here an open waveguide antenna with a gain of only 9 dBi is used, which explains the low amplitude. The low gain antenna is used to make sure the receiver is operated in the linear region.

## V. Industrial Applications

### A. Tube Extrusion for Plastic Materials

The first industrial application this sensor's capabilities are evaluated for is in the field of contactless process control of tube extrusion. A precise measurement of the material thickness of large plastic pipes is essential here. As the resolution of the sensor limits the lower limit for layer separation, high bandwidth is necessary. The high available spectrum in the D-Band makes this technology an ideal solution.

In Fig. 19 the measurement results and the related setup are shown. The compact sensor with a standard gain horn

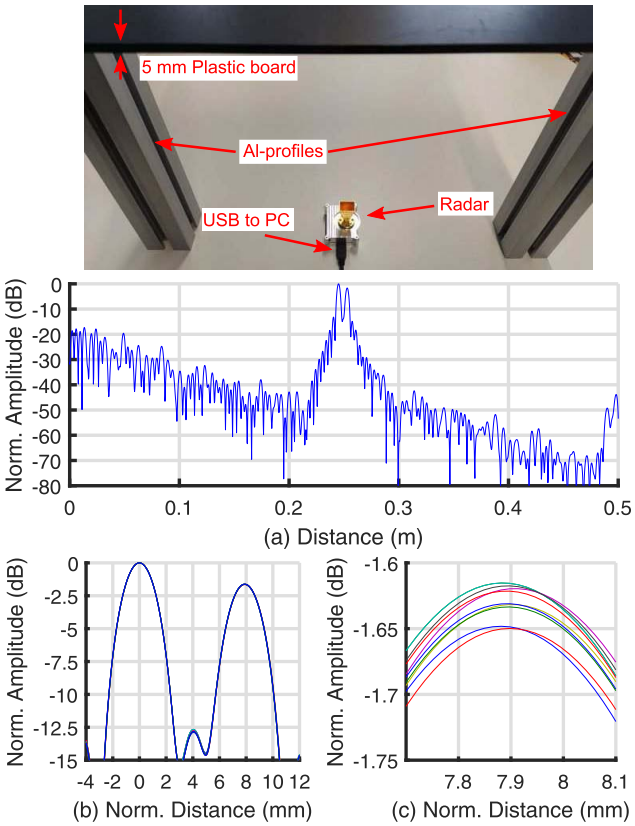


Fig. 19. Measurement setup to measure the thickness of plastic boards with a thickness of around 5 mm. The radar system is positioned on a table with a plastic board placed on top of two aluminum profiles. (a) Spectrum of the calibrated IF-signal. (b) Superposed results of board moved with linear track from 25 to 30 cm normalized to maximum position. (c) Zoom into second peak.

is directed at a plastic board with a thickness of approximately 5 mm. Due to the high available sweeping bandwidth, two reflections are easily separated at a distance of approximately 0.25 m. The amplitude in between the plastic board surfaces goes down by more than 12 dB. As a result of the permittivity, the plastic-to-air interfaces appear at a relative distance of 7.88 mm. The −6-dB width with a Tukey window is 3.94 mm. This proves that the prototype radar system can separate the reflections at both surfaces of this plastic board. Considering the −6-dB width even thinner boards should be possible. In Fig. 19(b) the superposed peaks of the plastic board in a distance from 25 to 30 cm (step size 5 mm) are shown. The results are barely distinguishable on this scale. In Fig. 19(c) a closer look into the second reflection shows a thickness variation of fewer than 30 $\mu$m.

### *B. 3-D Radar Imaging of Fiber-Composite Materials*

Next, we want to show the capabilities of the new sensor in terms of imaging quality. To this end, we consider an application from NDT of fiber composite materials arising in the manufacturing of wind turbine blades. As even small cracks and imperfections may compromise the resulting material and may cause expensive damages, an important issue consists here in inspecting the glass fiber layers during the manufacturing process. Still, nowadays this is in general done by sight-proof, such that only surface layers may be

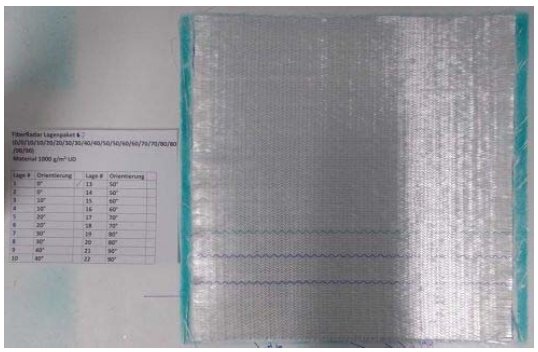

Fig. 20. Test sample of fiber layers with fiber orientations $2 \times 0°$, $2 \times 10°, \ldots, 2 \times 90°$.

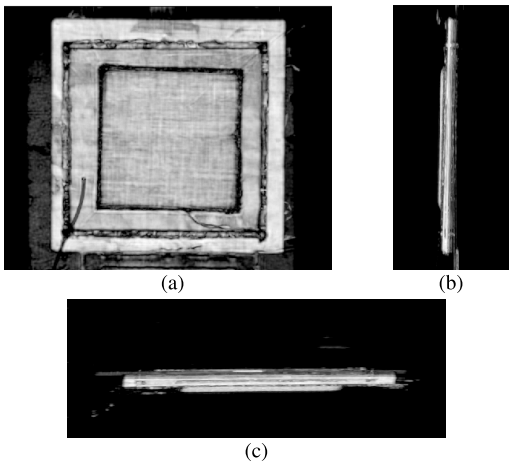


Fig. 21. Radar images (maximum projections), (a) front view, (b) side view, and (c) view from above.

investigated. Due to the increased range resolution, one can significantly improve the detection of defects in the different layers which are in general of less than 1 mm of thickness. We note that the refraction additionally improves the range resolution inside the material.

At first, we recall that the radar image itself consists of the fusion of single measurements by the creation of a corresponding aperture. In the present case, this is achieved by moving the radar sensor on a defined trajectory which leads to synthetic aperture radar (SAR) imaging. In the optical setting, SAR imaging corresponds to a focal lens with an optical aperture. However, the focusing is in our case achieved digitally by a corresponding reconstruction algorithm. In the present case, we use an improved back-projection algorithm to minimize the effects of the refraction inside the material, see [36], [37]. We note that the refraction in the uncompensated case leads to blurring effects and a false range information.

To show the capabilities of radar imaging to distinguish the different layers we used a test sample consisting of 20 fiber layers with different fiber orientations ($2 \times 0°$, $2 \times 10°, \ldots, 2 \times 90°$), cf. Fig. 20. For the measurement, we used the radar module with a standard gain horn antenna with a half-power beamwidth of $\theta \sim 18°$, which gives the cross-range resolution

$$\Delta x = \Delta y \sim \frac{\lambda}{4 \sin\left(\frac{\theta}{2}\right)} \sim 3.24 \text{ mm}. \tag{3}$$

TABLE III
COMPARISON OF WIDEBAND mm-WAVE RADAR SENSORS

| Reference, Year | Tech. | Tx-/Rx-Channels* | Antenna Type | Freq. (GHz) | BW (GHz) | rFTR (%) | $\Delta$R (mm) | $P_{EIRP} \approx$ (dBm) | $P_{DC,MMIC}$ (mW) | $P_{DC,System}$ (W) |
|---|---|---|---|---|---|---|---|---|---|---|
| [22], [23], 2018 | SiGe 180 nm | 1 | RWG | 80 | 25 | 31.1 | 7.12 | 25 | 488 | 3 |
| [24], 2020 | SiGe 130 nm | 1 | RWG | 80 | 32.1 | 39.95 | 5.81 | 26 | 254 | 2.09 |
| [39], 2017 | SiGe 130 nm | 1/1 | AiP | 122 | 6 | 4.9 | | 14[&] | 540 | |
| [40], 2019 | CMOS 28 nm | 1/1 | on-chip | 145 | 13 | 8.97 | 11 | 11.5 | 500 | |
| [41], 2021 | CMOS 28 nm | 1/1 | on-chip | 145 | 13 | 8.97 | 30 | 11.6 | 500 | |
| [20], 2014 | SiGe 180 nm | 1 | RWG | 146 | 48 | 32.8 | 5.88 | 11 | 640 | 3.75 |
| [42], 2017 | SiGe 130 nm | 1/1 | on-chip | 156 | 16 | 10.3 | 9.7 | 40[&] | 360 | |
| [43], 2014 | CMOS 65 nm | 4/4 | AiP | 161.4 | 7 | 4.3 | | 18.8 | | 2.2 |
| [44], 2020 | SiGe 130 nm | 1/1 | on-chip | 168 | 20 | 11.8 | 21 | 15 | 1050 | |
| [44], 2020 | SiGe 130 nm | 1 | on-chip | 169 | 20 | 11.8 | 21 | 8 | 860 | |
| [45], 2017 | SiGe 130 nm | 1 | on-chip | 168.3 | 27.5 | 16.3 | 7 | 16.2 | 67 | |
| [46], 2019 | SiGe 55 nm | 1/1 | on-chip | 221.1 | 62.4 | 28.2 | 2.7 | 14[&] | 87 | |
| [5], 2019 | SiGe 130 nm | 1/1 | on-chip | 224 | 52 | 23.2 | 3.2 | 25[&] | | 3.5 |
| [47], 2016 | SiGe 130 nm | 1 | on-chip | 240 | 60 | 0.25 | 2.6 | 30[&] | | 1.6 |
| [16], 2021 | SiGe 130 nm | 1 | RWG | 148 | 53 | 35.8 | 4.6 | 10 | 340 | 2.2 |
| **[This], 2022** | SiGe 130 nm | 1 | RWG | 148 | 53 | 35.8 | 3.264 | 10 | 340 | 2.2 |

* Single digit values represent channel number of monostatic systems and the dash-separated numbers represent channel count of quasi-monostatic, bistatic, or multi-static systems with first digit being number of TX-channels and second digit number of RX-channels (TX/RX). [&]not explicitly given

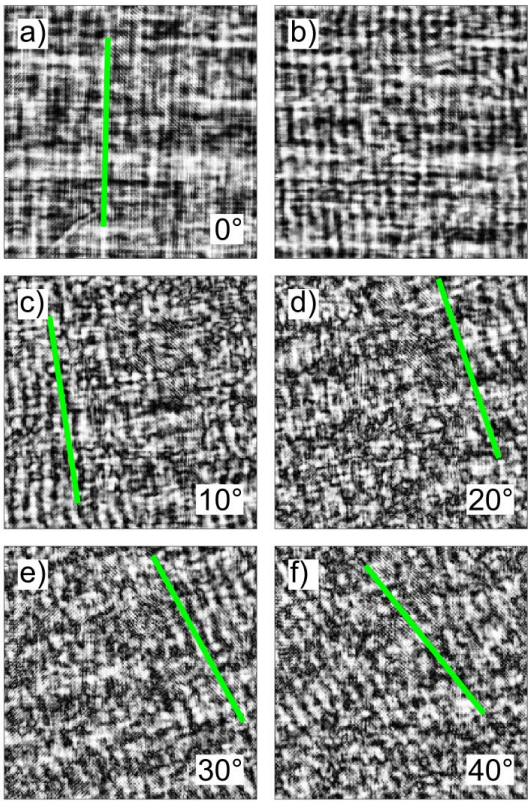


Fig. 22. Fiber Layers for different depths: (a) 0 mm (surface), (b) 1.41 mm, (c) 2.81 mm, (d) 4.22 mm, (e) 5.63 mm, and (f) 7.03 mm.

The opening angle of the antenna acts as a natural AAF, such that the spatial sampling rate of the aperture may be increased, and hence, the data volume may be reduced. From (3) we obtain due to the low wavelength a sufficiently small cross-range resolution. For the measurement itself, we put the sample in front of a wooden plate and placed a vacuum bag over the sample. The bag was sealed and the air drawn out by a vacuum pump. This technique is, e.g., used for vacuum-assisted resin transfer molding (VARTM) to manufacture wind turbine blades [38]. Before the real manufacturing process, the resin is led in, it is crucial to check that the corresponding fiber lays are oriented correctly. To this end, an SAR measurement has been performed [see Fig. 21(a)–(c)].

To distinguish the layers, we applied a refraction compensation method from [36]. In Fig. 22(a)–(f) the different layers with the corresponding fiber orientations are shown. To increase the contrast we applied a histogram filtering. One may distinguish the orientations of the different layers up to a depth of 7.03 mm. Then the images become compromised with higher depth due to possible artifacts from lower layers.

## VI. CONCLUSION

In this article, we presented a monostatic *D*-band FMCW radar based on a fully integrated monostatic single-channel SiGe transceiver chip.

The signal source on MMIC features a wide tuning range of 56.42 GHz (rFTR = 37.7 %) at 149.76-GHz center frequency. A constant output power of around 1 dBm over the whole tuning range is achieved. With the LO-TX-RX coupling network and bond wire and pad compensation network on the chip, an output power at the output of the MMIC of around $-5$ dBm is realized. The MMIC's output signal is coupled by a wideband fully-differential SIW based coupling network with a measured insertion loss of 1.9 to 1.2 dB. Thus, a constant output power of more than $-10$ dBm over a bandwidth of more than 37.5 GHz is measured at the system WR-6.5 antenna flange. For a chirp within a single-loop PLL circuit from 174.5 GHz down to 121.5 GHz an excellent spatial resolution of 5.4 mm at a distance of 0.6 m is achieved. This is further improved to 3.264 mm (or 3.84 mm when a Tukey window for reduced sidelobe level is used) by performing a radar calibration. The radar performs well when compared to the current state of the art (see Table III). Due to the high rFTR of $\approx$ 35.8 % at a center frequency of 148 GHz, the high absolute bandwidth of 53 GHz can compete with systems with higher center frequencies also. In the literature, to the best of the authors' knowledge, the rFTR is only excelled by this

system's lower-frequency sibling in the *E*-Band. Even though the peak output power is only around −6.6 dBm measured at the WR-6.5 antenna a high dynamic range of more than 70 dB is measured with a metallic plate at a distance of 0.6 m.

The achieved results and proven concept enable the exploration of a wide range of industrial applications in the *D*-Band. In two use cases, we presented the potential. First, in industrial tube extrusion, where the thickness of the plastic layer is of importance. Here the system can separate the reflections of both material-to-air interfaces with ease. Second, in a radar-imaging example, we showed that this sensor can identify the orientation of hidden fiber layers. This shows that this radar technology can be a solution for automated NDT and quality assurance.

## ACKNOWLEDGMENT

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