Quasi-Load Insensitive Doherty PA Using Supply Voltage and Input Excitation Adaptation

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***Abstract*— This article presents a quasi-load insensitive (QLI) Doherty power amplifier (DPA). The proposed theory makes the amplifier load insensitive in terms of output power, while its efficiency is slightly degraded for complex loads. The load insensitiveness is achieved by dynamically changing the supply voltages (V_{DD}) and the input power splitting for both the carrier and peaking transistors. The optimal, load-dependent, V_{DD} values are theoretically derived from back-off (BO) and full power conditions using load line theory. The optimal input excitation signals for the carrier and peaking devices are also derived for these variable V_{DD} conditions. A 3.6-GHz QLI DPA was designed, and a complete system, composed of the DPA output stage, a two-channel medium power driver, an adaptive input driving stage, and a load sensing system, was implemented. The laboratory measurements have been performed for loads distributed inside a 2.0 maximum voltage standing wave ratio (VSWR) circle and show an output power variation between 43.8 and 42.6 dBm and a BO efficiency between 50% and 35%. Under modulated signal excitation, for the worst case loads, the peak output power capability of the DPA is improved from 41.7 to 43.1 dBm, and the average efficiency is increased from 32.6% to 43%.**

***Index Terms*— Doherty power amplifier (DPA), load insensitivity, power amplifier (PA), supply voltage modulation.**

I. Introduction

POWER amplifiers (PAs) are used for various applications, and their performance has a considerable impact on the overall system operation. Normally, PAs are designed to operate with a fixed output load. However, they can be forced to operate under varying load conditions due to various causes and in different scenarios, such as microwave cooking [1], plasma heating in, e.g., plasma-enhanced chemical vapor deposition (PECVD) processes [2], or in the charging of particle accelerators cavities [3]. In telecommunication applications, the PA output load can also change due to moving objects on the antenna proximity, e.g., the hand effect [4], or also due to mutual coupling between different antenna elements on fifth-generation (5G) massive multiple-input multiple-output (MIMO) base stations (BSs) with beamforming capabilities [5].

In this nonoptimal regime, the PA performance is degraded, mainly in terms of output power, drain efficiency, and linearity. In order to compensate for this performance degradation, various techniques have been proposed during the last years. Using tunable matching network (TMN) techniques, such as switched variable length stubs [6], varactors [7], or switched capacitors [8], [9], on the PA output matching network (OMN) is one possibility. However, these techniques, being based on variable components, result in an increase in the output losses of the PA, reducing its efficiency. Moreover, it can be difficult to design the required variable elements for higher power applications, and the design complexity of the OMN becomes much higher. Other techniques are based on the PA supply voltage (V_{DD}) variation, which can be very attractive with modern dc-to-dc converters that are highly efficient and can provide high output power. Paul *et al.* [10] use a combination of adaptive power supply and adaptive impedance tuning to compensate for load variations and also to increase back-off (BO) efficiency when lower output power levels are required. However, the load compensation is still mainly based on TMN techniques with the previously introduced disadvantages. In [11], a load-dependent supply voltage was derived and successfully used to reduce the maximum output power variation of single-ended PAs under load varying conditions. However, the efficiency is not compensated, even reduced in some cases, due to the power dissipated in the dc-to-dc converter.

Although many of the described techniques are effective and have been proven for single-ended PAs, in modern telecommunication applications dealing with high peak-to-average power ratio (PAPR) signals, this should be extended to PAs based on topologies with high BO efficiency, such as the Doherty or Outphasing PAs. In fact, the performance degradation and, consequently, the expected correction also depends on the considered PA topology [12], so the following approaches are focused on reducing the performance degradation due to load variations on PA topologies with higher BO efficiency.

Chappidi *et al.* [13] exploit active load pulling in a multiport combiner to improve voltage standing wave ratio (VSWR) tolerance at peak power. For the theoretical analysis, they consider a digital-to-analog converter (DAC)-based PA and a specifically designed two-way combiner. Moreover, the

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nominal output power is set to half of each channel's full power (FP) capability, by using only half of the DAC cells. Then, by turning on or off some of the cells, they are able to compensate the output load of the ON-state cells and, consequently, achieve performance correction for mismatched loads. However, the presented practical implementation is based on a two-cell Doherty-like PA and shows 2 dB of output power and more than 10% of power-added-efficiency (PAE) degradation for a 4:1 VSWR circle. Lyu and Chen [14] present a reconfigurable PA that can work in quasi-balanced DPA (QB-DPA) and balanced modes. The selection between modes is based on the control of a switch at the isolated port of the output quadrature coupler. The amplifier operating in QB-DPA mode was demonstrated to ensure high efficiency across the test loads distributed in a 2:1 VSWR circle. For operation in balanced mode, the linearity is increased for some loads, despite the reduced efficiency. In [15], a digital Doherty PA was presented, where appropriate driving signals are used to reduce the performance degradation under load varying conditions. Driving signals of digital Doherty PAs can be designed to use some power of the peaking amplifier to correct the carrier load, but this will degrade the BO efficiency of the PA and can only compensate for variations toward lower loads. In [16], a reconfigurable series/parallel DPA is designed using adaptive bias voltage sources (for the gate biasing) and a quadrature-coupler-based combining, which includes a switch at the isolation port to change the operation mode. This allows a reconfigurable DPA operation, changing the carrier and peaking roles. The carrier/peaking drain current capability and phases can also be adjusted using switched parallel transistors at the output stage and tunable phase delay lines at the input, respectively. The authors can achieve a worst case output power and FP PAE degradation of 1.7 dB and approximately 10%, respectively, for loads across a 3:1 VSWR circle. Note also that the drain current capability of the carrier/peaking devices is set to approximately half of the maximum value for operation with a 50-Ω nominal load.

In summary, analyzing the described techniques, we can conclude the following.

1) In order to maintain BO performance, the output stage devices' peak current must be reduced for operation under the nominal load.
2) In order to compensate for load variations for both higher and lower (than nominal) loads, it is necessary to include some kind of switched-mode operation at the combiner.
3) For most cases, neither the output power nor the drain efficiency have been completely restored.

This article presents a technique that is able to completely restore the DPA output power for nonoptimal real and complex loads. The drain efficiency is also completely compensated for nonoptimal real loads, while, for complex ones, some degradation is still expected. The peak current of the devices is also reduced for operation under the nominal load, but a typical, static, DPA combiner is used at the output.

This article is an expanded version of [17], in which a load-dependent supply voltage variation was proposed to correct the performance of DPAs operating under nonoptimal loads.

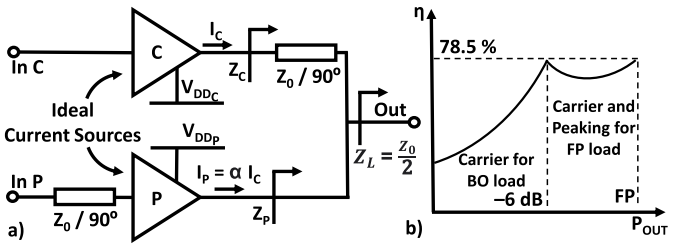

Fig. 1. (a) Ideal two-way symmetrical DPA considered during the theoretical derivations. (b) Ideal efficiency profile of the considered DPA under nominal load operation.

In [17], it was demonstrated that two independent drain voltages should be used for the carrier and peaking devices. It was also shown that, for this correction technique to be effective, the PA should be designed for a different FP load, which must be higher than the devices' maximum power one, resulting in the lower current (and power) for the nominal load. This design case guarantees higher current capability for mismatched loads. Then, by properly controlling the drain voltages of the devices, we achieve reduced load sensitivity. In this expanded version, we go one step further, showing that this correction technique is only effective if the radio frequency (RF) input signals of the carrier and peaking devices are load-dependent. These optimal input signals are derived, presented, and implemented using an analog adaptive input driving stage. The complete system is composed of the DPA output stage, an impedance tracking circuit, a two-channel medium power driving stage, and an adaptive input stage.

This article is organized as follows. Section II presents the theoretical derivation of the optimal carrier and peaking supply voltages and RF input signals for Doherty operation under nonoptimal loads. Section III shows a comparison between a typically designed Doherty, a Doherty designed for a higher nominal load, and the proposed quasi-load insensitive (QLI) one (designed for the higher load and including V_{DD} compensation). Section IV validates the introduced theory with static measurements and load-pull (LP) results of the QLI Doherty prototype. Section V presents the dynamic performance of the system for a fully automated operation under synthesized load variations, using continuous wave (CW) and modulated signal excitations. Finally, Section V summarizes the advantages and drawbacks of the proposed technique.

II. Carrier and Peaking Supply Voltage and Input Signal Theoretical Derivation

This section is devoted to the theoretical derivation of the optimal:

1) load-dependent V_{DD};
2) FP design impedance for the QLI DPA;
3) driving signals for both the carrier and peaking devices.

The presented derivation assumes an ideal two-way symmetrical Doherty PA, as shown in Fig. 1(a), as well as independent V_{DD} sources for the carrier and peaking devices (V_{DD_C} and V_{DD_P}, respectively). Class B operation is assumed, leading to optimal loading of the devices on the real axis.

To maintain the DPA ideal behavior for nonoptimal loads, it is necessary to guarantee that both the BO and FP output

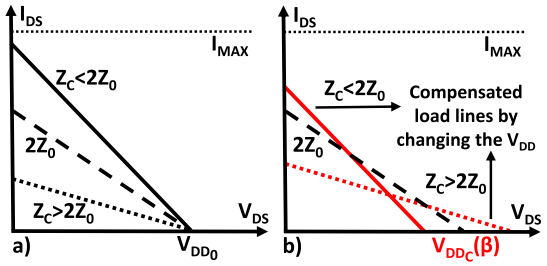

Fig. 2. (a) Uncompensated carrier load lines for three output loads: lower than optimal (continuous), optimal (dashed), and higher than optimal (dotted). (b) Load lines for the same loads when V_{DD} compensation is applied (in red).

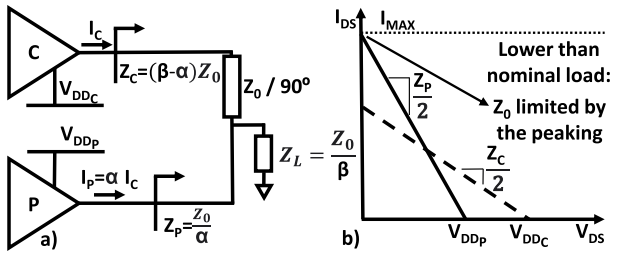

Fig. 3. (a) Considered DPA output combiner and correspondent carrier and peaking impedances. (b) Load lines illustrating the case where Z_0 is limited by the peaking load, for lower than nominal output impedances.

power levels are kept constant. As illustrated in Fig. 1(b), to fulfill this condition, it is necessary to ensure that the maximum output power of the carrier device for the BO load is constant. Moreover, the maximum combined output power of the carrier and peaking devices for their FP loads must also be kept constant and equal to four times (6 dB) the BO output power.

At BO, since the peaking is OFF, the DPA operation is determined by the carrier. When there is an output load change, the voltage and/or current excursions at the intrinsic drain change, as illustrated in Fig. 2(a). Consequently, the output power and efficiency vary, and so, as introduced in [11], we can compensate for these variations by modifying the drain supply voltage, V_{DD_C}, as shown in Fig. 2(b).

The condition for preserving the BO output power level is given by

$$P_{O_C}^{\mathrm{BO}}(\beta) = P_{O_C}^{\mathrm{BO}}(\beta = \beta_0) \tag{1}$$

where β represents the output load variation and is equal to (Z_0/Z_L), Z_0 is the devices' nominal FP load, and Z_L is the DPA output load. Note that, for the nominal operation condition, $\beta = \beta_0 = 2$, which corresponds to $Z_L = (Z_0/2)$.

As known [18], for a piecewise linear current source with an ideal $R_{\mathrm{ON}} = 0$, the saturated output power, $P_O(Z_D)$, for operation with a load, Z_D, higher or equal to the maximum power load (ensuring saturation at the triode region) is given by

$$P_O(Z_D) = \frac{1}{2}\frac{{V_{\mathrm{DD}}}^2}{|Z_D|^2}\mathrm{Re}(Z_D). \tag{2}$$

Note that this expression will be used to calculate the output power of the carrier and peaking PAs in different scenarios, by replacing the generic load, Z_D, with their correspondent output loads. Now, to preserve the BO power, it is possible to further develop (1) using (2) and replace Z_D with the carrier BO load, $Z_C^{\mathrm{BO}}(\beta) = \beta Z_0$

$$\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta|^2}\mathrm{Re}(\beta) = \frac{{V_{\mathrm{DD}_0}}^2}{|\beta_0|^2}\mathrm{Re}(\beta_0) \tag{3}$$

where V_{DD_0} is the nominal supply voltage. Note that, as expected from class B terminations, Z_0 is a real impedance. The previous expression can then be solved for $V_{\mathrm{DD}_C}(\beta)$, assuming β_0 real, resulting in

$$V_{\mathrm{DD}_C}(\beta) = \frac{|\beta|}{\sqrt{\beta_0 \mathrm{Re}(\beta)}}V_{\mathrm{DD}_0} \tag{4}$$

which gives the carrier amplifier supply voltage that maintains the BO output power level constant.

As previously introduced, the combined FP of both the carrier ($P_{O_C}^{\mathrm{FP}}$) and peaking ($P_{O_P}^{\mathrm{FP}}$) PAs must also be preserved to ensure the correct DPA operation. This condition can be described as

$$P_{O_C}^{\mathrm{FP}}(\beta) + P_{O_P}^{\mathrm{FP}}(\beta) = 4 \cdot P_{O_C}^{\mathrm{BO}}(\beta = \beta_0). \tag{5}$$

Equation (5) can be further developed using (2), considering the carrier and peaking FP impedances, $Z_C^{\mathrm{FP}}(\beta, \alpha) = (\beta - \alpha)Z_0$ and $Z_P^{\mathrm{FP}}(\alpha) = (Z_0/\alpha)$, respectively, as shown in Fig. 3(a), where $\alpha = (I_P/I_C)$; this results in

$$\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta - \alpha|^2}\mathrm{Re}(\beta - \alpha) + V_{\mathrm{DD}_P}(\beta)^2\mathrm{Re}(\alpha) = 4\frac{V_{\mathrm{DD}_C}(\beta)^2}{|\beta|^2}\mathrm{Re}(\beta). \tag{6}$$

Then, to ensure that both devices operate at the on-set of saturation at FP, their voltage excursion should be equal to twice their V_{DD} bias

$$\begin{cases} V_{\mathrm{DD}_P}(\beta) = |I_P| \cdot \left|Z_P^{\mathrm{FP}}(\alpha)\right| \\ V_{\mathrm{DD}_C}(\beta) = |I_C| \cdot \left|Z_C^{\mathrm{FP}}(\beta, \alpha)\right| \end{cases} \tag{7}$$

and so, it is possible to obtain a relationship between $V_{\mathrm{DD}_C}(\beta)$ and $V_{\mathrm{DD}_P}(\beta)$ as

$$V_{\mathrm{DD}_C}(\beta) = V_{\mathrm{DD}_P}(\beta)|\beta - \alpha|. \tag{8}$$

Finally, by replacing the obtained relationship in (6), the following equation is obtained:

$$|\beta| = 2|\beta - \alpha| \tag{9}$$

which can be used in (8) to remove the dependence with α. The obtained expression can then be further developed, using (4), to achieve

$$V_{\mathrm{DD}_P}(\beta) = \frac{2}{\sqrt{\beta_0 \mathrm{Re}(\beta)}}V_{\mathrm{DD}_0} \tag{10}$$

which gives the peaking amplifier supply voltage to maintain the correct DPA operation. The obtained V_{DD} values for the carrier and peaking devices are plotted in Fig. 4, using a V_{DD_0} of 25 V.

Analyzing the carrier and peaking load lines is relevant to understand how these variable supply voltages maintain a constant output power. Fig. 5 presents these load lines for a conventional Doherty (a)–(c) and for the proposed QLI version (d)–(f).

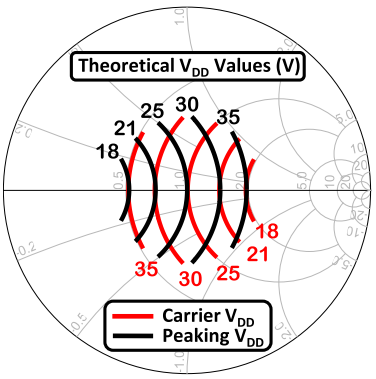

Fig. 4. Theoretical drain voltage values for the carrier and peaking devices for a nominal V_{DD} of 25 V. The Smith chart Z_0 is the nominal design load.

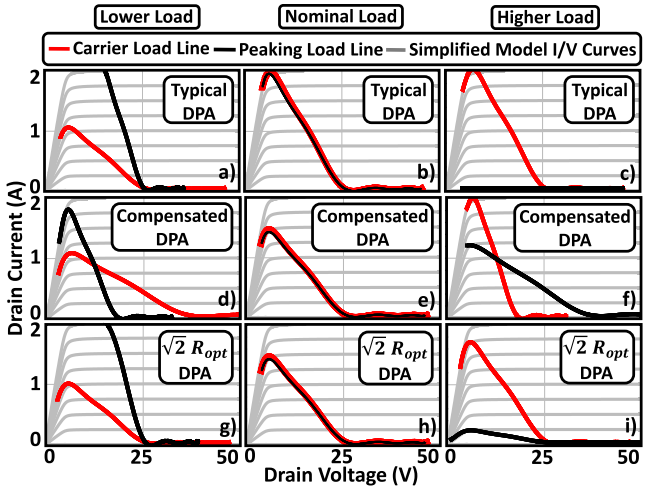

Fig. 5. Load lines of the carrier and peaking devices of the DPA designed for (a)–(c) typical nominal load, (d)–(f) for the optimal nominal load with V_{DD} compensation, and (g)–(i) for the optimal nominal load without V_{DD} compensation. Each of the cases is shown (b), (e), and (h) for operation under the nominal load, (a), (d), and (g) half the nominal load, and (c), (f), and (i) twice the nominal load.

Considering the conventional DPA operating for lower than nominal output impedances (a), the peaking load becomes lower, degrading the efficiency and output power, and the carrier load becomes higher, reducing the output power. For higher output impedances (c), the carrier load becomes lower, degrading the BO efficiency. In this last scenario, the peaking PA is not used because it would LP the carrier to even lower loads, decreasing its output power and efficiency, due to current saturation.

Instead, in the proposed DPA operating for lower than nominal output impedances (d), the carrier load becomes higher, and its maximum current becomes lower. Thus, its V_{DD_C} is increased to maintain the output power. On the other hand, the peaking load becomes lower, and its maximum current becomes higher. Thus, its V_{DD_P} is decreased to keep the device on the on-set of saturation, increasing its efficiency. For higher output impedances (f), the carrier load becomes lower, and its maximum current becomes higher. Thus, its V_{DD_C} is decreased to keep the device on the on-set of saturation, increasing its efficiency. The peaking load becomes higher, and its maximum current becomes lower, and so its V_{DD_P} is increased to guarantee the necessary output power.

As it is also seen in Fig. 5, the load lines of the proposed PA do not reach the maximum current, I_{MAX}, for the nominal load (e). This happens because, as previously introduced, the PA was designed for a higher nominal FP load. In this way, none of the devices becomes current saturated for any load in the VSWR design range. If this is not taken into consideration, the peaking would be current saturated for lower loads (d), and the same would happen to the carrier under operation for higher loads (f). Thus, in order to assure that I_{MAX} is only reached for the worst case loads, it is necessary to calculate the optimal nominal FP load, Z_0. This can be calculated using the load line expression, $|I_{MAX}| = 2V_{DD}/|Z_L|$, with V_{DD} equal to the carrier and peaking derived supply voltages, and $|Z_L|$ equal to their FP impedances, as illustrated in Fig. 3(b) and described by the following equations:

$$\begin{cases} Z_{0_C} = R_{opt}\sqrt{\dfrac{4}{\beta_0 \,.\, \mathrm{Re}(\beta)}} \\ Z_{0_P} = R_{opt}\sqrt{\dfrac{4|\alpha|^2}{\beta_0 \,.\, \mathrm{Re}(\beta)}} \end{cases} \tag{11}$$

where $R_{opt} = 2V_{DD0}/|I_{MAX}|$ is the device's maximum power load [corresponding to the load line shown in Fig. 5(b)].

It is also important to notice that, from (9), we can obtain various solutions for α. However, only the solution $\alpha = (\beta/2)$ guarantees an equal peak current for the peaking and carrier devices at the nominal load. Furthermore, it is also the only alpha that guarantees an equally limited nominal FP impedance, Z_0, for a symmetrical load variation (around the nominal load). Thus, (11) must be calculated using $\alpha = (\beta/2)$. The output impedance, Z_L, used to calculate the β value, should be chosen considering the worst case scenarios, i.e., the output load with higher real part for the carrier expression, Z_{0_C}, and the output load with lower real part for the peaking expression, Z_{0_P}. Thus, for a $\beta_0 = 2$ and a load variation of 4:1 ($(Z_0/4) < Z_L < Z_0$), equivalent to a maximum VSWR of 2.0, the optimal FP load is equal to $\sqrt{2}R_{opt}$. This analysis can be expanded for other mismatch levels, as long as the load variation is centered on the nominal load. For these cases, the optimal Z_0 can be obtained by $\sqrt{x}R_{opt}$, with x being the maximum VSWR considered for correction. Thus, we sacrifice power (i.e., the power that we can obtain for a certain device area operating at the nominal output load) in exchange for the correction radius.

However, it is important to notice that designing the DPA for the calculated FP load is necessary, but not sufficient, to compensate for load variations, as shown in Fig. 5(g)–(i), where the V_{DD} is fixed at the nominal value. It is shown that, for lower loads, the peaking is severely reducing the FP efficiency, and for higher loads, the carrier is reaching the maximum current earlier.

To reach the optimal operation shown in Fig. 5(d)–(f), the designed Doherty PA also requires digital input splitting, i.e., it is driven with different input driving signals for each load. These input signals have been calculated so that the carrier reaches the on-set of saturation for BO and FP, and

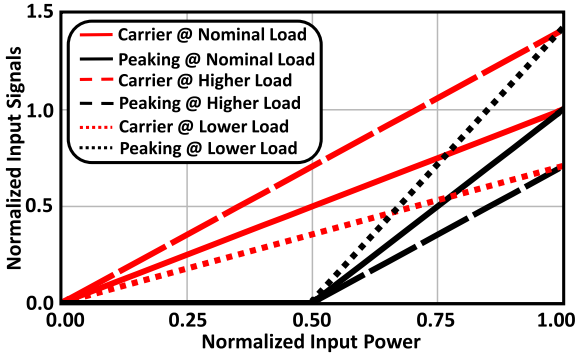

Fig. 6. Optimal input splitting ratio for the nominal load, twice, and half the nominal load.

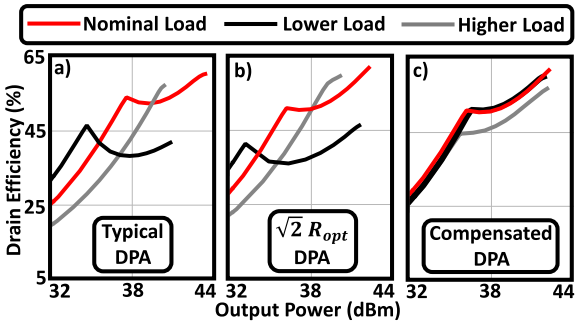

Fig. 7. Drain efficiency profile comparison between the DPA designed (a) for the typical nominal load and for the optimal nominal load without and with V_{DD} compensation, respectively, at (b) and (c).

the peaking also reaches the same condition for FP, ensuring high efficiency.

For the proposed QLI DPA, the peak current of the carrier at BO and FP can be calculated as

$$\begin{cases} \mathrm{IC_{BO}} = \dfrac{2V_{\mathrm{DD}_C}}{|\beta|Z_0} \\ \mathrm{IC_{FP}} = \dfrac{2V_{\mathrm{DD}_C}}{|\beta-\alpha|Z_0} \end{cases} \tag{12}$$

where $|\beta - \alpha|$ is equal to $(|\beta|/2)$ [from (9)]. Consequently, the FP peak current becomes twice the BO value, resulting in linear driving signals.

The peaking FP current is calculated as

$$\mathrm{IP_{FP}} = \frac{2V_{\mathrm{DD}_P}}{\frac{Z_0}{|\alpha|}} \tag{13}$$

where $\alpha = (\beta/2)$, as previously explained.

From the peak currents that have been calculated and knowing the transconductance, g_m, of the used devices, the optimal driving signals' amplitude was obtained and is shown in Fig. 6. Finally, since $\alpha = (\beta/2)$, $\beta = (Z_0/Z_L)$, and $\alpha = (I_P/I_C)$, the input driving signals phase should be

$$\angle V_{\mathrm{in}_P} - \angle V_{\mathrm{in}_C} = -\angle Z_L + \Phi \tag{14}$$

where Φ is the required input phase delay to align the carrier and peaking currents at the combiner node, i.e., compensate for the different phase lags between the peaking and carrier input matching networks (IMNs), OMNs, and imposed by the different biasing of the devices.

III. Simulated Performance Improvement

Fig. 7 presents the simulated drain efficiency of various DPAs: 1) the conventional DPA designed for the typical nominal load, R_{opt}; 2) the DPA designed for the optimal nominal load, $\sqrt{2}R_{\mathrm{opt}}$, with a fixed V_{DD}; and 3) the DPA designed for the optimal nominal load and with V_{DD} compensation (QLI DPA). Please note that, within this section, the presented DPA designs are based on a real transistor model, but their matching networks are based on ideal S-parameter blocks.

The conventional PA has a typical DPA efficiency shape and an output power of 43.1 dBm for the nominal load. However, for lower loads, its output power is degraded, and the efficiency is reduced, both at FP and BO. For higher loads, its output power is also degraded, and the BO efficiency is extremely reduced. For this case, the efficiency shape changes drastically, becoming similar to the one of a single-ended PA. The amplifier that was designed for the FP load of $\sqrt{2}R_{\mathrm{opt}}$, but operates for a fixed V_{DD}, presents a lower output power of 42.3 dBm for the nominal load. For lower loads, its output power is degraded, its efficiency is reduced, and the BO level increases. For higher loads, the output power is also decreased, and the DPA efficiency shape is lost, degrading the BO efficiency. Thus, comparing the amplifier designed for the nominal load of $\sqrt{2}R_{\mathrm{opt}}$ with the typical case, the output power relative reduction is mitigated, but the worst case value is lower. In terms of efficiency, for lower loads, the degradation is smaller at FP, and for higher loads, the efficiency shape is slightly less degraded. The proposed PA, with V_{DD} compensation, also delivers a lower output power of 42.3 dBm for operation under the nominal load but maintains its efficiency profile for nonoptimal loads, guarantying higher BO efficiency and constant maximum output power.

TABLE I
Summarized LP Performance Comparison for the Three PAs

	Worst-case P_{out} (dBm)	**P_{out} Degradation (dB)**	**Wors-case FP eff. (%)**	**Worst-case BO eff. (%)**
Typical PA	40.6	2.5	43	29
$\sqrt{2}R_{opt}$ PA	40.4	2	49	33
Comp. PA	**42.3**	**0.3**	51	**45**

The LP contours presented in Fig. 8 compare the performance of the DPA designed for the typical load (black) and the proposed QLI version (red). These two cases correspond to the cases already presented in Fig. 7(a) and (c), respectively. In Fig. 9, the presented LP contours correspond to the PA that was designed for the optimal nominal load of $\sqrt{2}R_{\mathrm{opt}}$, without V_{DD} compensation (black) and the proposed QLI PA (red), which corresponds to (b) and (c) PAs of Fig. 7, respectively. The performance of the three presented cases is summarized in Table I for mismatched loads up to a VSWR of 2.0.

From the analysis of the presented simulation results, it is concluded that the proposed QLI DPA is able to maintain its efficiency profile and the output FP for all the tested loads.

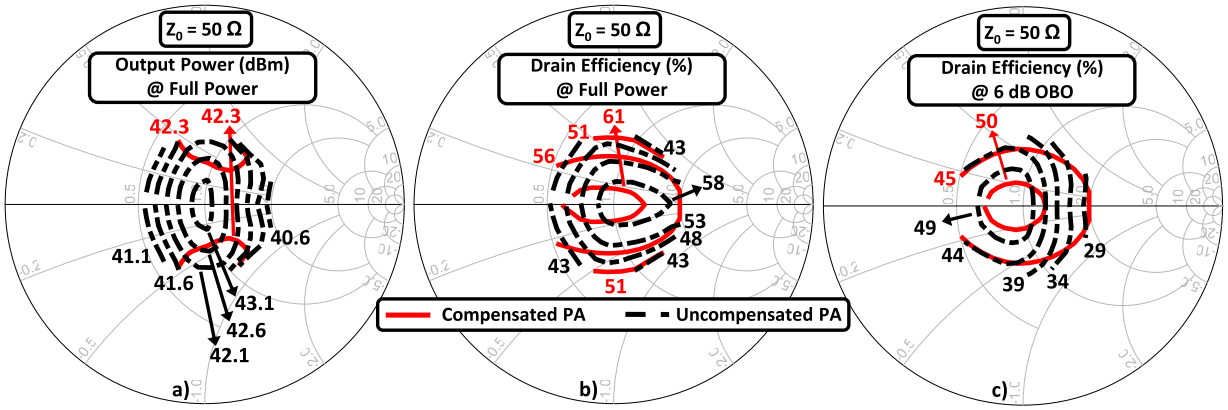

Fig. 8. Simulated LP comparison between the V_{DD} compensated DPA and the DPA designed for the typical FP load (R_{opt}) without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the 6-dB OBO drain efficiency in (c).

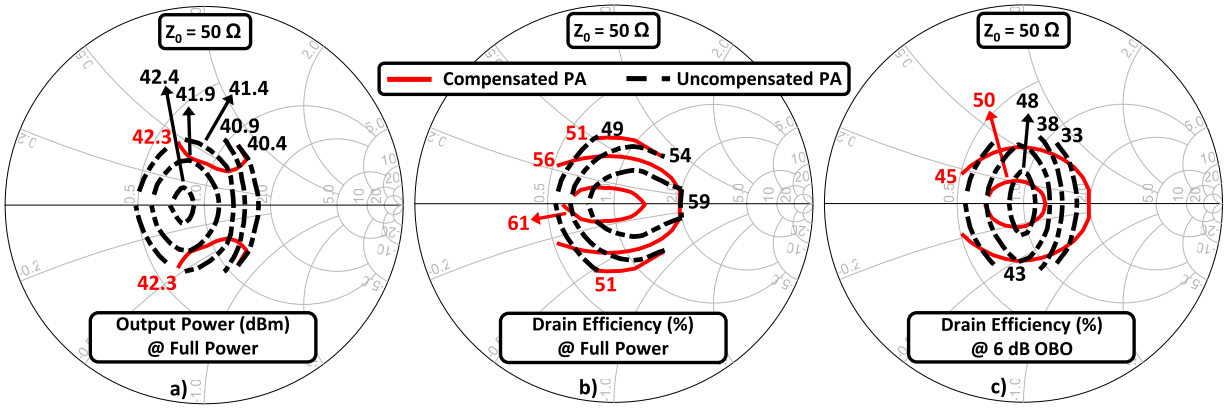

Fig. 9. Simulated LP comparison between the V_{DD} compensated DPA and the DPA designed for the same load ($\sqrt{2}R_{opt}$) but without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the 6-dB OBO drain efficiency in (c).

The efficiency value is slightly degraded for complex loads, as expected. Nonetheless, the worst case output power of the QLI DPA is almost 2 dB higher than it is for any of the uncompensated cases and almost 15% more efficient at BO.

IV. System Architecture and Static Experimental Validation

In this section, a QLI DPA prototype, designed using the derived theory, is presented. Various static measurements characterizing the operation with different loads are also shown, with the objective of testing the performance under load varying scenarios that can happen in various applications, as described in Section I. The system was designed for 3.6 GHz and is shown in Fig. 10. It is composed of the DPA output stage, a medium power two-channel driver, an adaptive input splitting predriver stage, and also an impedance measurement circuit. The impedance measurement stage was already extensively described and presented in [19].

The DPA output stage is based on two Wolfspeed CGH40010F devices biased with a nominal V_{DD_0} of 25 V. Both devices operate with class B harmonic terminations, the carrier is biased with 25 mA of quiescent current (1.2% of I_{MAX}), and the peaking is in shallow class C. The amplifier was designed to present the optimal impedance of $\sqrt{2}R_{opt}$ at the devices' intrinsic current source plane, in FP,

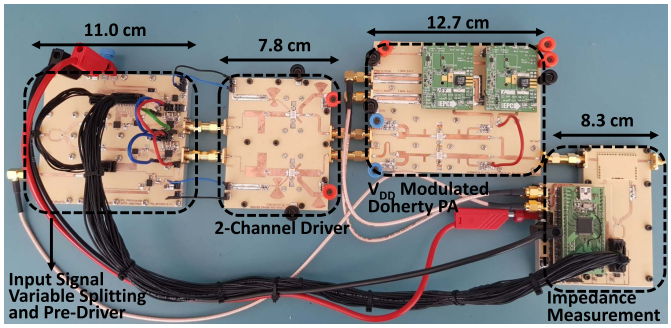

Fig. 10. Implemented DPA system with input splitting control and impedance tracking. The dimensions of each stage are displayed in cm.

for an output load of 50 Ω. This DPA stage was also designed to present real impedances at the devices' intrinsic current source planes for real load impedances. This allows us to obtain the load-dependent V_{DD} values directly from the theory presented in Section II, from load measurements at the PA output port. In order to change the drain supply voltage of both devices, two dc-to-dc gallium nitride (GaN) buck converters from EPC, based on EPC8009 transistors and supplied by the same voltage source, were also added to the design. Note that, although we have used commercial dc-to-dc converters, for the required frequencies, they can be designed to be very compact and efficient. Please also note that, as shown in Fig. 4,

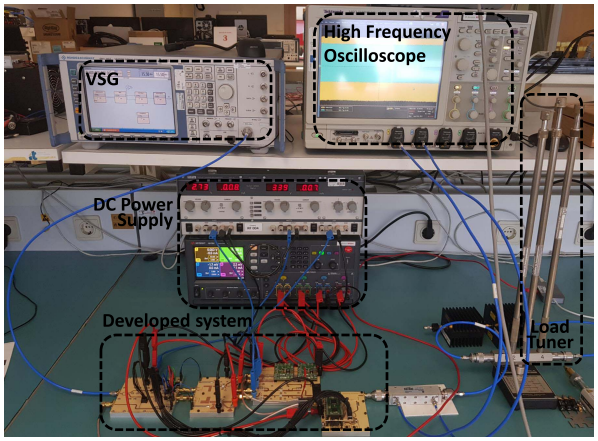

Fig. 11. Measurement setup, including the stub-based manual load tuner that was used to synthesize nonoptimal loads.

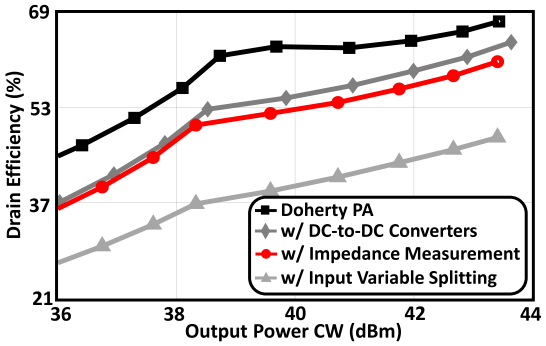

Fig. 12. Drain efficiency of the DPA alone, including the dc-to-dc converters, the dc-to-dc converters and impedance tracking circuit, and all the previous plus the variable input splitting circuit.

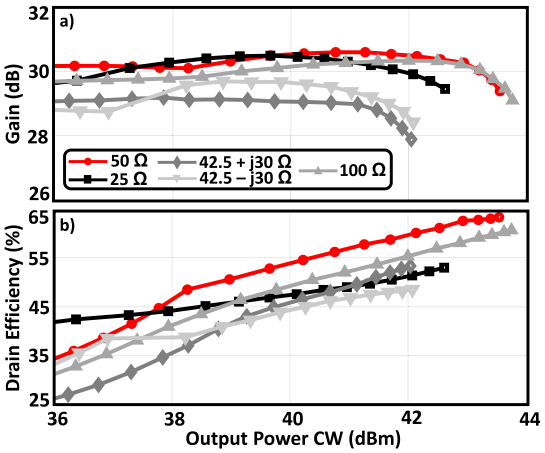

Fig. 13. (a) Measured gain and (b) drain efficiency of the complete DPA (excluding the power dissipated at the driving stage) for various output loads without V_{DD} compensation. We present two traces (gain and efficiency) for each load, which corresponds to one specific color and symbol as represented in the plot legend.

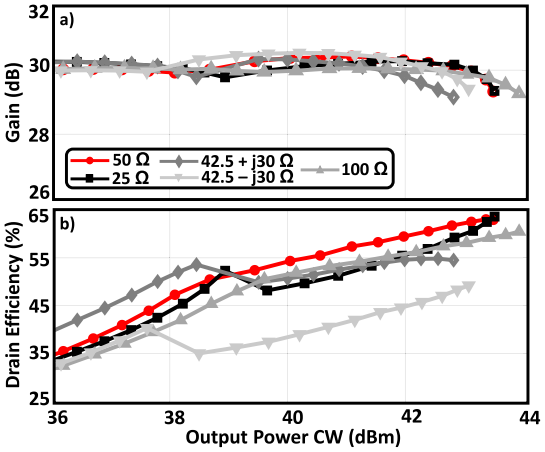

Fig. 14. (a) Measured gain and (b) drain efficiency of the complete DPA (excluding the power dissipated at the driving stage) for various output loads with V_{DD} compensation. We present two traces (gain and efficiency) for each load, which corresponds to one specific color and symbol as represented in the plot legend.

for the worst case loads, the drain voltage of the devices is increased above their recommended nominal voltage of 28 V. However, since the PA is not expected to operate for long amounts of time under extreme mismatched loads, this should not significantly affect the devices' reliability, especially for modern GaN devices with breakdown voltages of 120 V. If, for some application/reason, it is necessary to operate under higher mismatch levels, the nominal voltage (V_{DD_0}) should be reduced trading between load compensation zone and required device area, for a specific output power.

The medium power driving stage is composed of two independent drivers, for the main and peaking channels. It was also designed using two Wolfspeed CGH40010F devices. However, since the required maximum output power is lower than it is at the output stage, the devices are biased at 17 V, ensuring high efficiency. This stage has three purposes: 1) amplify the input signals to the required level; 2) change the peaking turn-on point, using a load-dependent gate bias voltage for the peaking driver; and 3) isolate the input and output stages since the drivers were designed for the impedance presented by the main and peaking output amplifiers, and their IMNs present 50 Ω to the input stage.

The input stage is composed of a Wilkinson power divider, a phase shifter from Qorvo (TGP2108-SM), two variable attenuators from Analog Devices (HMC792ALP4E), and also two amplifiers from Skyworks (SKY66313-11). This stage is used to split the input signal for the carrier and peaking channels and to preamplify each channel. Moreover, it includes an adaptive phase and amplitude relation between the two channels, which can be modified according to the output load to implement the optimal input driving signals. The common-mode amplitude is also controllable to keep the amplifier gain constant with load variations. Please note that this input variable splitting is performed automatically by the fabricated system, and it is controlled by the impedance measurement system using real-time load measurements.

The PA was measured using the setup shown in Fig. 11. Since the complete PA has a single input, the input RF signal was generated using a single channel vector signal generator (VSG). A high-frequency oscilloscope was used to sample the incident and reflected waves at the output of the PA in order to measure the delivered power. Finally, a manual load tuner from Weinschel Associates was used to synthesize various output loads.

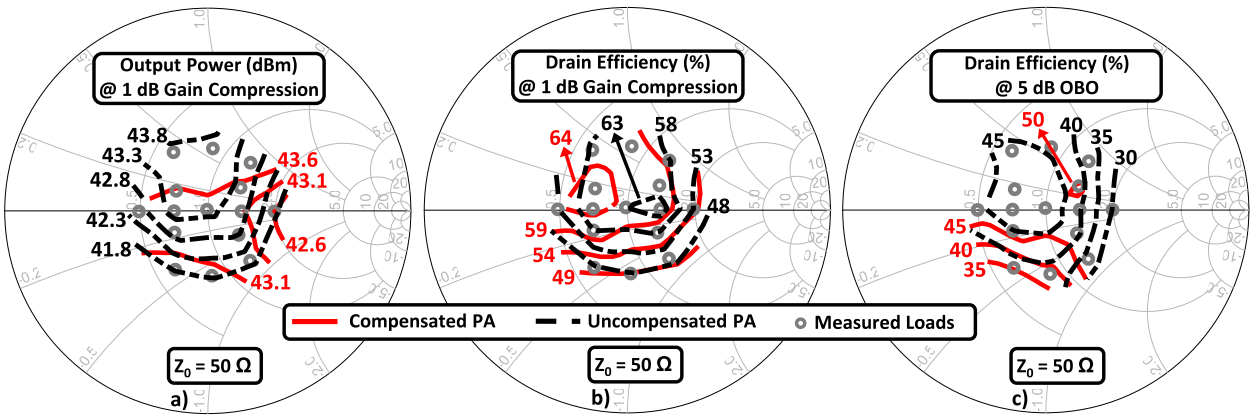

Fig. 15. Measured LP comparison between the V_{DD} compensated DPA and the DPA designed for the same load but without V_{DD} compensation. The output power and efficiency at FP are presented in (a) and (b), respectively, and the BO drain efficiency in (c).

In order to validate the Doherty behavior of the PA and check the impact of its various stages on the compound efficiency, it was first measured for operation with the nominal output load of 50 Ω. Fig. 12 shows the drain efficiency profile of the PA. The BO level is almost 6 dB, as expected for a symmetrical Doherty. The DPA output stage, in black (squares), shows efficiency of 62% and 68% at BO and FP, respectively. The dark gray plot (diamonds) presents the efficiency of the output stage, including the used dc-to-dc converters, and the efficiency is reduced to 53% at BO and 64% at FP. Including the impedance measurement circuit at the PA output further reduces the efficiency by around 3%, due to the added insertion loss, as shown by the red plot (circles). In light gray (triangles), the efficiency of the PA including the dc-to-dc converters, the impedance measurement circuit, and also the power dissipated in the driver and predriver stages is shown. Accounting for the power dissipated in the driving stages corresponds to an efficiency reduction of 12%, both at FP and BO. The drain efficiency presented in the following tests corresponds to the red plot, which includes only the dc-to-dc converters and the impedance measurement circuit. The input driving stage is excluded as it was not designed for high efficiency and is not mandatory to validate the presented technique. Moreover, most of the dissipated power comes from the predriver, whose objective is to increase the gain of the PA, and so, it would also be necessary for the typical DPA without V_{DD} compensation.

Fig. 13 shows the measured gain and drain efficiency of the fabricated PA for various loads without V_{DD} compensation. This case corresponds to the "$\sqrt{2}R_{opt}$ PA" of Section III, which was designed for the calculated load of $\sqrt{2}R_{opt}$ but operates for a fixed V_{DD}. In this case, as expected, the PA output power capability and BO level are not maintained for nonoptimal loads. The nominal load of 50 Ω is shown in red (circles) and presents an output power capability of around 43.5 dBm and a BO level of more than 5 dB with an efficiency above 46%. For the worst case load, which corresponds to the higher load of 100 Ω, in dark gray (diamonds), the amplifier is only capable of delivering 42 dBm, the Doherty efficiency profile is degraded, and the efficiency at BO is greatly reduced (below 30%). For lower loads, such as 25 Ω, shown in black (squares), the amplifier is still not able to deliver the required output power (43 dBm), and the efficiency is higher at BO, but it is degraded by around 10% at FP.

TABLE II
SUMMARIZED MEASURED LP PERFORMANCE COMPARISON FOR THE TWO PAS

	Worst-case P_out (dBm)	P_out Degradation (dB)	Wors-case BO eff. (%)	Worst-case FP eff. (%)
$\sqrt{2}R_{opt}$ PA	41.8	2	30	48
Comp. PA	**42.6**	**1**	35	49

Fig. 14 presents the measured efficiency and gain of the amplifier applying the derived V_{DD} compensation theory and optimal input signals. For these measurements, the common-mode amplitude of the input signals is also load-dependent in order to keep the small-signal gain constant and equal to 30 dB. For this amplifier, the gain and efficiency profiles are similar to the optimal ones obtained for the nominal load of 50 Ω. The worst case, in terms of the maximum delivered power, is still the 100-Ω load, in dark gray (diamonds), but, now, the amplifier can reach more than 42.5 dBm (whereas, without V_{DD} compensation, it was only 42 dBm). The efficiency is degraded for loads with lower imaginary parts, as $42.5-j30$ Ω, in light gray (nablas); however, for loads with high imaginary part, the behavior is correctly compensated. This indicates that there may have been some inaccuracy in the manufacturing process, and so the optimal load of the fabricated amplifier can be slightly deviated from 50 Ω.

The LP contours for both amplifiers are plotted, for the 1-dB gain compression point in Fig. 15, and their performance is summarized in Table II. From these measurements, it is concluded that there is a significant improvement in the output power capability of the DPA (up to 1.3 dB). The DPA worst case efficiency is almost the same with and without compensation, as shown in Table II. However, for most of the loads, there is also a great efficiency improvement, such as, for example, for higher real loads, where the BO efficiency is improved from 30% to almost 50%. As previously mentioned,

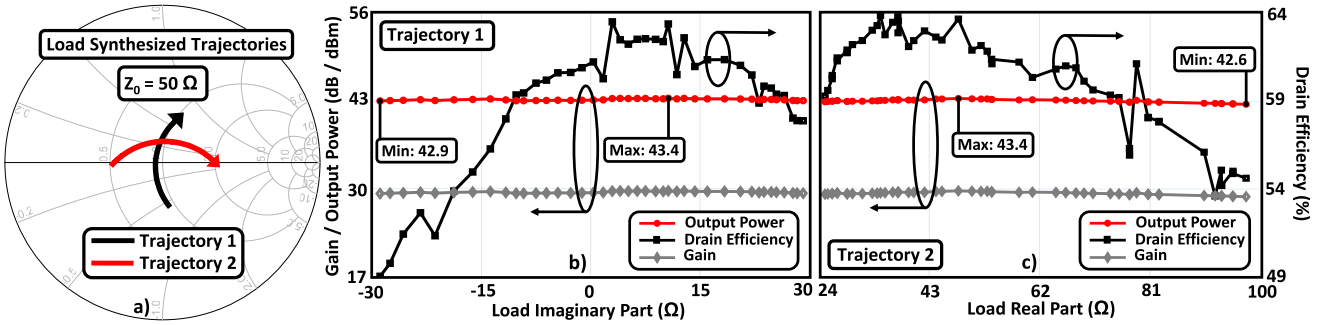

Fig. 16. DPA system performance under a continuous load variation. The load trajectories 1 and 2, in (a), correspond to plots (b) and (c), respectively. (b) and (c) Output power, gain, and efficiency over the synthesized load variations.

the QLI DPA presents these lower efficiency values for a restricted area of the Smith chart, where the compensation method was not able to restore the DPA efficiency shape, probably due to some deviation on the amplifier's nominal load.

V. Dynamic Characteristics Under Output Load Variation

This section presents the DPA CW performance under continuous load variations. During these load sweep measurements, the RF input level is kept constant, and the amplifier is automatically adjusting both supply voltages, as well as the input signal splitting. The operation with modulated signals excitation is also presented for various nonoptimal loads.

Fig. 16 presents the measured data during the load sweep tests. In Fig. 16(a), two load trajectories are presented: the first one, in black, along the 50-Ω real part circle, corresponds to the data of Fig. 16(b); the second one, in red, along the real axis, corresponds to the data shown in Fig. 16(c). Because of the time limitations on the measurement setup, namely, on the oscilloscope acquisition time, the load trajectories presented here have a duration of some seconds. However, the used microcontroller and dc-to-dc converters are capable of performing this compensation at the tens of milliseconds range, [11]. Note that, since the input excitation is constant, the output power and gain variations are equal.

During the first load sweep, the output power varies between 42.9 dBm, for the first loads with lower imaginary parts, and 43.4 dBm, for the loads closer to 50 Ω. This validates the load measurement and automatic adaptation performed by the PA since the performance is similar to what was expected from the LP presented in Fig. 15. The efficiency is also very similar, varying between 49% and 63%.

In Fig. 16(c), the load variation starts at the lower real values and moves toward the higher real values. Consequently, the output power varies between 43.4 and 42.6 dBm, reaching its minimum for the loads around 100 Ω. The efficiency is higher during this test, varying between 54% and 64%, since the load imaginary part does not pass through low negative values.

Now, the performance of the fabricated prototype under modulated signal excitation is presented. For these measurements, a long-term evolution (LTE)-like signal with 5 MHz of bandwidth and 5.5 dB of PAPR was used. The prototype was

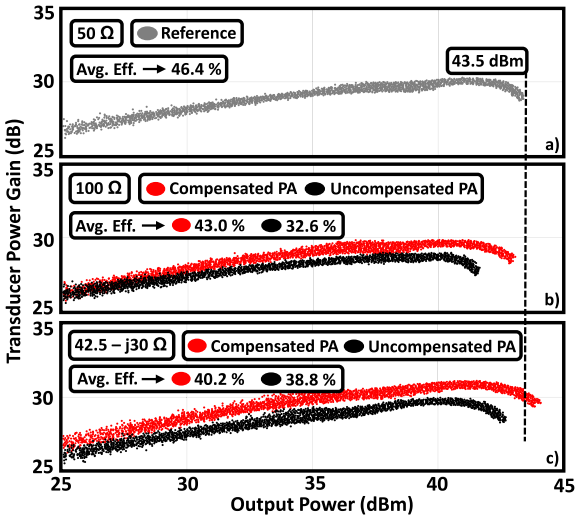

Fig. 17. Dynamic transducer power gain of the fabricated prototype with and without V_{DD} compensation for operation with modulated signal excitation under various output loads. The reference, for a 50 Ω load, in (a). For nonoptimal loads of 100 and 42.5 - j0 Ω, in (b) and (c), respectively.

measured for the nominal load of 50 Ω, which is the reference for comparison with other loads, and also for 100 and $42.5 - j30$ Ω, which are the worst case loads both in terms of output power and efficiency, as seen in the LP presented in Fig. 15. Note that the gain compression is the same for all the presented measurements, guaranteeing a fixed PAPR of the output signal of the amplifier.

In Fig. 17(a), the dynamic gain of the DPA for the reference load is presented, with a peak output power of 43.5 dBm and average efficiency of 46.4%. Then, in Fig. 17(b), the dynamic gain is shown for the 100-Ω load. As expected from the CW characterization, by using the proposed technique, the peak output power level is almost completely restored, and the average efficiency is increased by more than 10%. For the $42.5 - j30$ Ω load, as shown in Fig. 17(c), the output power is completely restored, and the average efficiency is maintained.

In Fig. 18, the phase shift of the implemented prototype with and without V_{DD} compensation is presented for the same three loads. From these plots, the output power compensation is also evident, but a slightly higher phase dispersion is noticed for the compensated amplifier.

In Fig. 19, the spectra of the DPA output signal are shown for the reference load of 50 Ω and for a nonoptimal load of 100 Ω. By comparing the spectra of the amplifier operating

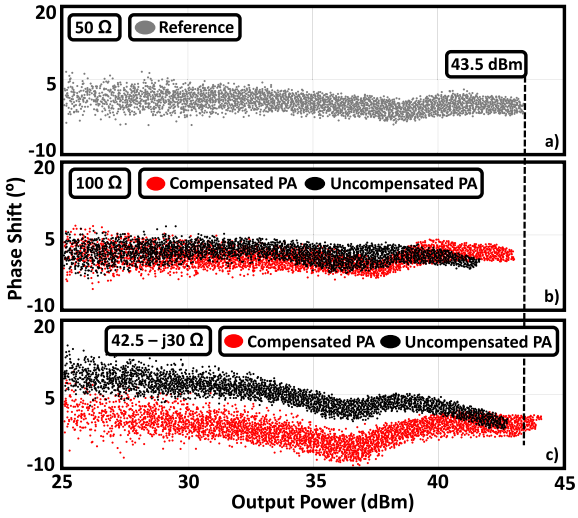

Fig. 18. Dynamic phase shift of the fabricated prototype with and without V_{DD} compensation for operation with modulated signal excitation under various output loads. The reference, for a 50 Ω load, in (a). For non-optimal loads of 100 and 42.5 - β0 Ω, in (b) and (c), respectively.

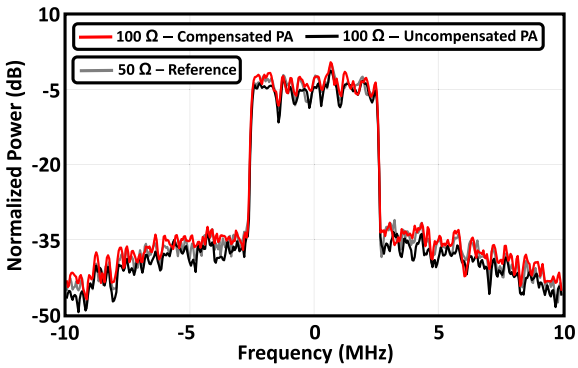

Fig. 19. Spectra of the DPA output signal for three different scenarios. The reference case, where the amplifier operates for a nominal 50-Ω output load, in gray. The case where the amplifier operates for a nonoptimal output load of 100 Ω, with and without V_{DD} compensation, in red and dark, respectively.

TABLE III
SUMMARIZED RAW ACPR AND NMSE OF THE DPA FOR DIFFERENT LOADS, WITH AND WITHOUT V_{DD} COMPENSATION

Load (Ω)	ACPR (dB) High Band	ACPR (dB) Low Band	NMSE (dB)
50 (reference)	-31.8	-32.6	-25.3
100 (w/o compensation)	-32.6	-32.9	-26
100 (w/ compensation)	-31.4	-32.1	-25.1
42.5-j30 (w/o compensation)	-28.8	-29.8	-22.8
42.5-j30 (w/ compensation)	-30.1	-30.9	-23.9

for an output load of 100 Ω, with and without V_{DD} compensation, it is concluded that the system linearity is not degraded by using the proposed technique. Moreover, in Table III, the raw (i.e., uncorrected) adjacent channel power ratio (ACPR) and normalized mean squared error (NMSE) values are shown, before and after compensation, for two different nonoptimal output loads, showing that the proposed technique does not degrade the linearity.

VI. CONCLUSION

In this article, a technique capable of improving the performance of a two-way symmetrical DPA operating for nonoptimal loads was presented. The optimal load-dependent V_{DD} voltages and input signals for the carrier and peaking devices were derived. The required devices' nominal design load for the compensation method to be effective was also shown to be $\sqrt{2}R_{opt}$, for load variations inside a maximum VSWR circle of 2.0. In the simulation, the proposed method has been shown to completely restore the DPA output power capability and efficiency profile, showing an improvement of 1.7 dB on the amplifier's worst case output power and 15% on its BO efficiency. The experimental validation was performed on a 3.6-GHz symmetrical DPA with a maximum nominal output power of 43.5 dBm and 5.1 dB of OBO with a drain efficiency above 50%. The tested system was composed of a DPA output stage, featuring a load-dependent adaptive supply voltage control, an impedance measurement circuit, and an input driving stage capable of implementing load-dependent amplitude and phase adjustments on the carrier and peaking channels. This system proved to be capable of automatically tracking load variations and correct the output stage amplifier's performance. The worst case measured output power capability of the PA was improved up to 1.3 dB and the BO efficiency by almost 20% using the proposed compensation method for loads varying inside a 2.0 maximum VSWR circle. Under modulated signal excitation, the PA peak output power was improved by 1.4 dB and the average efficiency by more than 10% for the worst case loads.

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