Silicon Micromachined Waveguide Calibration Standards for Terahertz Metrology

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***Abstract*— This article presents precision silicon micromachined waveguide calibration standards for use with terahertz vector network analyzers. This enables the creation of precise, highly repeatable, and traceable terahertz waveguide standards, surpassing the limits of current metrology techniques. A single silicon-on-insulator wafer with the appropriate device and handle layer thicknesses is used to implement a wide range of calibration and verification standards. The design of the standards is discussed from mechanical, electrical, and end-user perspectives. Silicon is shown to be the most promising material for the realization of precision metrology standards. We outline the potential to scale the presented design to at least 2.6 THz. Eight types of WM-570 standard, totaling 15 prototypes, are fabricated and characterized between 325 and 500 GHz. Despite some fabrication anomalies, all devices offer excellent performance. The best micromachined standards offer a return loss in excess of 40 dB, an insertion loss of below 0.1 dB, and a phase error of less than 1°. The standards are utilized in both one- and two-port calibrations, including the multiline through-reflect-line algorithm. These are benchmarked against calibrations performed using conventional metallic standards, with a high degree of agreement observed between error-corrected measurements of a range of test devices.**

***Index Terms*— Calibration, metrology, micromachined waveguide, terahertz, through-reflect-line (TRL), vector network analyzer (VNA).**

I. Introduction

ONCE restricted to niche scientific applications, terahertz technology continues to undergo rapid development in both academic and industrial sectors. The exploitation of the terahertz spectrum (0.3–3 THz) is spurred by improvements in semiconductor technology, packaging, and integration [1]. These advancements enable a range of new applications that make use of the unique properties of terahertz waves, such as sensing and imaging [2], [3]. In light of the continual increase in demand for wireless data, terahertz frequencies are of great interest in high data-rate wireless systems due to the wide swathes of available bandwidth [4]. The terahertz spectrum is predicted to form a key part of the next generation of mobile networks—6G—where this available bandwidth can be combined with new concepts to deliver unprecedented performance [5]. This creates a pressing need for accurate, traceable terahertz metrological instrumentation and components.

The vector network analyzer (VNA) remains the central workhorse of the microwave test and measurement industry. Frequency extension modules extend the upper limit of VNA techniques to above 1 THz. The primary transmission medium at terahertz frequencies is the hollow rectangular waveguide, due to its low loss, mechanical form factor, frequency scalability, manufacturing compatibility, and historical prevalence. Test equipment at terahertz frequencies is built around rectangular waveguides that are typically realized in CNC-milled metallic split blocks, allowing for modular system construction. CNC milling offers $\pm 2.5-\mu$m tolerances at best [6]. Each split block is connected to the other parts of the system via a standardized flange interface. In a VNA test setup, a device under test (DUT) is then connected to the test ports by a similar interface. The mechanical tolerances of these CNC-milled interfaces lead to poor alignment between the DUT and test ports, limiting return loss and dynamic range, while the poor repeatability of such connections creates measurement uncertainty. Misalignment between waveguide flanges is the primary source of error in terahertz VNA instrumentation [7]. The IEEE P1785 standard was formulated to provide recommendations for acceptable dimensions and tolerances of metallic waveguides and flange interfaces, with the aim of improving quality and reducing these errors [8]. In spite of this, waveguide manufacturers often utilize differing flange designs, creating additional sources of misalignment and increasing uncertainty [9].

Prior to characterizing a DUT, the VNA must be calibrated to remove systematic errors from the measured S-parameters. A myriad of calibration techniques exists, each requiring different calibration standards with varying electrical properties. Of these, the through-reflect-line (TRL) algorithm [10] is among the most accurate and popular techniques due to its self-calibration nature and the small number of calibration standards required. By combining the information from multiple line standards in an optimum manner, multiline TRL (mTRL) [11] provides extended bandwidth and improved accuracy over the standard TRL algorithm. mTRL is commonly regarded as one of the most accurate calibration techniques currently available. Both TRL and mTRL require one or

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more precision line standards and a pair of reflective standards and a flush through connection. For TRL, the electrical length of the line standard must be between 20° and 160° across the measured frequency band to avoid instabilities in the calibration, with 90° ($\lambda_g/4$) at the center of the band being optimal. Above 220 GHz, a $\lambda_g/4$ waveguide line has a physical length of less than 0.5 mm and is as low as 48 μm for the WM-106 frequency band (1.7–2.6 THz; see Table I). Such lines are usually realized as "shims"—thin sheets of metal of thickness $\lambda_g/4$ in which the waveguide aperture is formed. This causes two problems. First, metal shims of such low thickness are extremely fragile, making them difficult to manufacture and handle and prone to degradation over time [12]. Second, if manufactured by CNC-milling, their accuracy is limited by the same mechanical tolerances that affect terahertz waveguide flanges. Alternative calibration methods have been proposed to overcome the former limitation, either by replacing the flush through standard with an additional line or by using a pair of $3\lambda_g/4$ line standards in two separate TRL calibrations that are later combined [13]. These approaches are suboptimal and can only be scaled to a certain point before fragility concerns again arise. The latter problem has seen little development. The mechanical properties of metals that are compatible with such processes also hamper their rigidity. Fabrication tolerances also limit the use of other calibration algorithms that require well-known calibration standards and prevent metrological traceability from being established [14]. Scaled to 3.3 THz, the tolerances of the P1785.2a standard result in a worst-case return loss of just 3 dB [15]. Alternative methods for realizing waveguide interfaces and calibration standards are clearly needed.

In [16], we presented a new design of waveguide calibration shim, which seeks to overcome the aforementioned issues, manufactured using silicon micromachining. The design allowed for the use of extremely thin silicon layers without any of the above mechanical concerns. The use of silicon as a mechanical material is well-documented [17]. Silicon has previously been used to realize terahertz packaging [18], integration [19], and wafer probing solutions [20]. Silicon layers can be manufactured with $\pm 0.1-\mu$m thickness uncertainty. In-plane dimensional tolerances of less than 1 μm can be achieved using silicon micromachining techniques, while standard photomask lithography permits positional accuracies and tolerances as low as 0.1 μm. These capabilities far surpass the limitations of traditional CNC milling. Batch processing techniques allow such components to be manufactured in parallel, reducing fabrication costs and increasing product uniformity. These properties make silicon micromachining highly suitable for the implementation of calibration standards, which requires high-dimensional accuracy and uniformity. By combining these attributes with our improved mechanical design, it is possible to create micromachined calibration standards for WM-106 (2.6 THz) and beyond, up until the point at which the silicon layer becomes too thin to withstand the stresses incurred during practical use.

Here, we harness the mechanical properties of silicon and the accuracy of silicon micromachining techniques to create a range of waveguide calibration standards for use at 325–500 GHz (WM-570). We analyze the mechanical and electrical designs of the micromachined calibration standards, describe the fabrication process, and present characterization results from a total of 15 prototype calibration standards. From there, we implement four different calibration algorithms using the micromachined standards and use them to characterize a range of one- and two-port components, including micromachined verification standards.

TABLE I
TERAHERTZ WAVEGUIDE DIMENSIONS

Waveguide	Dimensions	Frequency Range	$\lambda_g/4$ (μm) [1]
WM-864	864 μm × 432 μm	220 – 330 GHz	360
WM-570	570 μm × 285 μm	330 – 500 GHz	239
WM-380	380 μm × 190 μm	500 – 750 GHz	158.5
WM-250	250 μm × 125 μm	250 – 1100 GHz	109
WM-164	164 μm × 82 μm	1.1 – 1.7 THz	73
WM-106	106 μm × 53 μm	1.7 – 2.6 THz	48

[1] Length of ideal Line calibration standard as defined by [21].

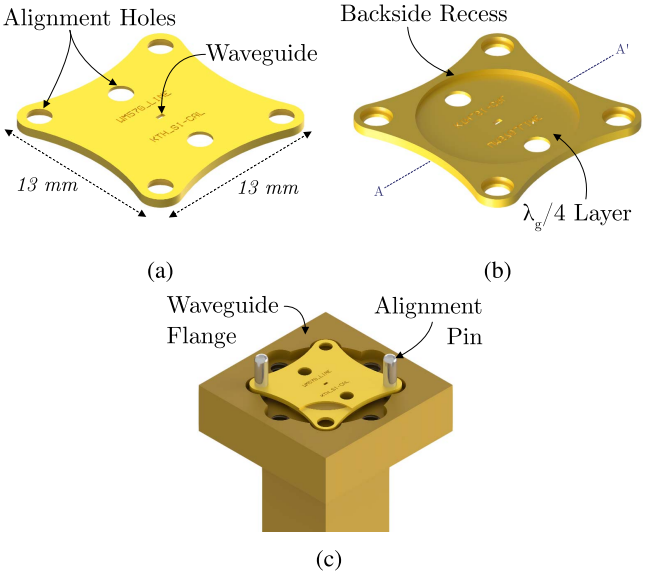

Fig. 1. CAD model of a micromachined $\lambda_g/4$ standard. (a) Front side of the shim with all alignment features. (b) Back side, featuring the large circular recess for the flange inner boss. (c) Standard mounted on a waveguide flange.

II. MECHANICAL DESIGN

A waveguide calibration standard is a physical device, which must be handled by the user and is subject to a range of environmental conditions. The mechanical design of a calibration standard requires balancing its ease-of-use, durability, and interface compatibility with constraints imposed by the properties of its constituent material. Electrical requirements place additional restrictions on the design and geometry of the standard. Here, we outline the proposed micromachined calibration standards from mechanical, electrical, and end-user viewpoints and consider the impact of the above criteria.

TABLE II
MECHANICAL PROPERTIES OF TERAHERTZ WAVEGUIDE MATERIALS

Material	E (GPa)	ν (-)	σ_y (MPa)	σ_u (MPa)	CTE (ppm/°C)	K_{Ic} (MPa$\sqrt{\text{m}}$)
Silicon [22]	**130-185**	**0.22-0.27**	**N/A**	**7000**	**2.6-3.3**	**0.8-1**
Aluminium [23]	69	0.34	24-480	76-540	16-26	20-50
Brass [23]	82-117	0.34	34.5-683	124-1030	18-26	24-90
Steel [23]	200	0.25	350	420	9.5-12.6	100-250
Gold [23]	77.2	0.42	20-205	100-220	13.5-14.5	40-90
Copper [23]	128	0.308	33.3	209	16-16.7	40-100
Su-8 [24]	4.02	0.22	34	-	21-102	-
ABS [25]	2	0.36	30	30	72-108	1.2-4.2
PC [25]	1.8	0.36	35	48	65-70	2.0-2.2

A. Mechanical Properties of Silicon

Table II summarizes the mechanical properties of common waveguide materials. Silicon offers a combination of high Young's modulus (E), low Poisson ratio (ν), and low coefficient of thermal expansion (CTE), which makes it highly suited to precision metrology applications. A high Young's modulus provides silicon components with greater stiffness, reducing potential deflection. Silicon is a brittle material, as reflected by its low fracture toughness (K_{Ic}), meaning that it will shatter when its ultimate tensile/compressive strength (σ_u) is exceeded. Ductile materials, such as common metals, deform plastically under stress, which exceeds their yield strength (σ_y). Silicon offers a significantly higher ultimate tensile strength than most metals, with no yield strength. As such, a metallic component will become deformed under applied force long before an equivalent silicon component would shatter. Silicon's low Poisson ratio limits in-plane deformation due to out-of-plane loads. In the context of waveguide systems, this eliminates potential change in the waveguide's cross-sectional dimensions when clamped to a flange interface. The low CTE of silicon improves the thermal stability of waveguide components, reducing dimensional variations due to temperature shifts. This is highly desirable for calibration standards, the electrical properties of which should ideally be time-, temperature- and humidity-invariant.

The other materials in Table II can be classified into two distinct groups: metals and polymers/plastics. Although metals can offer similar mechanical properties to silicon, they are inherently limited by their relatively low yield strength and high CTE. Of these, only certain alloys are suitable for processing with precision CNC milling tools. Some metals also have electrical limitations, as their low conductivity results in higher waveguide losses. Surface roughness created by the milling process adds additional loss. Fabricating CNC milled waveguides in an alloy, which is amenable to milling and later depositing an additional high conductivity layer, is an established workaround to balance mechanical and electrical concerns. Polymer materials, such as plastics, resins, and rubbers, have low Young's moduli and yield/tensile strengths. These materials have become relevant for RF applications with the advent of 3-D-printing techniques. Their mechanical characteristics make them unsuitable for our current application. Numerous composite materials have been developed to allow for 3-D-printing of metals. Despite an improvement over regular polymers, their performance is limited by that of the embedding medium [25]. However, 3-D-printing techniques are yet to achieve the level of precision available in micromachining processes, with tolerances of up to 10 μm reported in [26], and are, thus, not suitable for terahertz frequencies. Several attempts to realize micromachined calibration standards have been published [27], [28], based on electrodeposition of nickel in a thick photoresist mold, with dimensional tolerances as high as 10 μm. A review of the electrical performance of various terahertz waveguide and packaging technologies based on the above materials can be found in [19].

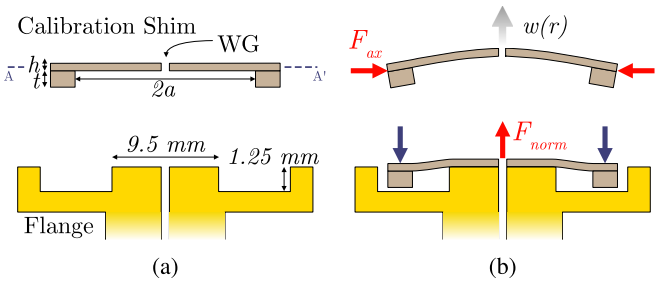

Fig. 2. Cross section schematic of the calibration shim design. (a) Geometrical parameters. (b) Uniaxial (F_{ax}) and normal (F_{norm}) forces applied to shim during use.

B. Calibration Standard Design

A simple waveguide $\lambda_g/4$ line can be created by etching a silicon wafer of a suitable thickness, similar to [29]. This approach is not feasible above 500 GHz as silicon layers of such thickness are challenging to handle and prone to damage during use. To overcome this limitation, we propose an alternative design of calibration standard, first reported in [16] and illustrated in Fig. 1. Our design comprises a thin layer, which is mechanically suspended across a recess in a thicker supporting layer, creating a large circular diaphragm. The presence of the supporting layer prevents axial forces (F_{ax}; see Fig. 2), which arises when the user handles the device, from causing the diaphragm to bend. This greatly simplifies the handling of the standard and eliminates a potential failure mode. A normal force is exerted on the diaphragm by the face of the inner flange boss (F_{norm}). This occurs when the user mounts the standard to the flange, pressing the diaphragm

against the inner flange boss. The diaphragm must be designed such that the stress resulting from F_{ax} and F_{norm} does not cause it to break or deform. In addition to overcoming the mechanical limitations of current designs, our design utilizes the benefits of silicon-on-insulator micromachining to allow the creation of calibration standards up to 2.6 THz without the need for any postfabrication alignment or assembly.

The deflection of a circular diaphragm under uniform pressure at distance r from its center can be described by

$$w(r) = w(0)\left(1 - r^2/a^2\right)^2; \;\; w(0) = pa^4/64D \tag{1}$$

$$D = \frac{Eh^3}{12(1-\nu^2)} \tag{2}$$

where a is the diaphragm radius, p is the applied pressure, D is the flexure rigidity, and h is the diaphragm thickness [30]. The flexural rigidity of silicon diaphragms is similar to that of common metals [see Fig. 3(a)]. Deflection alone does not cause degradation of the diaphragm. If the stress generated in the diaphragm made of a ductile material is below σ_y, any deformation will be elastic, and the diaphragm will return to its original shape upon removal of the applied force. Brittle materials, such as silicon, deflect elastically until σ_u is reached and the material fails. The stress in the diaphragm is at a maximum along its circumference ($r = a$) and has both radial (T_r) and tangential (T_t) components, as defined by

$$T_r = \frac{3}{4}\frac{a^2}{h^2}p; \;\; T_t = \frac{3}{4}\nu\frac{a^2}{h^2}p. \tag{3}$$

T_r is independent of the materials intrinsic E and ν and depends only on the geometry of the diaphragm. As $\nu < 0.5$ for isotropic solid materials, $T_t < T_r$. The design of the diaphragm, therefore, requires the choice of a suitable a/h such that T_r does not exceed the yield/tensile strength of the material. The maximum force that can be applied to the diaphragm can be determined from

$$F_{\max} = \frac{4}{3}\frac{h^2}{a^2}\sigma_y A = \frac{4\pi}{3}h^2\sigma_y \tag{4}$$

where A is the area of the diaphragm. The maximum force $F_{\max}$ for diaphragms with $h = \lambda_g/4$ (see Table I) over σ_y/σ_u is plotted in Fig. 3(b), where $a = 4.85$ mm. The relevant tensile/yield strengths of several relevant materials (see Table II) are indicated. $F_{\max}$ is at least an order of magnitude greater for silicon diaphragms. At the highest frequencies of interest, where $\lambda_g/4 = 48$ µm, $F_{\max}$ is of the order of a few Newton for the metals shown, making metal diaphragms overly fragile for practical use. Polymer- or resin-based implementations of the proposed design offer insufficient $F_{\max}$ to be feasible. Fig. 3(b) confirms the scalability of the proposed silicon micromachined calibration standard design to frequencies above 1 THz, as such thin diaphragms can withstand normal forces of over 60 N.

The above discussion sets clear limits on a for a given h, σ_u/σ_y and ν. Thickness h defines the physical length of the waveguide. This, in turn, corresponds to a certain electrical length depending on the waveguide's cross-sectional dimensions. VNA calibration algorithms require standards of varying electrical lengths (see Section IV-C), restricting h.

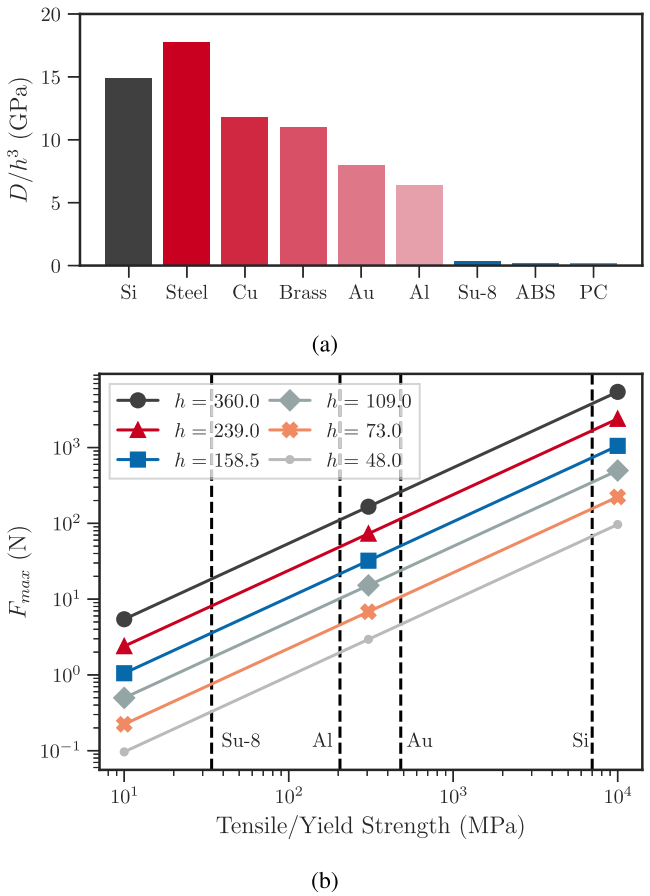

Fig. 3. (a) Diaphragm flexural rigidity for the materials listed in Table II. (b) Maximum force $F_{\max}$ of the a circular diaphragm against tensile/yield strength σ_u/σ_y of its constituent material. $a = 4.85$ mm.

We are, thereby, not free to choose h in order to control the mechanical characteristics of the diaphragm. According to (3), a should be minimized to reduce the T_r and, hence, increase $F_{\max}$. This implies making the calibration standard as small as possible. The minimum a is defined by the diameter of the inner waveguide flange boss, as the backside recess must fit around it. From an end-user perspective, reducing a makes the standard more difficult to handle. The curved outline of our design improves its ergonomics. In addition, this shape ensures that the waveguide flange screws do not interfere with the standard. Our design contains all six waveguide flange alignment holes prescribed in the IEEE 1785.2a standard [8], allowing it to be used with regular waveguide flanges. Elliptical holes [29] are utilized for both inner and two of four outer alignment holes and are designed to provide a 99.5% probability of fitting. The remaining two outer alignment holes are circular and are oversized to allow the insertion of a pair of alignment pins without binding. By accounting for the worst case tolerances of both the inner and outer pins, this design allows for their simultaneous use, with an expected maximum misalignment between the micromachined standard and waveguide test port of 5.75 µm in the devices reported here, where the alignment pins have a nominal diameter

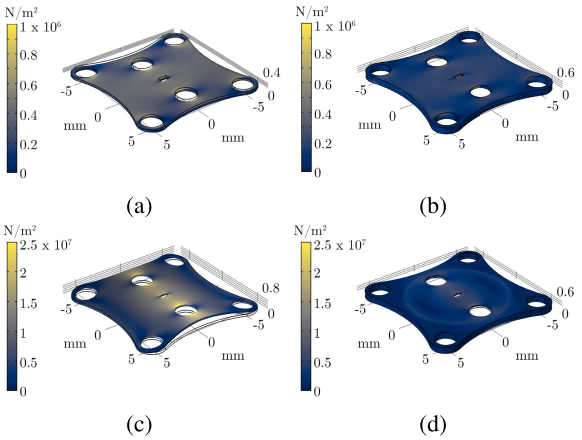

Fig. 4. Von Mises stress and deformation of the proposed design (b) and (d) with and (a) and (c) without the thick supporting structure for 1-N applied (a) and (b) uniaxial and (c) and (d) normal force. Deformation scaled by (a) and (b) 1000, and (c) and (d) 100. $h = 218$ μm, $t = 381$ μm, $E = 169$ GPa, and $\nu = 0.27$.

of 1562 μm and expected dimensional tolerance of (−13, +0 um) and the alignment holes a diameter of 1567 μm.

The addition of the waveguide aperture and alignment holes in the diaphragm creates discontinuities in the diaphragm, leading to local stress maxima. To verify that these stresses do not exceed the limits defined above and demonstrate the efficacy of our design, we performed a finite element analysis of the mechanical structure. COMSOL Multiphysics was used to simulate the deflection and resulting stress of a pair of calibration shims under load (Fig. 4); the first being a conventional single-layer shim of thickness $h = 218$ μm [Fig. 4(a) and (c)] and the second our proposed design of equal h and with $t = 381$ μm [Fig. 4(b) and (d)]. These parameters match the WM-570 prototype devices reported here (see Section V). The deflection was evaluated at the center of the shim. Two edges of the shim were pinned; the remaining edges were unsupported. E and ν of 169 GPa and 0.27 were assumed, with an applied force of 1 N. Normal loads were applied to the same circular area to ensure that the applied pressure was equivalent in both cases. Under uniaxial load F_{ax}, the single-layer design deflected by 0.17 μm, corresponding to a spring constant of 6.15e6 N/m. The deflection of the diaphragm design was 0.026 μm, giving k of 3.8e7 N/m, almost an order of magnitude greater. The maximum stress σ_{max} was 0.9 and 0.46 MPa in each case. Normal loading of each structure lead to greater deflection: 7 μm ($k = 1.4$e5 N/m) and 1.35 μm ($k = 7.39$e5 N/m), respectively. Again, $\sigma_{\max}$ is reduced, from 32.3 to 10.2 MPa.

III. Fabrication

An overview of the fabrication of the proposed silicon micromachined calibration shims was provided in [16]. Deep reactive ion etching (DRIE) is used to define the geometry of all calibration standards. The use of a standard silicon wafer to create line standards is limited to frequencies below 500 GHz. Etching an offset-short waveguide in a standard silicon process will result in a curved backshort with significant surface roughness [31]. A similar effect occurs if the structure shown in Fig. 2(a) is etched, leading to a large curvature at the bottom of the recess etch [see Fig. 5(a)]. This curvature creates a gap between the surface of the resulting shim and the waveguide flange to which it is connected. This gap and the high surface roughness create a poor ohmic contact between the shim and flange. Our approach relies on the use of SOI wafers to alleviate these issues. SOI wafers with device layer (DL), buried oxide (BOX), and handle layer (HL) thicknesses of (218±2) μm, 1 μm±5%, and (381±7) μm, respectively, are used throughout [see Fig. 5(b)]. The electrical length of the standards is determined by the thickness of the various layers alone; no control over etch depth is required. This configuration equates to waveguides with electrical lengths of 84° (DL), 147° (HL), and 231° (DL + BOX + HL) at 415 GHz. All geometry is defined in 2-μm-thick oxide hard masks, which are patterned using standard photomask lithography. Alignment holes are patterned in both layers. DRIE etching of the DL and HL creates the required features on each chip. The BOX layer acts as an etch stop during DRIE. This leaves a flat, optically polished surface on both sides. Wet etching with hydrofluoric acid removes the oxide masks post-DRIE and underetches the BOX layer, creating a gap between the waveguide sidewalls and backshort in one-port standards. Sputter deposition of 1.25 μm of gold ensures that this gap is filled and connects the various parts of the waveguide. As the layers of the SOI wafer are bonded together, no postfabrication assembly is necessary. Layer–layer alignment depends only on the alignment of the backside photomask during lithography.

Aspect ratio-dependent etching (ARDE) is a well-known phenomenon, which occurs in all deep silicon etching processes [32]. ARDE causes the sidewalls of an etch to vary in angle depending on its area, creating waveguides with tapered geometries [see Fig. 2(b)]. This makes the waveguide nonsymmetrical and changes its electrical parameters. Tapered waveguide calibration standards have different reference impedances, depending on which side of the taper is connected to each test port. The tapering causes a deviation from the expected S-parameters of the standard, leading to poor error correction if used with nonself-calibration algorithms. A sidewall angle of 5° results in a simulated worst-case return loss of as little as 25 dB and transmissive phase difference of 7° (see Fig. 6). Reducing the sidewall angle to below 1° improves these values to 45 dB and 1°, respectively, highlighting the importance of limiting undesired tapering. The angle and direction of the sidewalls depend on multiple process parameters and limit the repeatability of repeated fabrication runs. ARDE can be minimized, but not eliminated, by carefully controlling the DRIE process parameters. In [33], we introduced a new concept to simultaneously eliminate multiple ARDE related DRIE nonidealities. This is achieved by using releasable filling structures (RFSs) to restrict the aspect ratio of the etch. Additional areas of dummy silicon are placed inside all etched features, reducing the width and area of the etch [see Fig. 2(c)]. These serve no electrical purpose. The filling structures are mechanically isolated from the remainder of the standard in both the DL and HL and are, thus, connected only via the BOX layer. They are released in the post-DRIE

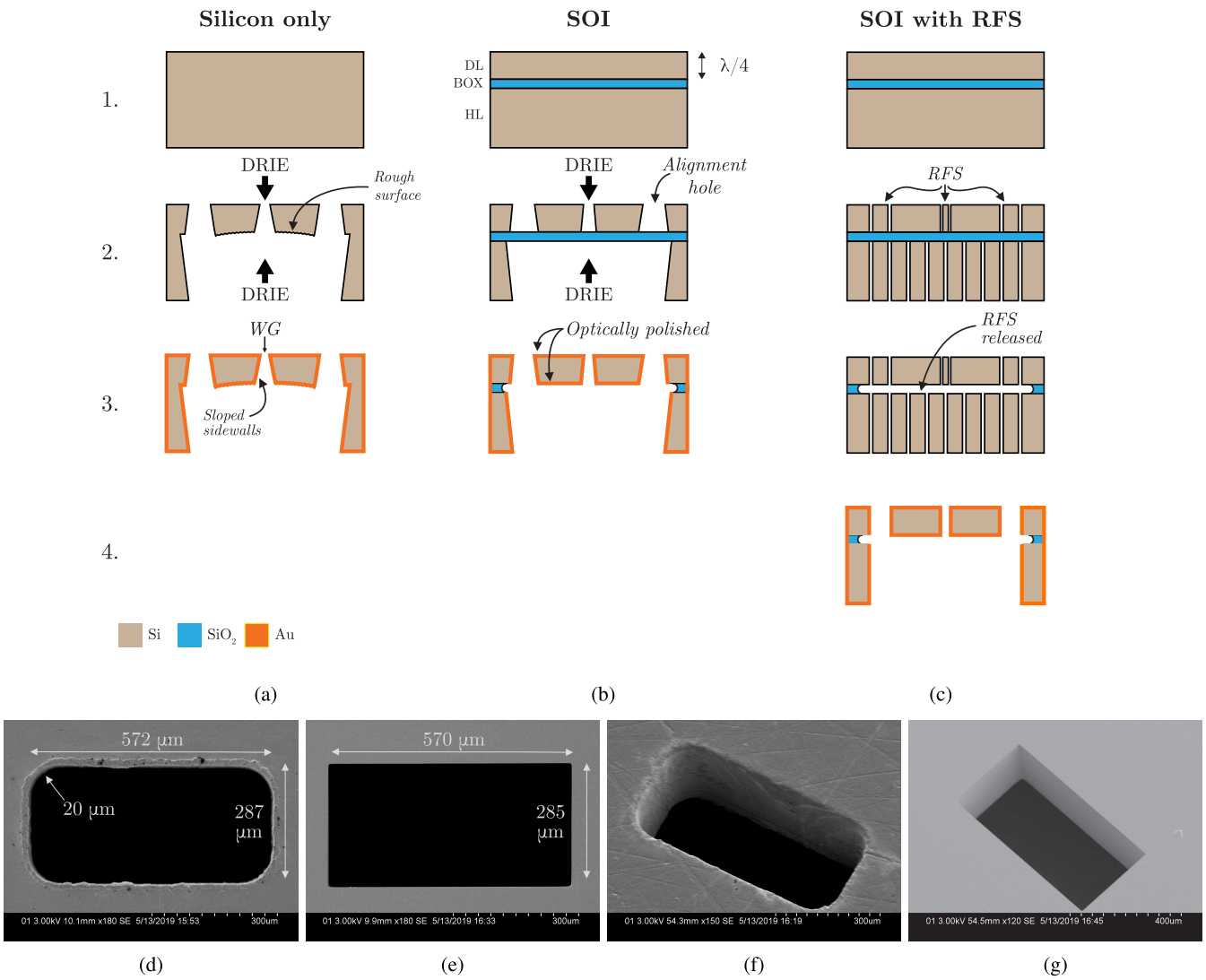

Fig. 5. Fabrication process flow for calibration shims realized using (a) standard silicon wafer, (b) SOI wafer, and (c) SOI wafer with RFSs. 1—Initial wafer layer stack. 2—DRIE etching of the required features. 3/4—Wet etching and metallization of the final shim. (d)–(g) SEM images of (d) and (f) metallic VDI and (e) and (g) micromachined line 0 $\lambda_g/4$ standards.

wet etching step and simply fall out, leaving the remainder of the device intact. The width of the trench formed by the addition of the filling structures can be modified to control the aspect ratio of the etch, allowing for localized control of the sidewall profile if desired. We utilized this approach to reduce the sidewall angle in a 1651-μm-wide waveguide from 4° to almost 0° [33]. Filling structures are implemented in all etched features in this work. This drastically reduces the effects of ARDE and leads to near-ideal geometries.

In Section V, we document the performance of prototype micromachined standards and compare them to traditional metallic ones. The aperture dimensions of both types of $\lambda_g/4$ shim were verified using scanning electron microscopy [SEM; see Fig. 5(d)–(g)]. An in-plane tolerance of 2 μm and corner rounding of 20 μm was observed in the metallic shim, while the tolerances of the micromachined shim were too small to accurately measure via SEM. Upon inspection, BOX residues were clearly visible on the bottom of the circular recess in several micromachined devices (see Fig. 7). These can be removed by increasing the length of the wet etch step in future fabrication runs. The effect of these residues on the performance of the shims is discussed in Section V. Section IV describes the various calibration standards, which can be realized in a single SOI wafer.

IV. RF Design

A. Calibration Standards

1) Waveguide Standards: Fig. 8 details the various calibration standards that can be implemented using the SOI technology outlined in Section II. Here, the $\lambda_g/4$ line standard is denoted line 0. Additional line (lines 1 and 2) standards can be implemented by etching the waveguide aperture in the SOI's HL or in both handle and DLs. Reflective standards are formed by omitting the waveguide aperture from a given layer and can be connected to both ports simultaneously.

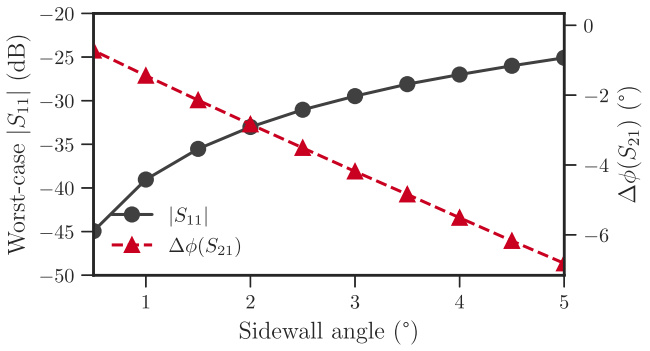

Fig. 6. Worst-case reflection coefficient and phase deviation resulting from tapering of the line 0 standard's sidewalls.

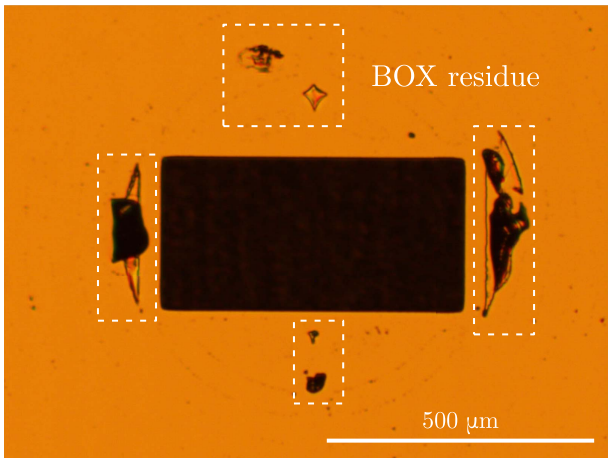

Fig. 7. Residues of the BOX layer on the bottom of the DL of a line 0 sample.

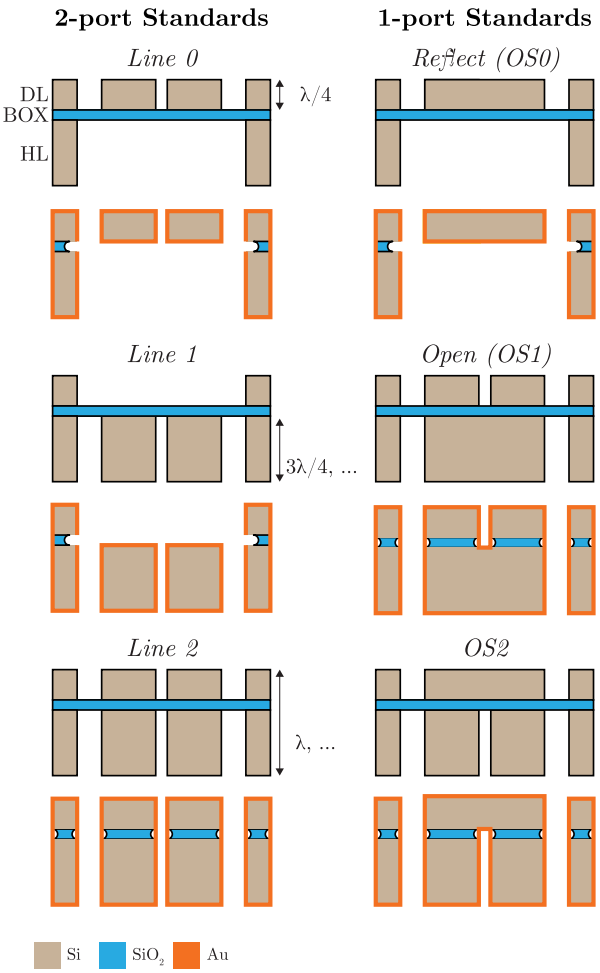

Fig. 8. Cross-section schematic of the possible calibration standards, which can be realized in the silicon-on-insulator technology presented here.

A flush short circuit [Reflect (OS0)] using the DL alone has the advantage of being of equivalent thickness to the line 0 standard. This allows for the test ports to be equidistant during both measurements and eliminates excess movement of the RF/LO cables in the test set, a known source of error when using frequency extender modules [12]. Offset-short standards are created in a manner analogous to lines 0 and 1, utilizing either DL (OS1) or HL (OS2) as the waveguide section and the nonetched layer as the backshort. Crucially, the presence of the BOX layer ensures that the bottom of the waveguide aperture is flat. Offset-short waveguides fabricated by this method are, thus, highly uniform and repeatable, with near-ideal geometry. This eliminates the need for EM simulation or modeling of an offset-short to accurately determine its reflection coefficient.

2) Radiating Opens: Radiating opens have historically been used as 1-port verification devices to verify the calibrated reference impedance but have gained new relevance as alternative one-port calibration standards. Liu and Weikle [34] developed a calibration algorithm, which is insensitive to flange misalignment, as it uses a radiating open standard to define the reference impedance of the calibration. Williams [7] investigated the application of this calibration to terahertz frequencies, noting that such calibrations can offer better performance if the radiating open is sufficiently precise and accurate. This approach was later developed to a full two-port calibration [35]. Its accuracy in practice is limited by errors in the predicted response of the radiating open standards. The presence of burrs, flange alignment pins, and other flange features alters a radiating open's reflection coefficient and limits the accuracy of closed-form models [36]. Hence, the ability to fabricate waveguide apertures that are free from burrs and highly accurate is of great appeal.

In lieu of a fully micromachined waveguide interface, we propose the use of calibration standards, connected to the test port, to create a well-known radiating open, which is free from defects. Provided that the alignment of the standard to the test port is sufficiently repeatable and radiation from its aperture can be accurately modeled, this offers an alternative radiating open standard with an equivalent Z_0 to the other micromachined standards. We developed a simulation model in CST Microwave Studio for the calibration shim design presented here to account for the reflections from the various features on the surface of the chip. The simulated reflection coefficient shows good agreement with the Legendre polynomial model of [36] [see Fig. 17(a)]. An additional simulation of the waveguide flange without the micromachined standard shows similar agreement. Sufficient computing power was

not available to simulate a model, which included alignment pins. Use of the radiating open standard in practical VNA calibrations is outlined in Section V-E.

B. Verification Standards

In addition to the one- and two-port calibration standards outlined above, precision verification standards are also required. Transmissive standards, such as precision airlines, are the most common verification standard in coaxial setups, as their S-parameters can be accurately predicted *a priori* [37]. In rectangular waveguide systems, hollow waveguide sections can be used as verification standards. However, at terahertz frequencies, accurately realizing such standards is extremely challenging, as previously outlined. Dimensional inaccuracies affect the impedance of the waveguide, while surface roughness and conductivity effects influence its insertion loss. Furthermore, in low-loss waveguide devices, attenuation standards may require physically large devices, which is undesirable from a practical viewpoint. For these reasons, alternative verification standards, such as cross-waveguides [38], reconfigurable waveguides [39], and mismatch shims [40], have been proposed. Cross-waveguide sections can easily be realized using the techniques described here and require a simple rotation of the rectangular waveguide aperture relative to the body of the shim. A cross-waveguide device allows verification of both transmission and reflection measurements. As the cross-waveguide acts in a similar manner to a standard rectangular waveguide below cutoff, evanescent propagation between the two ports of the device occurs. The attenuation can be predicted provided that the physical length of the device is accurate.

Three unique cross-waveguide lengths, providing three distinct levels of attenuation, can be realized from a single SOI wafer by utilizing the same layer scheme described above. Precision layer thicknesses available in micromachining processes can provide highly precise, accurate verification standards. Two-port calibrations can also be verified using any of the standards described in Section IV-A, which are not used during calibration of the VNA. The repeatability of these verification standards matches that of the calibration standards as they are co-fabricated on the same wafer, and identical elliptical alignment holes are used throughout. Several copies of the shortest cross-waveguide (218 μm, DL, Fig. 9) were included in the same photomask set used for the calibration standards. Their performance was verified using a range of calibrations, as described in Section V.

C. Complete Calibration Kits

Through careful selection of the layer thicknesses and combinations outlined above, device subsets suitable for various calibration algorithms can be created. By means of example, potential calibration kits and their corresponding standards include the following.

1) *TRL:* Flush through, OS0, and line 0.
2) *mTRL:* Flush through, OS0, line 0, line 1, line 2, …, line *N*.

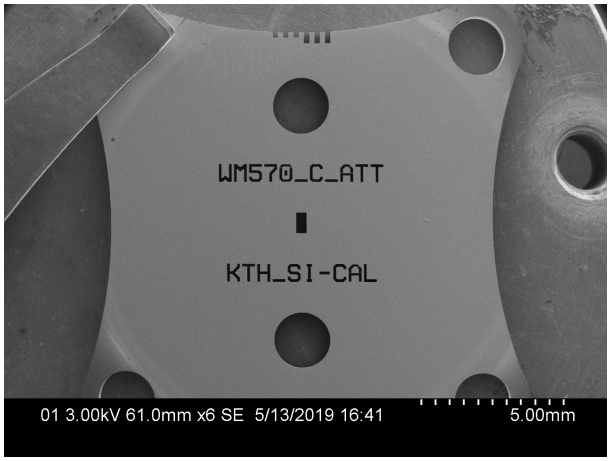

Fig. 9. SEM image of a fabricated cross-waveguide verification standard.

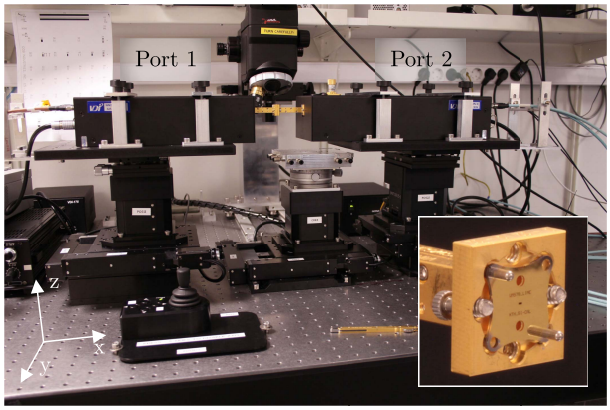

Fig. 10. Experimental setup used for device characterization. An image of a line 0 standard mounted on the test port is shown inset.

3) *12-Term:* OS0, OS1, OS2, …, OSN, or load, flush through.
4) *Short-Delay-Delay-Load (SDDL [34]):* OS0, OS1, OS2, radiating open, or load.

Using SOI wafers makes it possible to realize complete calibration kits from a single wafer, as three unique physical lengths and, thus, six distinct standards can be implemented (see Fig. 8). Multiple wafers with varying DL/HL thicknesses can be used to implement an arbitrary *N* standards. We designed a photomask set containing multiple line 0, line 1, line 2, OS0, OS1, and OS2 standards for the WM-570 waveguide band. The experimental performance of each standard and its use in one- and two-port calibrations are documented in Section V.

V. RF Characterization

The performance of all components was evaluated by connecting them to standard WM-570 waveguide test ports, driven by a pair of Virginia Diodes Inc., (VDI) frequency extenders connected to a Rohde & Schwarz ZVA-24 VNA. All measurements were performed using 1-kHz VNA IF bandwidth, 1001 frequency samples, and no averaging. Motorized platforms were used to position both frequency extenders

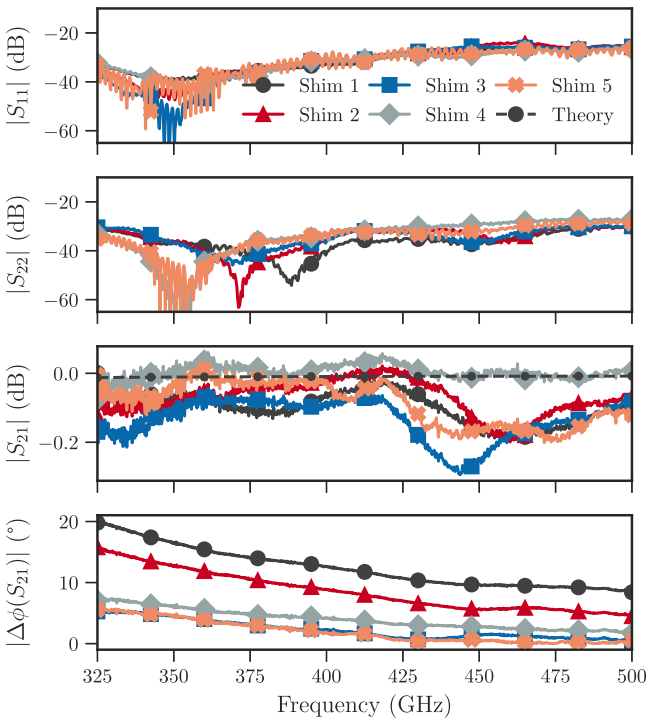

Fig. 11. Error correct S-parameters of the five line 0 prototypes, calibrated with the VDI $\lambda_g/4$ line standard. $\Delta\phi(S_{21})$is the phase difference between the measured and theoretical responses.

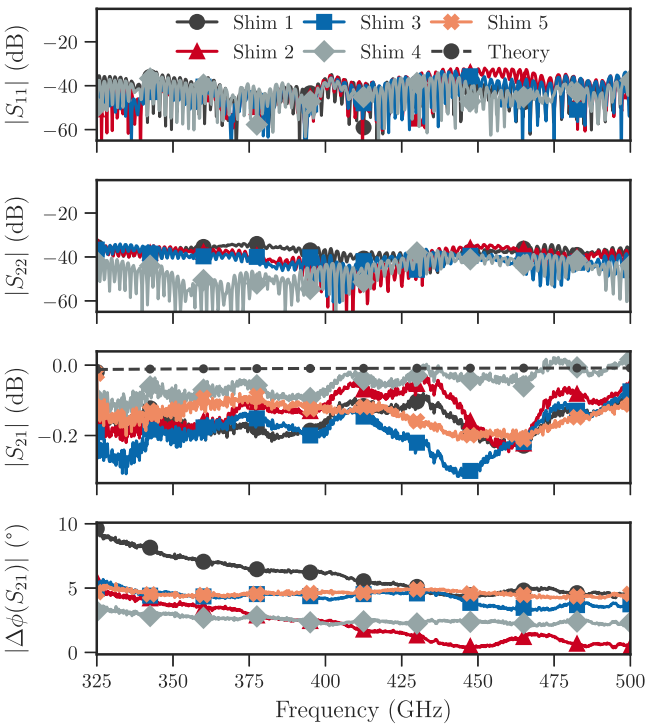

Fig. 12. Error corrected S-parameters of the five line 0 prototypes, calibrated with a line 0 line standard.

(see Fig. 10). Following the initial alignment of the system, the extender connected to port 1 remained fixed. Only port 2's frequency extender was moved during characterization in order to reduce cable flexure effects. The alignment between waveguide flanges was consistent throughout as test port 2 was moved uniaxially in x. Two types of calibration standards were used during measurement: commercial metallic standards from VDI and prototype silicon micromachined standards. A TRL calibration using the VDI standards was performed at regular intervals to act as a reference. The metallic calibration standards were previously used. Some discrepancy in their performance may have occurred as a result of previous use. A waveguide short circuit from this calibration kit was used to fasten the 1-port micromachined standards to the test ports. The use of a torque wrench (Rohde & Schwarz ZCTW) ensured repeatable contact between the test port and DUT. Additional errors, including thermal and LO drift, were not accounted for. However, we found that the technique suggested in [41] to correct false nonreciprocity provided significantly better agreement of $\phi(S_{21})$ to theoretical models, with much less ripple in the measured results. As such, we applied the correction $\bar{S_{12}} = \bar{S_{21}} = (S_{12} + S_{21})/2$ to all error-corrected S-parameters.

Proof-of-concept error correction was performed on the S-parameters of a separate waveguide line (VDI WM570, 1 in) and several micromachined verification standards. This waveguide line is a traditional CNC milled split-block assembly and is gold plated. Theoretical responses were determined using the relevant methods in scikit-rf, an open-source python module for RF engineering, or CST microwave studio. All calibration and data processing were performed in scikit-rf. Effective conductivity of $\sigma = 2.1\text{e}7$ S m^1 was assumed for all micromachined components based on values extracted from our previously reported work [42].

A. Verification of Prototype Devices

1) Two-Port Standards: Five $\lambda_g/4$ line 0 shims from a single wafer were characterized using the aforementioned setup and VDI TRL calibration. The micromachined shims have return loss greater than 25 dB across the band, with below 0.2 dB of insertion loss (see Fig. 11). The accuracy and precision provided by micromachining processes and the repeatability of the elliptical alignment hole method [29] ensure that the performance of the shims is largely similar. The insertion loss is somewhat higher than expected for all but Shim 4. We attributed this increase to a small gap between the DUT and test ports due to the residues of the BOX layer around the waveguide aperture (see Section III). This gap creates a virtual open circuit at $\lambda_g/2$ (460 GHz), leading to the sharp dip in $|S_{21}|$ around this frequency. The similarity of S_{11}/S_{22} indicates that the micromachined waveguide has the same cross-section on both sides, while their resonant nature suggests a difference in test port/DUT aperture dimensions in both the E- and H-planes [43]. The negative slope of the discrepancy in phase to the theoretical waveguide line ($|\Delta\phi(S_{21})|$; see Fig. 11) is the result of a difference in γ between the VDI Line and the micromachined standards. Shim 3's electrical length at 433 GHz is within 2.5° of its expected value. Some uncertainty in $\phi(S_{21})$ due to poor contact repeatability between DUT and test ports, caused by the BOX residues, was observed and may influence $\Delta\phi(S_{21})$. The mean reflection

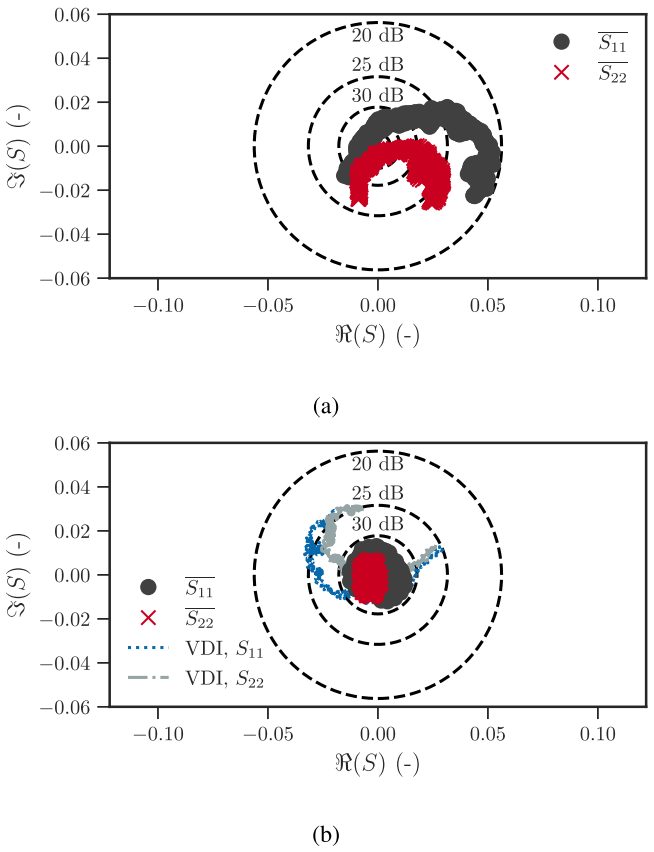

Fig. 13. Mean response of the five line 0 shims. (a) VDI TRL calibration. (b) Line 0 TRL calibration. The response of the VDI line under this calibration is also shown. Circles of constant return loss are plotted for reference.

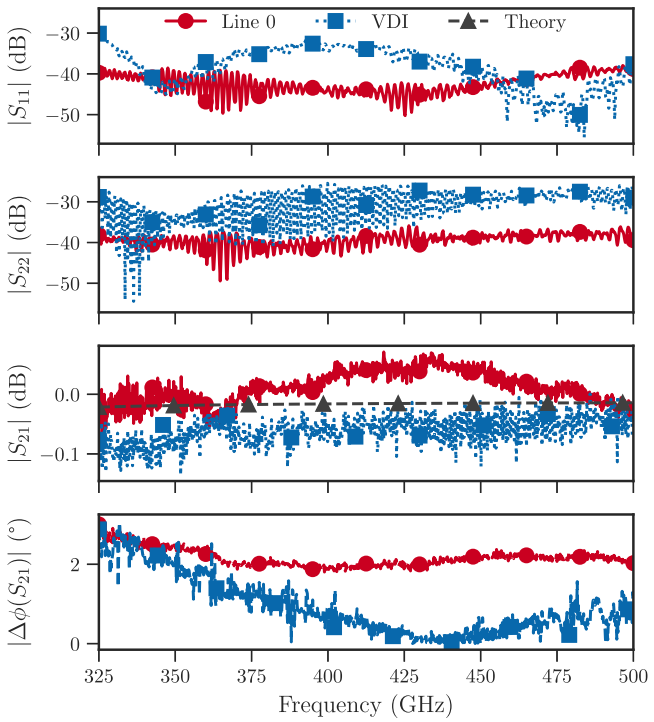

Fig. 14. Measured S-parameters of a line 1 standard, error corrected with line 0/VDI TRL calibrations. The theoretical insertion loss of a 381 μm long waveguide with $\alpha = 2.1\text{e}7$ S m^1 is also shown. $\Delta\phi(\bar{S_{21}})$ is the phase discrepancy to the theoretical value.

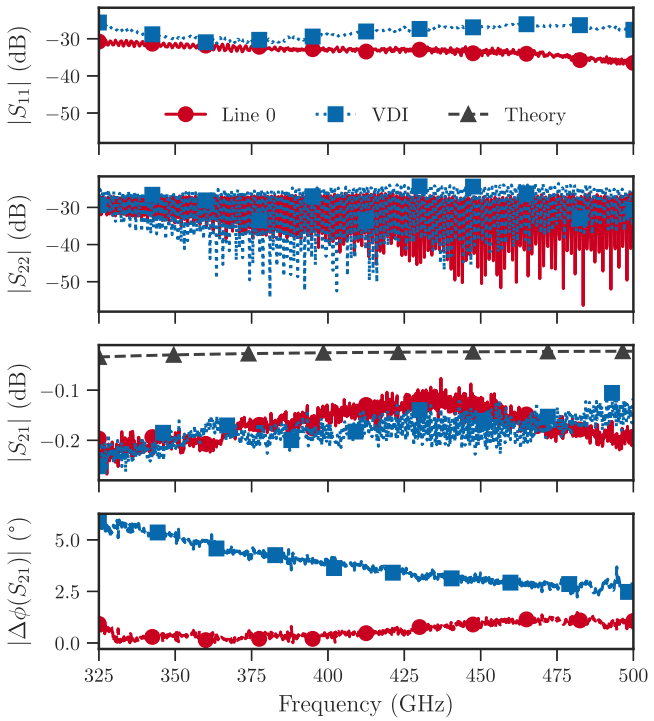

Fig. 15. Measured S-parameters of a line 2 standard, error corrected with line 0/VDI TRL calibrations. The theoretical insertion loss of a 600 μm long waveguide with $\alpha = 2.1\text{e}7$ S m^1 is also shown. $\Delta\phi(\bar{S_{21}})$ is the phase discrepancy to the theoretical value.

coefficient of the five line 0 shims is plotted in Fig. 13(a). A net positive admittance exists for all frequencies in S_{22}. The quadratic dependency of the shunt capacitance created by an E-plane offset creates a nonzero net admittance between test port and DUT [7]. Γ crosses zero at low frequencies, as the capacitance introduced by an E-plane offset is canceled out by an inductance resulting from an H-plane offset or rotation of the DUT. The real component of the reflection coefficient is primarily affected by differences in the impedance of the test ports/DUTs. These differences also impact the reference impedance of calibrations performed using both metallic and micromachined standards. Corner rounding of the VDI line's waveguide aperture (see Fig. 5) corresponds to an effective reduction in aperture width of 1.2 μm, leading to an increase in Z_0 of 2.6 Ω at 325 GHz [44], where the relative change in Z_0 is greatest.

Following initial verification, the data from Shim 5 were used to create a new TRL calibration. To allow for direct comparison, all other calibration measurements were reused from the VDI TRL calibration, meaning that any difference is a result of the line standard alone. Changing the line standard leads to a drastic change in the error-corrected S-parameters of the line 0 prototypes (see Fig. 12). As the reference impedance of the TRL calibration is defined by the line standard, the return loss of the shims is improved significantly. The return loss at both ports is over 40 dB at most frequencies and is flat across the band. Assuming that all five shims are identical, their return loss should be infinite under this calibration when measured with test ports of the same

dimension. In practice, it is limited by repeatability, misalignment, and any discrepancy in calibration/test port impedances. Shims 3–5 show good agreement with their theoretical phase response, with $|\Delta\phi(S_{21})|$ being flat across the band as the waveguide's β is correctly determined. The electrical length of Shim 2 at 433 GHz is 89.4° (<1% error) although its β deviates from the theoretical value. The alignment accuracy of the micromachined shim results in a much tighter spread of S_{ii} in the complex plane [see Fig. 13(b)]. As S_{ii} are almost purely real, we conclude that the behavior seen in Fig. 13(a) is the result of misalignment of the metallic line standard. This conclusion likens that of Williams [7], who ascribed the observed misalignment to the oversized alignment holes in metallic shims. Error correction of the VDI line standard using this calibration provides further evidence of dimensional mismatch and misalignment between the two standards: the locus of S_{11}/S_{22} comprises a significant imaginary component and is offset from the center of the complex plane [see Fig. 13(b)]. The return loss of the VDI standard is better than that of Fig. 13(a), with a maximum value of 24 dB.

A similar comparative set of calibrations was applied to the measured S-parameters of a line 1 and line 2 prototype. All measurements' bars of the line standard were shared between calibrations. As before, the change of line standard causes a noticable improvement in the return loss of both lines 1 and 2 (see Figs. 14 and 15). The flatness of $|S_{ii}|$ is also notable. Under the line 0 TRL calibration, $|S_{21}|$ of line 1 is greater than its theoretical value and also exceeds zero at certain frequencies, which is a nonphysical result. This is due to the high α of line 0, which is used to correct line 1's S-parameters. As it is the longer of the two waveguides, and both are fabricated from the same wafer, one would expect line 1 to have higher insertion loss. However, line 1 did not contain any observable BOX residues and, thus, did not suffer from the gap experienced by line 0. Line 1, thus, has lower insertion loss than line 0, leading to the observed result. The curvature of its insertion loss broadly matches that of Shim 5 in Fig. 12, with which it is calibrated. $|\Delta\phi(S_{21})|$ is within 3° of its theoretical value for both calibrations but is seen to vary with frequency for the VDI calibration.

Line 2's return loss is higher than that of the other two lines, while its insertion loss is also greater than expected. This increase in loss is due to poor metal coverage along the sidewalls of the BOX area. A complete absence of metal would create a 1 μm gap between the waveguides in the DL/HL and may contribute additional reflections, decreasing return loss. The envelope of line 2's insertion loss matches that of Shim 5, for the same reasons as previously discussed. A phase discrepancy of less than 1.25° occurred, and $|\Delta\phi(S_{21})|$was found to be largely flat across all frequencies, indicating the proper determination of β during calibration and high-dimensional accuracy.

Given that the TRL calibration using line 0 has been shown to work well, characterization results of the remaining prototypes are shown under this calibration only. Applying the VDI TRL calibration to the remaining results leads to much the same conclusions as above. These data are, therefore, excluded here for the sake of brevity. Application of the micromachined TRL calibration to nonmmicromachined devices is discussed in Section V-B.

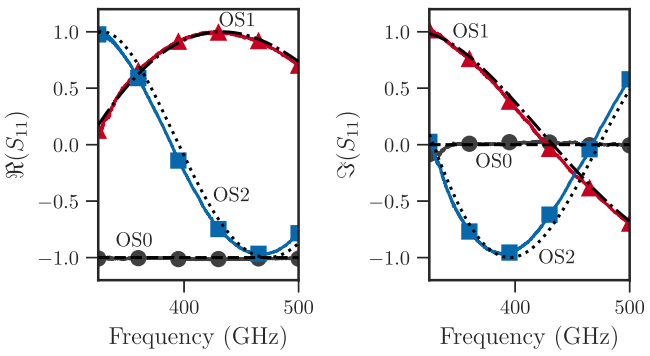

Fig. 16. Measured one-port calibration standards and TRL calibration. The theoretical responses are indicated by the dashed lines.

2) One-Port Standards: OS0, OS1, and OS2 standard were obtained from a single SOI wafer. The error-corrected S-parameters of the standards, as plotted in Fig. 16, show excellent agreement with the theoretical responses. Of the three standards, only OS2 exhibited a notable phase shift in S_{11}. A downward shift in the response of S_{11} indicates that the waveguide line was longer than expected. This may be due to the thickness tolerance of the SOI wafer's HL (±7 μm).

To implement the radiating open standards, the test port flange was first left unterminated and allowed to radiate into free space. Second, a line 1 prototype shim was mounted to the test port and allowed to radiate. The shim was placed with its backside recess towards the test port. Absorbing material (Thomas Keating TK-THz-RAM) was placed 7.5 cm from the radiating apertures to minimize reflections from the surrounding environment. The measured S-parameters of the flange radiating open [Flange RO; see Fig. 17(a)] show good agreement with the CST and theoretical models (see Section IV-A2), further verifying the work of [36]. Several measurements of the line 1 radiating open (line 1 RO) were performed. The shim was removed from the flange between measurements. No mechanical fixing was used, and the shim was seen to change position with each measurement. The large variation in the reflection coefficient is due to the lack of proper ohmic contact between it and the test port. For this technique to be viable, a method of affixing the shim to the flange is required. Despite the difficulty in achieving good contact, we believe that the accuracy of the micromachined waveguide aperture and repeatability of its alignment to the test port could be of use in terahertz metrology. Of the results in Fig. 17(a), Meas. 2 was closest to models of the standard and was, thus, chosen to create a range of SDDL calibrations (see Section V-E).

3) Verification Standards: Four cross-waveguide verification standards were fabricated from the same SOI wafer as used for the previous devices and characterized. Their error-corrected S-parameters are plotted in Fig. 17(b). Both $|S_{11}|$ and $|S_{21}|$ exhibit some discrepancy to their simulated values. These devices were implemented using the same layer configuration as line 0, with the waveguide section etched

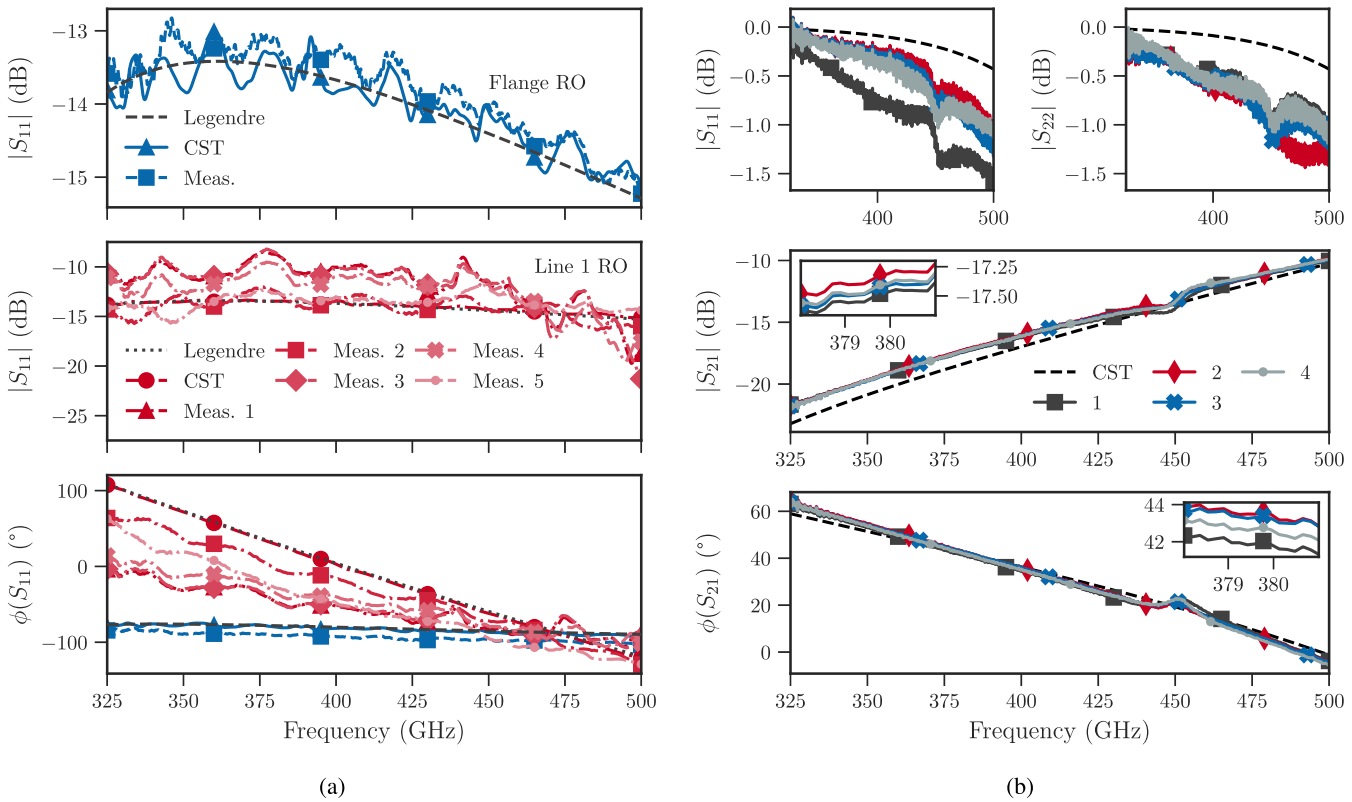

Fig. 17. Error corrected S-parameters of (a) flange radiating open (Flange RO) and line 1 radiating open (line 1 RO) and (b) cross-waveguide verification standards. Each trace in (b) represents a different device, while those in (a) show repeated measurements of a single device.

in the SOI's DL. BOX residues similar to those found on line 0 were present on the bottom of the DL of the cross-waveguides. This prevented proper ohmic contact between the DUT and test ports, resulting in leakage at the interface between them. This leakage is responsible for the increase in return loss with frequency, while the sharp resonance at 450 GHz is of the same origin as that seen in line 0. The measured insertion loss is 0.4–1.5 dB lower than predicted for all devices. This cause of this loss may be related to the poor connection to the test ports or other fabrication imperfections and requires further investigation. Additional simulation to account for these factors should permit better agreement between experimental and theoretical responses. Regardless, the repeatability of S_{21} is excellent, with variance in $|S_{21}|$ and $\phi(S_{21})$ as low as 0.1 dB and 0.2°, respectively.

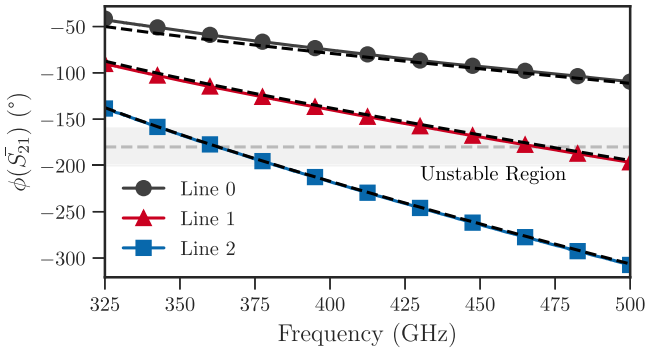

Fig. 18. Measured and theoretical phase responses of the three line standards. The region of TRL instability is represented by the shaded area.

B. TRL Calibration

The three micromachined line standards can be combined with any of the reflective standards to create a fully micromachined TRL calibration kit. Nine different configurations are possible; as the electrical length of the reflect standard does not affect the calibration (provided that it is equivalent at both ports), only three of these are unique, one for each of lines 0, 1, and 2. Of the prototype WM-570 standards implemented here, line 0 alone is suitable for TRL calibration across the full waveguide band, as the electrical lengths of lines 1 and 2 lie within the unstable region of 160°–200° at certain frequencies (see Fig. 18). Four TRL calibrations were performed; three of which used one of the above micromachined lines, the fourth the VDI line standard. A comparative plot of the S-parameters of the 1-in metallic waveguide is shown in Fig. 19. Only results from within the stable TRL region are plotted for each calibration. The return loss calibrated with the micromachined shims is particularly flat due to the highly accurate alignment between the calibration shim and test waveguide flange. Lines 0 and 1 provide very similar results below 450 GHz. S_{21} of all four error-corrected results is so close as to be indistinguishable. Disagreement with the theoretical phase response exists for all calibrations. $|\Delta\phi(S_{21})|$ decreases with frequency, likely due to a difference in β between the theoretical model and the physical device. Results from individual TRL calibrations

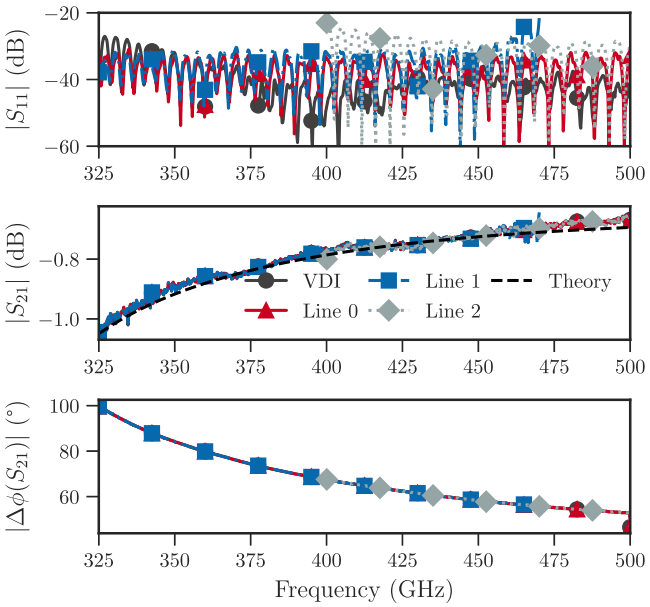

Fig. 19. Measured S-parameters of a 1-in WM-570 waveguide piece, where calibration was performed using the VDI shim and lines 0, 1, and 2. The theoretical insertion loss of the waveguide for $\sigma =$ 3.9e7 S m^1 is shown (theory). Results from each calibration are limited to frequencies outside the unstable TRL region.

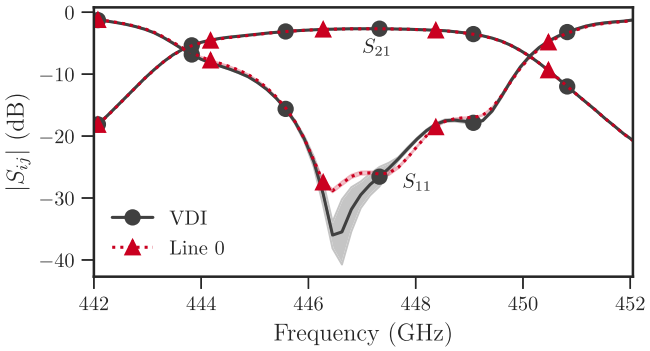

Fig. 20. Error corrected S-parameters of a micromachined bandpass filter from [45], under five and line 0 TRL calibrations. The mean response of each set of calibrations is indicated by the individual traces, while the shaded areas indicate the measured uncertainty ($\pm 3\sigma$).

across different subbands can potentially be combined using suitable weighting [13] to improve accuracy.

Additional proof-of-concept TRL calibrations were performed on a single micromachined bandpass filter of those reported in [45] to allow further benchmarking of the micromachined calibration standards. As before, the standard TRL procedure was followed; a total of five independent measurements of both the VDI and line 0 standard were performed, providing five TRL calibrations of each type. The Through and Reflect standard data were shared between all ten calibrations to ensure consistency. The resulting error-corrected S-parameters of the micromachined filter are plotted in Fig. 20, wherein the individual traces represent the mean response of each set of error-corrected data and the shaded areas the measured uncertainty ($\pm 3\sigma$). Both calibration sets show excellent agreement. The standard deviation of $|S_{11}|$ is seen to be significantly lower for line 0, indicating that the micromachined standards offer superior alignment and repeatability.

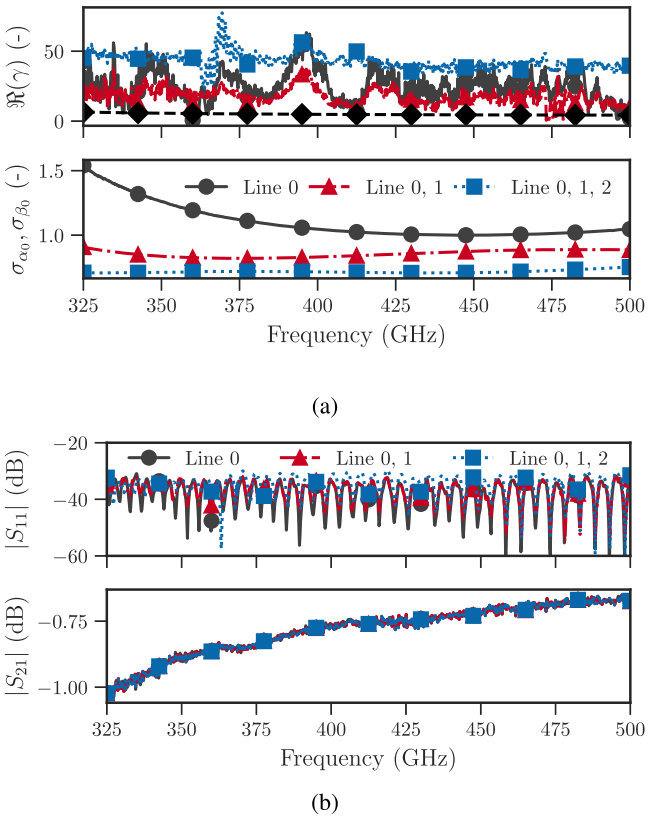

Fig. 21. (a) Waveguide α [$\Re(\gamma)$] and calibration normalized standard deviation extracted from the mTRL algorithm for three different combinations of line standard. The dashed line represents the theoretical waveguide α. (b) Error corrected S-parameters of the VDI waveguide under the above calibrations.

C. mTRL Calibration

A set of three mTRL calibrations was created using the data from the above TRL calibrations. The first of these used line 0 only and is, thus, equivalent to a standard TRL calibration. The latter two used the lines 0 and 1 and lines 0, 1, and 2, respectively. The reduction in uncertainty in α with N_{line} is clear [see Fig. 21(a)] and corresponds to the improvement seen in σ_{α_0}, the normalized standard deviation derived from the mTRL algorithm. However, the absolute value of α is erroneous for all calibrations, as none of the input line sets are free from the unexpected increases in insertion loss discussed in Section V-A1, creating a variance in α between the lines. This disagreement is most severe for the calibration which incorporated line 2. All three mTRL calibrations were applied to the measured S-parameters of the VDI waveguide. As at least one pair of lines in each calibration does not have $\Delta\phi(S_{21})$ of 0, 180° at all frequencies, the mTRL algorithm eliminates the instabilities observed in the standard TRL results [see Fig. 21(b)]. Excellent agreement is seen between all three calibrations, increasing confidence in the result.

D. Offset-Short Calibration

Raw S-parameters of the measured offset-short standards were used to implement a one-port calibration. Simple models of each standard were generated, based on lossless waveguide offset shorts of lengths corresponding to the thickness of

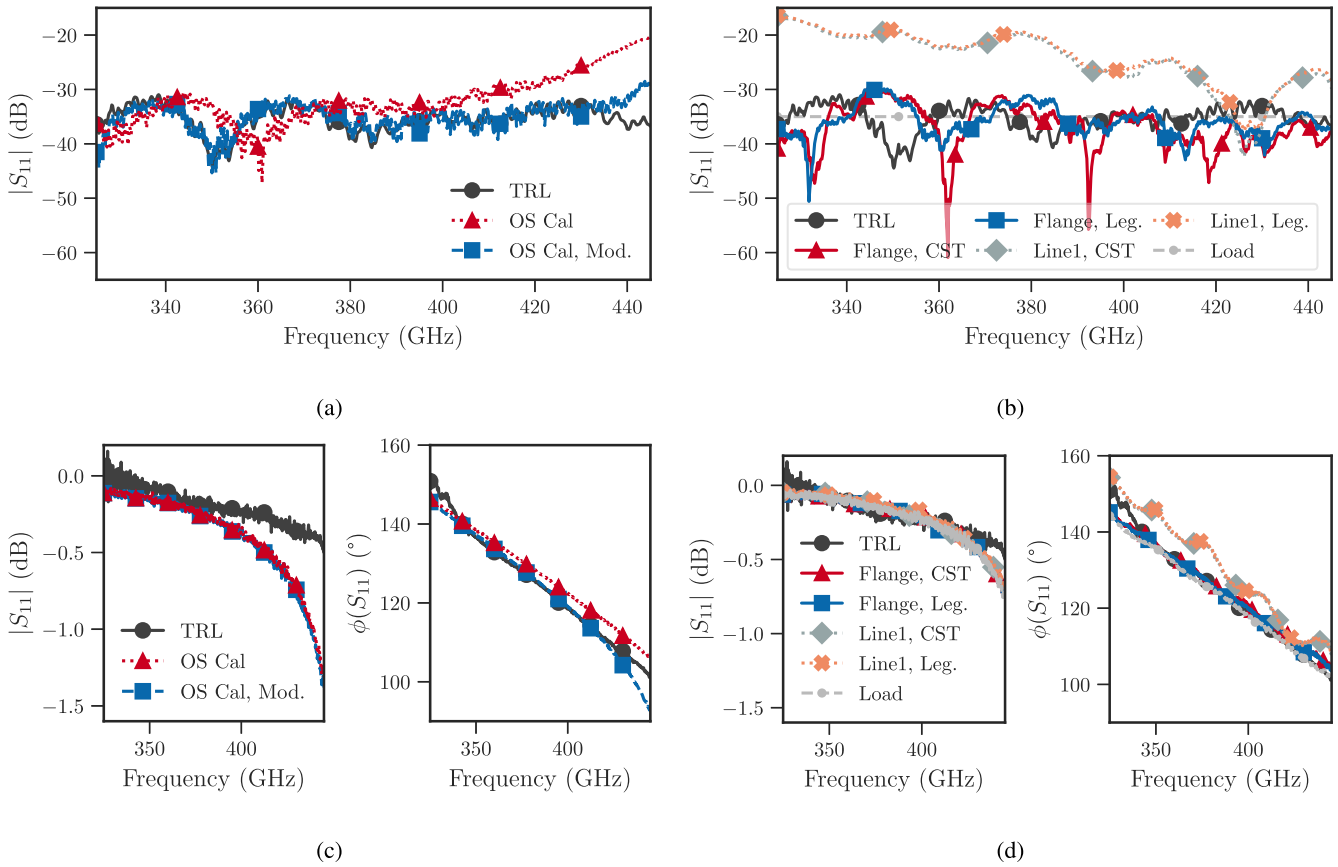

Fig. 22. Error corrected S-parameters of (a) and (b) VDI waveguide load and (c) and (d) micromachined cross waveguide for various (a) and (c) offset-short and (b) and (d) SDDL calibrations. The offset-short calibration used one set of standards of Fig. 16. The theoretical length of OS2 was increased by 7 μm to obtain the modified calibration (Mod.). (b) and (d) Flange = test port radiating open, line 1 = line 1 radiating open, and load = VDI waveguide load. CST and legendre (Leg.) models of each radiating open were used.

the relevant SOI layer (see Section III). This calibration was applied to the load standard of the VDI calibration kit and a single micromachined cross-waveguide. The error corrected S-parameters of these DUTs are plotted in Fig. 22(a) and (c). The S-parameters of OS0 and OS2 are identical at 465 GHz, while OS1 and OS2 are equivalent at 455 GHz (see Fig. 16), creating an ill-defined calibration around these frequencies. As such, the response of each DUT is plotted between 325 and 445 GHz only. Taking the TRL corrected responses as a reference, reasonable agreement in $|S_{11}|$ is seen. $\phi(S_{11})$ of the cross-waveguide exhibits some discrepancy, however. This was primarily due to the shift in the measured response of OS2 (see Fig. 16). An additional modified offset short calibration was created, wherein the theoretical length of OS2 was increased by 7 μm. This value corresponds to the specified tolerance of the SOI's HL, in which OS2 is etched. Agreement between the offset short and TRL calibrations improved significantly following this modification, both in magnitude and phase.

E. SDDL Calibration

The offset-short standards described above were used to implement a range of SDDL calibrations. Measured data were the same as the offset short calibrations to allow for direct comparison of each method. Calibrations utilizing the radiating open standards and a VDI waveguide load were performed. For each radiating open standard, two models of the Γ were used: one being a CST simulation and the other the closed-form Legendre polynomial model (see Section IV-A2). This gave a total of five independent calibrations. Again, the VDI waveguide load and micromachined cross-waveguide acted as DUTs.

All the SDDL calibrations become ill-conditioned at 465 GHz, for the same reasons, as described in Section V-D, and hence, a limited frequency span is plotted. Of the calibrations performed here, those that utilized the flange radiating open or waveguide load offered the best performance [see Fig. 22(b) and (d)]. In correction of the waveguide load measurement, the calibration that included this standard simply returns whichever Γ value was assumed, providing no useful information other than verifying that the calibration procedure was correct. Although the standard models as in the nominal offset-short calibration were used, a large difference in $|S_{11}|$ is apparent due to the self-calibration nature of the SDDL algorithm. However, if the TRL result is considered to be correct, the offset-short calibration provides better performance below 440 GHz. The low precision of the line 1 radiating open limits the quality of these calibrations. Their agreement to the other results improves in accordance with the increasing agreement seen in Fig. 17(a).

VI. Conclusion

This article presented the first silicon micromachined waveguide calibration standards suitable for terahertz

frequencies. By combining a unique mechanical design and the precision of silicon micromachining techniques and leveraging the mechanical properties of silicon, we realized highly accurate calibration standards for use between 325 and 500 GHz. The inherent layered structure of SOI wafers provides three distinct physical lengths, eliminating the need for multiple wafers to be used. Eight unique standards were implemented and a total of 15 prototypes from a single wafer characterized. All standards showed good agreement with theoretical models. Calibrations based on four different algorithms for both one- and two-port characterization were realized using these prototypes. We found that a classical three-term one-port calibration with fully known standards can provide excellent results if the standards are sufficiently accurate. This may spark a reevaluation of such methods, which are of appeal due to the simplicity of the calibration and its required standards. Attempts to realize an accurate micromachined radiating open were hampered by the poor connection to the test port. Mechanical fastening of the standard during measurement should alleviate this issue, providing further flexibility. Results from the TRL calibrations were found to be in agreement with those performed using metallic shims. The difference in error-corrected reflection coefficient between these calibrations highlights the need to match γ and Z_0 of the line standard as closely as possible to the DUT. The performance improvement offered by the mTRL calibration is clear, despite some variance in γ of the line standards. Our work makes such calibrations feasible at frequencies above 1 THz, allowing for precision metrology beyond current limits. Additional analysis is required to establish traceability of the silicon micromachined calibration standards, a task that we are currently undertaking. Nonetheless, our current micromachined standards offer excellent performance, which can only be expected to improve with subsequent design and fabrication iterations.

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