A 50-nm Gate-Length Metamorphic HEMT Technology Optimized for Cryogenic Ultra-Low-Noise Operation

Felix Heinz, Fabian Thome, Arnulf Leuther, and Oliver Ambacher

***Abstract*— This article reports on the investigation and optimization of cryogenic noise mechanisms in InGaAs metamorphic high-electron-mobility transistors (mHEMTs). HEMT technologies with a gate length of 100, 50, and 35 nm are characterized both under room temperature and cryogenic conditions. Furthermore, two additional technology variations with 50-nm gate length are investigated to decompose different noise mechanisms in HEMTs. Therefore, cryogenic extended *Ku*-band low-noise amplifiers of the investigated technologies are presented to benchmark their noise performance. Technology C with a 50-nm gate length exhibits an average effective noise temperature of 4.2 K between 8 and 18 GHz with a minimum of 3.3 K when the amplifier is cooled to 10 K. The amplifier provides an average gain of 39.4 dB at optimal noise bias. The improved noise performance has been achieved by optimization of the epitaxial structure of the 50-nm technology, which leads to low gate leakage currents and high gain at low drain current bias. To the best of the authors' knowledge, this is the first time that an average noise temperature of 4.2 K has been demonstrated in the *Ku*-band.**

***Index Terms*— *Ku*-band, cryogenic, high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), metamorphic HEMTs (mHEMTs), monolithic microwave integrated circuits (MMICs), noise, quantum computing, radio astronomy.**

I. Introduction

OPTIMIZING for low noise in electronic receiver systems has a long tradition in microwave engineering because noise caused by electronics mainly limits the sensitivity of the receiver. Highly sensitive systems are classically needed in radio astronomy. Extremely weak signals as the cold sky background temperature (as low as 2.7 K depending on the band of interest) demand for extremely low-noise electronics to be able to distinguish between signal and noise. Especially at microwave frequencies, it is, therefore, feasible to cool the receiver front end to cryogenic temperatures to reduce the impact of thermal noise.

Beside this classical cryogenic application, readout circuits for quantum computing systems require the lowest noise temperatures in the low gigahertz regime. The quantum processor containing the actual quantum bits (qubits) is cooled to only several tenths of millikelvins. This is not feasible for the readout circuit since cooling power at deep cryogenic temperatures is limited to a few microwatts. In order to not disturb the extremely weak signal of the qubits and to be able to control and read them, cryogenic ultra-low-noise amplifiers (LNAs) operating at only several kelvins are needed [1], [2].

The technology of a (cryogenic) LNA determines its minimal noise temperature that can be reached. High-electron-mobility transistors (HEMTs) based on InGaAs have demonstrated the lowest noise figures at cryogenic temperatures, especially in the lower gigahertz and millimeter-wave regime [3]–[6]. The active region of such transistors can either be grown directly on InP substrate or on GaAs substrate with a metamorphic buffer layer, which matches the different lattice constants. The latter ones are therefore called metamorphic HEMTs (mHEMTs). The maximum operation frequency of such HEMTs has been increased by gate-length scaling down to 20 nm reaching maximum oscillation frequencies above 1 THz [7], [8]. Scaling below the 100-nm node, the improvement of the noise figure settles and does not match the postulated expectations [9]. This seems to contradict the prediction of classical HEMT noise modeling approaches [10], which takes maximum transition frequency and gain as a noise suppressing factor into account. Investigations of mHEMTs with different gate lengths have shown that the increase in gate leakage current due to simultaneous Schottky barrier scaling becomes an important contributor to the noise temperature [11], [12].

Furthermore, a comparison of two mHEMT *W*-band LNAs with 50- and 35-nm gate length showed no significant improvement in noise temperature but revealed a much stronger bias dependence of the small-signal gain and the noise temperature of the 50-nm mHEMT LNA both at room [13], [14] and cryogenic temperature [15]. Understanding (cryogenic) noise mechanisms is a key to further optimize current InGaAs HEMT technologies for low noise figure.

In this article, we investigate the cryogenic performance of different sub-100-nm gate-length InGaAs mHEMTs and present a cryo-optimized technology variant of the 50-nm gate-length mHEMT. Three variations of a 50-nm mHEMT technology with different epitaxial layer stacks, as well as 100- and 35-nm mHEMTs, are investigated. This allows to separate between effects that are caused by different gate lengths and between mechanisms that are a consequence of

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the different epitaxial structures. The new cryo-optimized technology is compared with the other technology nodes at the example of an extended Ku-band LNA monolithic microwave integrated circuit (MMIC). Section II revises the theory of noisy transistor two ports and lists parameters affecting the noise temperature. In Section III, the InGaAs technologies and technology variations that have been investigated are introduced. Section IV deals with the cryogenic dc device performance, and in Section V, the device's RF results are discussed. In Section VI, the designed Ku-band LNA MMICs are presented and Section VII shows the measured LNA performance at room temperature and cryogenic temperatures. In Section VIII, the results will be discussed and compared to the state of the art. Section IX concludes this article.

II. Theory of Transistor Noise Temperature

The noise behavior of a two-port is fully specified by its noise parameters $T_{\min}$, $\underline{\Gamma}_{\text{opt}}$, and R_{n}, where $T_{\min}$ is the minimal noise temperature that is reached at the optimal source reflection coefficient $\underline{\Gamma}_{\text{opt}}$ and R_{n} determines the sensitivity of the noise temperature to mismatch. Although all noise parameters are interrelated, especially, $T_{\min}$ is a useful parameter to benchmark the performance of a low-noise technology since it defines the best performance that can be reached. The noise parameters can be calculated from the small-signal equivalent circuit with noise generators connected [16]–[18]. These noise sources model the origin of noise in the transistor and allow for a physically consistent model. Today's standard HEMT noise models [10], [19] show that the noise created in HEMTs originates from various physical effects at different positions in the transistor. Main noise sources in HEMTs are the thermal noise of the gate-line resistance, thermal noise of the access resistances, shot noise generated by gate leakage current, and channel noise [12].

Regarding their position in the transistor structure, the noise power created by different noise sources will contribute differently to the effective input noise temperature. Noise power generated at the output will not be amplified by the two-port and is therefore minimized by the device gain in the effective noise temperature [20]. This has been described for transistors empirically by Fukui [21] and later in a more consistent relation to the canonical noise parameter representation by Pospieszalski [10]. Both use the transition frequency (f_{T}) as a measure for device gain which minimizes the (output related) channel noise. Equation (1) gives the Pospieszalski relation [10] for the minimum noise temperature of an intrinsic HEMT in dependence on the channel noise temperature T_{d} related to the small-signal output conductance (g_{ds}) and the gate noise temperature (T_{g}) related to the intrinsic gate–source resistance (R_{gs})

$$T_{\min} \sim \frac{f}{f_{\text{T}}}\sqrt{g_{\text{ds}} T_{\text{d}} R_{\text{gs}} T_{\text{g}}}. \tag{1}$$

The channel noise is modeled to be thermal, but at a temperature T_{d} independent of the lattice temperature but dependent on the drain current and voltage. This has been motivated by the high electrical field across the short gate, which accelerates the channel electrons. This can be interpreted as higher temperature of the 2-D electron gas (2DEG). For typical amplifier bias points in sub-100-nm gate-length HEMTs, the channel electron temperature reaches several hundreds up to thousands of kelvin, making it the highest absolute source of noise power in the HEMT. Therefore, higher f_{T} (as a measure for gain) is extremely beneficial to minimize the high channel noise. However, both T_{d} and f_{T} are bias dependent, which demands a tradeoff. The following requirements for a low-noise technology conclude from this:

1) high f_{T};
2) low current and voltage bias for low channel noise;
3) low gate leakage current;
4) low parasitic device resistances.

The parasitic device resistances of the given technologies are already optimized for low-noise operation [22]–[25], and the investigation focuses on the influence of intrinsic noise sources and how the noise can be further optimized.

III. Metamorphic HEMT Technologies

The results shown in this article are based on mHEMT technologies with different gate lengths developed at Fraunhofer IAF. In Section III-A, three well-established mHEMT technologies with different gate lengths [22]–[25] are presented. Section III-B introduces two technology variations of the 50-nm process that have been processed to investigate and optimize the noise performance of cryogenic mHEMT LNAs. One technology variation is especially optimized for extremely low-noise amplification at cryogenic temperatures.

A. Established mHEMT Technologies

In this section, the well-established mHEMT technologies with a gate length of 100, 50, and 35 nm are presented. All technology nodes are processed on 100-mm semi-insulating GaAs wafers. The technologies have a linearly graded InAlGaAs metamorphic buffer layer in common, which is grown onto the wafer by molecular beam epitaxy (MBE). This adapts the lattice constant to the InP value, which allows to match the lattice of the lower $In_{0.52}Al_{0.48}As$ barrier layer.

The 2DEG of the 100-nm technology is formed in an $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ composite channel enclosed by $In_{0.52}Al_{0.48}As$ barrier layers. A Si-delta-doped layer above the channel increases the electron density in the channel. Ohmic contacts are formed by the GeAu deposition on a highly doped $In_{0.53}Ga_{0.47}As$ cap layer. The gate recess is etched with a succinic acid solution. The 100-nm Pt–Ti–Pt–Au T-gate is formed by electron beam lithography using a three-layer resist. A chemical vapor deposited (CVD) SiN layer passivates the wafer.

An $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ composite channel with $In_{0.52}Al_{0.48}As$ barrier layers forms the heterostructure of the 50-nm mHEMT technology (50-nm Technology A). The electron channel density of 4.2×10^{12} cm^{-2} is achieved by Si-delta doping of the top barrier. Ohmic contacts are employed by an $In_{0.53}Ga_{0.47}As$ saturation-doped cap layer and the recess is etched with succinic acid. The upper barrier layer thickness is reduced compared to the 100-nm technology in

TABLE I
COMPARISON OF THE EPITAXIAL STRUCTURE OF DIFFERENT GATE-LENGTH mHEMTs

100 nm mHEMT	50 nm mHEMT (A)	35 nm mHEMT
n++ $In_{0.53}Ga_{0.47}As$	n++ $In_{0.53}Ga_{0.47}As$	n++ $In_{0.53}Ga_{0.47}As$
Si-delta doped $In_{0.52}Al_{0.48}As$ barrier	Si-delta doped $In_{0.52}Al_{0.48}As$ barrier	Si-delta doped $In_{0.52}Al_{0.48}As$ barrier
$In_{0.65}Ga_{0.35}As$ channel	$In_{0.8}Ga_{0.2}As$ channel	$In_{0.8}Ga_{0.2}As$ channel
$In_{0.53}Ga_{0.47}As$ channel	$In_{0.53}Ga_{0.47}As$ channel	-
$In_{0.52}Al_{0.48}As$ barrier	$In_{0.52}Al_{0.48}As$ barrier	Si-delta doped $In_{0.52}Al_{0.48}As$ barrier
InAlGaAs metamorphic buffer	InAlGaAs metamorphic buffer	InAlGaAs metamorphic buffer
GaAs substrate	GaAs substrate	GaAs substrate

order to maintain proper channel control with shorter gate length. The 50-nm T-shaped gate is realized by electron beam lithography with a four-layer resist and consists of a Pt–Ti–Pt-Au layer sequence. The gate-line resistance of the 170-nm gate head is further reduced by placing a 450-nm-wide metal strip of the first metalization layer on top, which is important to achieve lowest noise temperatures. The gate is encapsulated in low-k benzocyclobutene (BCB) in order to reduce parasitic capacitances. A SiN passivation layer is deposited by CVD.

The 35-nm technology confines the electrons in a single $In_{0.8}Ga_{0.2}As$ channel enclosed by $In_{0.52}Al_{0.48}As$ barrier layers above and below. Both barriers are Si-delta doped close to the channel border to obtain a high electron density in the channel. Again, a highly doped $In_{0.53}Ga_{0.47}As$ layer caps the heterostructure to achieve low access resistances. After recess etching, the gate module is processed making use of two electron beam lithography masks. In a first step, the 35-nm-long PMMA 950 K resist opening is used to etch a SiN layer. This SiN layer acts in the second step as a shadow mask, in which the gate metal is evaporated to form the gate foot. The 100-nm gate head is processed in the second electron beam lithography step on top. The gate-line resistance is further reduced by placing a metal 1 line on the gate head.

All technologies feature metal–insulator–metal (MIM) capacitors; 100 and 50 nm use the 250-nm-thick SiN-layer with 0.225-fF/μm^2 sheet capacitance, whereas an 80-nm-thick SiN-layer with 0.8-fF/μm^2 sheet capacitance is used to form the capacitors of the 35-nm technology. All technologies feature temperature-independent NiCr thin-film resistors with a sheet resistance of 50 Ω/sqr. Isolation of the active region is achieved by wet chemical mesa etching. The technologies have two metal layers or three metal layers in the case of the 35-nm technology for interconnections, where the top layer can be used to realize airbridges. The wafers are thinned to 50 μm thickness to suppress parasitic substrate modes at high frequencies. Through-substrate via holes are dry-etched and a 2.7-μm plated Au layer is attached to contact the via holes. The epitaxial structures of the three technologies are compared in Table I. Table II compares the room-temperature device parasitics of the different gate-length mHEMTs, which are the main contributors of thermal noise in the devices.

B. Technology Variations

The observation that scaling at submicrometer gate lengths does not lead to the expected improvement in noise temperature anymore, caused the processing of technology variations of the established mHEMT processes. The influence of the InAlAs barrier thickness on the magnitude of the gate leakage current, which is a contributor to the noise temperature, is investigated. Therefore, a technology variation (50-nm Technology B) using the epitaxial structure of the 100-nm mHEMT in combination with the 50-nm mHEMT process has been fabricated to analyze the actual impact of the barrier thickness on the leakage current. In this way, a transistor structure with a 50-nm gate and a thicker Schottky gate barrier compared to the standard 50-nm technology is achieved. This shall allow for a better separation between the effects originating from gate-length scaling and effects resulting from different epitaxial parameters. The value for access resistance given in Table II for 100-nm mHEMT also applies for 50-nm Technology B since they share the same epitaxy. However, the gate-line resistance of Technology B is the same as for 50-nm Technology A due to the same front-side processing.

TABLE II
ROOM-TEMPERATURE PARASITICS OF DIFFERENT GATE-LENGTH mHEMTs

Parameter	100 nm mHEMT	50 nm mHEMT	35 nm mHEMT
R_g	400 Ω/mm	250 Ω/mm	270 Ω/mm
R_a	0.18 Ω mm	0.17 Ω mm	0.13 Ω mm

The aim of the second technology experiment (50-nm Technology C) is to examine the effect of the different epitaxial channel structures. This is done by processing a wafer in 50-nm technology, but with a slightly varied epitaxial structure. Instead of an $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ composite channel, a single $In_{0.8}Ga_{0.2}As$ channel with a single delta doping in the upper barrier layer is grown. The epitaxial structure is therefore equivalent to the structure of 50-nm Technology A, but with a single $In_{0.8}Ga_{0.2}As$ channel instead of the composite channel. This should allow to get an insight into different channel structures with proper channel control at 50-nm gate length. All parasitics given in Table II for 50-nm mHEMT also apply for 50-nm Technology C.

IV. DC CHARACTERIZATION

The different mHEMT technologies and the new technology variations described in Section III are characterized at an

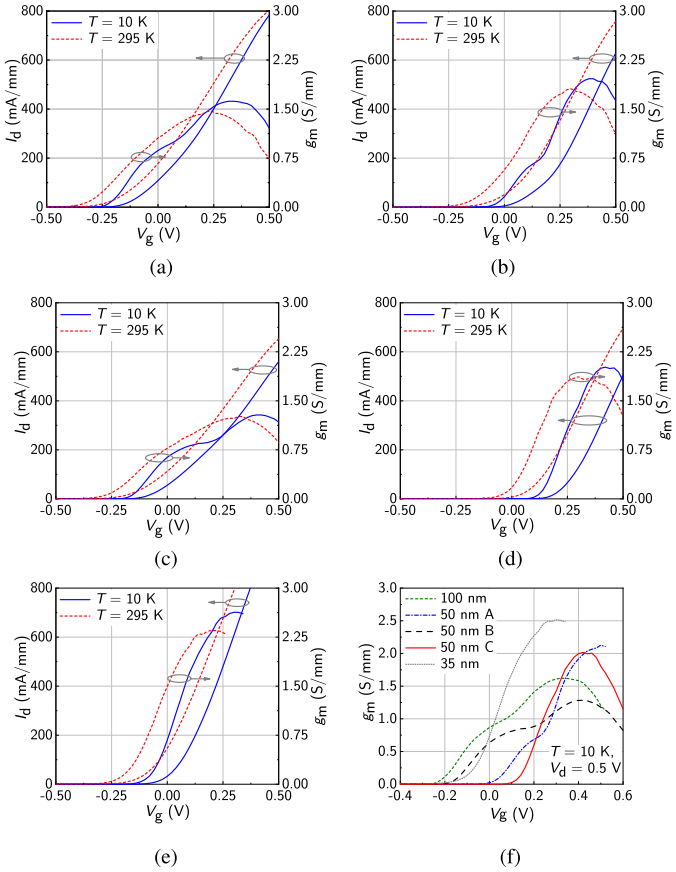

Fig. 1. Transconductance and corresponding drain current of two-finger transistors with a total gate width of 2×60 μm at a drain voltage $V_d = 0.5$ V. (a) 100-nm mHEMT technology. (b) 50-nm mHEMT Technology A. (c) 50-nm mHEMT Technology B. (d) 50-nm mHEMT Technology C. (e) 35-nm mHEMT technology. Dotted lines: room-temperature measurement (295 K). Solid lines: cryogenic measurement (10 K). (f) g_m at 10 K of the different technologies is compared.

ambient temperature of $T = 295$ K and $T = 10$ K. The measurements at cryogenic temperature have been done with a Lakeshore CRX-4K probe station. The station utilizes a closed-cycle refrigerator being capable of cooling down to temperatures as low as 4.5 K. Thermal isolation to ambient temperature is achieved by evacuating the cryogenic chamber to $< 1 \times 10^{-8}$ bar. A cooled radiation shield prevents heating of the device under test (DUT) by thermal radiation. The sample stage's temperature is digitally controlled and four probe arms form the electrical connections into the chamber.

Representative chips for cryogenic testing are selected by room-temperature wafer mappings, considering general dc performance, small-signal performance, and noise performance (in the case of amplifiers). After dicing, the sample chips are glued on a gold-platted copper disk with silver epoxy. This gold-plated sample holder is mounted on the cooling plate. Apiezon N grease is used for a good thermal connection of the cooling plate to the sample holder.

Fig. 1 shows the measured current–voltage (I–V) transfer characteristic and the corresponding transconductance (g_m) of 2×60 μm transistors of the different mHEMT technologies. The gate voltage has been swept in 20-mV steps and the dc-transconductance is obtained as the discrete derivative

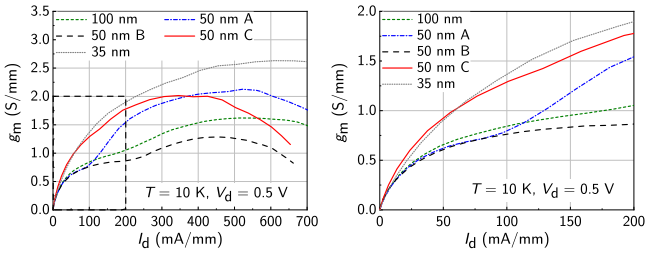

Fig. 2. Transconductance of the different mHEMT technologies plotted against the drain current of two-finger transistors with a total gate width of 2×60 μm at a drain voltage of $V_d = 0.5$ V at $T = 10$ K. Left: full current range. Right: close-up view on the lower bias region is plotted. The 100-nm mHEMT (short dashed line), 50-nm Technology A (dashed-dotted line), 50-nm Technology B (long dashed line), 50-nm Technology C (solid line), and the 35-nm mHEMT (dotted line) are shown.

of the measured drain current values with respect to the gate voltage.

Common to all technologies is a shift of the threshold voltage toward higher gate voltages at cryogenic temperatures, which is most pronounced for 50-nm Technology C. The maximal transconductance of all technologies is increased by approximately 10% at 10 K, except for 50-nm Technology B where the increase is only 2%. This seems to originate from the higher gate–channel distance of this epitaxial stack in combination with a 50-nm gate. This leads to decreased channel control compared with the other technology variations. The maximal transconductance of 50-nm Technology B at both room and cryogenic temperature is even lower compared to the 100-nm technology, which can be explained by the thicker gate barrier of this variation as well. However, the thicker barrier has been chosen with the aim to investigate the impact of the barrier thickness on the gate leakage.

At room temperature, the increase of the transconductance over gate voltage up to the peak value is a smooth curve for all technologies investigated. At cryogenic temperatures, the 100-nm mHEMT, 50-nm Technology A, and 50-nm Technology B show a plateau, where the increase in transconductance settles before it increases again until the maximum transconductance is reached. This cannot be observed for 50-nm Technology C and the 35-nm mHEMT. Therefore, this effect has to be gate length independent. All technologies showing this transconductance behavior have a composite channel, with a high indium content in the main channel and a lower indium content in the sub-channel. Hence, the change in transconductance seems to originate from the composite channel structure.

f_T of a (intrinsic) transistor is directly proportional to its (RF) transconductance. A noise-optimized device should have high transconductance at low bias current. Therefore, it is of special interest how much transconductance per drain current can be reached. The transconductance of the different technologies versus the drain current at 10 K is shown in Fig. 2.

As expected, the transconductance plateau of the split-channel technologies (100-nm mHEMT and 50-nm Technologies A and B) can also be seen when plotted versus the drain current. The slope of the g_m curve before the plateau is steep, but at the plateau, the increase of transconductance

becomes almost zero. The size of the plateau seems to depend on the composition of the channel. For the 100-nm epitaxial layer stack with both 100- and 50-nm gate (Technology B), the area, where the g_m-increase comes close to zero, lasts for an increase in drain current of approximately 100 mA/mm. The plateau of 50-nm Technology A is slightly shorter and the increase in transconductance after the plateau is higher, which is due to the high indium content in the main channel. However, the plateau is disadvantageous in terms of low-noise operation since high transconductance values are shifted toward higher current values, which leads to higher channel noise power. Both 50-nm Technology C and the 35-nm HEMT do not show this plateau behavior, which results in a constantly high increase of transconductance over drain current until the increase settles around the g_m-peak value. The 35-nm mHEMT has the highest peak transconductance with more than 2500 mS/mm at high drain currents. However, the transconductance increase at low bias currents up to 100 mA/mm is almost identical for 50-nm Technology C and 35-nm mHEMT, with a slightly higher g_m-increase for 50-nm Technology C. This indicates that the channel structure dominates the transconductance at low bias rather than the gate length. At 50 mA/mm, the transconductance of the single-channel technologies is approximately 50% higher than that of all the composite channel technologies. Especially, the improvement at constant gate length of 50-nm Technology C in comparison to the established 50-nm mHEMT (Technology A) is worth mentioning since the transconductance of Technology C is higher up to a drain current of $I_d = 350$ mA/mm. An improvement in noise performance can be expected by this since high gain at low current bias can be achieved. The drain current shall be kept as low as possible at cryogenic temperatures, and 50-nm Technology C shows the highest transconduction of all technologies investigated between 0 and 50 mA/mm.

Fig. 3 shows the magnitude of the measured gate current (I_g) over gate voltage at 10 and 295 K of the different technologies. The gate current at cryogenic temperature is approximately one order of magnitude lower than at room temperature for all mHEMT technologies. All technologies except the 35-nm technology node show gate currents in the same order of magnitude. However, the 35-nm technology has a gate current that is almost two orders of magnitude higher than the other technologies. The following conclusions can be drawn from this: the gate leakage current is only indirectly related to the gate length itself since 100 and 50 nm show similar results. The 35-nm technology, however, is the only technology with a very short gate-to-channel distance, to maintain proper channel control at very short gate length. This leads to a higher amount of electrons tunneling through the thin barrier. This tunneling effect seems to dominate the gate current at very thin barriers. Since tunneling will happen to the greatest extend temperature independent, high gate currents are observed at both room and cryogenic temperatures. The gate current introduces shot noise, and therefore, it shall be kept as low as possible since it degrades the noise performance. The gate barrier dimension of both the 50- and 100-nm epitaxial structures is well suited for

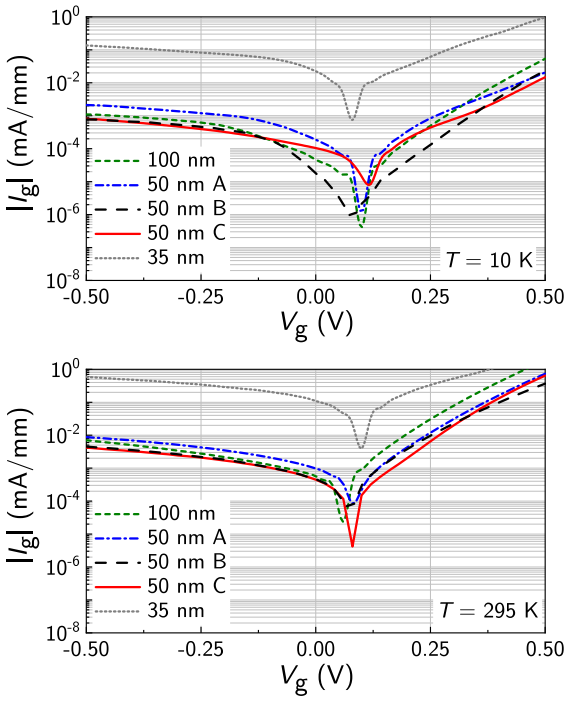

Fig. 3. Gate current measurement of two-finger transistors with a total gate width of 2×60 μm at a drain voltage $V_d = 0.5$ V. The 100-nm mHEMT technology, 50-nm mHEMT Technology B, 50-nm mHEMT Technology A, 50-nm mHEMT Technology C, and 35-nm mHEMT technology are shown. Top: cryogenic measurements are presented. Bottom: room-temperature measurements are shown.

extremely low gate currents. The leakage current of the 100-nm barrier and the 50-nm barrier is almost equal, indicating that the barrier thickness of 50-nm A and C is high enough for extremely low gate currents. As expected, the combination of a single channel with the thicker gate barrier (Technology C) shows extremely low gate leakage current as well.

Fig. 4 shows the output I–V characteristic of the different mHEMT technologies at room temperature and under cryogenic conditions. The gate voltage has been varied between -0.2 and 0.5 V with 0.1-V step size, and the drain voltage has been swept in 25-mV steps from 0 to 1 V for each gate voltage setting. All technologies show a kink-free output behavior both at room and at cryogenic conditions. The ON-state resistance (R_{ON}) of all mHEMT technologies is improved at 10 K. This seems to originate from the increased electron mobility due to reduced electron scattering with the lattice in combination with reduced resistance of the interconnecting metals.

V. RF Performance

On-chip S-parameters have been measured between 10 MHz and 50 GHz at a temperature of 10 K with an Agilent PNA vector network analyzer (VNA). Dedicated on-wafer calibration structures allow to calibrate the VNA directly at the transistor reference planes making deembedding unnecessary. An eight-term line-reflect-reflect-match (LRRM) calibration has been applied. The line is realized as a zero electrical length thru standard. This has the advantage that only the impedance of the resistor implementing the match standard needs to be known prior to calibration. The load is realized as a

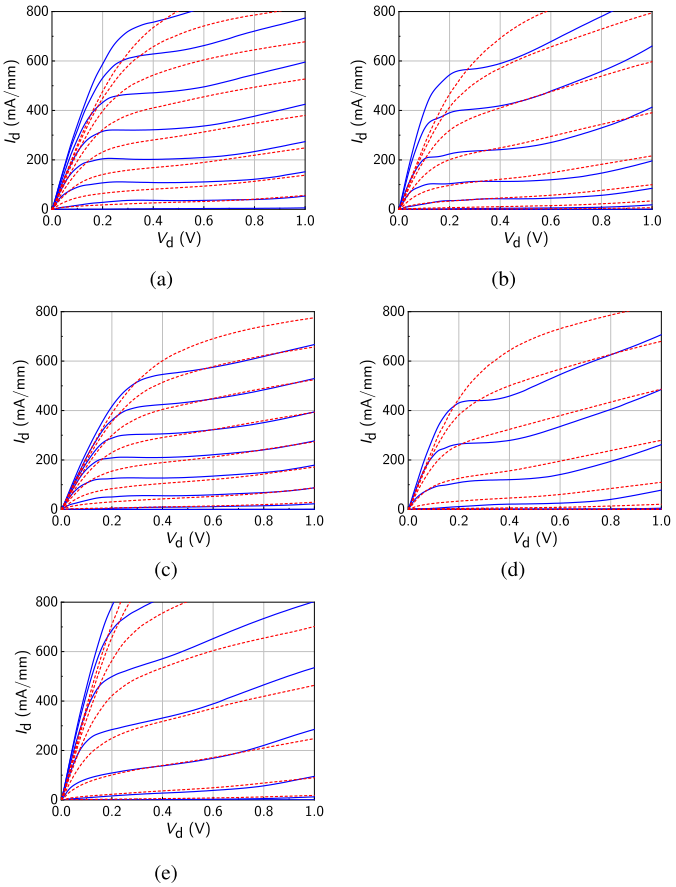

Fig. 4. Output I–V characteristic of two-finger transistors with a total gate width of 2×60 μm for gate voltages ranging from -0.2 to 0.5 V in 0.1-V steps. (a) 100-nm mHEMT technology. (b) 50-nm mHEMT Technology A. (c) 50-nm mHEMT Technology B. (d) 50-nm mHEMT Technology C. (e) 35-nm mHEMT technology. Dotted lines: room-temperature measurement (295 K). Solid lines: cryogenic measurement (10 K).

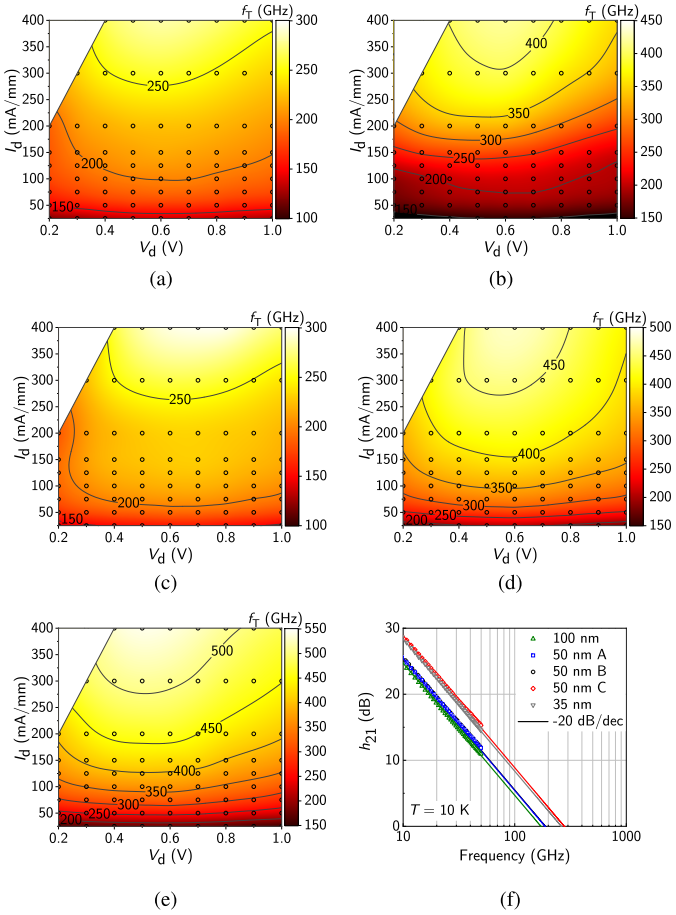

Fig. 5. Maximum (extrinsic) transition frequency of two-finger transistors with a total gate width of 2×60 μm dependent on the bias conditions measured at 10 K. (a) 100-nm mHEMT technology. (b) 50-nm mHEMT Technology A. (c) 50-nm mHEMT Technology B. (d) 50-nm mHEMT Technology C. (e) 35-nm mHEMT technology. (f) f_T-extrapolation of all technologies at $V_d = 0.5$ V and $I_d = 50$ mA/mm (symbols: measured h_{21} and lines: linear fit).

50-Ω NiCr thin-film resistor, which has a very low-temperature dependence and can be measured under cryogenic conditions.

S-parameters of all investigated mHEMT technologies of transistors with a total gate width of 2×60 μm have been measured. The bias of the HEMTs has been varied between drain voltages of 0.2–1 V in 0.1-V steps and drain current densities between 25 and 400 mA/mm in 25-mA/mm steps up to 150 mA/mm and in 100-mA/mm steps from 200 mA/mm onward. f_T of the technologies in dependence of the bias is of special interest since it is a figure of merit for RF gain, which should be as high as possible for an ultra-low-noise technology even at low bias. The current gain h_{21} of the transistors has been calculated from the S-parameter measurements at each bias point. f_T (extrinsic) has been extracted using a linear least-squares algorithm to fit a line with a slope of -20 dB per decade to the measured h_{21}. Fig. 5 shows f_T as a function of the bias. The circles denote the bias points where S-parameters have been measured and the contour plot has been achieved by interpolation between the measurement points. Fig. 5(f) shows the extrapolation at the example of measurements at $V_d = 0.5$ V and $I_d = 50$ mA/mm.

The 100-nm mHEMT technology has the lowest f_T-value over the whole bias range, which has been expected due to the long gate length. However, 50-nm Technology B shows only a minor improvement compared to the 100-nm technology, which matches the observed dc characteristics well (low transconductance). The gate barrier of variation B is not optimized for a 50-nm gate, which reduces the channel control and the improvement due to a shorter gate length in f_T is small; 50-nm Technology A has an over 100-GHz higher peak f_T compared to variation B and 100-nm mHEMT. However, the increase of f_T with the drain current is low at small current densities. In the lower bias regime, Technology A only yields a small improvement in comparison to 100-nm mHEMT and Technology B; 50-nm technology variation C and also the 35-nm technology both show a very steep increase of f_T over drain current. The maximum f_T of 50-nm Technology C is increased by over 75 GHz in comparison to Technology A, and especially, the improvement at low currents is impressive since the improvement of approximately 75 GHz is already achieved at a drain current densities of only 50 mA/mm. As expected, the 35-nm mHEMT has the highest f_T at high drain currents. Nevertheless, the f_T performance below 125 mA/mm is approximately equal to 50-nm Technology C.

The f_T bias dependence matches the observed dc-transconductance behavior. The technologies with a

composite channel show a low increase of f_T at low drain currents due to the plateau in the transconductance curve. Both 50-nm Technology C and 35-nm mHEMT have a steep f_T slope over drain current. The analysis of the f_T bias dependence ensures that the advantage in dc transconductance at low bias currents for 50-nm Technology C and 35-nm mHEMT also yields RF transconductance and gain, respectively. Furthermore, it is assured that no additional intrinsic capacitances are added since they would compensate for a higher transconductance in the transition frequency, which has not been observed.

VI. Cryogenic LNA MMIC Design

An extended Ku-band LNA MMIC has been designed, which was processed in 100-nm mHEMT technology and all 50-nm mHEMT technology variations using the cryogenic model described in [26] and [27]. A Ku-band LNA in 35-nm technology has not been processed since the presence of the increased leakage current is expected to degrade the noise performance especially in the target band. The MMIC design has been done with a focus on maximum comparability in terms of the transistor technologies investigated in this work. The series inductance of the input matching network of the 50-nm mHEMT LNAs has been slightly increased to provide the best power and noise matching. This increase compensates for the lower product of gate-line resistance and gate–source capacitance of the 50-nm technology.

The LNA comprises three common-source stages with inductive source degeneration for wideband performance. The MMIC utilizes a low-loss grounded coplanar waveguide system for interconnections and low-loss matching is done using spiral inductors and MIM capacitors. The design goals have been chosen according to the needs of ultra-low-noise receiver systems. The bandwidth should exceed the Ku-band (defined between 12 and 18 GHz) with as low as possible noise temperature, especially at cryogenic conditions. A chip photograph of the processed LNA MMIC in 100-nm technology is shown in Fig. 6. The MMICs occupy a chip area of 2.5 × 1 mm^2, including bias and RF pads.

Simultaneous noise and gain matching in the first amplifier stage is of special importance for LNAs since the first stage is mainly defining the overall noise performance [28]. Furthermore, losses in the passives before the first stage are critical as well and have to be avoided, which sets constraints for wideband matching. Inductive source degeneration is employed at all stages to enhance the amplifier bandwidth while simultaneously matching for minimal noise and highest gain. The choice of the transistor geometry affects the noise and gain behavior in various ways. Short transistor fingers usually yield a lower noise temperature of the active device but make low loss matching difficult. Moreover, high inductive source degeneration decreases the gain per stage and the amount of inductance needed increases for shorter fingers. However, HEMTs with high finger numbers can become unstable, especially under cryogenic conditions [29], [30], and due to their distributed nature, the device can behave nonideally. In the amplifier, transistors with a total gate width of 4 × 40 μm have been chosen. This allows for

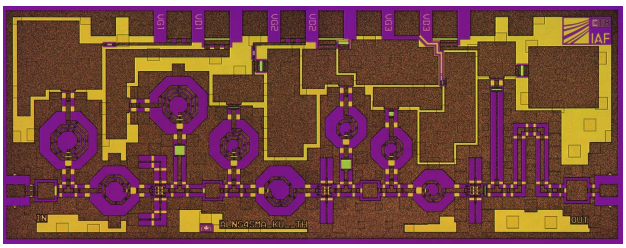

Fig. 6. Chip photograph of the three-stage extended Ku-band LNA in 100-nm technology. The chip occupies an area of 2.5 × 1 mm^2.

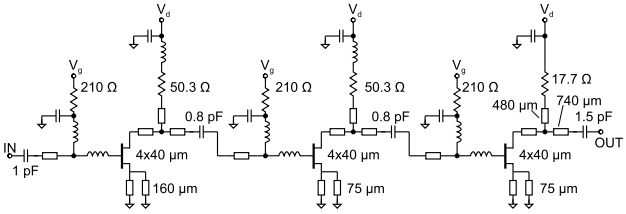

Fig. 7. Simplified schematic of the three-stage Ku-band LNAs.

broadband noise and power matching in the Ku-band with sufficiently low effective gate-line resistance. Airbridges are used to connect the two-transistor drain electrodes to ensure stability at cryogenic temperatures according to [29]. Furthermore, the stability of the circuit at various reflection coefficients at the amplifier input and output has been checked by simulating the reflections at each transistor port according to [31]. Matching is realized with on-chip spiral inductors in airbridge technology, which have been optimized using 3-D electromagentic field solvers and on-chip grounded coplanar transmission lines. Fig. 7 shows a simplified schematic of the Ku-band LNA.

VII. LNA Measurement Results

The room-temperature performance of the fabricated MMICs has been investigated using on-wafer S-parameter and noise temperature measurements. Both measurements have been performed in one probe contact with a PNA-X VNA system from Keysight. The system has an integrated receiver that is dedicated to noise figure measurements up to 50 GHz and a tuner to perform vector correction to noise temperature measurements. The room-temperature noise is measured with the cold-source method [32]. The measurements of the LNAs of different technologies have been done using the same calibration to ensure maximal comparability. Fig. 8 shows the on-wafer results at room temperature. On the left, a full measurement set (S-parameter and noise temperature) at the example of 50-nm mHEMT Technology C is shown. The small-signal gain, in the middle, and the noise temperatures of all four Ku-band MMICs, on the right, are compared. Both the S-parameter measurements as well as the noise temperature measurements have been taken at the bias conditions where the average noise temperature over the amplifier bandwidth becomes minimal (optimal noise bias).

The Ku-band LNA in 100-nm technology and 50-nm Technology B exhibits the lowest gain of on average 33.2 and 32.3 dB, respectively. Variation A has a higher average gain of 36.4 dB over the amplifier bandwidth and Technology C has the highest average gain of the four technologies with 38.7 dB.

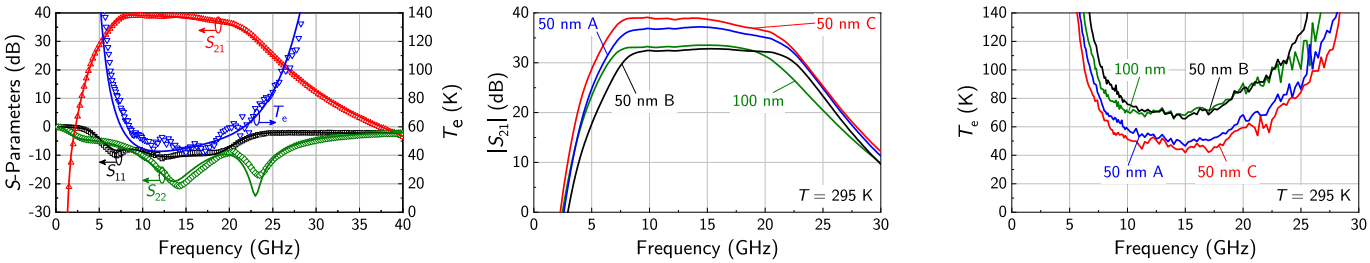

Fig. 8. On-wafer S-parameter and noise temperature measurement of the extended Ku-band LNAs at $T = 295$ K. Left: simulation (lines) and the S-parameter and noise measurements (symbols) of the Ku-band LNA in 50-nm Technology C. Measured small-signal gain S_{21} (lines, middle) and measured noise temperature (lines, right) of the 100-nm mHEMT (green line), 50-nm Technology A (blue line), 50-nm Technology B (black line), and 50-nm Technology C (red line) are compared. Each LNA is operated in the bias point where the average noise temperature over the whole amplifier bandwidth reaches its minimum.

The noise temperature is highest for 50-nm Technology B with 76.3 K between 8 and 18 GHz. However, the 100-nm technology shows only a slightly improved noise temperature of 73.2 K. The noise temperature decreases significantly for 50-nm Technology A, which yields on average 57.7 K of effective input noise temperature. The lowest noise temperature is obtained for 50-nm Technology C, with only 51 K average noise temperature from 8 to 18 GHz and a minimum of only 41.9 K.

The measured circuit performance matches the observed device performance well. The 100-nm mHEMT and 50-nm Technology B have the lowest transconductance and f_T at room temperature, and consequently, they exhibit the lowest amplifier gain. Technology A shows higher transconductance and f_T, which causes the increased gain of this technology's LNAs. The outstanding gain of 50-nm Technology C originates from much higher transconductance at low currents. The noise temperatures of 100-nm mHEMT and 50-nm Technology B are higher than those of 50-nm Technologies A and C due to the lower gain per stage. The higher gain of 50-nm Technology C compared to Technology A is again directly related to the higher device gain. This indicates that Technology C is more robust against changes of the bias point in terms of optimal gain and noise bias than Technology A, which shows slightly less gain at the optimal noise bias point.

The on-chip noise temperature of the MMICs at 10 K ambient temperature has been measured using the cold attenuator method [33]. A 20-dB attenuator chip with integrated temperature sensor, which was characterized beforehand, is glued in front of the DUT and the connection to the LNA input is done via wire bonding. The wire bond is kept as short as possible so that the input matching of the LNA is not changed. The combined MMICs are contacted by the probe arms, one arm at the attenuator input and the second arm contacts the DUT output. The cold and hot state for the Y-factor method is provided by a Keysight 346C noise diode. A room-temperature broadband low-noise measurement amplifier is used for preamplification and the noise powers are measured with an Agilent N8975A noise figure analyzer (NFA). The worst case measurement uncertainty has been estimated to be $\pm$ 1.4 K. This uncertainty estimation takes the diode ENR uncertainty, the uncertainty of the attenuator temperature sensor, probe arm noise temperature uncertainty, NFA measurement uncertainty, and mismatch of all components in the measurement chain into account. The cryogenic measurements of the LNAs of different technologies have been done using the same calibration set for maximal comparability.

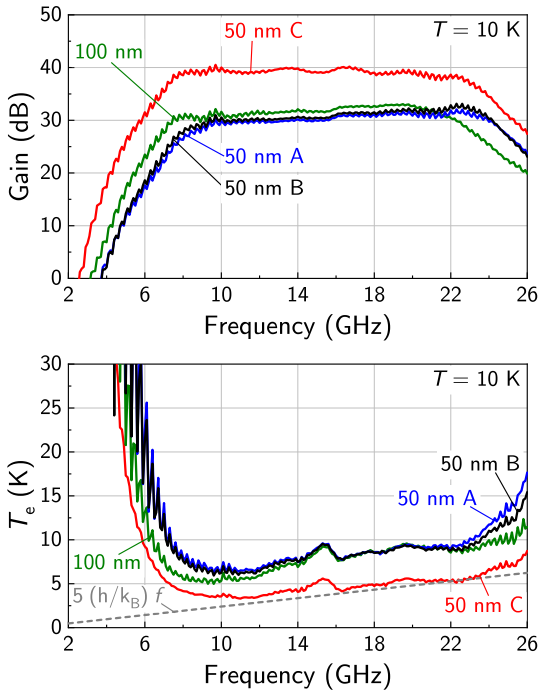

Fig. 9. Scalar noise gain (top) and noise temperature (bottom) measurement of the extended Ku-band MMICs at $T = 10$ K. The measurement of the assembled MMICs in 100-nm mHEMT Technology (green line), 50-nm Technology A (blue line), and 50-nm Technology B (black line) and 50-nm Technology C (red line) is compared. All measurements are taken at the bias where the noise temperature of the technology becomes minimal.

Fig. 9 shows the cryogenic measurement results of the LNAs. All MMICs have been measured at bias points where the noise temperature becomes minimal. The 100-nm mHEMT technology exhibits an average gain of 31.5 dB from 8 to 18 GHz. The gain of 50-nm mHEMT Technology A and B is almost identical in the chosen bias point with average values of 29.7 and 30.3 dB from 8 to 18 GHz, respectively. A significant improvement in gain is observed for 50-nm Technology C (as it is also the case for the room-temperature measurements), which shows an average gain of 39.4 dB between 8 and 18 GHz with a maximum value of 40.5 dB.

The highest noise temperature at 10 K has been measured for 50-nm Technology A and B, which are almost identical and yield on average 7.6 and 7.5 K effective noise temperature, respectively. The 100-nm mHEMT shows a slightly lower

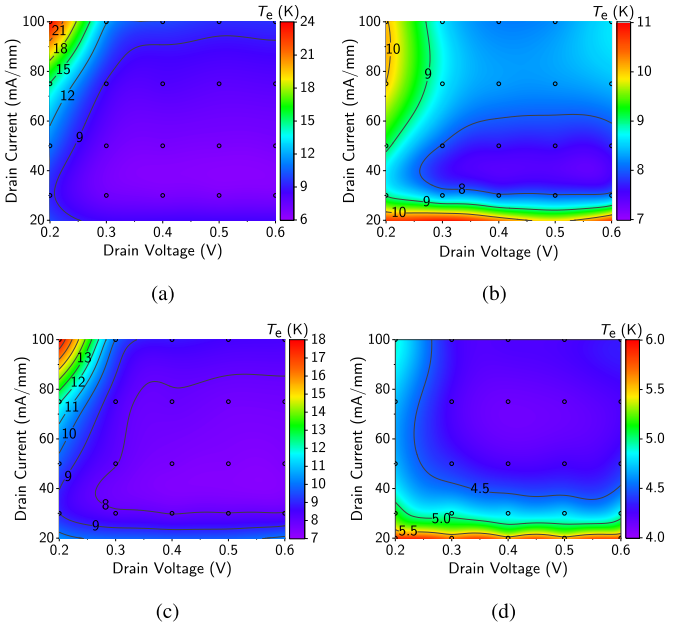

Fig. 10. Noise temperature of the different Ku-band LNAs dependent on the first-stage bias conditions measured at an ambient temperature of 10 K. (a) 100-nm mHEMT technology. (b) 50-nm mHEMT Technology A. (c) 50-nm mHEMT Technology B. (d) 50-nm mHEMT Technology C. The circles denote the bias points where the noise has been measured and the contour is obtained by interpolation.

average noise temperature of 6.9 K; 50-nm Technology C exhibits the best noise performance, which provides a significantly lower average noise temperature of only 4.2 K between 8 and 18 GHz with a minimum of 3.3 K at 11 GHz at an ambient temperature of 10 K. The cryogenic LNA measurements are in good agreement with the dc and RF measurements as well as with the room-temperature S-parameter and noise measurements. The optimal first-stage transistor bias point of all technologies investigated besides 50-nm Technology C is $V_d = 0.5$ V and $I_d = 50$ mA/mm. The 50-nm Technology C's optimal first-stage HEMT bias point has been found to be $V_d = 0.4$ V and $I_d = 75$ mA/mm.

The dependence of the amplifier noise temperature on the bias point of the first stage, which is most critical in terms of noise performance, has been investigated. Fig. 10 shows the measured average noise temperatures between 8 and 18 GHz of the four Ku-band LNAs of different technologies dependent on the first-stage bias point at an ambient temperature of 10 K (mind the different color scales). The circles mark the bias points at which the noise was measured and the contour is obtained by interpolation. The second and third stages of all variants are biased with $V_d = 0.5$ V and $I_d = 50$ mA/mm for maximal comparability.

The dependence of the amplifier noise temperature on the first-stage bias of the 100- and 50-nm Technology B is quite robust against bias variations. However, their noise temperature is already at the minimum considerably higher than the noise temperature of 50-nm Technology C; 50-nm Technology A shows an almost similar noise performance as 100- and 50-nm Technology B at the optimal noise bias point, but is more sensitive to changes in the bias. The noise-optimized 50-nm Technology C shows a lower noise temperature over the whole bias range than the other technologies; 50-nm Technology C is relatively robust against changes in the first-stage bias, especially under consideration of the much lower average noise temperatures.

The observed bias dependence matches the dc and RF measurements; 100- and 50-nm Technology B both show a very wide plateau in the g_m curve leading to a low increase of transconductance and f_T with current. Since the plateau is quite wide, it is not beneficial to further increase the current from the point on that the plateau is reached since this results in higher channel noise power with only slightly increased gain. Since the transconductance slope over I_d is low at the plateau, the optimal bias point is smeared out leading to the observed robustness against changes in the bias; 50-nm Technology A also shows a g_m plateau, but it is much narrower and the overall slope of the transconductance over drain current is higher. This is due to the higher indium content in the main channel. This results in the higher sensitivity of the noise temperature on changes in the bias since the minimum is reached before the short transconductance plateau. At the plateau, the noise increases slightly, and when the slope of the transconductance increases again (which is much earlier compared to 100- and 50-nm Technology B), a slight improvement in noise is observed again. When the current is further increased, the channel noise increases as well, and therefore, the noise temperature increases again (not shown in Fig. 5); 50-nm Technology C does not show a transconductance plateau, and due to the high indium content in the channel, a very steep transconductance slope is obtained. This leads to a very low-noise temperature even at very low bias currents. Furthermore, the absence of a g_m plateau allows to beneficially use slightly higher drain currents since transconductance and consequently f_T strongly increase at very low currents. Hence, the point where channel noise becomes as high that it cannot be compensated for by higher f_T is reached at higher currents. This explains the slightly higher optimal current bias of Technology C compared with the other technology variations.

At optimal noise bias, the amplifiers in 100-nm Technology, 50-nm Technology A, and 50-nm Technology B consume 19.6 mW of dc power, and 50-nm Technology C dissipates 24.4 mW. However, the power consumption of 50-nm Technology C can be further reduced without a major loss in noise performance by adjustment of the second- and third-stage biases. At an overall power consumption of only 4.2 mW, an average noise temperature of 5.1 K with an average gain of 30.6 dB between 8 and 18 GHz is measured.

VIII. Discussion

The Ku-band LNA in the newly developed 50-nm Technology C shows superior cryogenic gain and noise performance. The decreased noise temperature is achieved by simultaneous optimization of gate leakage current, gain, and bias behavior of the transistor technology. The short gate length of 50 nm leads to high device gain and high transition frequency. However, scaling the gate length alone does not lead to an advanced low-noise technology. This has been shown in the example of 50-nm Technology B, where the gate–channel barrier was

TABLE III
STATE-OF-THE-ART CRYOGENIC *Ku*-BAND LNAS

Ref.	Technology	Topology	$T_{amb.}$ (K)	P_{dc} (mW)	Freq. (GHz)	Gain (min. – max.) (dB)	Gain avg. (dB)	T_e (min. – max.) (K)	T_e avg. (K)
[34]	InP HEMT	module	4	22	6 – 20	30.5 – 33.5	32	3 – 8	4.7
[35]	130 nm InP HEMT	3-stage hybrid IC	10	13	6 – 20	-	35.9	-	5.8
[36]	GaAs HEMT	module	19	32	1 – 18	33 – 37	35	4.5 – 8	6.5
[37]	50 nm mHEMT	3-stage hybrid	20	6.43	10 – 20	21 – 30	23.9	9.6 – 16	13.5
[38]	35 nm InP HEMT	3-stage MMIC	10	109.7	5 – 35	16 – 30	-	10 – 18	-
[39]	120 nm BiCMOS	2-stage cascode MMIC	17	60	1 – 20	23 – 27	-	9 – 30	18
[40]	HEMT	3-stage hybrid	15	-	14 – 16	28 – 36	-	19 – 30	-
[41]	150 nm GaAs pHEMT	2-stage MMIC	17	11	8 – 18	19 – 23	21	20 – 45	-
This work	100 nm mHEMT	3-stage MMIC	10	19.6	8 – 18	29.6 – 32.8	31.5	5.0 – 9.3	6.9
This work	50 nm (A) mHEMT	3-stage MMIC	10	19.6	8 – 18	26.3 – 31.1	29.7	6.2 – 9.6	7.6
This work	50 nm (B) mHEMT	3-stage MMIC	10	19.6	8 – 18	27.4 – 31.5	30.3	5.9 – 9.5	7.5
This work (low power)	50 nm (C) mHEMT	3-stage MMIC	10	4.2	8 – 18	29.2 – 31.8	30.6	3.8 – 6.4	5.1
This work (opt. noise)	50 nm (C) mHEMT	3-stage MMIC	10	24.4	8 – 18	38.4 – 40.5	39.4	3.3 – 5.6	4.2

kept at the size of the 100-nm mHEMT. Although gate leakage currents are sufficiently low, this technology variation does only gain a small benefit from the shorter gate length in terms of transconductance and gain enhancement. The decrease in gate length reduces the capacitance below the gate, which reduces the ability to control the channel electrons properly. Simultaneous scaling of the barrier thickness can be used to maintain the channel control, as it has been demonstrated with 50-nm Technologies A and C and the 35-nm mHEMT. Aggressive barrier scaling, however, results in increased gate leakage currents due to tunneling effects. This creates noise power and increases the effective noise temperature. Both effects need to be traded against each other and an optimal combination of a preferably short gate length and a barrier thickness small enough for high f_T, but still high enough to allow only small gate currents to flow, needs to be found. For the given $In_{0.52}Al_{0.48}As$ barrier, this optimum is found for the barrier used in 50-nm Technologies A and C. The gate currents stay almost in the same range at 50-nm gate length as for the 100-nm mHEMT for this epitaxy, but the technology offers a higher transconductance and, therefore, higher gain and transition frequency.

The 50-nm Technology C shows approximately 50% more transconductance at low bias currents than Technology A, which allows to operate the HEMTs with less channel noise power at the same gain level or with higher gain at the same channel power level. It has been shown that this transconductance increase directly translates to higher f_T values, proofing that the enhanced transconductance is not compensated by higher device capacitances. These advancements have been achieved by the use of a single channel with 80% indium content. The single channel removes a plateau from the dc transconductance curve that has been observed for composite channels at cryogenic temperatures. This decrease in the slope of the transconductance moves high transconductance values toward higher drain currents. A hypothesis that might explain the reason of the g_m plateau for composite channels at cryogenic temperatures is given in the following.

The overall channel thickness is larger for composite channels due to the subchannel, which was originally introduced to provide higher breakdown voltages. When the HEMT is driven from ON-state to pinchoff, the conduction band level is bend above the Fermi level, resulting in the depletion of the channel. This causes a shift of the carrier concentration toward the subchannel, which increases the distance between the gate and the carriers. At low gate voltages (just before pinchoff), the majority of the channel electrons is located in the lower part of the composite channel since the conduction band is just slightly bent below the Fermi level. The higher gate-to-carrier distance worsens the carrier control and consequently limits the transconduction. The pinchoff behavior is degraded by this movement of the carriers, which dynamically modulates the threshold.

When the gate voltage is swept into the opposite direction, driving the channel from pinchoff to conduction state, the carrier concentration moves toward the gate. Once the majority

of carriers concentrates in the main channel, a better control of the carriers is obtained and the transconductance is not limited by high gate-to-effective-channel distance anymore. Therefore, the transconductance increases again after the plateau.

The use of a single channel with high indium content results in a well-shaped transconductance behavior with a very high slope at low current values, making 50-nm Technology C the optimal choice for low-power and low-noise operation.

Table III compares the presented amplifiers with state-of-the-art cryogenic Ku-band LNAs. All presented LNAs demonstrated an average gain of more than 29 dB in the frequency regime between 8 and 18 GHz and an average noise temperature below 7.6 K at 10 K ambient temperature is achieved for all variants.

The noise-optimized 50-nm Technology C exhibits the highest gain of all cryogenic LNAs reported in the literature with an average of 39.4 dB. An average noise temperature of 4.2 K between 8 and 18 GHz at an ambient temperature of 10 K is obtained with a minimum of only 3.3 K. To the best of the authors' knowledge, this is the first time that a cryogenic LNA demonstrates such a low effective noise temperature in the Ku-band. It shall be mentioned that this LNA is implemented as a full MMIC solution with on-chip input matching network, which provides options for compact cointegration into multifunctional or multichannel chips.

IX. Conclusion

In this article, an investigation of mechanisms causing noise in mHEMTs at cryogenic conditions is shown. mHEMTs of different gate length and epitaxial structures have been investigated to separate the origin of effects influencing the noise temperature at cryogenic conditions. Several observations for the design of ultra-low-noise HEMT technologies conclude from this investigation: high transconductance and gain at low current bias can be achieved by the use of a single, thin InGaAs-channel structure with high indium content. It has been demonstrated that composite channel structures can limit the increase of transconductance with the drain current at low currents due to a plateau in the transconductance curve at cryo.

Gate-length scaling below 100-nm needs to account for different effects such that it provides advantages in terms of noise temperature. Reducing the heights of the gate barrier layer maintains channel control but increases gate leakage due to tunneling effects, which degrades the noise performance. A tradeoff between a favorably short gate length and a gate–channel distance, which is high enough to maintain low leakage currents but thin enough to provide proper channel control, is necessary. The newly developed 50-nm Technology C combines all the mentioned advantages by the use of a single channel with high indium content, a precisely scaled gate barrier providing low leakage currents, and a short enough gate length for high gain and high transition frequency. The state-of-the-art noise performance of this technology variation at cryogenic temperatures has been demonstrated at the example of an extended Ku-band LNA MMIC. To the best of the authors' knowledge, the LNA has the lowest noise temperature among cryogenic LNAs reported in the Ku-band. An average noise temperature of 4.2 K with a minimum value of only 3.3 K at an ambient temperature of 10 K has been achieved at 8–18 GHz. This proofs that the noise-optimized 50-nm Technology C is the optimal candidate for cryogenic ultra-low-noise amplification.

It has been demonstrated that further scaling of the gate length of HEMTs even below the 100-nm node can be done successfully, even in terms of noise performance, when related parameters are optimized as well. It is the belief of the authors that the findings presented in this article should also apply to InP HEMTs due to the similar structure of the active epitaxial layers.

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