New Transistor Behavioral Model Formulation Suitable for Doherty PA Design

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***Abstract*— This work presents a new artificial neural network (ANN) model formulation for RF high-power transistors which includes the S-parameters of the active device. This improves the small-signal extrapolation capability, and the OFF-state impedance approximation, making it suitable for Doherty power amplifier (DPA) design. This extrapolation capability plays a key role in the correct Doherty load modulation prediction, since, at low power levels, the peaking PA is subjected to active loads that cannot be synthetized with a passive load-pull system, forcing the model to extrapolate. Thus, the proposed model formulation is able to solve the issues that are normally observed when ANN-based models are used in complex PA architectures as the Doherty PA. To validate the proposed behavioral model, a 700-W asymmetrical LDMOS DPA, centered at 1.84 GHz, was simulated and measured.**

***Index Terms*— Artificial neural network (ANN), behavioral model, Doherty, load modulation, passive load-pull, power amplifier.**

I. Introduction

THE Doherty power amplifier (DPA) is, nowadays, the wireless base-station workhorse in what RF signal amplification is concerned [1]–[4].

Accurate nonlinear models for the state-of-the-art high-power transistors are very difficult to obtain mostly because of the thermal issues and the distributed nature of these devices [5]. Therefore, the conventional Doherty design process is normally based on load-pull and S-parameter measurements. From these measurements, the optimal power load (Z_{pwr}) is determined and the optimal efficiency termination for a particular VSWR, defined on this chosen power load, is selected. This VSWR imposes the back-off for the first efficiency peak, which is often referred to as the load-pull ratio (LPR) [6]–[8]. With this information, the output matching networks (OMNs) are designed to perform the necessary impedance transformation between the drain terminal of the device and the output combiner node, for two specific output power levels. The final step is to design the input matching networks (IMNs) to impose gain, ensure stability, and guarantee that the currents are, indeed, added in phase at the combining node. This step is usually done in the laboratory by performing fine adjustments to specific delay lines while evaluating the overall performance, which is usually a very time-consuming process. Therefore, PA designers would benefit from having the load-pull information accurately represented in the simulation environment, so that this fine-tuning process could be done *a priori*.

There are several ways to incorporate measurements in CAD simulators, which can be divided into two groups: look-up tables (LUTs) and equation-based behavioral models.

LUT-based models are perhaps the most direct way to incorporate measurements in CAD simulators. However, there are some known difficulties in data interpolation and extrapolation capabilities of such approaches. On one hand, they require a considerable amount of measurements to be accurate within a given extraction area and those measurements must be stored in memory during simulation. On the other hand, they also reveal poor extrapolation capabilities, as demonstrated in [9]. These drawbacks promote the usage of equation-based approaches that can accurately interpolate the data and reduce the required measurements.

The most well-known equation-based behavioral models in the literature can be divided into poly-harmonic distortion (PHD) models [10], Padé-approximation-based formulations [11], and artificial neural networks (ANNs) [12]. The PHD model is a black-box, frequency-domain, modeling technique based on the idea of extending S-parameters for large-signal conditions [9]. Over time, several behavioral formulations based on this approach have been proposed, such as the X-parameters [10] and the Cardiff model [13], [14]. Both formulations have been successfully used in power amplifier design. In [10] and [13], the X-parameters proved to be suitable for Doherty PA design, as long as they are made load-impedance-dependent, which requires an internal

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LUT for the model parameters for each load condition. In [14], an active device behavioral model is created through the Cardiff formulation. In this model, the core principle is to take advantage of the periodicity of the phase to create a multidimensional Fourier series to approximate a PHD function. Other options such as Padé-approximation-based models [11], [15] and Bayesian inference-based models [16], [17] have been proposed, but all of them need a large number of coefficients or have to internally incorporate an LUT to mimic the load dependence.

The previously mentioned model implementations rely on polynomial forms in which the number of parameters grows exponentially with the number of inputs and with the polynomial order, a problem known as the Curse of Dimensionality [18]. In the ANN case, the number of parameters only grows either linearly or quadratically [5], reducing the model complexity since it is able to represent complex functions with a low number of coefficients, [5], [9], [19]. In the active device modeling framework, the sigmoid is one good example of an activation function normally used for the neurons, as its graphic shape resembles the typical transistor current source or the PA's gain compression characteristics. For all these reasons, ANNs are conquering their space in the microwave circuits modeling world [19], [20].

Most of these models are very accurate in mimicking the single-ended PA responses, where we are mostly interested in the high-power region and so small signal is not critical except for stability analysis. However, the Doherty PA introduces an additional challenge: the small-signal behavior of the peaking PA becomes relevant near the first efficiency peak, since it will determine the impedance presented to the carrier device. Unfortunately, erroneous extrapolation can occur when a behavioral model is considered, especially when it is extracted from passive load-pull data. This issue will be further explored in Sections II and III.

In this article, we intend to solve the problem in ANN-based models by creating a new behavioral model formulation that incorporates the small-signal S-parameters of the transistor. With the improved extrapolation for very low power levels, it will be possible to accurately predict the DPA's AM/AM and AM/PM characteristics and the load modulation trajectories for both the carrier and the peaking PAs.

This article is organized as it follows. In Section II, we take the conventional modeling approach as a starting point to analyze and demonstrate the problem and then describe in detail the proposed formulation. The validation results are presented in Section III where we demonstrate the validity of the proposed formulation by comparing its predictions of a 700-W DPA performance with those of a conventional ANN behavioral model.

Since the main goal is to evaluate the accuracy of the model formulation, we chose a transistor with an available equivalent-circuit model. Even though this model is not very accurate, as it is normal for high-power devices, it allows us to assess the viability of the proposed formulation without any measurement or calibration errors. Thus, if we compare the available circuit model with the ANN models, any differences are solely due to the ANN model formulation.

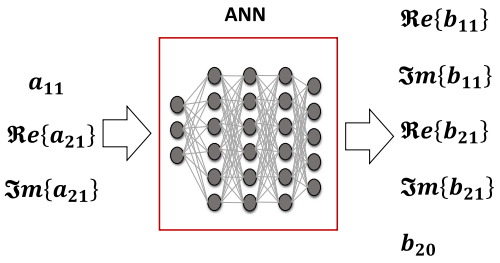

Fig. 1. Conventional ANN behavioral model formulation.

II. ANN Formulations Based on Passive Load-Pull Data

In cellular base stations, it is necessary to use devices with large gate peripheries to achieve the desired high-power levels. This requires the use of transistors with built-in prematching circuitry allowing the transformation of the very low impedances at the intrinsic reference plane, to manageable impedance values, at the package plane [5], [21]. Along with the package, this prematching circuitry sets the harmonic impedances at the intrinsic reference plane, regardless of the harmonic terminations at the output [5]. Therefore, extracting behavioral models for these high-power devices becomes simplified, since only the fundamental and baseband data are needed [23]. Besides this modeling simplification, in this work, the modeled data are restricted to the zone that contains the efficiency and power termination of the transistor, not the entire Smith chart.

Hence, the swept power load-pull data, which PA designers have already been using to characterize field-effect transistors, can be used to develop a behavioral model.

A. Conventional Formulation

The direct approach to behavioral modeling using power waves is to represent the reflected waves, b_{ph}, as a function of the incident waves, a_{ph}, where p indicates the port and h the harmonic order. Conventionally, when using the ANN modeling approach, this relationship is mapped directly using the formulation

$$[b_{p1}, b_{20}] = F_{\text{ANN}}(a_{11}, a_{21}) \tag{1}$$

where the representation, presented in Fig. 1, has been truncated to: 1) only model the fundamental and baseband responses (as previously indicated) and 2) model the transistor for a specific bias. Moreover, a_{11} is taken as a phase reference, which means that the measured power waves will be normalized in phase before calculating the ANN and denormalized after. This approach is taken throughout the article and so: 1) the outputs are always at harmonic zero or one and 2) there is no dependence on components at harmonic 0; and a_{11} is always considered a real, positive, number.

The a_{11} phase normalization must respect the principle of time invariance, that is, for the hth harmonic, the normalization should be $a_{ph}e^{-jh\angle a_{11}}$ and $b_{ph}e^{-jh\angle a_{11}}$. The denormalization adds back the phase of a_{11}: $a_{ph}e^{jh\angle a_{11}}$ and $b_{ph}e^{jh\angle a_{11}}$.

This also guarantees that the model behaves similarly (except for the phase rotation) for any phase of a_{11}, as expected for a time-invariant device.

Taking all this into consideration, the ANN model outputs are, then, the real and imaginary parts of the scattered power waves, b_{11} and b_{21}, at the fundamental frequency ($h = 1$), and the dc component ($h = 0$) for efficiency calculation, b_{20}, that is computed in the same way as the fundamental power waves, but using the dc current and voltage. Since the drain and gate voltages are fixed, there is no need to feed a_{20} or a_{10} to the model. Since no dc gate current is observed for the used LDMOS device, b_{10} is not required as an output. The inputs are the incident power waves at the fundamental in port 1, a_{11}, a real number since it is the phase reference, and in port 2, a_{21}, represented by its real and imaginary parts, as distinct inputs.

Note that although the ANN formulation is formulated as $b_{ph}(a_{11}, a_{21})$, it is in fact extracted with a_{11} and Γ_L sweeps, where a_{21} is obtained by $a_{21} = \Gamma_L b_{21}$, that is, a passive load-pull method, which is commonly the only available method for high-power devices.

The ANN training step is performed until the load-pull measurements are predicted with an acceptable degree of accuracy. The selection process of the ANN architecture will be discussed in Section III. However, for a robust practical implementation in CAD environment, additional care must be taken to ensure well-behaved interpolation and extrapolation capabilities for correct simulations and power amplifier design. Thus, different formulations can lead to different predictions when used in a simulator, although the obtained error during the extraction can be almost the same.

Improper interpolation within the range of measurement conditions usually occurs due to overfitting, which can be minimized through division of the original measured data into three sets for training, validation, and testing.

The extrapolation capability, however, depends greatly on the formulation. While large-signal extrapolation is usually important during simulation convergence, if the underlying formulation provides a smooth and limited response, the simulator is able to converge in most situations. However, the small-signal extrapolation can be problematic since there are PA architectures that use a mix of class AB and class C devices whose large-signal and small-signal performance is interdependent.

Although with this formulation the large signal response of the device under CW excitation can be well-represented, as long as the complexity of the model is enough to represent the measurements, it can be demonstrated that this behavioral model approach is not suitable for DPA design. The model may not only incorrectly extrapolate b_{21} when $a_{21} \neq 0$ and $a_{11} = 0$, resulting in an incorrect peaking OFF-state output admittance, $Y_{22_{\text{OFF}}}$, but also incorrectly predict the small-signal gain either by extrapolation reasons or poor extraction conditioning.

To explain the problem of wrong small-signal gain prediction, let us analyze how the error in the output reflected wave, Δb_{21}, is propagated to the gain at small signal, that is, when

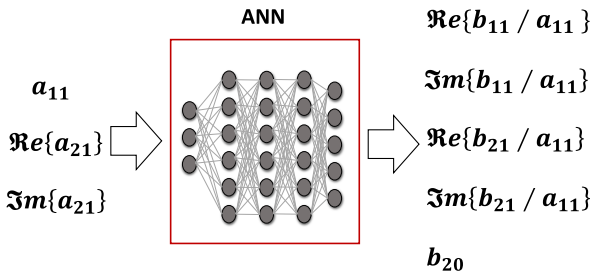

Fig. 2. Detailed formulation of the ANN using a gain formulation.

a_{11} is very small

$$\Delta G_T = \hat{G}_T - G_T = \frac{\left|\hat{b}_{21}\right|^2 - |a_{21}|^2}{|a_{11}|^2} - \frac{|b_{21}|^2 - |a_{21}|^2}{|a_{11}|^2} = 2\frac{|b_{21}|\cos(\Delta\theta)}{|a_{11}|^2}|\Delta b_{21}| + \frac{|\Delta b_{21}|^2}{|a_{11}|^2} \tag{2}$$

where $\Delta\theta$ is the phase difference between b_{21} and Δb_{21}. For the worst case, this error becomes

$$\Delta G_{T,\max} = 2\frac{|b_{21}|}{|a_{11}|^2}|\Delta b_{21}| + \frac{|\Delta b_{21}|^2}{|a_{11}|^2}. \tag{3}$$

As seen in (3), the error Δb_{21} is magnified when propagated to the small-signal gain error, since it is divided by a very small a_{11} excitation.

A possible alternative that partially solves these low-power extrapolation problems could be to use a gain formulation. This would force b_{21} to tend to zero as a_{11} decreases toward zero; the conventional formulation can be reformulated as

$$[b_{p1}/a_{11}, b_{20}] = F_{\text{ANN}}(a_{11}, a_{21}) \tag{4}$$

which means that to extract the ANN we must normalize the reflected waves by a_{11}, as shown in Fig. 2.

Thus, for small values of a_{11}, the reflected waves will also tend to be small, directly solving the small-signal prediction problem. This can be understood if we perform the same small-signal gain error analysis as before. Now, the error in b_{21} wave is proportional to the amplitude of a_{11}, $\Delta b_{21} = a_{11}\hat{e}$ and so the error of the small-signal gain can be given by

$$\Delta G_{T,\max} = 2\frac{|b_{21}|}{|a_{11}|}|\hat{e}| + |\hat{e}|^2. \tag{5}$$

As seen from (5), this formulation does not completely solve the problem since one term of the error is still inversely proportional to a_{11}, but it considerably reduces the error magnification.

As previously explained, characterization of high-power devices is normally done at their package reference planes. Because of that, OMNs are usually optimized at this plane, from where the optimum efficiency and output power loads were extracted. When these previously characterized high-power active devices are used in Doherty PA arrangements, for small power levels, the peaking amplifier should be seen as an open circuit, one of the reasons why some offset lines are needed at the peaking PA output [22]. Unfortunately, the OFF-state output admittance of the device changes with frequency due to the parasitic elements of the package, and so

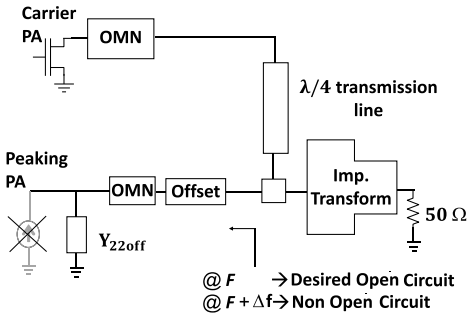

Fig. 3. Illustration of how $Y_{22\text{off}}$ can originate load impedances different from the desired open circuit in broadband Doherty implementations.

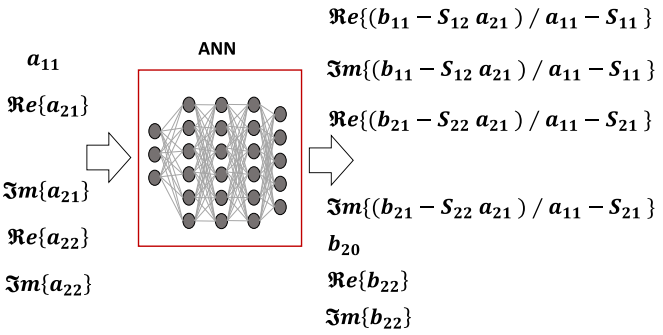

Fig. 4. Proposed ANN formulation.

the impedance presented by the peaking PA can be different from the desired open circuit within the PA bandwidth. This is represented in Fig. 3 by $Y_{22\text{off}}$, the PA OFF-state output admittance. Since $Y_{22\text{off}}$ is not an open circuit, some of the output current of the carrier PA will flow into the peaking PA, possibly even consuming some power if $Y_{22\text{off}}$ is not purely reactive. From the perspective of the peaking device, it is being loaded with an active load. However, since the model was extracted only using passive load-pull data, the model will extrapolate the behavior of the device under these conditions.

Although gain formulation may solve the single-ended performance at small signal, the simulation of a DPA configuration will certainly have problems both in small-signal and peaking impedance prediction, since S_{22} of the model will always be zero. This can be proved by the following expression:

$$S_{22} = \left.\frac{b_{21}}{a_{21}}\right|_{a_{11}=0} \left.\frac{F_{\text{ANN}}}{a_{21}} a_{11}\right|_{a_{11}=0} = 0. \tag{6}$$

This means that a different formulation must be considered, where a_{21} must also play a role in small-signal extrapolation.

To solve this problem, active load pulling could be a solution to capture the behavior of the peaking PA in those conditions. Unfortunately, there are cases where these systems cannot be used: either the required nonlinear network analysis instrumentation is too expensive [19]; [23]–[25] or the DUT is a very large device, which requires a very high power and linear excitations to synthesize the loads. The alternative is to use a passive load-pull system, though the capability to synthetize active loads is lost.

B. Proposed Formulation

Since the behavioral model will be extracted from passive load-pull characterization data collected at the transistor package reference plane, we can embed the peaking PA $Y_{22\text{off}}$ in the model by including the small-signal S-parameters into the formulation, as follows:

$$\begin{cases} b_{p1} = \left[F_{\text{ANN}}(a_{11}, a_{21}) + s_{p1}\right] a_{11} + s_{p2} a_{21} \\ b_{20} = F_{\text{ANN}}(a_{11}, a_{21}) \end{cases} \tag{7}$$

which means that to extract the ANN a mathematical manipulation is needed *a priori*, as shown in Fig. 4.

Note that now, even for the case where a_{11} is equal to zero, b_{21} may not be zero, due to the presence of a_{21}, which is exactly what happens in the Doherty PA when the peaking is off. In fact, the new formulation now imposes that b_{21} is linearly dependent on a_{21} when a_{11} is zero and forces the correct S_{22}. Thus, with this approach, both small-signal and load modulation trajectories of the main and peaking PAs will be correctly modeled.

Although, in this work, we have focused on modeling a prematched device for a high-power Doherty PA, where the prematching reactances act as harmonic traps, and thus the harmonic excitation at the package plane does not have any significant impact on the behavior of the device, the proposed formulation can also be expanded to include this dependence. That formulation, along with a brief analysis, can be found in Appendix A.

III. Application to a Practical Doherty PA

This section presents the results of the conventional and the proposed formulation in a Doherty PA. The objective is to demonstrate the problems derived from the conventional formulation and to validate our proposed formulation.

The ANN models were implemented in the Advanced Design System (ADS) circuit simulator through an FDD block, which enables the creation of nonlinear components based on user-defined equations, in the frequency domain. This ADS model is then compared with the existent commercial circuit model for performance evaluation. Although the main goal is to evaluate the behavioral model in a DPA simulation, the single-ended class B and C amplifiers are also used in the analysis.

A. Behavioral Model Extraction

The carrier and peaking PA behavioral models were extracted via ADS simulations using the passive load-pull approach.

In the single-ended simulations, the models were cross-validated, that is, different sets of loads were used for extraction and validation. These loads are represented in Fig. 5 alongside with the two loads selected for the gain and efficiency power sweep plots (black crosses). The extraction was done by sweeping the power from 23 to 48 dBm, that is, 25 dB of back-off, while the validation was done from 13 to 48 dBm, that is, 35 dB of back-off. In this way, it is possible to observe the model extrapolation in very low-power regions.

Using the corresponding MATLAB toolbox, the ANN model was extracted for several layer sizes as shown

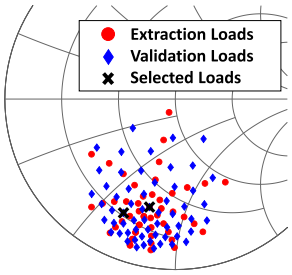

Fig. 5. Loads used in simulation (Z_0= 3Ω).

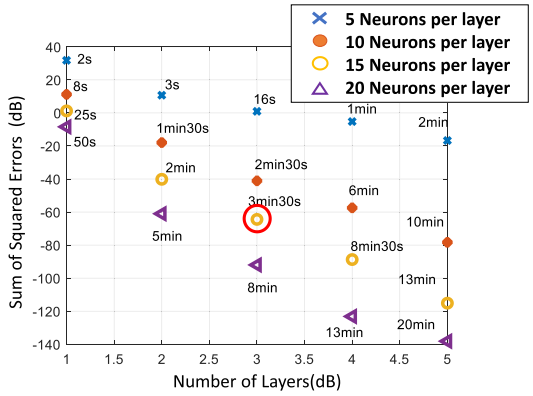

Fig. 6. Performance of several ANN architectures for this implementation (sum of squared errors (sse)/complexity/extraction time).

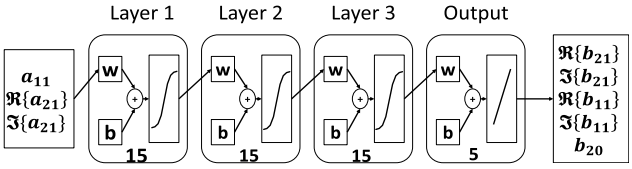

Fig. 7. ANN structure for the conventional formulation. For the proposed formulation, the structure is the same, but with the respective outputs.

in Fig. 6. An ANN with three layers of 15 neurons each ([15 × 15 × 15]) was chosen, since it proved to be sufficient to fit the measurements with the best compromise between complexity, accuracy, and extraction time. The hyperbolic tangent was chosen as the activation function of these neurons. The selected ANN structure is presented in Fig. 7. Naturally, the inputs and outputs were adapted to be coherent with each model formulation. The tested formulations followed the ANN models depicted in Figs. 1 and 4.

The Bayesian regularization algorithm from MATLAB was used to train the ANNs used in this work. This algorithm not only seeks to optimize the cost function but also seeks to reduce the number of effective parameters and lower their values. This has proven to be beneficial to improve the interpolation capabilities of the model and reduce the overfitting problem.

Note that the behavioral model is parametrized in frequency and in the V_{GG} bias voltage, which means that we can use the same model for the peaking and main amplifiers by changing the correspondent bias voltage. The source impedance Z_S was set to be the one estimated for the final DPA arrangement, but since we are also modeling b_{11} we could change Z_S during the design.

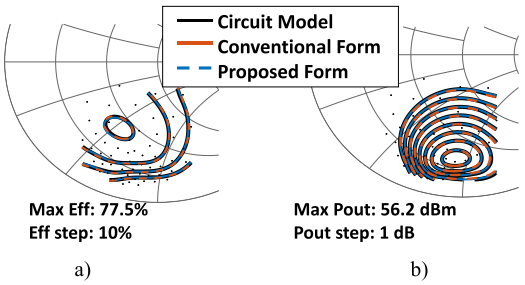

Fig. 8. (a) Efficiency and (b) output power contours for class B biasing (Z_0= 3Ω).

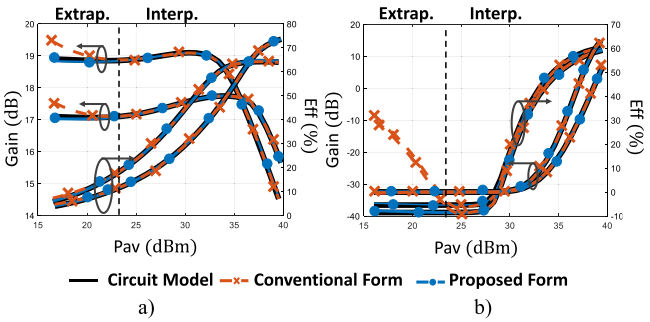

Fig. 9. Gain and efficiency plots for (a) class B and (b) class C biasing for two different load conditions.

B. Load-Pull Contours

As previously discussed, the conventional formulation can accurately represent the active device as long as the transistor is not driven outside the extraction region. So, if we only analyze the model considering the power or efficiency contours, the model will seem to be accurate enough for PA design, as can be seen in Fig. 8 for class B biasing. In fact, if we compare with our proposed formulation, we will not detect any significant differences.

The models must be tested in different conditions to be properly evaluated. Thus, we started by evaluating the single-ended PA case. Since we are interested in designing a Doherty PA, both class B and class C will be analyzed.

C. Single-Ended Amplifier

By taking the conventional and proposed model formulations and simulating the gain and efficiency over a large power sweep for class B biasing, we obtain the results presented in Fig. 9(a). Note that these results show us two different load terminations and test the lower power extrapolation by 5 dB.

By observing these class B results, the differences between the formulations are already clear in the low-power extrapolation region. However, the problem aggravates for the class C amplifier. At low input power, this amplifier operates in the cutoff region, so small-signal problems will become much more noticeable, as can be seen in Fig. 9(b). Here, we can observe that in the conventional formulation, the gain prediction in the extrapolation region does not behave in a controlled manner.

By including the S-parameters in the proposed model, it remains very accurate in the low-power region. This demonstrates that the small-signal extrapolation problems can indeed be solved using the proposed formulation.

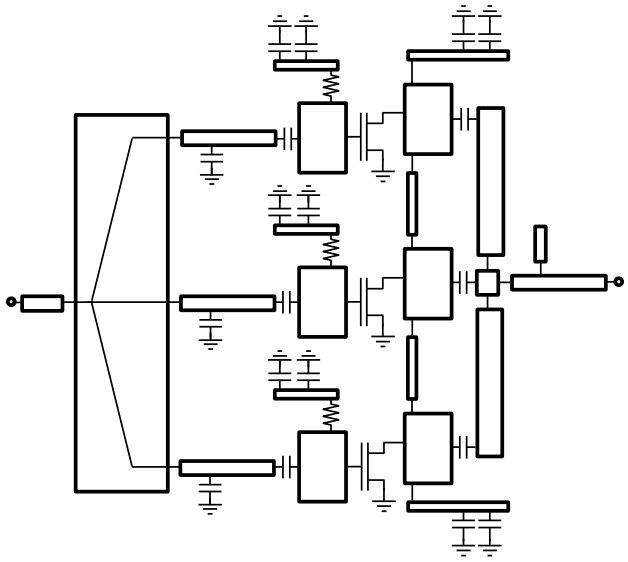

Fig. 10. Two-way Doherty PA topology used in this work.

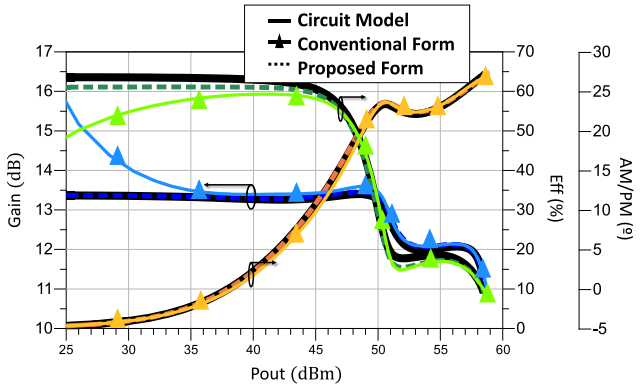

Fig. 11. Comparison between the circuit model and ADS behavioral models (conventional and proposed) of gain, efficiency, and AM/PM curves.

D. Doherty Power Amplifier

To validate the proposed behavioral model approach for DPA simulations, we designed and implemented a 700-W, two-way asymmetric DPA at 1840 MHz. The DPA is composed of three 250-W LDMOS devices, one for the carrier PA and two for the peaking PAs that will provide the appropriated load modulation. The circuit and behavioral models were used to simulate the DPA in the ADS simulator. The complete DPA schematic is presented in Fig. 10.

Fig. 11 depicts the efficiency, gain, and AM/PM performance obtained for both formulations (conventional and proposed) using the designed Doherty PA at 1.84 GHz.

It is possible to observe that the conventional formulation is inaccurate in the low-power region. In fact, in Fig. 9 we can already observe this issue. Naturally, the same problem happens in Doherty operation and is further aggravated by the wrong prediction of the peaking impedance trajectory at back-off, which results in a wrong impedance presented to the carrier. In Fig. 12, this problem is highlighted in a red circle. Since this error cannot be controlled during the model extraction due to improper formulation, the model will

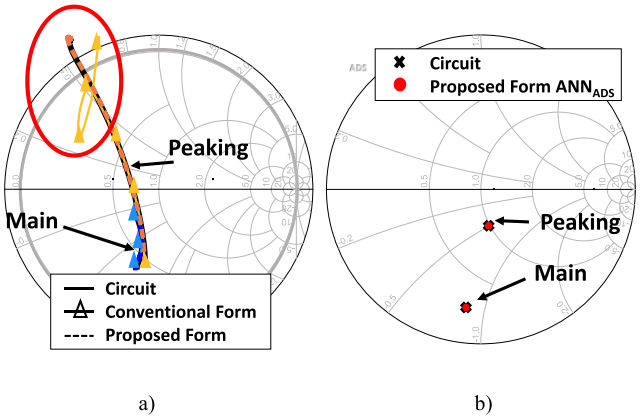

Fig. 12. Comparison between the circuit model and ADS behavioral models (conventional and proposed) of main and peaking: (a) impedances trajectory at the fundamental and (b) S_{22} values (Z_0= 3Ω).

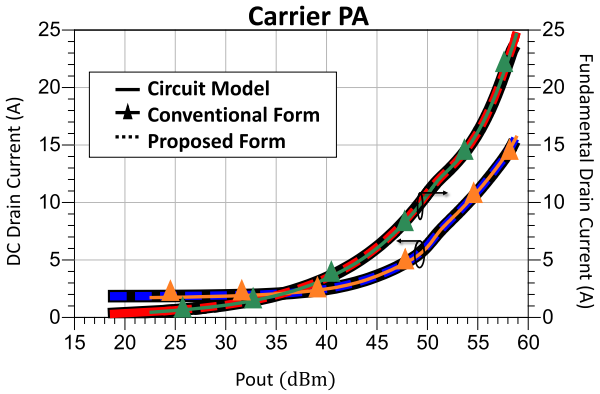

Fig. 13. Comparison of dc and fundamental drain current curves between the circuit and ANN models, for both formulations (conventional and proposed), for the carrier PA.

extrapolate differently for different extractions, resulting in a high variance on the performance prediction.

On the contrary, our proposed formulation presents a good agreement with the circuit results, solving the aforementioned extrapolation problems and thus proving to be much more suitable to predict the Doherty behavior.

To further validate the proposed model formulation, S_{22} of the carrier and the peaking amplifier are presented in Fig. 13. As observed, the S_{22} values are correctly predicted. No results of S_{22} are presented for the conventional formulation, because the simulation does not provide reasonable results, since it is extrapolated to $|S_{22}| > 1$, that is, an active load impedance.

In addition, in Figs. 13 and 14 we show the comparison of dc and fundamental drain current curves between the circuit and ANN models for both formulations. As observed in Fig. 14, the error in the prediction of the ANN model with the conventional formulation is greater than that of the proposed formulation.

To further illustrate the advantages of the proposed model, regarding the small-signal extrapolation issue, another example is presented in Appendix B, where the behavioral model is used to predict the circuit simulation performance of a two-stage amplifier.

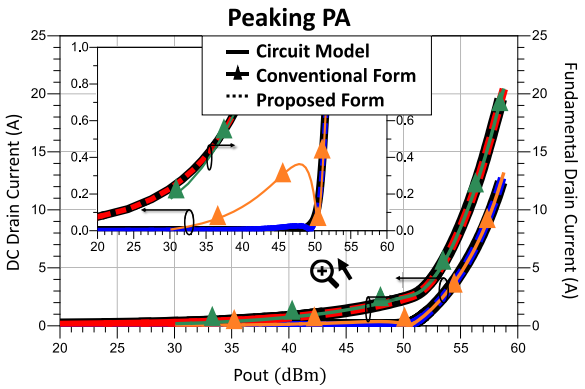

Fig. 14. Comparison of dc and fundamental drain current curves between the circuit and ANN models, for both formulations (conventional and proposed), for the peaking PA.

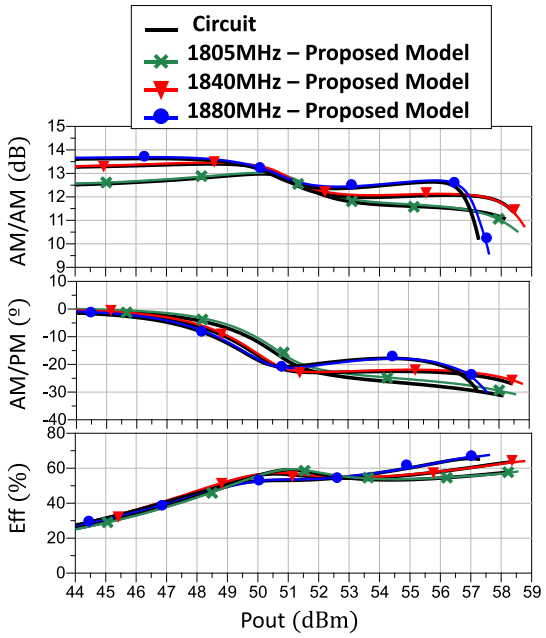

Fig. 15. Comparison of AM/AM, AM/PM, and efficiency obtained with the DPA circuit simulation and with the proposed behavioral model formulation.

E. Model Validation and Experimental Results

It is now important to evaluate the model in several frequencies to correctly verify its validity in Doherty operation. The Doherty PA was implemented and measured at 1.805, 1.84, and 1.88 GHz.

In Fig. 15, AM/AM, AM/PM, and efficiency curves are presented, where we can verify that the behavioral model successfully emulates the circuit model. This means that the model can be effectively used as a substitute to circuit models in cases where those are not possible to obtain. In Fig. 16, the AM/AM, AM/PM, and efficiency measurements are shown.

Comparing the simulation results with the measurements, it is possible to observe that except for the frequency of 1880 MHz, the output power predicted by the simulations is higher. Furthermore, the high-power measured efficiency is lower than the simulated one, and some differences start to be

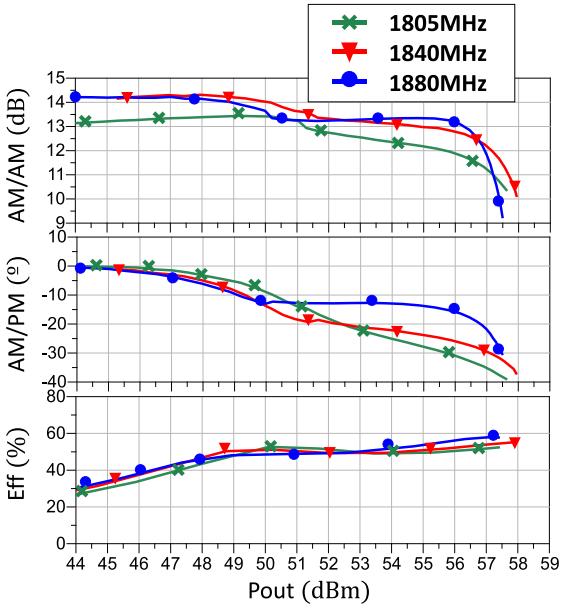

Fig. 16. AM/AM, AM/PM, and efficiency measurements for 1805, 1840, and 1880 MHz.

noticeable in the AM/PM curves from 50 dBm onward of the output power.

These results may indicate that the transistor large-signal nonlinear model is not completely accurate, as is common for high-power devices, in addition to some imprecision in the Doherty implementation and measurement process.

To increase the accuracy of the proposed ANN behavioral models, they should be extracted directly from the swept power passive load-pull measurements, which most of the time is easier than to extract a more accurate circuit-level model for high-power transistors, this being one of the ANN behavioral model advantages.

IV. Conclusion

In this work, we demonstrated that incorporating the active device small-signal S-parameters in the behavioral model formulation solves small-signal and active load prediction problems in a Doherty PA configuration. These problems occur due to improper extrapolation of the conventional model formulation and cannot always be solved simply by performing more measurements. For example, if a passive load-pull system is used, the active loads cannot be tested.

Based on an ANN, a behavioral model was formulated, implemented in a commercial simulator, and validated for an implementation of a DPA. The final model formulation allows the use of passive load systems without compromising its accuracy, by including the description of the S-parameters, a typically simple, commonly available, added measurement. As demonstrated, the model can predict the active loads produced by the Doherty peaking PA, so that there is no need to use an active load-pull system. This advantage is particularly useful for very high-power transistors, commonly used in wireless communications.

Appendix A

The model formulation proposed in this work can be expanded to include the output second-harmonic dependence

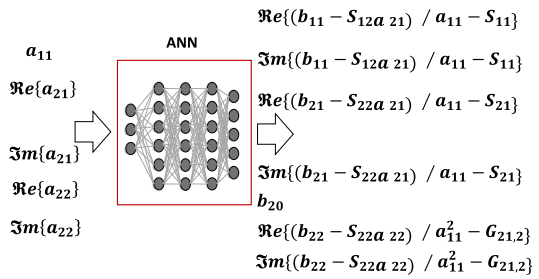

Fig. 17. Proposed ANN formulation with the second-harmonic drain information.

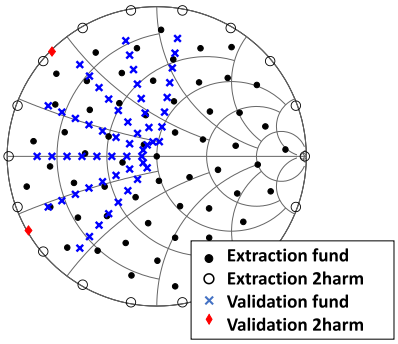

Fig. 18. Extraction and validation loads for the second-harmonic implementation (Z_0= 50Ω).

according to (8). Note that in this case, the ANN function can be understood as the conversion gain from fundamental to second harmonic. In that sense, similar to what we have done for the fundamental formulation when we included the S-parameters, here we are including a conversion gain parameter, $G_{21,2}$, which can be defined as (9)

$$\begin{cases} b_{p1} = \left[F_{\mathrm{ANN}_{p1}}(a_{11}, a_{21}, a_{22}) + s_{p1}\right]a_{11} + s_{p2}a_{21} \\ b_{20} = F_{\mathrm{ANN}_{20}}(a_{11}, a_{21}, a_{22}) \\ b_{22} = \left[F_{\mathrm{ANN}_{22}}(a_{11}, a_{21}, a_{22}) + G_{21,2}\right]a_{11}^2 + s_{22}a_{22} \end{cases} \tag{8}$$

$$G_{p_2p_1,h_{p_2}} = \left.\frac{b_{p_2h_{p2}}}{a_{p_1 1}^{h_{p2}}}\right|_{a_{22}=0,a_{12}=0.} \tag{9}$$

This G-parameter may be extracted from the load-pull information by the least-squares method. The block diagram of this implementation can be found in Fig. 17, where the mathematical manipulation that is required to extract the ANN is presented.

As previously mentioned, the transistor used in this work is a 220-W prematched LDMOS device whose prematching reactances behave as harmonic traps, making it insensitive to the input and output harmonic terminations. Thus, to validate this expanded model, we have now selected the CGH40010F packaged transistor, a 10-W GaN HEMT device from Wolfspeed. The load terminations used in this part are shown in Fig. 18. The power level was swept from −5 to 30 dBm, the center frequency was 2 GHz, and the device was biased at V_{DD}= 28 V and $V_{\mathrm{GG}} = -3.03$ V.

Fig. 19 shows the simulated efficiency and output power load-pull contours for a second harmonic where the efficiency is maximized, in (a), and minimized, in (b). As shown, the error is acceptable for both cases and the model can correctly predict the behavior of the transistor.

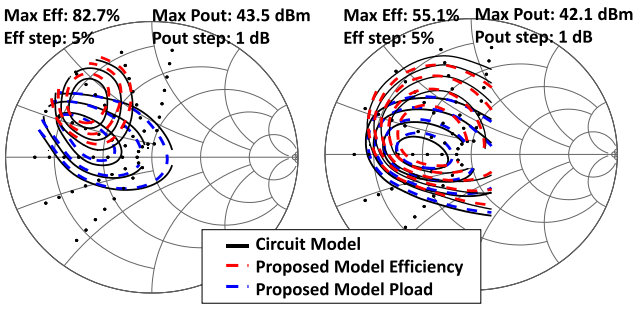

Fig. 19. Gain and efficiency contours for the (a) best and (b) worst second-harmonic loads.

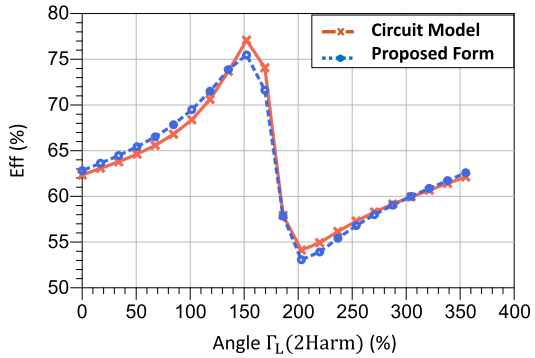

Fig. 20. Efficiency at 3 dB of gain compression for a constant fundamental frequency load and several second-harmonic loads.

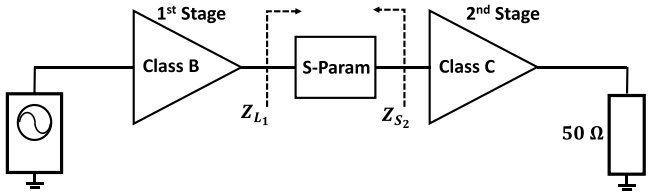

Fig. 21. Simplified block diagram of the implemented two-stage power amplifier.

To demonstrate the prediction capability of the model for a wider range of second-harmonic terminations, Fig. 20 presents the efficiency at 3 dB of gain compression for the same fundamental load. The second-harmonic loads are always kept in the edge of the Smith chart, that is, $|\Gamma_L| = 1$, and the phase is swept. As shown, there is a good agreement between the prediction obtained with the circuit model and from the proposed ANN model.

APPENDIX B

The small-signal problem treated in this article is relevant for many other applications beyond the Doherty operation. Any configuration where several stages of amplifiers are used may not be possible to simulate if the S-parameters cannot be accurately predicted. For instance, in a multistage monolithic microwave integrate circuit (MMIC) PA, where several devices are cascaded to boost the gain, it is very important to adapt the input of one PA to the output of a previous one. Thus, correctly predicting the input impedance, Z_{in}, is fundamental.

A simple two-stage cascaded PA, represented in Fig. 21, was built in the simulator, to demonstrate the impacts of

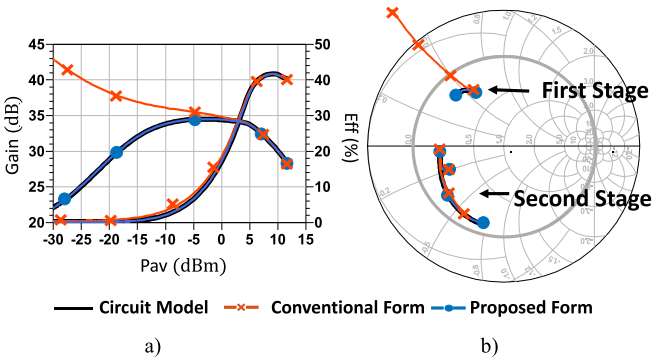

Fig. 22. (a) Gain and efficiency power sweeps and (b) input impedance for the two-stage cascaded power amplifier (Z_0= 10Ω).

poor small-signal prediction on these architectures. The represented S-parameter block guarantees the correct load and source terminations of the first- and second-stage amplifiers, respectively. For these simulations, the CGH4010F packaged transistor model from Cree was used.

The devices used in the first and second PA stages were biased above and below the threshold voltage, $V_{GG} = -2.4$ V and $V_{GG} = -3.2$ V, respectively. In both cases, the ANN models were extracted with a data set with the following characteristics: an operation frequency of 2 GHz; an available power between 0 and 35 dBm with 31 equally distributed values; and 50 loads distributed within a circle of $|\Gamma_L| = 0.8$, normalized to the optimum load at that frequency. Despite this load selection, the model is extracted with power waves normalized to 50Ω.

The two-stage PA gain and efficiency profiles are shown in Fig. 22(a). This shows that the conventional formulation starts to fail as soon as it starts to extrapolate, leading to a wrong small-signal prediction. On the contrary, the formulation presented in this work is able to mimic the reference circuit model. This is also evidenced by the input loads of both PAs, represented in Fig. 22(b). The conventional formulation fails to predict both impedances for all power levels. However, the prediction of the input impedance of the second-stage PA is better. This is expected, since the power level on the second stage is higher, and so the small-signal extrapolation problems are less notable. The proposed formulation proves to be highly accurate, demonstrating that unlike the conventional approach, this formulation is not only suitable for Doherty operation but also it can be used in many other circuits such as the herein shown multistage PA.

REFERENCES

[1] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[2] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, Feb. 2015.

[3] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA, USA: Artech house, 2002.

[4] B. Kim, I. Kim, and J. Moon, "Advanced Doherty architecture," *IEEE Microw. Mag.*, vol. 11, no. 5, pp. 72–86, Aug. 2010.

[5] P. Aaen, J. A. Plá, J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. New York, NY, USA: Cambridge Univ. Press, 2007.

[6] J. C. Nanan, D. Holmes, M. Bokatius, and J. Staudinger, "Tutorial on Doherty power amplifier circuits and design methodologies," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013, pp. 43–53.

[7] J. C. Pedro, L. C. Nunes, and P. M. Cabral, "A simple method to estimate the output power and efficiency load–pull contours of class-B power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1239–1249, Apr. 2015.

[8] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "Impact of trapping effects on GaN HEMT based Doherty PA load-pull ratios," in *Proc. Integr. Nonlinear Microw. Millimetre-Wave Circuits Workshop (INMMiC)*, Taormina, Italy, Oct. 2015, pp. 1–3.

[9] G. Avolio, A. Raffo, M. Marchetti, G. Bosi, V. Vadala, and G. Vannini, "GaN FET load-pull data in circuit simulators: A comparative study," in *Proc. 14th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Paris, France, Sep. 2019, pp. 80–83.

[10] D. E. Root, "Polyharmonic distortion modeling," *IEEE Microw. Mag.*, vol. 7, no. 3, pp. 44–57, Jun. 2006.

[11] J. Cai, J. B. King, B. M. Merrick, and T. J. Brazil, "Padé-approximation-based behavioral modeling," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4418–4427, Dec. 2013.

[12] Q.-J. Zhang, K. C. Gupta, and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design–from theory to practice," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 4, pp. 1339–1350, Apr. 2003.

[13] H. Qi, J. Benedikt, and P. J. Tasker, "Nonlinear data utilization: From direct data lookup to behavioral modeling," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 6, pp. 1425–1432, Jun. 2009.

[14] P. Tasker and J. Benedikt, "Waveform inspired models and the harmonic balance emulator," *IEEE Microw. Mag.*, vol. 12, no. 2, pp. 38–54, Apr. 2011.

[15] J. Cai, J. B. King, A. Zhu, J. C. Pedro, and T. J. Brazil, "Nonlinear behavioral modeling dependent on load reflection coefficient magnitude," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 5, pp. 1518–1529, May 2015.

[16] J. Cai, J. King, and J. C. Pedro, "A new nonlinear behavioral modeling technique for RF power transistors based on Bayesian inference," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 624–626.

[17] J. Cai *et al.*, "Bayesian inference-based behavioral modeling technique for GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 6, pp. 2291–2301, Jun. 2019.

[18] N. Gershenfeld, *The Nature of Mathematical Modeling*. New York, NY, USA: Cambridge Univ. Press, 1999.

[19] J. Cai, J. Wang, C. Yu, H. Lu, J. Liu, and L. Sun, "An artificial neural network based nonlinear behavioral model for RF power transistors," in *Proc. IEEE Asia–Pacific Microw. Conf. (APMC)*, Nov. 2017, pp. 600–603.

[20] C. M. Bishop, *Pattern Recognition and Machine Learning*. New York, NY, USA: Springer, 2006.

[21] J. Staudinger, P. Hart, and D. Holmes, "Behavioral modeling of Si LDMOS pre-matched devices with application to Doherty power amplifiers," in *Proc. IEEE Top. Conf. Power Modeling Wireless Radio Appl.*, Santa Clara, CA, USA, Jan. 2012, pp. 89–92.

[22] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42–50, Oct. 2006.

[23] J. Sirois, S. Boumaiza, M. Helaoui, G. Brassard, and F. M. Ghannouchi, "A robust modeling and design approach for dynamically loaded and digitally linearized Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 9, pp. 2875–2883, Sep. 2005.

[24] S. P. Woodington, R. S. Saini, D. Willams, J. Lees, J. Benedikt, and P. J. Tasker, "Behavioral model analysis of active harmonic load-pull measurements," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 1688–1691.

[25] J. Cai, J. Su, and J. Liu, "Large signal behavioral modeling of power transistor from active load-pull systems," in *Proc. IEEE Int. Symp. Radio-Frequency Integr. Technol. (RFIT)*, Nanjing, China, Aug. 2019, pp. 1–3.

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