Dynamic Supply Voltage Control for PA Output Power Correction Under Variable Loading Scenarios

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***Abstract*— This article presents an automatic system that is able to dynamically restore the output power capability of a power amplifier (PA) under variable loading scenarios. This is accomplished by dynamically adapting the supply voltage, V_{DD}, of the PA according to the developed theoretical model. To dynamically vary V_{DD}, a GaN dc–dc converter, based on the commercial EPC 9067 Demo Board, was used. The load is measured using an impedance meter, which is based on the slotted line principle and was specifically designed for low insertion loss. This impedance meter also generates a load-dependent pulsewidth modulated signal that controls the dc–dc converter switching, regulating V_{DD}. The prototype was designed for 3.55 GHz and tested with CW and modulated signal excitations, being able to compensate the output power degradation under variable loading conditions inside a 2.1 voltage standing wave ratio circle. For a constant gain compression level, the average efficiency degradation over the tested range of impedances is less than 5%, and the average power improvement is 0.7 dB. The worst case measured output power of the PA is compensated from 37.0 to 39.9 dBm, which corresponds to a 2.9 dB improvement. Using a modulated signal excitation, the peak envelope power, which is compressed by almost 3 dB without V_{DD} compensation, is restored, and the average output power is improved by 0.6 dB. The system can track the load and adjust V_{DD} with a worst case step-up delay of 25 ms.**

***Index Terms*— Load insensitivity, power amplifiers (PAs), V_{DD} modulation.**

I. Introduction

POWER amplifiers (PAs) are usually designed for a fixed output load, which implies that their performance can be severely degraded when operating with variable loading conditions, namely, in terms of conversion efficiency, linearity, output power capability, and even reliability. This load variation can happen due to the change of the load physical proprieties, in applications such as microwave cooking [1], plasma heating in, e.g., plasma-enhanced chemical vapor deposition (PECVD) processes [2], or cavities charging on particle accelerators [3]. In mobile communication devices, the load impedance presented to the radio frequency (RF) PA can also change due to moving objects in the proximity of the antenna, e.g., the hand effect [4], caused by the proximity between the hand and the antenna while holding a mobile phone. In fifth-generation (5G) massive multiple-input multiple-output (MIMO) base stations (BSs) with beamforming capabilities, the input impedance of different antenna elements also changes due to their mutual coupling [5].

Various techniques have been studied to improve PA's performance under variable loading operations. Circulators have been used for many years, being able to reduce the load variation seen by the PA by dissipating the reflected power in a dummy load, but do not maintain the delivered power [6]. In 5G massive MIMO antenna arrays, techniques that aim at reducing the mutual coupling at the antenna level can reduce the load variation seen by the PA, but they are dedicated only to MIMO applications [7].

Some complex PA architectures, for instance, balanced, Doherty, and outphasing PAs, have also been used to reduce load sensitivity in various applications [8]–[10]. Balanced amplifiers are based on two transistors operating in quadrature and on two quadrature couplers. They can deliver an almost constant output power under mismatch conditions at the expense of power dissipation in a dummy load when mismatched, as the combination becomes unbalanced, reducing the amplifier efficiency [8]. Digital Doherty PAs (i.e., Doherty PAs of two independent inputs in which the signal separation is performed at the digital level) can be driven with the appropriate signals to reduce the load variation seen by the carrier PA. In this case, some power of the peaking amplifier will be used to correct the carrier's load, but this will degrade the back-off efficiency of the PA and reduce its maximum delivered power. Moreover, this method is only able to compensate for variations toward loads lower than the nominal value, which is not

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always the case [9]. Sánchez-Pérez *et al.* [10] designed a tunable Chireix-type combiner to reduce the efficiency and output power variation of the amplifier under mismatch. However, the implemented combiner is tuned by manually changing the used components, and the extra losses added by tunable components are not measured.

Solutions implemented at the PA's output matching network (OMN) have also been tested. Transmission line resistance compression networks (TLRCNs) are very promising, but they require at least two loads varying synchronously [11]. Various tunable matching networks (TMNs), using varactors [12], [13], switched capacitor banks [14], or switched variable-length stubs [15] to perform a dynamic load matching, have also been implemented. This approach is very versatile and has a good tunability range but suffers from the extra losses added by the additional tunable components. These extra losses can be compensated by the increased efficiency for operation under the adjusted optimal load. However, note that just 0.3 dB of extra losses already cause a constant efficiency degradation of around 5% (for a 70% nominal efficiency), even when the amplifier operates under the nominal load. Thus, this technique is challenging in terms of losses, and it is only effective for a large mismatch, where the amplifier efficiency is degraded by more than 5%.

Load-dependent bias voltages can also improve PA performance under variable loading scenarios [9], [16], [17]. This can be done by controlling only the drain, or both the drain and gate, dc voltages to improve the performance of the PA for some loads. This solution becomes more attractive as the efficiency of dc–dc converters become higher. It is also implementable without adding extra components or added complexity in the RF path of the designed PAs.

This work is an extended version of [16] in which a theory-based load-dependent supply voltage, V_{DD}, variation that compensates the output power capability of PAs operating under variable loading conditions is developed. In [16], a PA was also developed under the introduced theory, and it was shown that the V_{DD} variation is a practical method to compensate the power degradation under variable loading conditions. Now, a complete system based on an impedance meter and the PA introduced in [16] is presented. This system is able to track the output load of the PA and dynamically change its V_{DD} according to the previously developed theory in a fully autonomous way, both under CW and modulated signal excitations. This system is physically implemented with a supply modulator made with a fast and efficient gallium nitride (GaN)-based switched dc–dc converter and an impedance meter that was specifically designed for low insertion loss, imposing a very small overall efficiency degradation. The architecture of the presented system makes it similar to envelope tracking (ET) applications, but with lower timing constraints. While, in ET PAs, V_{DD} must track the carrier envelope, requiring fast supply modulators that considerably reduce the total efficiency [18], in our case, V_{DD} should only track the movement of users, moving obstacles near antennas or other sources of load variation, which are typically much slower than the carrier envelope of telecommunication signals. Moreover, the required V_{DD} amplitude variation is lower than it is in ET PAs, so the necessary slew rate is much lower both due to the reduced speed and voltage swing requirements.

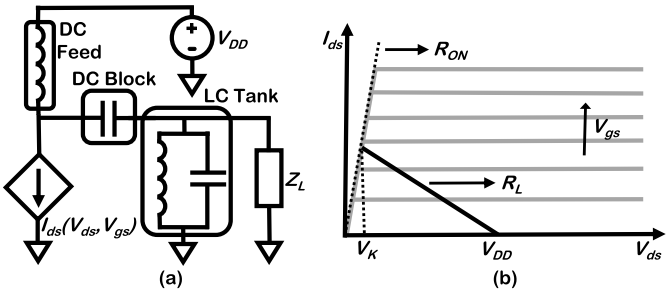

Fig. 1. (a) Simplified PA output circuit for the theoretical analysis. (b) Considered piecewise linear current source model.

This article is organized as follows. Section II demonstrates the derivation of the theoretical load-dependent V_{DD} values that correct the amplifier's output power capability. Section III presents the design and simulation of a Class B GaN PA using the derived V_{DD} values. Section IV shows the practical static validation of the proposed V_{DD}. Section V introduces the automatic V_{DD} controlled PA and its behavior under CW excitation. Section VI presents the system behavior under modulated signals. Section VII addresses the dynamic performance of the system and identifies its possible improvements. Section VIII presents the conclusions of this work.

II. Supply Voltage Variation Theory

The objective of this work is to achieve a load insensitive PA, from an output power capability perspective, while maintaining high-efficiency operation. To do this, first, it is necessary to calculate the dependence of the output power capability on V_{DD} and load terminations. Then, the drain voltage to be applied for each load, Z_L, needed to maintain the desired maximum output power, can be determined.

In order to achieve a constant maximum output power, the PA cannot be designed for the maximum power load. This happens because, when the load is shifted toward a lower value, increasing the V_{DD} would not compensate the power capability of the PA since the transistor would become current limited. Having this in mind, and also ensuring high-efficiency operation, the PA is designed for the maximum efficiency load, $R_{L_{\mathrm{eff}}}$. After applying the V_{DD} compensation, the maximum output power of the PA will be constant for every load within a voltage standing wave ratio (VSWR) circle centered on the efficiency load and equal to the maximum power delivered by the PA at the efficiency load, $P_{\mathrm{out_{eff}}}$.

Going back to PA fundamentals, this analysis starts by considering a simplified circuit for the output of the amplifier, as shown in Fig. 1(a). The transistor current source is approximated by a piecewise linear model with a constant R_{ON}, as shown in Fig. 1(b).

The first step is to calculate the output power of the PA. It is calculated for a fundamental current component, I_1, and load, Z_L, as

$$P_o = \frac{1}{2}\mathrm{real}(Z_L)|I_1|^2. \tag{1}$$

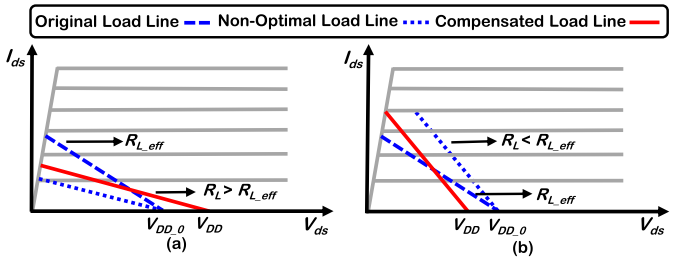

Fig. 2. Correction of the variations toward (a) higher real part loads and (b) lower real part loads.

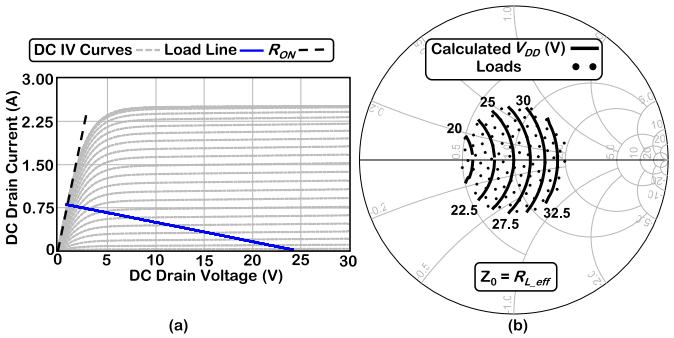

Fig. 3. (a) DC I/V characteristic of the used device, maximum efficiency load line, and calculated R_{ON}. (b) Calculated V_{DD} values for the used Wolfspeed device at the intrinsic current source plane. Please note that the design V_{DD}, V_{DD0}, is 25 V; therefore, it is the optimal V_{DD} for the designed load, $R_{L_{\mathrm{eff}}}$.

The fundamental component of the drain current is given by $(I_P/2)$ for a half-sine wave assuming a peak current equal to I_P. For loads higher than the maximum power load, I_P is defined by the load and the maximum voltage excursion imposed by the triode region, as described in

$$I_P(Z_L, V_{\mathrm{DD}}) = 2\frac{V_{\mathrm{DD}} - V_K}{|Z_L|} \tag{2}$$

where V_{DD} is the supply voltage and V_K is the I/V curve's knee voltage. This expression can be further developed by including the widely used constant R_{ON} approximation model [19]. The peak current is then given by

$$I_P(Z_L, V_{\mathrm{DD}}) = \frac{2V_{\mathrm{DD}}}{|Z_L| + 2R_{\mathrm{ON}}} \tag{3}$$

and the corresponding maximum output power by

$$P_{\mathrm{out}}(Z_L, V_{\mathrm{DD}}) = \frac{1}{2}\frac{\mathrm{real}(Z_L)}{(|Z_L| + 2R_{\mathrm{ON}})^2}{V_{\mathrm{DD}}}^2. \tag{4}$$

Then, the maximum delivered power for the efficiency load, which is real and equal to $R_{L_{\mathrm{eff}}}$, is given by

$$P_{\mathrm{out_{eff}}} = \frac{1}{2}\frac{R_{L_{\mathrm{eff}}}}{(R_{L_{\mathrm{eff}}} + 2R_{\mathrm{ON}})^2}{V_{\mathrm{DD_0}}}^2 \tag{5}$$

for the designed supply voltage equal to $V_{\mathrm{DD_0}}$.

Finally, since the goal is to keep the maximum output power constant and equal to its value for the designed load, it is necessary to solve

$$P_{\mathrm{out}}(Z_L, V_{\mathrm{DD}}) = P_{\mathrm{out_{eff}}} \tag{6}$$

for V_{DD}, which results in the following expression:

$$V_{\mathrm{DD}}(Z_L) = \sqrt{\frac{R_{L_{\mathrm{eff}}}}{\mathrm{real}(Z_L)}}\,\frac{V_{\mathrm{DD_0}}(|Z_L| + 2R_{\mathrm{ON}})}{(R_{L_{\mathrm{eff}}} + 2R_{\mathrm{ON}})} \tag{7}$$

that gives a load-dependent V_{DD} that maintains the maximum output power at the required constant value, $P_{\mathrm{out_{eff}}}$.

Now, for better understanding, consider that the amplifier may suffer a variation of the real part of the load ($R_L = \mathrm{real}(Z_L)$) so that it now sees either a higher R_L or a lower R_L compared with the one considered in the design stage ($R_{L_{\mathrm{eff}}}$). Then, for higher loads, the fundamental current will be lower, as shown in Fig. 2(a). Thus, in this situation, V_{DD} given by (7) will be higher in order to restore the power capability of the PA (raising the voltage excursion). For lower loads, the maximum current swing becomes higher, increasing the maximum output power. However, the efficiency for the designed power is reduced (since the PA operates in back-off), as shown by the nonoptimal load line of Fig. 2(b). Thus, in this case, V_{DD} calculated using (7) will be lower in order to increase the efficiency, by keeping the maximum output power limited to its design value of $P_{\mathrm{out_{eff}}}$. In this analysis, it is assumed that the input power level is increased for operation under lower loads and decreased for operation under higher loads. This will maintain the device on the onset of saturation. Furthermore, this technique can only be used up to the point where the device clips in current for lower loads or enters into breakdown for higher loads.

After this qualitative explanation, using a simplified example for real load variations, expression (7) will be solved for various loads (including complex values) and using the design parameters of a real transistor. In this work, a class B design was used, and the chosen class B definition assumes a V_{GS} bias that corresponds to the I_{ds} third-order derivative null (for $V_{\mathrm{DD}} = V_{\mathrm{DD0}}$) with respect to V_{gs}. Thus, the maximum efficiency load, $R_{L_{\mathrm{eff}}}$, can be determined by the expression deduced in [19] that depends on the quiescent current, I_{dq}. R_{ON} can be approximated using the simulated I/V characteristics of the device, as shown in Fig. 3(a), for the device adopted in this work (Wolfspeed CGH40010F). These estimations using the I/V curves are correspondent to the intrinsic impedances at the current source plane but are useful to understand the behavior of the V_{DD} model. For this device, the estimated efficiency load, at the intrinsic plane, is 30 Ω, and the R_{ON} is 1.1 Ω. Since the V_{DD} model (7) is mostly insensitive to R_{ON}, a dc estimate is enough to compute it. As shown in Fig. 3(b), V_{DD} was calculated for loads within a 2.1 VSWR circle, which is a good estimate of the variation in active phased arrays [20].

III. PA Design and Simulation

In order to test the developed theory, a class B PA was designed. The PA operates at 3.55 GHz and is based on the Wolfspeed GaN device used in Section II. The OMN was designed to convert 50 Ω to the maximum efficiency load and to present short circuit harmonic terminations at the current source plane, ensuring class B operation at the design frequency.

The simulated output power and drain efficiency of the PA at the 1-dB gain compression point are shown in Fig. 4(a), in blue and red, respectively. The simulations were made for

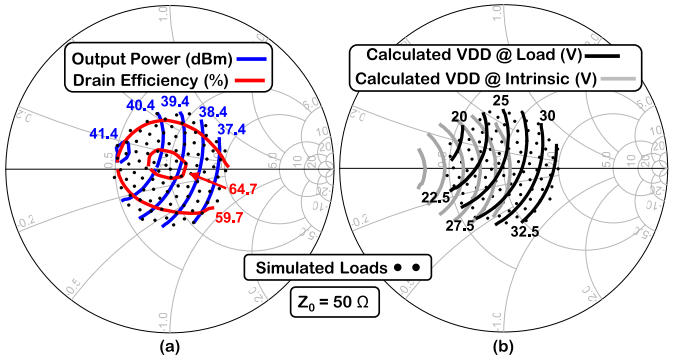

Fig. 4. (a) Simulated load–pull of the designed PA, with drain efficiency in red and output power in blue. The maximum output power is 41.4 dBm, and contours' step is 1 dB. The maximum efficiency is 64.7% with a contours' step of 5%. (b) Calculated V_{DD} at the intrinsic source (gray) and load (black) planes of the designed PA.

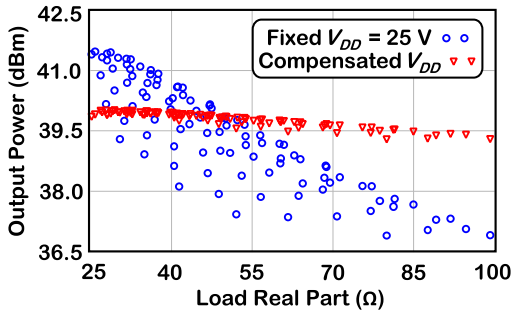

Fig. 5. Simulated output power of the designed PA for a fixed 25 V and the calculated supply voltages at the 1-dB compression point.

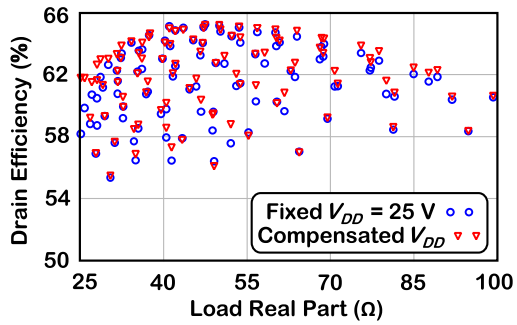

Fig. 6. Simulated drain efficiency of the designed PA for a fixed 25 V and the calculated supply voltages at the 1-dB compression point.

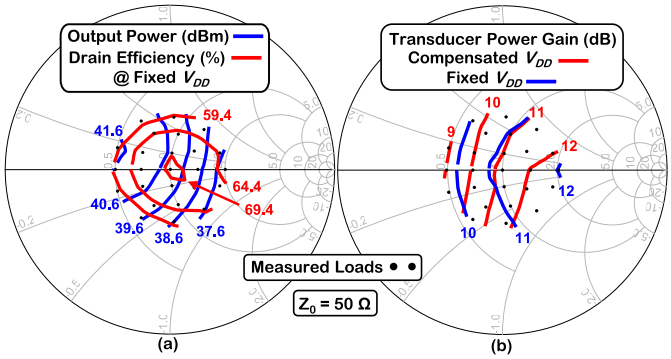

Fig. 7. (a) Measured load–pull of the fabricated amplifier for a fixed V_{DD} of 25 V. The maximum output power is 41.6 dBm, and the contours are shown with a step of 1 dB. The maximum efficiency is 69.4%, and the contours' step is 5%. (b) Measured transducer gain of the fabricated amplifier for a fixed V_{DD} of 25 V and the compensated V_{DD} values.

100 different loads, distributed inside a 2.1 VSWR circle, which corresponds to the typical magnitude variation expected in antenna arrays [21]. The input power was adjusted to maintain the compression level at 1 dB for all the tested loads.

Now, in order to test the designed PA with the predicted optimal V_{DD} values, these values [as plotted in Fig. 3(b)] need to be transformed from the current source plane of the used device to the load plane of the designed PA. To perform this reference plane shift, the used S-parameters correspond to the network between the device current source plane and PA load reference plane, which includes the intrinsic and extrinsic elements of the device, as well as the designed OMN. These S-parameters were extracted by optimization to match the load plane output power contours with the current source plane ones, which are aligned with the real axis. The V_{DD} values plotted at the load plane of the PA are shown in Fig. 4(b).

The simulated output power for each tested load is presented in Fig. 5, for the 1-dB gain compression point. The output power variation without V_{DD} compensation is 4.6 dB with a minimum value of 36.9 dBm. Using the calculated optimal V_{DD} values, the variation is reduced to 0.7 dB, and the minimum value is increased to 39.3 dBm, which corresponds to an increase of 2.4 dB of the output power capability of the PA for the worst case load.

The simulated drain efficiency of the amplifier is shown in Fig. 6. The variation, maximum, and minimum values are identical before and after compensation. The drain efficiency varies from 65.5% down to 56.0%, and on average, for the tested loads, it is 61.9%.

IV. Static Experimental Validation of the Load-Dependent V_{DD}

Before performing a full dynamic validation, it is necessary to verify if the developed load-dependent V_{DD} theory can indeed be used to correct the output power capability of the fabricated PA. The fabricated PA can be seen in [16] or in Fig. 11. Although, for validation purposes, the V_{DD} bias could be manually changed according to the measured load, a dc–dc buck converter, based on the EPC 9067 GaN demo board, has already been incorporated in the implemented class-B amplifier so that it can be used later on during the dynamic measurements that will be presented in Section V. The dc–dc converter is designed using two EPC8009 devices, in switched operation, with a switching frequency of 1 MHz, and the V_{DD} is varied using a pulsewidth modulation (PWM) signal. For this validation, V_{DD} is manually varied by setting the duty cycle that controls the buck converter according to the output load, which is measured using a vector network analyzer (VNA).

First, the amplifier was measured without the buck converter, for a 25-V fixed drain voltage and for 25 test loads synthesized in the laboratory using a manual load tuner. The obtained load–pull contours, measured at the 1-dB gain compression point, are presented in Fig. 7(a); for completion, the transducer gain is shown in Fig. 7(b) by the blue contours.

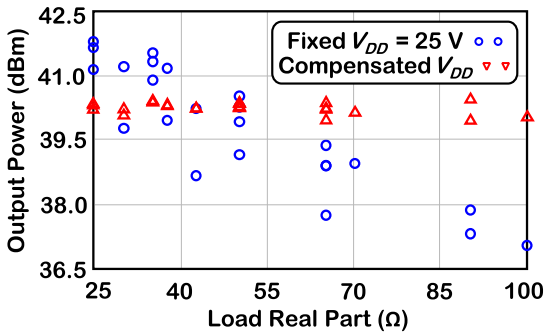

Fig. 8. Measured output power of the implemented PA for the fixed and optimal supply voltages at the 1-dB compression point.

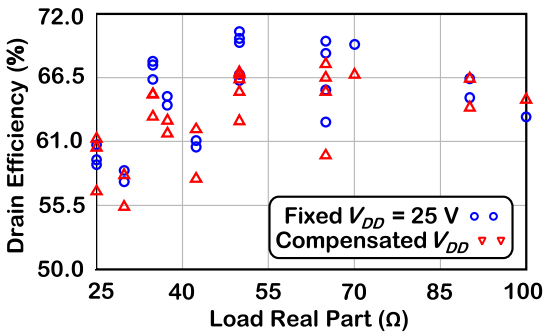

Fig. 9. Measured drain efficiency of the implemented PA for the fixed and optimal supply voltages at the 1-dB compression point.

The output power contours were compared with the simulated ones in order to verify their alignment. This comparison revealed a small phase rotation between the measured and simulated data. This small error can be corrected with an offset in the simulation reference plane and was corrected using a small (ideal) 50-Ω offset line at the load plane of the PA. Thus, in order to obtain the V_{DD} values for the laboratory measurements, this line was considered, and V_{DD} was recalculated for this corrected load reference plane.

The PA was then measured using the recalculated V_{DD} values. Now, the variation of the transducer gain using the compensation V_{DD} values is almost 4 dB, as shown by the red contours in Fig. 7(b), which is 2 dB higher than without V_{DD} compensation. This variation is taken into account in Sections V and VI to equalize the system small-signal gain, for both the fixed V_{DD} and compensated V_{DD} cases.

The output power is shown in Fig. 8 for the 1-dB gain compression point. The uncompensated PA shows a maximum output power variation of 4.7 dB and a minimum value of 37.0 dBm. Using the optimal V_{DD}, the obtained results show a variation of 0.5 dB and a minimum value of 39.9 dBm, which corresponds to a reduction of 4.2 dB in the variation and a worst case output power capability improvement of 2.9 dB. The average output power improvement over the range of tested impedances is 0.4 dB. This value increases to 0.7 dB if the uncompensated PA is operated at back-off for the lower loads to keep its output power at the nominal value of 40 dBm.

The drain efficiency, measured at the same gain compression point, is shown in Fig. 9. Without V_{DD} compensation, the efficiency varies between 56.6% and 69.5%, a variation of 12.9%, and on average, for the tested loads, it is 64.7%. With V_{DD} compensation, the efficiency is, on average, 1.7% lower for the same amount of variation. Note that the average efficiency over the tested range of loads would be lower for the uncompensated PA if it would be operated at back-off for lower loads to keep its output power at the nominal value of 40 dBm. Moreover, the efficiency includes the power dissipated in the buck converter only for the case of the variable V_{DD}. The presented measurements are static, i.e., the supply voltage was manually adjusted, and the load was measured with a VNA.

The measured output power and efficiency validate the developed theoretical load-dependent V_{DD} model, showing a compensation of the PA output power, though slightly reducing its average efficiency. This reduction is attributed to the losses in the buck converter, which increases with the switching frequency and with the V_{DD} (duty-cycle) reduction. The 1-MHz switching frequency was chosen to permit varying the V_{DD} fast enough to compensate load variations due to moving objects or beamforming on MIMO antenna arrays, even for extreme cases such as high-speed trains (HSTs) [22]; 1 MHz allows a variation of the PA supply at a rate below 1 ms, but, later, it is shown that the limiting factor for the compensation speed is not due to the switching frequency but due to the computation time necessary to calculate the load during the impedance measurement.

V. Automatic V_{DD} Control Integrated With an Impedance Meter

In Section IV, we have validated the correction of the output power capability variation with the load using the theoretical load-dependent V_{DD} model. However, to use this method as a fully operational system, it is necessary to integrate the V_{DD} control with impedance tracking so that V_{DD} can be automatically adjusted according to the load. This section is devoted to presenting this automatic V_{DD} controlled PA prototype, as well as its behavior under CW excitation. The measurement setup used to validate the integration of the fully automatic V_{DD} correction, as shown in Fig. 10, is composed of the system under test (SUT), a vector signal generator (VSG), one driver to feed the prototype, a load tuner to permit varying the loading conditions of the SUT, and a power 50-Ω load. The impedance measurements were acquired by a 16-GHz oscilloscope that was connected to the mainline through a bidirectional coupler. A 500-MHz oscilloscope is also used to measure the dc voltage that is actually applied to the PA. A one-port short-open-load (SOL) calibration was performed to correctly track the impedance using the oscilloscope, and an additional power calibration was also performed using a power meter, allowing power measurements directly from the oscilloscope measured waves.

The built prototype is shown in Fig. 11. It is composed of the previously presented class B PA with the dc–dc converter and by an accurate and low loss impedance meter system. The impedance measurement method is based on the slotted line theory and the synthesis of a standing wave replica by adding

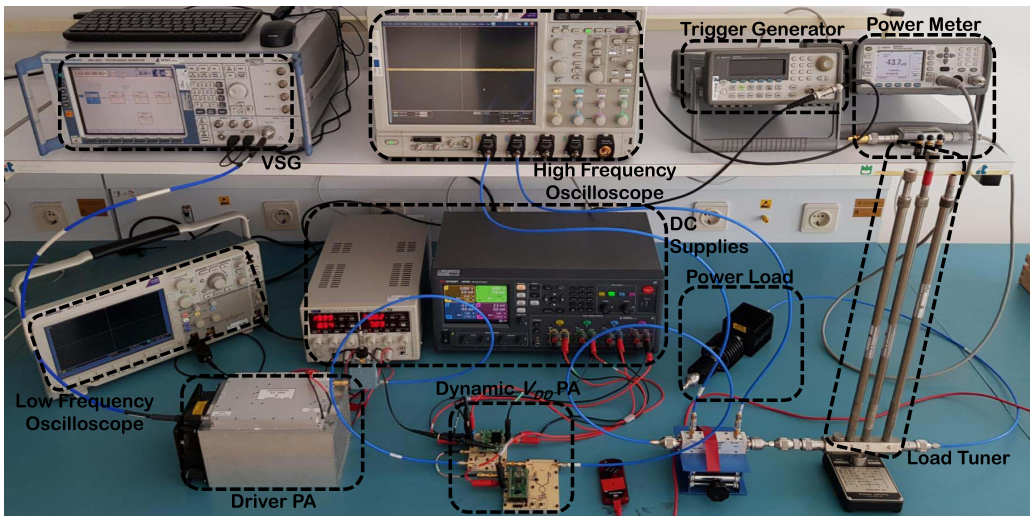

Fig. 10. Photography of the measurement setup. On the right half of the image, notice the manual stub-based load tuner that was used to vary the loading conditions of the SUT. Due to the limitations of manually varying the load conditions of the SUT, the load varies at slightly different time rates in multiple tests, as shown in Figs. 12 and 14.

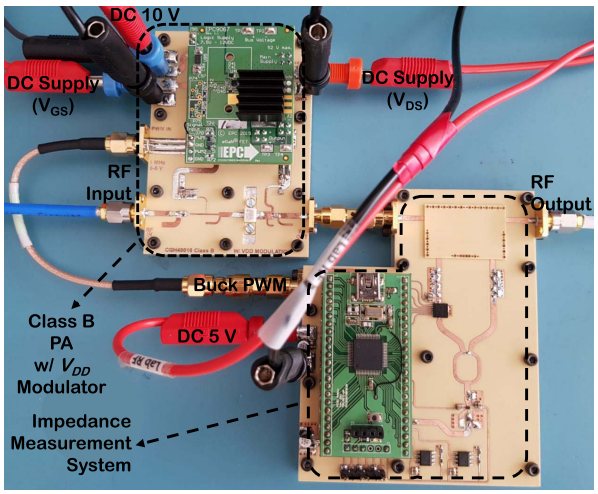

Fig. 11. Photography of the Class B PA with the impedance meter, resulting in the final system prototype.

the reflected wave with phase delayed versions of the incident wave (using a phase shifter). The time required to complete one measurement is around 12 ms, of which 11 ms is the time required for the computation of the measurement algorithm, and could be reduced by increasing the computational power or improving the algorithm. The used microcontroller runs the calibration and the measurement algorithm and is also responsible for generating a PWM signal to control V_{DD} by changing the duty cycle of the buck converter. Due to the limitations of the used PIC 32 internal PWM generator, the switching frequency of the buck converter was reduced to 500 kHz. Nevertheless, the time required to change V_{DD} is still limited by the impedance measurement time (≈12 ms). By adding this system to the PA, a reduction of its maximum drain efficiency of around 4.2%, on average for all the loads inside a 2.1 VSWR circle, is expected. The causes of this efficiency degradation were attributed to different elements of the built system and are described in Table I.

TABLE I
CAUSES OF EFFICIENCY DEGRADATION ON THE BUILT SYSTEM

Buck Converter (applying optimal VDD)	Impedance Meter (insertion loss)	Impedance Meter (consumed dc power)
1.7 %	1.3 %	1.2 % (380 mW)

Contrary to Section IV, where the amplifier characterization was presented for the 1-dB compression point, here, the input excitation amplitude was computed to compensate for the small-signal gain variations with the change of the output impedance, Z_L. Thus, assuming linearity, this would lead to constant output power, as intended. Consequently, it is necessary to perform a small-signal analysis to create a model for $P_{\mathrm{in}}(Z_L, V_{\mathrm{DD}})$. However, for the case where no V_{DD} compensation is applied to the PA, it will operate in deep saturation due to its reduced output power capability.

In this test, the load is slowly varied within a 13.5-s window, and the synthesized variation is shown in Fig. 12 along with the variation on the intrinsic current source plane. Note that the load impedance starts at lower real part loads and varies toward higher real part loads. Fig. 13 shows the PA metrics for this load variation with the automatic V_{DD} control to maintain the RF output power capability, as well as the results for a fixed V_{DD}. The optimal V_{DD} for compensation is plotted along with the measured compensation V_{DD}, and it can be seen that the circuit correctly tracks the optimal values. As a result, the output power degradation is compensated for the higher loads (by 1.7 dB) and the efficiency, which already includes the power dissipated in the sensing circuit and buck converter, slightly improved for lower loads (by 5%).

Note that, in Fig. 13, the efficiency reduction is higher than expected by analyzing Table I, reaching 11% for some loads. This happens for loads where the efficiency degradation caused by the dc–dc converter (applying the optimal V_{DD}) is higher than its average of 1.7%. It is also aggravated by the

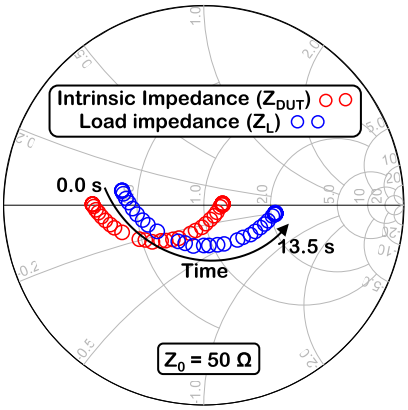

Fig. 12. Synthesized load trajectory for CW measurements (blue) and correspondent intrinsic current source plane impedance (red).

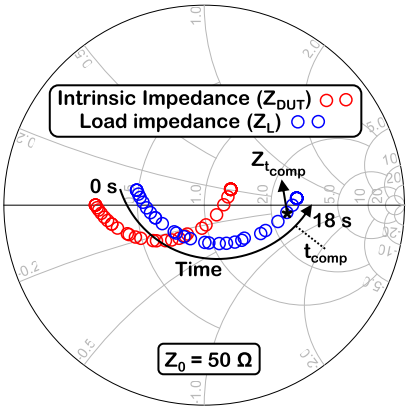

Fig. 14. Synthesized load trajectory for modulated signal measurements (blue) and correspondent intrinsic current source plane impedance (red).

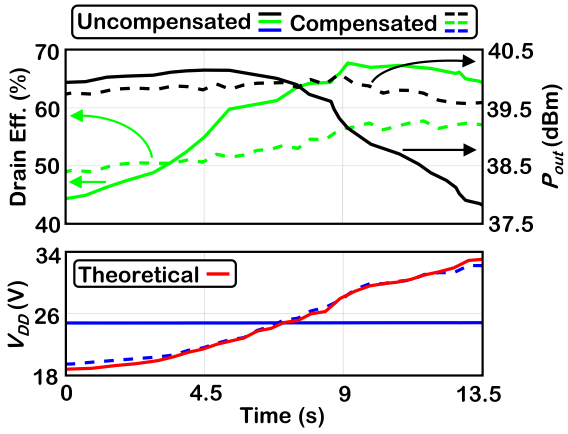

Fig. 13. Compensated and uncompensated output power and efficiency of the PA, along with the fixed and compensation V_{DD}'s that were used in the uncompensated and compensated cases, respectively. In addition, the theoretical optimal V_{DD} calculated from the measured load is plotted in red.

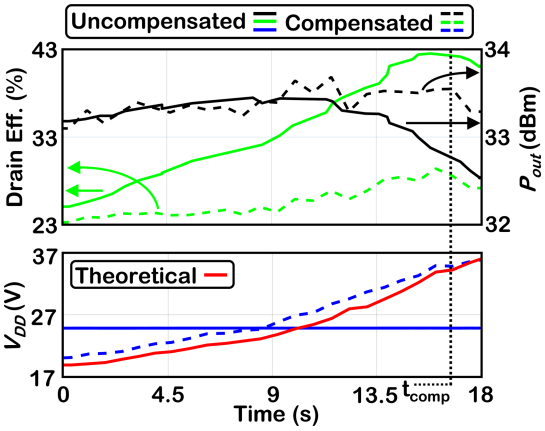

Fig. 15. Compensated and uncompensated average output power and average efficiency of the PA operating with modulated signal excitation, along with the fixed and variable V_{DD} used in the uncompensated and compensated cases, respectively. In addition, the theoretical V_{DD}, calculated from the measured load, is plotted in red.

higher gain compression of the PA when the V_{DD} is fixed at 25 V. This higher compression happens due to: 1) V_{DD} being lower and 2) the used input power being computed from the small-signal gain to try to achieve a constant output power, as previously explained. Up to around 7 s, there is also an error of a few tenths of dB on the targeted output power, causing the compression level to be slightly higher for the uncompensated case, which can also substantially increase the measured drain efficiency.

VI. Load Insensitiveness Under Modulated Signal Excitation

In PAs operating with telecommunication signals, the amplitude of the incident and reflected waves is time-dependent, due to the amplitude modulation. Therefore, other challenges arise, namely, on the impedance measurement under modulated signals. This section is dedicated to test the impedance measurement system under modulated signal and presenting the advantages of using the V_{DD} compensation for these telecommunication signals. For these tests, an OFDM signal with 20-MHz bandwidth and approximately 9.4-dB peak-to-average power ratio (PAPR) was used. Fig. 14 shows the synthesized load variation for the modulated signal test, simulating the movement of users or any obstacle near the antenna. Please note that the load impedance will vary in a much slower time scale than the envelope rate, and so a low-pass filter was added on the envelope detector used in the impedance meter. The impedance variation with time goes from lower to higher real part loads and one specific load, $Z_{t_{comp}}$, is marked at t_{comp}. This is the load for which the RF envelope of the modulated signal will be analyzed and compared with the envelope for operation under the nominal load, Z_{ref}.

Fig. 15 shows the automatic V_{DD} control performance under modulated signal excitation, presenting the measured average output power and efficiency versus time when the load is varying. The error in tracking the optimal V_{DD} is higher when compared with the CW case. This is caused by an increased imprecision on the load measured by the impedance meter. The actual V_{DD} is higher, which will slightly reduce the average drain efficiency. Nevertheless, the reduction should be small as the maximum error in voltage is 2.4 V. The sources of drain efficiency reduction between the uncompensated and compensated cases are the same that have been identified

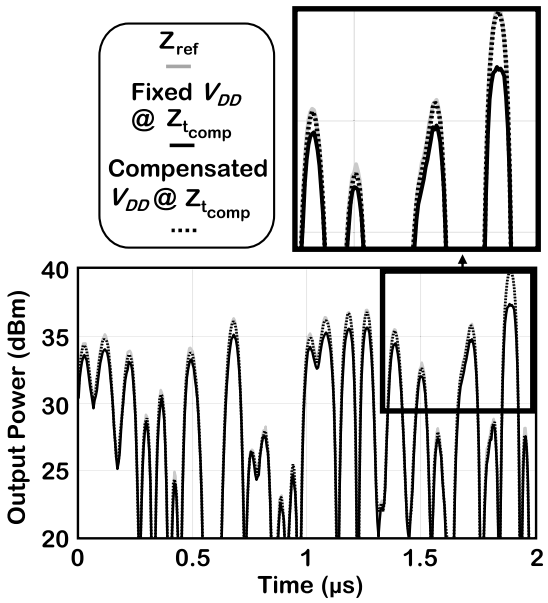

Fig. 16. Output power envelope for a section of the used signal for two load conditions: Z_{ref} (gray) and $Z_{t_{comp}}$ (black). For $Z_{t_{comp}}$, which produces a high output power degradation, a comparison of the output signal envelopes with and without V_{DD} compensation, in dashed and solid black lines, respectively, is shown.

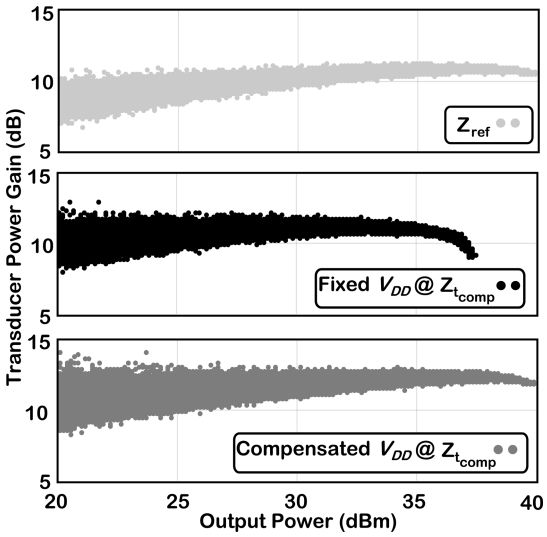

Fig. 17. Dynamic transducer gain of the amplifier for two load conditions: Z_{ref} (light gray) and for $Z_{t_{comp}}$, which shows a high output power degradation. For $Z_{t_{comp}}$, the black plot corresponds to the case where no V_{DD} compensation is applied, and the darker gray plots the case with V_{DD} compensation.

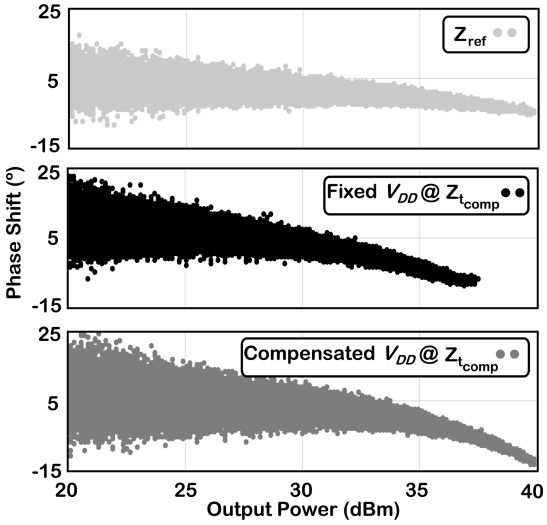

Fig. 18. Dynamic phase shift of the amplifier for two load conditions: Z_{ref} (light gray) and for a $Z_{t_{comp}}$, which shows a high output power degradation. For $Z_{t_{comp}}$, the black plot corresponds to the case where no V_{DD} compensation is applied, and the darker gray plots the case with V_{DD} compensation.

in Section V. However, the efficiency degradation is slightly higher because the PA is less compressed due to the higher actual compensation V_{DD}. In addition, in the time region where the uncompensated PA compresses, a larger efficiency drop is observed. However, in this time region, the efficiency of the uncompensated case is higher than it should be, due to the PEP compression of the signal envelope and consequent PAPR reduction, which causes an increase in the average output power and average efficiency. The average output power is also presented in Fig. 15 for a fixed V_{DD} of 25 V and the compensated V_{DD}. Now, due to the high PAPR of the used signal, only the peak power of the signal is degraded. This causes a degradation of the average output power of only 0.7 dB that was compensated to 0.1 dB. Fig. 16 presents the instantaneous output power envelope captured with the oscilloscope (which was previously calibrated) for two different impedance load conditions: 1) Z_{ref}, which is the reference and no compensation is needed and 2) $Z_{t_{comp}}$, with output power degradation (which is the load marked at t_{comp} in Figs. 14 and 15) and so requiring V_{DD} compensation. By analyzing Fig. 16 for a fixed V_{DD}, a reduction of almost 3 dB on the peak power and a distorted envelope are noticeable. However, for the compensated V_{DD}, the peak power is restored, and the envelope shape is almost entirely corrected.

Figs. 17 and 18 show the amplifier's dynamic transducer gain and phase shift under the same modulated signal excitation (for the same three cases considered before). In Fig. 17, it is shown that applying V_{DD} compensation slightly increases the small-signal gain, as shown in Section IV. Also, the peak power of the signal is restored, and the abrupt gain compression is eliminated. However, the output signal phase shift is slightly increased, as shown in Fig. 18.

In order to further check the amplifier's linearity when V_{DD} is compensated through the presented system, the signal spectra (once again for the three cases considered before) are shown in Fig. 19. The adjacent channel power ratio (ACPR) was calculated for all cases and presented in Table II. These results show that the system's linearity under V_{DD} compensation is not degraded. In fact, the ACPR is slightly lower than it is under the same load variation but without V_{DD} compensation. Although the distortion power is not reduced with the V_{DD} compensation, this reduction of ACPR is justified by an increase of the channel power.

VII. System Time Performance

In the previous sections, the built prototype was validated as an automatic V_{DD} controlled PA under CW and modulated

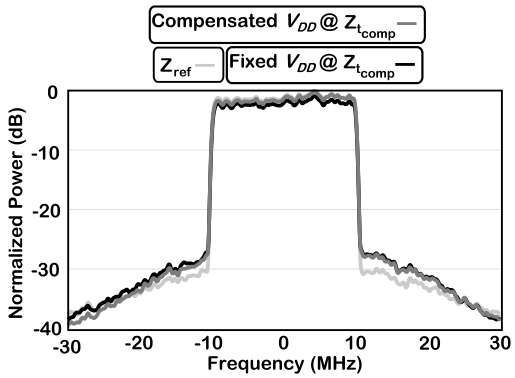

Fig. 19. Spectra of the output signal of the amplifier for three different cases: Z_{ref} (light gray) and $Z_{t_{comp}}$ (black), where there is high output power degradation without V_{DD} compensation. The same load, $Z_{t_{comp}}$, with V_{DD} compensation, in darker gray.

TABLE II

CHANNEL POWER, DISTORTION POWER, AND ACPR FOR THE THREE DIFFERENT CASES

	Reference Load	High Load Fixed VDD	High Load Comp. VDD
Norm. Channel Power (dB)	0.0	-1.0	-0.2
High Band Power (dB)	-31.7	-29.6	-29.8
Low Band Power (dB)	-32.0	-30.3	-31.0
ACPR Low (dB)	**-31.7**	**-28.7**	**-29.6**
ACPR High (dB)	**-32.0**	**-29.4**	**-30.8**

signal excitations. However, the synthesized loads for validation were slowly varying (13- and 18-s time frames with around 15 V of V_{DD} variation). In this section, the prototype is tested for faster load variations, which mimics load variations that would occur in real applications, in order to analyze its time constraints. Fig. 20 presents a comparison between the developed theoretical V_{DD} model, which was calculated from the measured load, and the actually measured V_{DD} for different-shaped pulses that correspond to the synthesized load variations. In Fig. 20(a), a sequence of different pulses with different shapes and time characteristics is presented. The prototype is able to correctly track the optimal V_{DD} for the presented transitions, which validates the capability of the proposed system to compensate for V_{DD} under different variable loading profiles. In order to check the response of the system to fast load variations, Fig. 20(b) and (c) presents a fast optimal V_{DD} step-up and step-down profiles, respectively. The maximum delay between the optimal and measured V_{DD} is expected to be, roughly, the time necessary to measure the load and change the V_{DD} twice and occurs when the waveform acquisition for the load computation happens right before the steady state of the optimal V_{DD} step, as shown in Fig. 21. In this case, V_{DD} will not change to its final value, and a second measurement will be needed, delaying the final V_{DD} value by 2×13 ms. However, although there may be some inaccuracy associated with the time axis of the presented

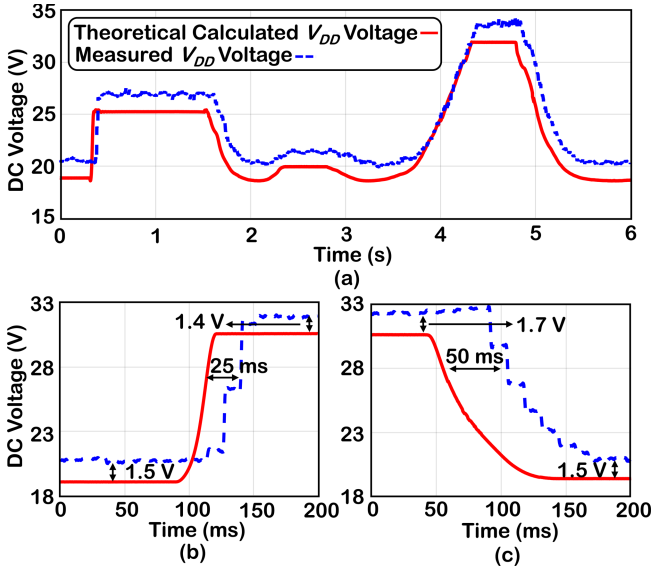

Fig. 20. Comparison between the measured supply voltage used on the compensated PA and calculated optimal supply voltage, for three cases. (a) Variable loading sequence of 6 s. (b) Fast step-up transient. (c) Fast step-down transient.

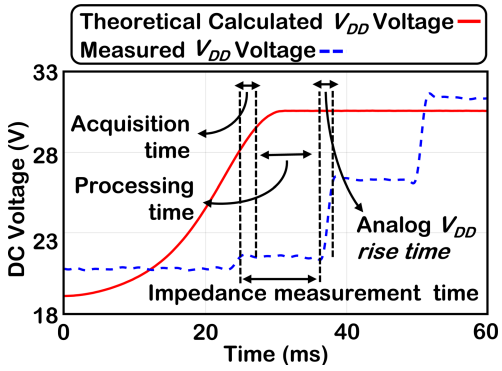

Fig. 21. Analysis of the rise time of V_{DD}, as well as the acquisition and computation times of the impedance measurement under a fast step-up pulse.

measurements, due to different trigger delays and response times of the used measuring instruments, the maximum step-up delay between the optimal and measured V_{DD} is around 25 ms. During the step-down, the delay can achieve higher values, up to 50 ms, but, since the actually applied V_{DD} is higher than the optimal one, this will cause a hardly noticeable reduction on the average drain efficiency of the PA but will have no effect on the output power capability compensation. It is suspected that these higher than expected measured delays are caused by imprecision on the impedance measurement, resulting in an underestimated V_{DD} during the optimal V_{DD} step-up and an overestimation during the step-down. The impedance measurement imprecision is probably caused because the impedance meter is acquiring data to compute the load value, while the load is varying at a similar time rate. However, this phenomenon is not further investigated since it is considered more important to first reduce the computation time, which is the highest temporal limitation, as shown in Fig. 21.

Fig. 21 shows that the time required to change the V_{DD} of the PA, which is roughly 13 ms, is imposed by the time required to measure the output impedance of the PA (≈12 ms). This measurement time can be divided into the acquisition time (≈1 ms), which is the time required to acquire the synthesized stationary wave, and the computation time (≈11 ms), which is the time necessary to compute the algorithm that gives the output load of the PA. Thus, as previously introduced, the computation time is the highest temporal limitation of the built prototype, and since it can be reduced by increasing the computational power or improving the control algorithm, the time performance of the dynamic V_{DD} control can be greatly improved.

VIII. Conclusion

This work presented an automatic system that is able to restore the output power capability of a PA, by dynamically changing its V_{DD}, under variable loading scenarios. The calculated V_{DD} values have been validated in simulation and laboratory measurements for a 3.55-GHz GaN class B PA. The presented prototype is able to track down the output load of the PA and dynamically change its supply voltage accordingly. For that, a high-efficiency GaN dc–dc converter was used and controlled by a low loss impedance meter. The presented system is able to correctly track down the load and apply the calculated V_{DD} to the PA, for CW and modulated signals. For a fixed gain compression of 1 dB, the output power was compensated by 4.2 dB, and the power capability of the PA was improved by 2.9 dB, for the worst case loads. Under the modulated signal excitation, the proposed system is able to restore the peak power of the output signal, which was degraded by almost 3 dB for the worst case loads using a fixed V_{DD}, and the ACPR is maintained. The cost is the added complexity and a reduction in the drain efficiency due to the losses added by the dc–dc converter (1.7%) and the impedance meter (2.5%). The compensation was effective for all the loads within a 2.1 VSWR circle. The time limitation of this system is the required time for the microcontroller to compute the load and generate the PWM signal, causing delays up to 25 ms on the V_{DD} step-up. Nevertheless, this is believed to be enough for the time rate required by most of the proposed applications and can also be improved by increasing the computational power of the system or the control algorithm.

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