A Circuit-Inspired Digital Predistortion of Supply Network Effects for Capacitive RF-DACs

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***Abstract*— This article presents a novel digital predistortion (DPD) approach to compensate for nonlinear dynamic distortions caused by the supply network of capacitive radio frequency digital-to-analog converters (RF-DACs). The developed DPD concept recreates the voltage distortion on the RF-DAC's supply network and modulates the input signal such that the effects on the output signal of the RF-DAC are canceled. In contrast to conventional DPD approaches such as pruned Volterra series or memory polynomials, the complexity of the proposed concept is reduced to a feasible level, allowing for implementation in integrated circuits. Furthermore, the derived DPD model allows to use linear estimation algorithms for coefficient training. The presented DPD is demonstrated by measurements of two different capacitive RF-DAC designs and compared with conventional DPD approaches. EVM and adjacent channel power ratio (ACPR) can be improved by up to 6 and 7 dB, respectively, outperforming conventional approaches.**

***Index Terms*— Digital predistortion (DPD), memory effects, memory polynomial (MP), power amplifier (PA), radio frequency digital-to-analog converter (RF-DAC), switched-capacitor power amplifier (SCPA), Volterra series.**

I. Introduction

THE demand for high data rates, robust transmissions, and power efficiency poses stringent requirements on the design of integrated wireless transceiver systems. Increasing the data rate, while simultaneously providing a reliable and power-efficient transmission, is closely related to the linearity of the communication systems.

In radio frequency (RF) wireless communication transmitters, the key component in terms of linearity and power efficiency is the radio frequency power amplifier (RF-PA) [1]. Circuit implementations tend to nonlinear characteristics when operated in a power-efficient manner. Moreover, high signal bandwidths exceeding 20 MHz emphasize frequency-dependent nonlinear effects, i.e., the so-called memory effects [2], [3].

A way to overcome this limitation is to use digital predistortion (DPD), where the input signal of the PA is modulated by a nonlinear operator such that the overall system's behavior is linear [4]–[6]. The performance achieved by DPD systems heavily depends on the underlying mathematical model of the predistorter. Sophisticated memory-based DPD approaches, such as the Volterra series [7], [8], achieve excellent performance but require large coefficient sets. The so-called pruned Volterra models, such as the memory polynomial (MP) [9], [10] or the generalized MP (GMP) [11], reduce the complexity of the Volterra series by sacrificing some performance and allow the implementation on integrated circuits.

Another approach to increase the system's power efficiency is to utilize the advantages of integrated circuitry based on digital building blocks [12]. One promising concept is the radio frequency digital-to-analog converter (RF-DAC), which shifts the circuit complexity for wireless transmitters further to the digital domain, reducing the number of required active and passive components [13], [14]. RF-DACs combine the functionality of a DAC and an upconversion mixer in a single circuit, allowing an efficient implementation on a monolithic die and leveraging the benefits of scaled CMOS technology with increased usage of fast and programmable digital blocks. RF-DACs have gained an increasing amount of interest in the Wireless Communications Society [14]–[18].

One specific architecture of RF-DACs is the so-called capacitive RF-DAC or switched-capacitor PA (SCPA), which was first published in the literature by Yoo *et al*. [18]–[20]. The capacitive RF-DAC combines high linearity over a wide frequency range with high power efficiency [18]. Moreover, dedicated architectures can provide enough signal gain to omit an additional conventional RF-PA [21], [22].

Nevertheless, also RF-DACs suffer from internal and external nonidealities, limiting their linearity. Hence, DPD concepts have also been proposed for RF-DAC-based transmitters [23]–[27]. These published DPD systems use conventional black-box approaches to model and hence mitigate the nonlinear effects. DPD concepts targeting specific nonlinear effects of capacitive RF-DACs have been proposed by

Manuscript received June 15, 2020; revised August 11, 2020; accepted August 17, 2020. Date of publication September 23, 2020; date of current version January 5, 2021. This work was supported in part by the Austrian Federal Ministry for Digital and Economic Affairs and in part by the National Foundation for Research, Technology and Development. *(Corresponding author: Stefan Trampitsch.)*

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Digital Object Identifier 10.1109/TMTT.2020.3022382

Markovic *et al.* [28], [29]. The resulting mathematical models are based on the detailed analysis of the origin and the resulting effects of the nonlinearities of the RF-DAC design, resulting in low complexity, but powerful DPD approaches.

This work follows the methodology of analyzing and modeling dedicated nonideal effects of capacitive RF-DACs. One of the major drawbacks of the capacitive RF-DAC is its low power supply rejection. As a consequence, any distortion or noise affecting the supply is visible at the output, causing undesired spectral regrowth and degraded EVM. The proposed concept introduces a low-complexity memory-based DPD approach. The voltage distortions on the capacitive RF-DAC supply are digitally recreated. This information is used to modulate the input signal such that the effect of supply voltage variations on the output of the RF-DAC is suppressed. The complexity of the proposed DPD is reduced to a feasible level for circuit implementation. Moreover, linear adaptive system identification algorithms can be used for coefficient estimation. The introduced DPD is capable of mitigating static as well as dynamic nonlinear effects and can thus be used for wideband signals exceeding 100 MHz.

The remainder of this article is structured as follows. Section II gives a brief introduction to the capacitive RF-DAC and the origins of its nonidealities. Furthermore, the section introduces the causes and effects of supply voltage distortions of capacitive RF-DACs. In Section III, the novel circuit-inspired DPD method, combating the effects of the supply voltage distortions, is detailed. Measurement results of two capacitive RF-DAC implementations, augmented with the proposed DPD method, are discussed in Section IV. Finally, Section V concludes this article.

II. Capacitive RF-DAC

The capacitive RF-DAC architecture is based on switched-capacitor circuits, using individual switching capacitor cells to form a capacitive voltage divider, as principally shown in Fig. 1. Capacitive RF-DACs can be implemented as polar, quadrature, multiphase, or even as hybrid IQ transmitters [17]–[22], [30]–[32].

The capacitive RF-DAC comprises N cells, each consisting of a capacitor C_i, with $1 \leq i \leq N$, a driving inverter, and an LO gate, as shown in Fig. 1. The digital amplitude information, $(d_1, \ldots, d_N)$, is fed to the LO gates by the digital front end (DFE), determining the number of active switching cells. In this way, upconversion of the digital amplitude with the LO is inherently achieved. Inactive cells are not switching and kept at ground potential. Without loss of generality, all capacitor cells are assumed to be unitary, i.e., $C_1 = C_2 = \cdots = C_N = C_u$.

The output voltage of the unloaded capacitive RF-DAC, decomposed into a Fourier series, and assuming infinitely steep signal transitions, is given by [33]

$$v_o(t) = V_{\mathrm{DD}} \frac{n(t)}{N} \left(\frac{1}{2} + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\sin[(2k-1)\ \omega_{\mathrm{LO}}\, t]}{2k-1} \right) \quad (1)$$

where $(n(t)/N)$ is the ratio of the number of active switching cells to the total number of cells, V_{DD} is the supply voltage,

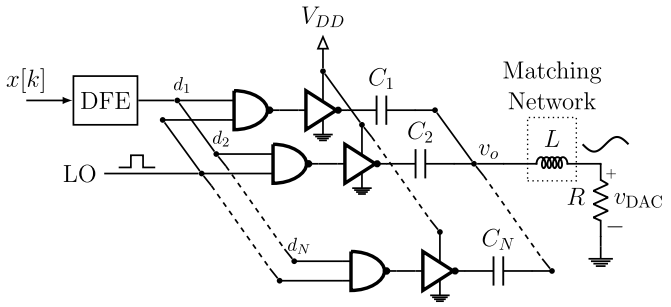


Fig. 1. Simplified block and circuit diagram of a single-ended capacitive RF-DAC.

and $f_{\mathrm{LO}} = \omega_{\mathrm{LO}}/2\pi$ is the (fundamental) LO frequency. To restore the sinusoidal from this square wave, an output matching network comprising an inductive element L, as shown in Fig. 1, is part of the capacitive RF-DAC. The inductor L resonates the RF-DAC's capacitance C_{tot}, filters higher order harmonics, and provides impedance matching. C_{tot} with

$$C_{\mathrm{tot}} = \sum_{i=1}^{N} C_i \quad (2)$$

is the total array capacitance seen from the matching network [18], which is independent of the number of active switching cells $n(t)$. Thus, the circuit operates as a single-ended series bandpass filter with the first harmonic given by

$$v_{\mathrm{DAC}}(t) = \frac{2}{\pi} V_{\mathrm{DD}} \frac{n(t)}{N} \sin(\omega_{\mathrm{LO}}\, t). \quad (3)$$

A. Nonidealities of Capacitive RF-DACs

Due to manufacturing variations, the driving inverters and especially capacitors in the matched cells slightly deviate from their ideal values, causing a nonlinear relation from the input signal to the output amplitude as the weight of active switching cells is no longer linearly related to the input signal, i.e., $(n(t)/N)$ does not perfectly hold anymore in (3) [34]. Quadrature-based capacitive RF-DAC architectures additionally suffer from mismatches between in-phase and quadrature-related cells, causing an undesired IQ image in the output spectrum of the RF-DAC. The detailed analysis and a cancellation technique have been proposed by Markovic *et al*. [29]. Polar architectures, on the other hand, suffer from bandwidth expansion of the required magnitude and phase modulation, degrading the ACPR especially for wideband input signals [35].

Additional internal nonidealities arise from misalignment of the sampling instant between data and the respective LO signals or nonideal sign operation, increasing the noise floor and generating unwanted spurs in the output signal [36]. Similar effects are generated by the misalignment of the switching times caused by different lengths of the LO signal distribution into the individual cells.

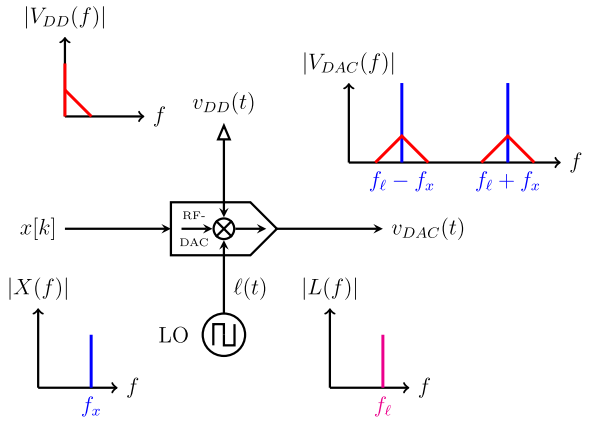


Fig. 2. Effect of supply voltage variation on the output of the capacitive RF-DAC.

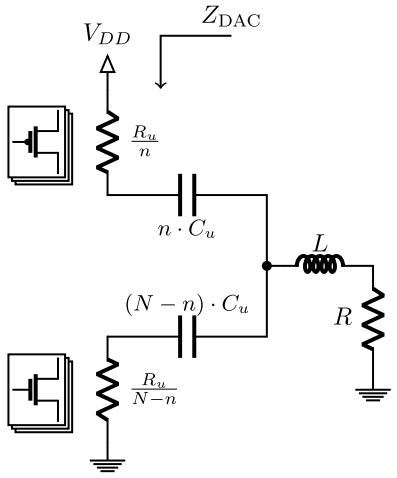


Fig. 3. Simplified schematic model of the capacitive RF-DAC [41].

Another origin of nonlinear effects results from the mismatch of the respective pMOS and nMOS ON-resistances of the driving inverters in each switching cell. Unequal ON-resistances change the charging and discharging time constant of the cell array, resulting in a code-dependent modulation of the output phase, causing AM–PM distortion [18], [33].

External contributors to the nonideal behavior of the capacitive RF-DAC arise from the LO generation and the supply network. Long-term clock jitter and the corresponding phase noise of the LO contribute directly to the output of the RF-DAC, increasing the out-of-band noise floor [34]. Furthermore, polar and multiphase architectures rely on the dynamic (resolution) of a digital phase-locked loop (DPLL) or a digital-to-time converter (DTC) to achieve the required bandwidth of the modulated digital input signal [14], [37]. Furthermore, the so-called remodulation occurs due to the pulling effect caused by the electromagnetic coupling of the RF-DAC and the used digitally controlled oscillators (DSOs) of the DPLL, generating undesired spurs and thus degrading the EVM and ACPR. Detailed analysis and digital cancellation technique were proposed by Markovic *et al.* [28].

Nonlinear effects caused by the supply network of the capacitive RF-DAC, which are the focus of the proposed DPD, are addressed in Section II-B.

For further details on the implementation and digital enhancement of capacitive RF-DACs, the reader is referred to the literature [14], [17]–[19], [21], [38], [39].

B. Effects of Supply Voltage Variations

The supply voltage V_{DD} of the capacitive RF-DAC is also its reference voltage. Hence, noise and distortions of the supply voltage are directly modulated with the input signal and the LO. This causes undesired spectral regrowth and degradation of the in-band performance, as briefly shown in Fig. 2.

Apart from thermal noise, supply voltage variations are typically deterministic, including, but not limited to, switching ripples of dc–dc converters [40]. However, the supply current $i_{\mathrm{DD}}(t)$ drawn by the capacitive RF-DAC is (input) signal dependent, causing an undesired voltage drop $v_d(t)$ over the supply network impedance $Z_{\mathrm{SN}} \neq 0$, i.e., $v_{\mathrm{DD}}(t) = V_{\mathrm{dc}} + v_d(t)$. Inserting the supply voltage variation into the output of the RF-DAC (3) yields

$$v_{\mathrm{DAC}}(t) = \frac{2}{\pi}\left[V_{\mathrm{dc}} + v_d(t)\right]\frac{n(t)}{N}\sin(\omega_{\mathrm{LO}}\, t). \tag{4}$$

The drawn supply current $i_{\mathrm{DD}}(t)$ depends on the number of active switching cells $n(t)$ as the impedance of the RF-DAC Z_{DAC} seen from the supply changes with $n(t)$. To show this, the RF-DAC is simplified to the model shown in Fig. 3 [41]. All active and inactive cells are combined to two equivalent impedances, respectively. Without loss of generality, C_u represents the (assumed) unitary capacitance of every cell and R_u is the equivalent ON-resistance of the drivers' pMOS and nMOS [41]. The active cells are assumed to be connected to V_{DD}. With that, the input impedance of the RF-DAC for a given $n(t) = n$ is given by

$$Z_{\mathrm{DAC}}(s) = \frac{s\,R_u\,C_u + 1}{s\,C_u} \times \left[\frac{1}{n} + \frac{s\,L + R}{\frac{s\,R_u\,C_u+1}{s\,C_u} + (N-n)(s\,L+R)}\right] \tag{5}$$

where the number of active switching cells n is determined by the baseband input signal $x[k]$. The supply current $i_{\mathrm{DD}}(t)$ of the RF-DAC and the resulting voltage drop $v_d(t)$ over the supply network's impedance $Z_{\mathrm{SN}}(s)$ in the Laplace domain are given by

$$I_{\mathrm{DD}}(s) = \frac{1}{Z_{\mathrm{DAC}}(s)}\,V_{\mathrm{dc}} \tag{6a}$$

$$V_d(s) = I_{\mathrm{DD}}(s) \cdot Z_{\mathrm{SN}}(s) \tag{6b}$$

assuming an ideal supply voltage V_{dc} and linear behavior of the supply network. The characteristic of the supply network is, apart from design specific circuitry such as low-dropout regulators (LDOs), dominated by parasitics, rendering its prediction with simulation tools with sufficient accuracy impossible.

The supply current $i_{\mathrm{DD}}(t)$ and, consequently, the voltage drop $v_d(t)$ depend nonlinearly on the number of active switching cells $n(t)$ and thus on the baseband input signal $x[k]$,

resulting in low-frequency variations on $v_{\mathrm{DD}}(t)$. The switching behavior of the capacitive RF-DAC also causes high-frequency distortions on $i_{\mathrm{DD}}(t)$ and $v_d(t)$ [34], respectively. However, these high-frequency variations are suppressed by the (local) decoupling capacitance of the supply network of the RF-DAC. Thus, their contribution on the output signal of the RF-DAC is practically negligible and, in the following, only the low-frequency variations of the supply current and supply voltage are considered. These low-frequency voltage variations are modulated with the RF-DAC's input signal and upconverted by the LO on the RF-DAC's output, as shown in Fig. 2. However, due to the nonlinear dependence of $v_d(t)$ on the input signal $x[k]$, the bandwidth of the distortions on the supply is, in general, larger than the input signal's bandwidth, i.e., $(\max f_x < \max f_{v_d} \ll f_{\mathrm{LO}})$.

As indicated in (5), the supply voltage distortions correspond to the number of active switching cells, where the dependence of $n(t)$ on the baseband input signal $x[k]$ is different for different RF-DAC architectures. In polar architectures, the number of active switching cells $n(t)$ is determined by the magnitude of the input signal. Contrarily, for quadrature capacitive RF-DACs, $n(t)$ depends on the sum of the magnitudes of the in-phase and the quadrature signal. The normalized number of active switching cells for polar and quadrature architectures, respectively, is given by

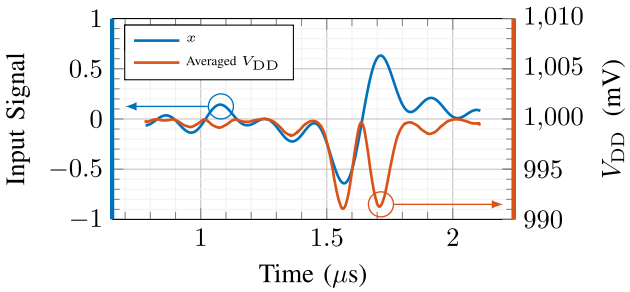
$$x_{\mathrm{on}}[k] = O_n(x[k]) = \begin{cases} |x[k]|, & \text{for polar} \\ |x_I[k]| + |x_Q[k]|, & \text{for quadrature} \end{cases} \tag{7}$$

where $x[k] = x_I[k] + j\,x_Q[k]$ and $x_{\mathrm{on}}[k] \propto n[k]$. Hence, the low-frequency distortions on $v_{\mathrm{DD}}(t)$ depend either on the magnitude of the input signal or on the sum of the magnitudes of the in-phase and the quadrature components of the input signal.

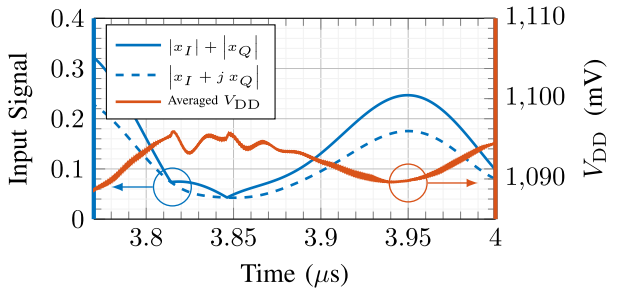
Fig. 4 shows the simulated low-frequency voltage drop of $v_{\mathrm{DD}}(t)$ for a polar and a quadrature architecture, respectively. The voltage drop of the polar architecture, for $V_{\mathrm{dc}} = 1$ V, shown in Fig. 4(a), follows the magnitude of the exemplary chosen real-valued input signal, i.e., $x[k] \in \mathbb{R}$ and, thus, no phase modulation of the LO. In contrast, the voltage drop of the quadrature architecture for $V_{\mathrm{dc}} = 1.1$ V depends on the sum of the magnitudes, as shown in Fig. 4(b). The sudden changes of the supply voltage of the quadrature architecture correspond to the discontinuities of $|x_{\mathrm{I}}| + |x_{\mathrm{Q}}|$. In contrast, at the same time instances, the magnitude $|x_{\mathrm{I}} + j\,x_{\mathrm{Q}}|$ is smooth. Furthermore, these discontinuities excite the resonance behavior of the RLC supply network and cause the ringing on $v_{\mathrm{DD}}(t)$, as shown in Fig. 4(b).

Fig. 5 shows the PSDs of a simulated polar capacitive RF-DAC with ideal and nonideal supply network, respectively, using the switched linear state-space modeling approach presented in [34] and [41], which allows to analyze the impact of a nonideal supply network on an (chosen) idealized model of the RF-DAC.

Typically, LDOs are used to regulate and provide a stable supply voltage for capacitive RF-DACs. LDOs with a gain–bandwidth equal or larger than the input signal



(a)



(b)

Fig. 4. Variation of the supply voltage v_{DD} of (a) polar and (b) quadrature capacitive RF-DAC.

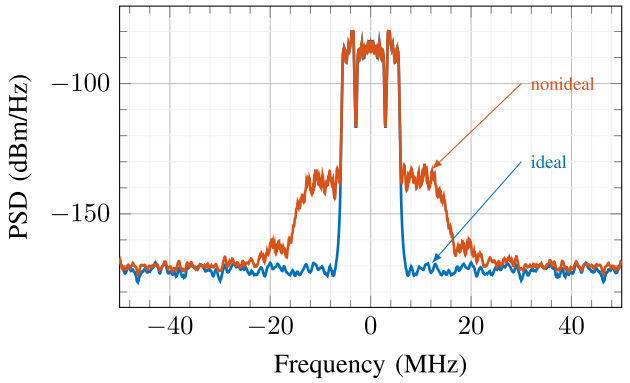


Fig. 5. PSDs of the downconverted RF-DAC output with ideal and nonideal supply network for a multitone input signal with 10-MHz bandwidth, simulated with switched state-space models [34].

bandwidth are needed to provide the necessary low supply impedance. To also keep track of higher intermodulation distortions (third, fifth, and higher orders), which are caused by the nonlinear signal-dependent voltage drop over the supply network (6b), LDOs with even higher gain–bandwidth are required. Specifically designed LDOs are still feasible to meet the required quality of the power supply for the capacitive RF-DAC for, e.g., 4G communications [17]. However, for future wireless standards, the limits of this remedy will soon be reached due to the necessity of further improvements in power efficiency and reduction in off-chip external components. Moreover, at the same time, larger effective transmission bandwidths, 160 MHz and beyond, higher constellation orders, exceeding 1024-QAM, will impose even more stringent quality requirements on the linearity and the dynamics of the capacitive RF-DAC. Thus, another way of suppressing these

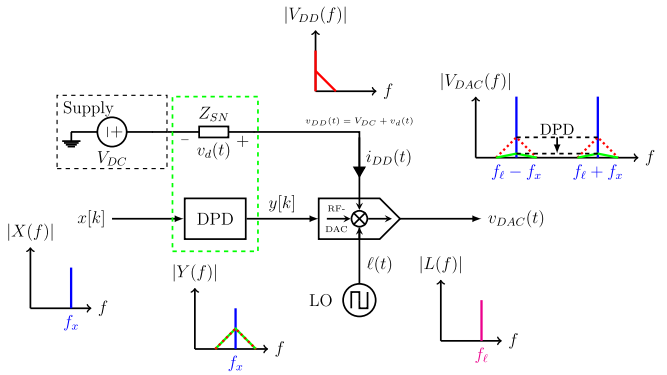


Fig. 6. Overview of the SNDPD approach, which modulates the input signal with an estimated voltage drop such that the effects of a varying supply voltage on the RF-DAC output are suppressed.

effects is required. The proposed DPD approach specifically targets the signal-dependent supply voltage variation of the RF-DAC and offers an efficient way to compensate for these effects by using digital signal processing techniques.

III. Supply Network DPD for Capacitive RF-DACs

The DPD concept focuses on the cancellation of the supply network effects discussed in Section II. Fig. 6 shows the principle block diagram of the proposed DPD, which recreates the signal-dependent voltage drop $v_d(t)$ over Z_{SN} and modulates the input signal such that the resulting effect of the supply voltage variation on the RF-DAC's output signal is suppressed. The presented DPD approach is thus referred to as supply network DPD (SNDPD).

This section solely focuses on the equivalent (discrete-time) baseband signal. Thus, all signals and functions are represented with discrete-time samples, i.e., $x(t) \rightarrow x(k \cdot T_s) = x[k] \in \mathbb{C}$. Furthermore, the capacitive RF-DAC input–output characteristic (4) is reduced to

$$\begin{aligned} v_{\mathrm{DAC}}[k] &= x[k] \cdot v_{\mathrm{DD}}[k] \\ &= x[k] \cdot (V_{\mathrm{dc}} + v_d[k]) \end{aligned} \tag{8}$$

where $x[k]$ is the equivalent complex-valued baseband input signal and $v_d[k]$ represents the baseband (low-frequency) distortions of the supply voltage, as discussed earlier. Only the low-frequency supply variations of $v_{\mathrm{DD}}[k]$ are considered. High-frequency (switching) distortions are, as described earlier, assumed to be negligible and thus are not considered in this work.

A. Motivation

To achieve suppression of the supply voltage distortion, $x[k]$ is modulated by a signal $\alpha[k]$ such that the predistorted RF-DAC input signal $y[k]$ is given by

$$y[k] = x[k] \cdot (1 - \alpha[k]). \tag{9}$$

Inserting (9) into the ideal RF-DAC transfer characteristic (8) yields

$$\begin{aligned} v_{\mathrm{DAC}}[k] &= y[k]\, v_{\mathrm{DD}}[k] \\ &= x[k]\, [V_{\mathrm{dc}} + v_d[k] - \alpha[k]\, V_{\mathrm{dc}} - \alpha[k]\, v_d[k]]. \end{aligned} \tag{10}$$

Hence, an ideal compensation of $v_d[k]$ would be achieved by

$$\alpha[k] = \frac{v_d[k]}{V_{\mathrm{dc}}} \left(\frac{1}{1 + \frac{v_d[k]}{V_{\mathrm{dc}}}} \right). \tag{11}$$

However, the signal-dependent voltage distortions $v_d[k]$ are unknown, and are, as described earlier, dominated by the parasitic supply network components of the RF-DAC. Thus, $\alpha[k]$ is infeasible to be accurately predicted by simulation and is therefore targeted to be estimated. Furthermore, choosing $\alpha[k]$ as in (11) results in a nonlinear parameter estimation problem.

Therefore, assuming that $v_d[k] \ll V_{\mathrm{dc}}$ and thus $(v_d[k]/V_{\mathrm{dc}}) \ll 1$, $\alpha[k]$ can be approximated by

$$\alpha[k] = \frac{v_d[k]}{V_{\mathrm{dc}}}, \tag{12}$$

which leads to the RF-DAC output signal

$$v_{\mathrm{DAC}}[k] = x[k] \cdot \left(V_{\mathrm{dc}} - \frac{v_d[k]}{V_{\mathrm{dc}}} \cdot v_d[k] \right). \tag{13}$$

The term $x[k] \cdot (v_d^2[k]/V_{\mathrm{dc}})$ represents a systematic error introduced by the DPD (9) caused by the proposed approximation of $\alpha[k]$ in (12). However, $(v_d^2[k])$ is almost at the RF-DAC's (quantization) noise floor level. For example, taking an 8-mV drop of $v_{\mathrm{DD}}(t)$ from Fig. 4(a) and referring it to a 15-bit RF-DAC with a 1-V reference voltage results in approximately 2 LSBs of the RF-DAC for $v_d^2[k]$. Hence, the contribution of $x[k] \cdot (v_d^2[k]/V_{\mathrm{dc}})$ is negligible such that

$$\begin{aligned} v_{\mathrm{DAC}}[k] &= x[k] \cdot \Big[V_{\mathrm{dc}} - \underbrace{v_d[k] \cdot \alpha[k]}_{\approx 0} \Big] \\ &\approx x[k] \cdot V_{\mathrm{dc}} \end{aligned} \tag{14}$$

yields the desired, distortion-free output.

The concept (9) with $\alpha[k]$ as proposed in (12) does not represent a perfect inversion of the RF-DAC's nonlinearity. However, the dominating distortions caused by $v_d[k]$ can be canceled, as indicated in (14).

B. Concept of the DPD

The details of the proposed DPD are shown in Fig. 7. The algorithm maps the RF-DAC input signal $x[k]$ to the equivalent supply current and uses a digitally implemented supply network model to recreate the voltage distortion $\hat{\alpha}[k] = (\hat{v}_d[k]/V_{\mathrm{dc}})$, which is further used as a modulation signal for the input signal as in (9). The concept is valid for polar and quadrature capacitive RF-DAC architectures. The parameterization of the predistorter can be estimated by employing conventional (linear low-complexity) adaptive system identification techniques and a feedback receiver, as will be shown in Section III-D.

The block with $O_n(x[k])$ in Fig. 7 maps the input signal to the normalized number of active switching cells $x_{\mathrm{on}}[k]$, depending on the RF-DAC architecture as in (7).

$g(x_{\mathrm{on}})$ is a static nonlinear function, mapping the equivalent number of active cells $x_{\mathrm{on}}[k]$ to the low-frequency input current $i_{\mathrm{DD}}[k]$ of the capacitive RF-DAC. This function is comparable to an instantaneous nonlinearity used in the

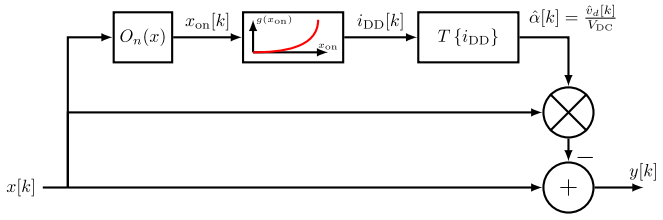


Fig. 7. Concept of supply network predistortion [42].

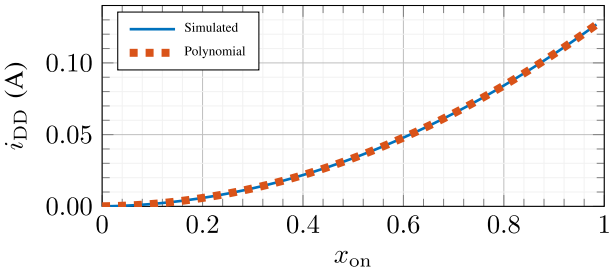


Fig. 8. Simulated and approximated low-frequency capacitive RF-DAC supply current over constant number of active switching cells for a polar-based architecture, i.e., $x_{\text{on}} = |x|$.

Wiener and Hammerstein models [5], [43]. For example, $g(x_{\text{on}})$ can be modeled by a polynomial with order J or by a lookup table, where the respective coefficients are determined either by measurements or by circuit-level simulations. Fig. 8 shows a second-order polynomial, modeling the simulated low-frequency supply current of a polar capacitive RF-DAC for constant input signal magnitudes.

Finally, the operator $T\{\cdot\}$ models the frequency-dependent supply network impedance, as indicated in (6b). The output $\hat{\alpha}[k]$ of $T\{\cdot\}$ is an estimate of the actual voltage drop $v_d[k]$ over the supply network, normalized by V_{dc}. The supply network characteristic is dominated by parasitic effects due to wiring and process variation. Therefore, predicting its values with simulation is unreliable for DPD, and hence, $\hat{\alpha}[k]$ is targeted to be estimated. In contrast to the static nonlinear function $g(x_{\text{on}})$, the model of the supply network $T\{\cdot\}$ accounts for frequency-dependent effects of the supply network, including inductive and capacitive effects. Thus, the proposed approach incorporates compensation of static nonlinearities as well as dynamic (memory) effects.

The output of the supply network model $\hat{\alpha}[k]$ is first multiplied with $x[k]$ and then subtracted from the input signal $x[k]$. The resulting mathematical representation of the concept is given by

$$y[k] = x[k] \cdot (1 - \hat{\alpha}[k]) \tag{15a}$$

$$= x[k] \cdot \left(1 - \frac{\hat{v}_d[k]}{V_{\text{dc}}}\right) \tag{15b}$$

$$= x[k] \cdot (1 - T\{g(x_{\text{on}}[k])\}). \tag{15c}$$

C. Modified Parallel Hammerstein Model

To be implemented, the static and dynamic nonlinearities in (15c) must be realized with mathematical functions. In this work, $g(x_{\text{on}})$ is modeled by a polynomial of order J. The operator $T\{\cdot\}$ is realized by a digital FIR filter of length M,

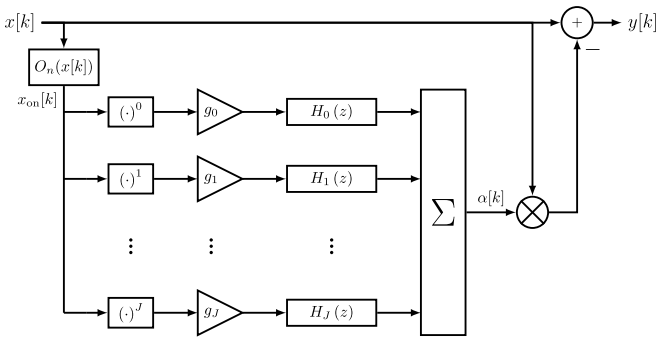


Fig. 9. Block diagram of the proposed SNDPD for polar and quadrature capacitive RF-DAC architectures.

which models the impulse response of the supply network as indicated in (6b), i.e., $T\{\cdot\} \rightarrow T[k] = \sum_{m=0}^{M-1} h_m\, \delta[k-m]$. Thus, $\hat{\alpha}[k]$ is given by

$$\hat{\alpha}[k] = \sum_{m=0}^{M-1} h_m \cdot \left(\sum_{j=0}^{J} g_j \cdot x_{\text{on}}^j[k-m]\right) \tag{16}$$

having $(J+1+M)$ coefficients. Inserting $\hat{\alpha}[k]$ in the proposed DPD (9) gives

$$y[k] = x[k] \cdot \left[1 - \sum_{m=0}^{M-1} h_m \cdot \left(\sum_{j=0}^{J} g_j \cdot x_{\text{on}}^j[k-m]\right)\right]. \tag{17}$$

Using (16) to model the voltage distortion is similar to a typically used Hammerstein approach, where a static nonlinear function is followed by one FIR filter. Moving h_m inside the inner sum and introducing the coefficients $a_{jm} = h_m \cdot g_j, \forall(m = 0, \ldots, M-1;\ j = 0, \ldots, J)$ leads to

$$y[k] = x[k]\left(1 - \underbrace{\sum_{m=0}^{M-1}\sum_{j=0}^{J} a_{jm}\, x_{\text{on}}^j[k-m]}_{\hat{\alpha}[k]=\frac{\hat{v}_d[k]}{V_{\text{dc}}}}\right). \tag{18}$$

Considering the a_{jm} as $(J+1)\cdot M$ independent coefficients leads to an even more general DPD concept, where separate FIR filters are applied for each monomial as shown in the block diagram in Fig. 9. Furthermore, with (18), the output is linear in the parameters a_{jm} and linear estimation algorithms can be used as will be shown next.

The derived DPD (18) uses a parallel filter structure similar to the general (parallel) Hammerstein model [9] and the MP. Furthermore, the SNDPD shows similarities to the envelope MP (EMP) model [44], [45]. However, the input to the SNDPD's predistorter depends on the normalized number of switching cells $x_{\text{on}}[k]$, changing with the architecture of the RF-DAC as in (7). Although, for polar architectures where $x_{\text{on}}[k] = |x[k]|$, the proposed SNDPD is equivalent to the EMP.

D. Parameter Estimation

The goal is to estimate the parameters a_{jm} through observation of the equivalent baseband output signal $v_{\mathrm{DAC}}[k]$ of the RF-DAC, similar to typically used DPD models such as the MP and the GMP. With (8) and using vector notation, the RF-DAC output without DPD can be modeled by

$$v_{\mathrm{DAC}}[k] = x[k]\left(V_{\mathrm{dc}} + \underbrace{\mathbf{x}_{\mathrm{on}}[k]^T \mathbf{a}_{jm}}_{\hat{\alpha}[k]}\right) \tag{19}$$

where

$$\mathbf{x}_{\mathrm{on}}[k] = \begin{bmatrix} x_{\mathrm{on}}^0[k-0] \\ x_{\mathrm{on}}^1[k-0] \\ \vdots \\ x_{\mathrm{on}}^J[k-0] \\ x_{\mathrm{on}}^0[k-1] \\ x_{\mathrm{on}}^1[k-1] \\ \vdots \\ \vdots \\ x_{\mathrm{on}}^J[k-M+1] \end{bmatrix}, \tag{20}$$

and the unknown parameter vector is defined as

$$\mathbf{a}_{jm} = [a_{00}\ a_{10}\ \ldots\ a_{(J)0}\ a_{01}\ a_{11}\ \ldots\ a_{(J)(M-1)}]^T. \tag{21}$$

The term $\mathbf{x}_{\mathrm{on}}[k]^T\mathbf{a}_{jm}$ with $\mathbf{x}_{\mathrm{on}}[k] \in \mathbb{R}^{(J+1)\cdot M\times 1}$ and $\mathbf{a}_{jm} \in \mathbb{C}^{(J+1)\cdot M\times 1}$ represents the model of the supply voltage distortion as in (12), i.e., $\hat{\alpha}[k] = (\hat{v}_d[k]/V_{\mathrm{dc}})$.

Putting the samples of $v_{\mathrm{DAC}}[k]$ and $x[k]$ together to vectors, one can write the output of the RF-DAC in vector–matrix notation

$$\mathbf{v}_{\mathrm{DAC}}[k] = \mathbf{x}[k]\, V_{\mathrm{dc}} + \mathbf{D}_x[k]\cdot\mathbf{X}_{\mathrm{on}}[k]\cdot\mathbf{a}_{jm} \tag{22}$$

with

$$\mathbf{v}_{\mathrm{DAC}}[k] = [v_{\mathrm{DAC}}[k]\ v_{\mathrm{DAC}}[k-1]\ \ldots\ v_{\mathrm{DAC}}[k-K+1]]^T \tag{23}$$

and

$$\mathbf{x}[k] = [x[k]\ x[k-1]\ \ldots\ x[k-K+1]]^T. \tag{24}$$

Matrices $\mathbf{X}_{\mathrm{on}}[k]$ and $\mathbf{D}_x[k]$ in (22) are, respectively, given by

$$\mathbf{X}_{\mathrm{on}}[k] = \begin{bmatrix} \mathbf{x}_{\mathrm{on}}[k]^T \\ \mathbf{x}_{\mathrm{on}}[k-1]^T \\ \vdots \\ \mathbf{x}_{\mathrm{on}}[k-K+1]^T \end{bmatrix} \tag{25}$$

and

$$\mathbf{D}_x[k] = \mathrm{diag}(\mathbf{x}[k]) \tag{26}$$

with $\mathbf{X}_{\mathrm{on}}[k] \in \mathbb{R}^{K\times(J+1)\cdot M}$ and $\mathbf{D}_x[k] \in \mathbb{C}^{K\times K}$. Each row of (25) consists of the input samples to the parallel filter structure as in (19) for the $[k-i]$th sample with $i = 0, \ldots, K-1$.

Defining the so-called observation matrix $\mathbf{H}_x[k] = \mathbf{D}_x[k]\cdot\mathbf{X}_{\mathrm{on}}[k]$ finally yields the affine model

$$\mathbf{v}_{\mathrm{DAC}}[k] = \mathbf{x}[k]\, V_{\mathrm{dc}} + \mathbf{H}_x[k]\,\mathbf{a}_{jm}. \tag{27}$$

Hence, the output of the RF-DAC $\mathbf{v}_{\mathrm{DAC}}[k]$ is linear in the unknown parameter vector $\mathbf{a}_{jm}$ using the model of the supply network distortion, as shown in (18). From (27), one can thus derive a linear estimator such as the linear (complex-valued) least-squares estimator to estimate the unknown coefficient vector [46], [47], i.e.,

$$\hat{\mathbf{a}}_{jm}[k] = \left[\mathbf{H}_x[k]^H\mathbf{H}_x[k]\right]^{-1}\mathbf{H}_x[k]^H(\mathbf{v}_{\mathrm{DAC}}[k] - \mathbf{x}[k]\, V_{\mathrm{dc}}) \tag{28}$$

where $(\cdot)^H$ is the Hermitian transpose and $\mathbf{v}_{\mathrm{DAC}}[k]$ are the (measured) equivalent baseband data samples of the capacitive RF-DAC's output.

Thus, the proposed SNDPD model in (17) with $\alpha[k]$ (12) allows to use linear estimation algorithms to determine the parameters a_{jm} from the output of the RF-DAC, similar to the typically used DPD solutions. The SNDPD model is based on the modeling of the effects of a varying supply voltage of the capacitive RF-DAC and therefore does not cover all nonidealities of the RF-DAC. However, estimating parameters a_{jm} by minimizing some cost function of the difference between the output signal and the input signal, as proposed above, inherently considers also some other nonlinearities. As will be shown next, the SNDPD outperforms conventionally used models such as the MP and the GMP, validating the presented circuit-inspired DPD and modeling approach.

IV. Measurement Results of the Supply Network DPD

This section presents the measured results achieved with the proposed SNDPD approach. The figures of merit are, as for typical DPD evaluations, the in-band performance in terms of EVM and the out-of-band performance in terms of the adjacent channel power ratio (ACPR). The SNDPD is validated with two quadrature capacitive RF-DAC designs: a capacitive RF-DAC-based digital PA (DPA) [21] and a wideband low-noise quadrature capacitive RF-DAC, similar to [22].

Furthermore, the performance of the SNDPD is compared to the MP [10] and the GMP [11]. In contrast to the MP and the GMP, the SNDPD explicitly uses the equivalent number of active switching cells $x_{\mathrm{on}}[k]$ (7) as input to the predistorter, which corresponds to the dependence of the supply voltage distortion on the number of active switching cells, as discussed in Section II-B. Both measured RF-DACs are based on a quadrature architecture, and hence, the input to the SNDPD is $x_{\mathrm{on}}[k] = |x_I[k]| + |x_Q[k]|$, whereas MP and GMP use the magnitude $|x[k]|$.

A. Evaluation Setup

The measurement setup, similar for both capacitive RF-DACs, is shown in Fig. 10. The (predistorted) input signal is loaded to an on-chip RAM, which streams the digital code samples to the RF-DAC. A vector signal analyzer (VSA) is connected to the antenna output of the RF-DAC, terminated by a 50-Ω resistor. The VSA also performs the downconversion from the RF to the equivalent baseband signal, similar to a feedback receiver for on-chip implementations. The DPA and the wideband RF-DAC are supplied by an ideal (nonswitching)

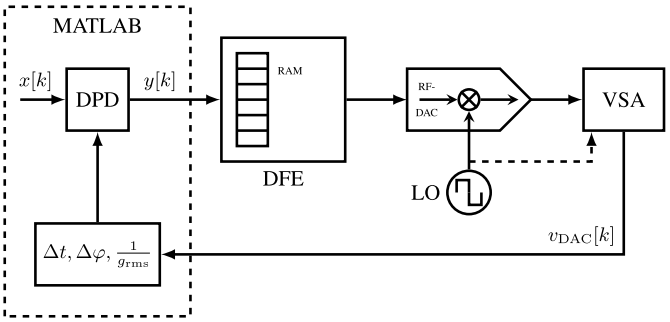


Fig. 10. Measurement setup for DPD evaluation.

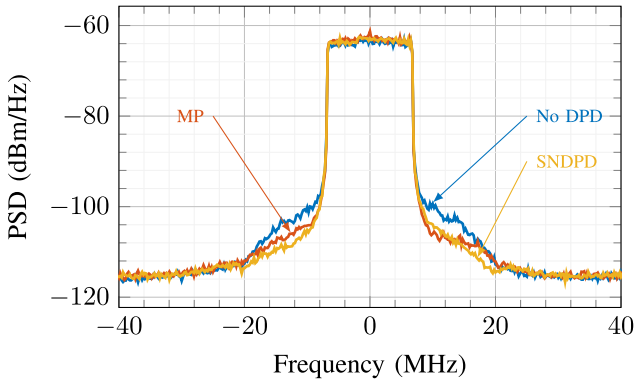


Fig. 11. PSDs of 15-MHz signals without DPD, with MP, and with SNDPD.

voltage source. The LO (clock) for both designs is generated by an external clock generator, which is limited in terms of phase noise performance, as will be discussed next.

The evaluated adjacent channel power is integrated over the same bandwidth as the input signal for the upper and lower adjacent channel, respectively. Thus, for a 20-MHz input signal, the upper out-of-band signal power is integrated over $\Delta f_G + 10$ MHz $\leq f \leq \Delta f_G + 30$ MHz, where Δf_G is a guard band for the respective bandwidth. The reported numbers in the tables correspond to the lower ACPR of either the upper or the lower adjacent channel.

The predistortion and the estimation of the model coefficients are performed with MATLAB using the downconverted baseband signal $v_{\mathrm{DAC}}[k]$ from the VSA. The downconverted output signal is normalized by the expected linear rms gain of the RF-DAC g_{rms} and further time (Δt) and phase ($\Delta\varphi$) synchronized to the input data, as shown in Fig. 10 [4]. The direct and the indirect learning methods have been applied [1] using the complex-valued least-squares algorithm (28) to estimate the coefficients. Coefficient estimation and predistortion are combined in the DPD block in Fig. 10.

B. DPA Measurement Results

The DPA connects four quadrature capacitive RF-DAC cores to a power combiner to increase the output power up to 25 dBm [21]. Even though the supply network was specifically designed to be very low ohmic, the DPD further reduces the spectral regrowth generated by distortions of the supply network.

The VSA for the DPA predistortion evaluation was limited to 40-MHz baseband bandwidth. Thus, DPD performance for spectral regrowth was evaluated using a 15-MHz input signal. The in-band performance, however, was evaluated using a standard-compliant 20-MHz Wi-Fi input signal, using also a 20-MHz signal as a training sequence for the DPD. The coefficients of the models have been estimated by using only one iteration of the indirect learning method.

Here, the SNDPD is compared to the MP using the following implementations:

$$y_{\mathrm{SNDPD}}[k] = x[k]\left(1 - \sum_{m=0}^{M-1}\sum_{j=0}^{J-1} a_{jm}\, x_{\mathrm{on}}^{j}[k-m]\right) \tag{29}$$

TABLE I
KEY PARAMETERS OF FIG. 11

DPD type	Coefficient Set (J/M)	Power (dBm)	ACPR (dB)
No DPD	0/0	7.48	-40.81
MP	3/4	8.21	-44.52
SNDPD	3/4	7.94	-45.13

$$y_{\mathrm{MP}}[k] = \sum_{j=0}^{J-1}\sum_{m=0}^{M-1} a_{jm}\, x[k-m]\,|x[k-m]|^{j} \tag{30}$$

where J defines the highest order of the nonlinearity and M is the filter length. The MP also includes the linear memory terms for $j = 0$, whereas the SNDPD model for $j = 0$ becomes $x[k] \cdot (1 - \sum_m a_{0m})$, adding only a constant term to $y[k]$. Thus, the MP inherently includes more degrees of freedom.

Fig. 11 and Table I show the PSDs and key parameters of the comparison of the SNDPD and the MP for the out-of-band radiation. The SNDPD achieves similar results compared to the MP although the SNDPD model's complexity is significantly lower.

The achieved improvement of the EVM using the SNDPD and the MP, respectively, is shown in Fig. 12. Both DPD approaches use a coefficient set of $J = 3$ and $M = 4$. The input signal is a 20-MHz, 64-QAM modulated orthogonal frequency-division multiplexing (OFDM) signal. The coefficients are estimated once at 14-dbm output power and then used over the whole input signal power range. Here, the SNDPD outperforms the MP by approximately 1 dB over the tested output power range. At 14-dbm output power, the SNDPD improves the EVM by almost 4 dB compared to the measurement without any DPD.

C. Wideband Capacitive RF-DAC Measurement Results

Compared to the DPA, the wideband quadrature capacitive RF-DAC is designed for less output power. However, high linearity and minimized out-of-band noise floor is achieved even without DPD. Its spectral regrowth is significantly lower compared to the DPA. Furthermore, due to increasing EVM requirements for the latest communication standards such as 5G and Wi-Fi 6, also the in-band performance is improved.

Another distinction to the DPA is the supply network. An internal LDO regulator is used to compensate for dc–dc

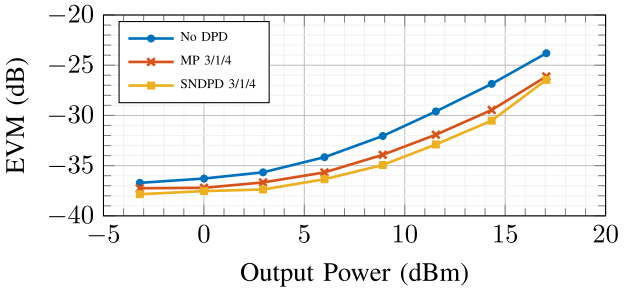


Fig. 12. EVM comparison of the DPA with no DPD, with MP, and SNDPD.

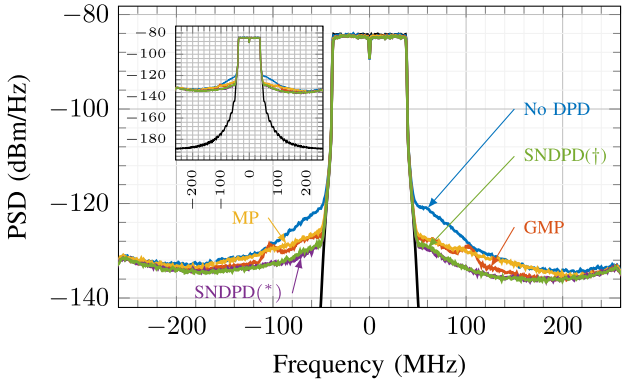


Fig. 13. PSDs of 80-MHz OFMD modulated signals. Comparison between GMP, MP, and SNDPD.

TABLE II
KEY PARAMETERS OF FIG. 13

DPD type	Coefficient Set $(J/L/M)$	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	$0/0/0$	-5.68	-33.83	-39.94
GMP	$7/0/4$ ($N_{\text{lead}} = N_{\text{lag}} = 1$)	-5.83	-38.26	-44.33
MP	$7/0/4$	-5.86	-39.02	-43.74
SNDPD(*)	$7/0/4$	-6.01	-39.03	-46.73
SNDPD(†)	$2/0/4$	-5.99	-39.02	-46.40

voltage ripple and the signal-dependent current feedback. However, the LDO is not designed to track the applied high-bandwidth signals, and thus, the supply network effects degrade the ACPR.

The bandwidth of the used VSA for these measurements was 600 MHz, which allowed to validate the DPD for signal bandwidths up to 160 MHz.

Contrary to the DPA measurements, the direct and the indirect learning methods were applied, using indirect learning for the initial calibration, followed by three iterations of using direct learning to update the coefficients [48].

Here, the performance of the SNDPD is compared with the MP and the GMP. The implemented realizations are given by

$$y_{\text{SNDPD}}[k] = \sum_{m=0}^{M_{\text{lin}}-1} a_{0m}\, x[k-m] - \left(x[k] \cdot \sum_{m=0}^{M-1} \sum_{j=1}^{J-1} a_{jm}\, x_{\text{on}}^{j}[k-m] \right) \tag{31}$$

$$y_{\text{MP}}[k] = \sum_{m=0}^{M_{\text{lin}}-1} a_{0m}\, x[k-m] + \sum_{j=1}^{J-1} \sum_{m=0}^{M-1} a_{jm}\, x[k-m]\, |x[k-m]|^{j} \tag{32}$$

$$\begin{aligned} y_{\text{GMP}}[k] = & \sum_{m=0}^{M_{\text{lin}}-1} a_{0m}\, x[k-m] \\ & + \sum_{j=1}^{J-1} \sum_{m=0}^{M-1} a_{jm}\, x[k-m]\, |x[k-m]|^{j} \\ & + \sum_{j=1}^{J-1} \sum_{m=0}^{M-1} \sum_{n=1}^{N_{\text{lag}}} b_{jmn}\, x[k-m]\, |x[k-m-n]|^{j} \\ & + \sum_{j=1}^{J-1} \sum_{m=0}^{M-1} \sum_{n=1}^{N_{\text{lead}}} c_{jmn}\, x[k-m]\, |x[k-m+n]|^{j}. \end{aligned} \tag{33}$$

The parameters are summarized as follows.

1) J defines the highest order of the nonlinearity.
2) M defines the number of used memory taps for the nonlinear terms.
3) M_{lin} defines the number of memory taps for the linear memory terms, represented by the first row of each DPD model above.
4) N_{lag} and N_{lead} define the number of off-diagonal elements of the GMP.

In the results shown next, the parameter L defines whether the linear memory terms are included in the model, i.e.,

$$L = \begin{cases} 0, & \dots M_{\text{lin}} = 1 \\ 1, & \dots M_{\text{lin}} = M. \end{cases} \tag{34}$$

Thus, if $L = 1$, the linear memory is included. Depending on the individual definitions in the literature, the MP and the GMP can inherently include linear memory terms. However, the SNDPD model as defined in (18) does not account for these terms. To provide a better comparison, these linear terms are additionally included in the SNDPD. For $L = 0$, i.e., $M_{\text{lin}} = 1$, the SNDPD in (31) becomes again the proposed approach as in (18). However, as is shown next, including the linear memory terms improves the performance of the SNDPD for the measured RF-DAC.

Fig. 13 and Table II show the comparison of the different predistortion approaches for an 80-MHz 802.11ac Wi-Fi signal. The SNDPD approach outperforms the MP and the GMP, which show a higher noise floor in general, as shown in Fig. 13. The increased noise floor of the MP and GMP is most probably caused by estimation errors due to the higher number of coefficients and basis functions used in the DPD, respectively. For the GMP, this even causes small humps as can be seen in the spectrum at ± 100 MHz. However, the ACPR can still be improved by almost 5 dB. In contrast, the SNDPD is robust for the same polynomial order J and memory taps M. Furthermore, the SNDPD uses the sum of magnitudes, i.e., $x_{\text{on}}[k] = |x_I[k]| + |x_Q[k]|$, as input to the

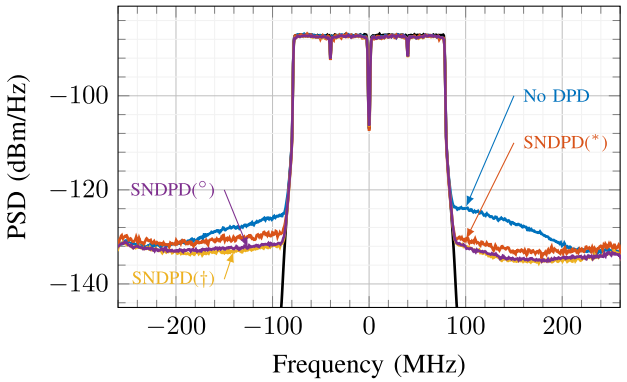


Fig. 14. PSDs of 160-MHz OFMD modulated signals. Comparison between different coefficient sets of the SNDPD.

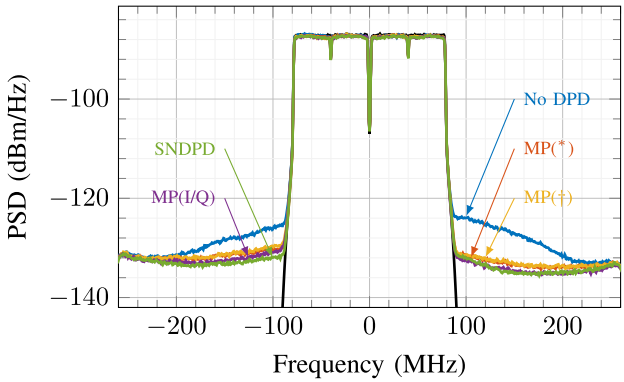


Fig. 15. PSDs of 160-MHz OFMD modulated signals. Comparison between MP and SNDPD.

TABLE III
KEY PARAMETERS OF FIG. 14

DPD type	Coefficient Set $(J/L/M)$	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.49	-34.82	-39.78
SNDPD(*)	5/0/4	-5.61	-39.17	-42.72
SNDPD(†)	5/1/4	-5.70	-39.77	-44.81
SNDPD(°)	5/1/14	-5.64	-39.89	-44.43

TABLE IV
KEY PARAMETERS OF FIG. 15

DPD type	Coefficient Set $(J/L/M)$	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.49	-34.82	-39.78
MP(*)	5/0/4	-5.57	-39.32	-43.68
MP(†)	5/1/4	-5.59	-39.37	-43.35
MP(I/Q)	5/1/4 (I/Q)	-5.69	-39.68	-44.20
SNDPD	5/1/4	-5.70	-39.77	-44.81

predistorter, hence achieving better performance although less basis functions are used in the model. As will be shown next, also the performance of the MP can be improved by using $x_{\text{on}}[k]$ instead of $|x[k]|$.

Moreover, the SNDPD even achieves comparable performance by only using the second-order nonlinearities in the DPD model, i.e., $J = 2$. This indicates the relation of the SNDPD model to the actual behavior of the supply current $i_{\text{DD}}(t)$, which has a quadratic-like behavior, as shown in Fig. 8. The EVM can be improved by more than 5 dB and the ACPR can be improved by almost 7 dB, as shown in Table II.

The small plot in Fig. 13 depicts the difference between the input signal and the output signals on a larger scale. The achievable noise floor of all measurements is limited by the accuracy of the used measurement equipment, especially by the phase noise of the used LO (clock) generator. All further plots thus only show the zoomed area.

Fig. 14 and Table III show the performance of the SNDPD approach for different coefficient sets for a 160-MHz input signal. Adding the linear memory terms in the DPD, i.e., $L = 1$, improves the ACPR by additional 2 dB. In addition, also the number of filter taps is increased to 14. However, this only shows a minor impact on the DPD performance. Using $J = 5, L = 1$, and $M = 4$ improves the EVM and ACPR by 5 dB while still keeping the complexity low. At particular frequency bins, the spectral leakage could be decreased by almost 12 dB.

Another interesting comparison is shown in Fig. 15 and Table IV, where the SNDPD approach is compared with the MP for a 160-MHz 802.11ac Wi-Fi signal. Here, the linear memory terms are now also used in the MP. Furthermore, the I/Q case uses the sum of magnitudes, i.e., $x_{\text{on}}[k]$, as input to the nonlinear terms of the MP, equivalent to the SNDPD. Including the linear terms and using the sum of magnitudes

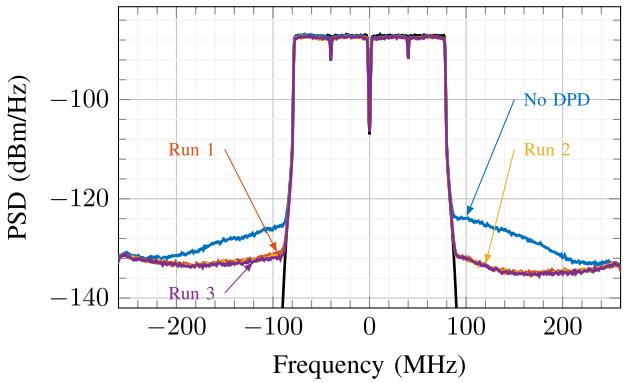


Fig. 16. PSDs of a 160-MHz Wi-Fi signal for three coefficient learning iterations using the SNDPD approach with $J = 5$, $L = 1$, and $M = 4$.

TABLE V
KEY PARAMETERS OF FIG. 16

Run	Learning Method	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	none	-5.49	-34.82	-39.78
Run 1	indirect	-5.70	-39.86	-44.39
Run 2	direct	-5.72	-39.81	-44.65
Run 3	direct	-5.70	-39.77	-44.81

results in almost the same improvement of the EVM and the ACPR compared with the SNDPD, as shown in Table IV. This indicates that the nonlinear characteristic of the quadrature capacitive RF-DAC is dominated by the sum of magnitudes $|x_I[k]| + |x_Q[k]|$ rather than by the magnitude $|x[k]|$, corresponding to the derived dependence of the supply network variations on the number of active switching cells $x_{\text{on}}[k]$, as discussed in Section II-B.

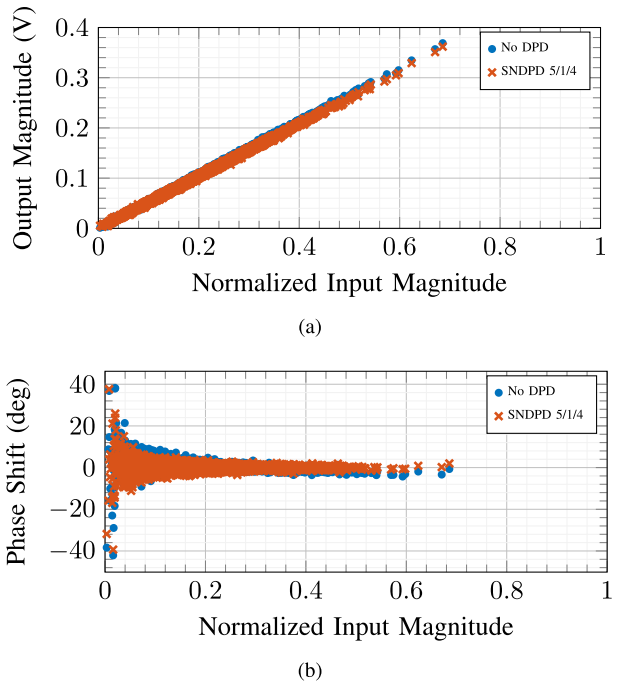


Fig. 17. (a) AM–AM and (b) AM-PM of measured wideband RF-DAC without DPD and with SNDPD with $J = 5, L = 1$, and $M = 4$. The performance was limited by the measurement setup, phase noise of the LO (clock) generator.

Fig. 16 and Table V show the results of three iteration steps of the coefficient estimation of the SNDPD with $J = 5$, $L = 1$, and $M = 4$ using a 160-MHz 802.11ac Wi-Fi signal. The DPD already achieves a significant improvement after the first iteration, using indirect learning. Additional iterations only have a minor impact on the ACPR and the EVM, which most probably result from the limited accuracy of the measurement setup.

Fig. 17 additionally shows the respective AM–AM and AM–PM plots without DPD and with SNDPD. The performance, especially for the AM–PM, indicates the limits of the phase noise of the external LO generator.

The presented measurement results validate that the SNDPD is an effective method to significantly improve the ACPR and the EVM of capacitive RF-DACs. Due to the circuit-inspired modeling approach of the RF-DAC's nonidealities, the proposed SNDPD allows for a feasible implementation on an integrated circuit while even outperforming conventional DPD models, such as the (generalized) MP.

V. Conclusion

This work introduced a novel concept of a circuit-inspired DPD technique to compensate for nonlinear effects generated by nonideal supply networks of capacitive RF-DACs.

The proposed SNDPD digitally recreates the signal-dependent distortions on the supply voltage and utilizes this information to modulate the input signal such that the distortions on the capacitive RF-DAC's output are canceled. The developed underlying mathematical model of the DPD requires a limited set of coefficients, allowing for feasible implementations on integrated circuits. Furthermore, the parameterization of the presented SNDPD can be estimated by employing conventionally linear low-complexity adaptive system identification techniques. The concept accounts for static as well as dynamic (memory) effects and is valid for polar and quadrature capacitive RF-DAC architectures.

The input of the SNDPD depends on the normalized number of active switching cells $x_{\text{on}}[k] = O_n(x[k])$, changing with the used RF-DAC architecture. This approach differs compared to the typically used DPD models such as the MP, the GMP, and the EMP that always use the magnitude of the baseband input signal $|x[k]|$. In general, the SNDPD can be seen as a special case of the GMP (similar to the EMP), which only uses the relevant basis functions corresponding to nonlinear effects caused by the nonideal supply network. This also yields a more robust behavior of the SNDPD model compared to the GMP even when using higher polynomial orders and a larger set of memory taps.

The proposed SNDPD focuses on canceling nonideal supply effects of capacitive RF-DACs. As such, the SNDPD does not include special cancellation techniques for additional architecture-specific nonlinear effects such as LO remodulation, IQ image generation, and PM–PM/PM–AM distortions, which may be implemented additionally to the SNDPD. However, due to the chosen estimation concept, also, nonlinear distortions other than supply network effects are inherently compensated to some extent. Future works may additionally address the mentioned effects by extending the SNDPD model.

The SNDPD has been validated by measurements using two different quadrature-based capacitive RF-DAC architectures. It outperformed state-of-the-art black-box models such as the MP and the GMP while keeping computational complexity at a minimum. The EVM of the tested RF-DACs was improved by up to 6 dB for input signals with bandwidths of up to 160 MHz. Furthermore, the ACPR was decreased by up to 7 dB, whereas for dedicated frequency bins, the spectral emission outside the signal band could even be reduced by 12 dB. Conclusively, the SNDPD considerably increased the linearity of the measured capacitive RF-DACs.

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