Micromachined Silicon-Core Substrate-Integrated Waveguides at 220–330 GHz

Aleksandr Krivovitca, Umer Shah, *Member, IEEE*, Oleksandr Glubokov, *Member, IEEE*, and Joachim Oberhammer, *Senior Member, IEEE*

***Abstract*— In this article, we present a new technology platform for creating compact and loss-efficient wafer-scale integrated micromachined substrate-integrated waveguides with silicon-core (Si-SIWs) for the 230–330-GHz frequency range. The silicon dielectric core enables highly integrated sub-millimeter-wave systems, since it allows for downscaling the waveguide's cross section by a factor of 11.6, and the volume of components by a factor of 39.3, as compared to an air-filled waveguide. Moreover, geometrical control during fabrication of this type of waveguides is significantly better as compared to micromachined hollow waveguides. The measured waveguide's insertion loss (IL) is 0.43 dB/mm at 330 GHz (0.14 dB/λ_g, normalized to the guided wavelength). A low-loss ultrawideband coplanar-waveguide (CPW) transition is implemented to enable direct measurements of devices and circuits in this waveguide platform, and this is also the very first CPW-to-SIW transition in this frequency range. The measured IL of the transition is better than 0.5 dB (average 0.43 dB above 250 GHz), which is lower than for previously reported CPW-to-SIW transitions even at 3 times lower frequencies; the return loss is better than 14 dB for 75% of the band. As devices examples implemented in this platform, a filter and H-plane waveguide bends are shown. The waveguides and the devices are manufactured by deep-silicon etching using a cost-efficient two-mask micromachining process.**

***Index Terms*— Coplanar waveguide (CPW), CPW probes, CPW transition, microfabrication, micromachining, substrate integrated waveguide (SIW), waveguide filter.**

I. Introduction

COMMERCIAL interest in highly integrated, cost-efficient, simple, and reliable ultra-high frequency platforms has grown dramatically in the last couple of decades [1]. Computer numerical control (CNC) milling of metal in split-block designs is the most established method to fabricate waveguide components, since this technology provides relatively high precision and relatively low surface roughness resulting in acceptable low insertion loss (IL) [2]. However, the manufacturing process requires a large support metal block, resulting in bulky devices, and the whole process is not scalable to volume production. A promising alternative fabrication technology is silicon-micromachining using deep reactive-ion-etching (DRIE), which allows for batch fabrication, has superior (micrometer) precision, enables high-complexity geometries, as well as nanometer surface roughness and thus better insertion loss. Impressive device performance has been achieved by micromachining in various sub-THz frequency bands, for instance, for waveguides [3]–[5], couplers [6], low-loss filters [7], [8], OMTs [9], antennas [10], [11], and MEMS-reconfigurable devices such as waveguide switches [12] and phase shifters [13].

A promising concept to compromise between IL and bulkiness [14] is the substrate-integrated waveguide (SIW) technology. One of the main advantages of SIWs is substantial downscaling, i.e., by the square root of dielectric's relative permittivity in all dimensions, as compared to air-filled waveguides; this property provides higher integration density for SIW. The SIW approach allows for manufacturing not only RF passive elements but also integrating microelectronic active components to build up hybrid circuits [15]. SIW have so far only been shown up to 180 GHz [16]. The basic transmission medium of SIW technology is a dielectric-filled waveguide in which the wave is guided by a metal confinement. Due to the inserted dielectric, the losses in SIW are higher than in air-filled waveguides, but still substantially lower compared to planar transmission lines [17]. To create the transmission medium in conventional SIWs, conducting through-substrate vias are embedded in a dielectric substrate that electrically connect the top and bottom metal plates. The disadvantage of conventional SIW's is related to their fabrication which requires vias limiting the waveguide's height to substantially smaller than standard, resulting in reduced power handling capabilities of SIW. Furthermore, geometrical limitations of vias in conventional SIW result in nonideal sidewalls, leading to higher IL and practically restricting the operation frequency range to about up to *W*-band. Furthermore, probing interfaces require high geometrical accuracy, which limits SIW to frequencies below 100 GHz when using printed-circuit-board (PCB) fabrication techniques. Therefore, micromachining of silicon-filled waveguides has been recently investigated [18], [19] and has achieved excellent performance which rivals conventional SIW and even air-filled waveguides in the *W*-band [5].

Manuscript received June 2, 2020; revised August 3, 2020; accepted August 15, 2020. Date of publication September 21, 2020; date of current version December 3, 2020. This work was supported in part by the Swedish Foundation for Strategic Research Synergy under Grant Electronics SE13-007, and in part by the European Research Council (ERC) through the European Union's Horizon 2020 research and innovation programme under Grant 616846. *(Corresponding author: Aleksandr Krivovitca.)*

The authors are with the Department of Micro- and Nanosystems, KTH Royal Institute of Technology, SE-100 44 Stockholm, Sweden (e-mail: alekr@kth.se).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2020.3022060

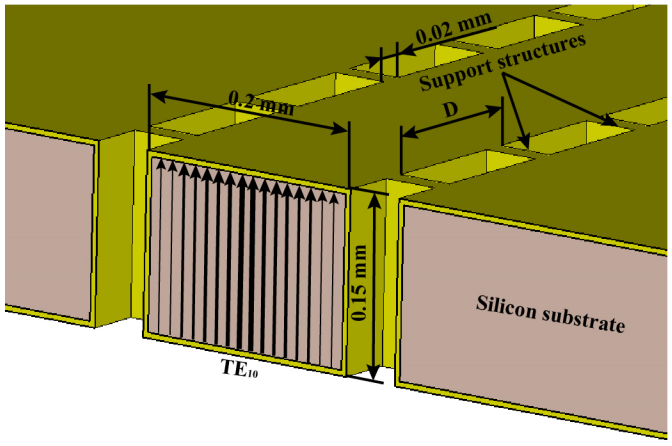

Fig. 1. Basic structure of Si-SIW waveguide, micromachined into a silicon wafer, with support structures.

In this article, which extends our conference publication [20], we present a new fabrication technology platform for implementing integrated rectangular waveguides in the 220–325-GHz frequency range using micromachining with DRIE. The new platform, combining micromachining with photolithography, allows fabricating sub-THz and THz devices with CPW-to-Si-SIW transition enabling direct on-chip measurements of various components, such as first time reported here bends and filters. In the future, the platform can be used for integrating active components and building complex sub-THz and THz circuits.

II. Silicon-Core Substrate Integrated Waveguide

A. Silicon-Core Substrate-Integrated-Waveguide

Fig. 1 shows the cross section of the proposed Si-SIW designed in the bulk layer of a silicon wafer. The Si-SIW consists of a straight piece of silicon with a rectangular cross-section surrounded by etched through trenches. All the surfaces of the presented structure are metallized. Microfabrication techniques allow patterning the front-side metal layer of the chip with micrometer precision to create planar features for integrating other components or creating interfaces. To mechanically suspend the Si-SIW to the rest of the wafer, support structures are implemented. To minimize discontinuities the width of the support structures is chosen to be 20 μm, which is substantially less than the guided wavelength ($\lambda_g = 516$ μm at the center frequency of 275 GHz). The support elements still create periodic discontinuities [21] and thus introduce a series of resonances in its frequency response, at frequencies corresponding to the condition $\lambda_g = 2 \cdot D/n$, where n are integer numbers, which is demonstrated in Fig. 2. With increasing distance D between the support elements, the resonant frequency increases and eventually even the second harmonic influences the performance of the waveguide for large values of D.

For comparing different waveguide technologies, the losses should be related to the guided wavelength and not per unit length, as distributed-component size and functionality is related to the guided wavelength size. Fig. 3 shows the simulated IL for three waveguide types in the frequency range 230–330 GHz: a Si-SIW with height $H_{si} = 150$ μm and width $W_{si} = 200$ μm (these dimensions are used for the design of Si-SIW in this article), a hollow waveguide with the standard

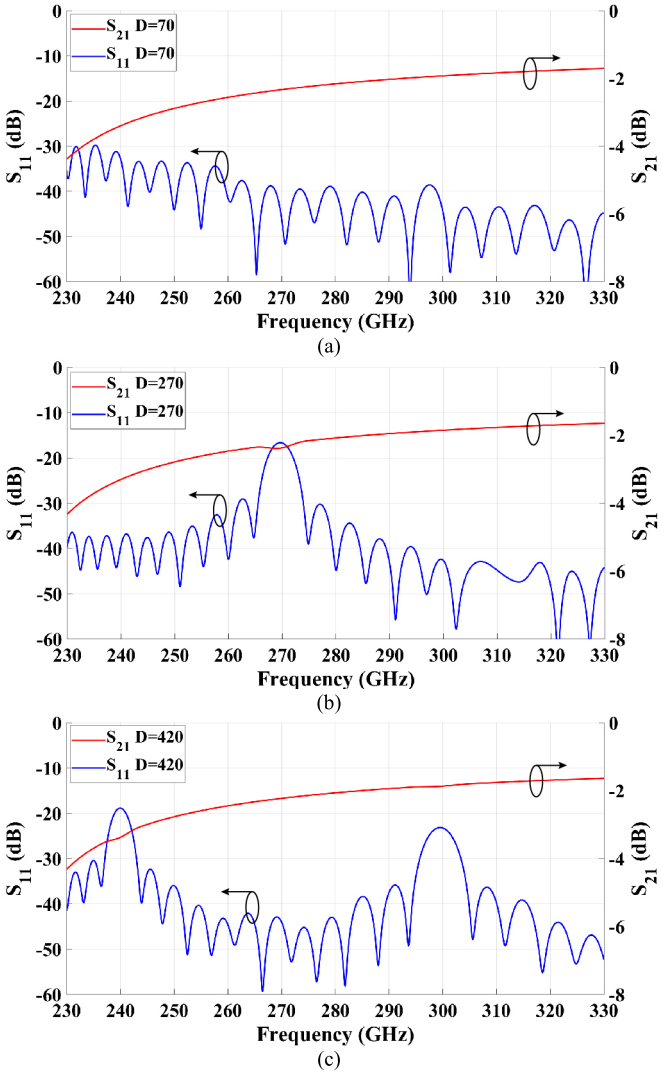

Fig. 2. Simulated S-parameters of a 5-mm waveguide piece with variation of the support structure periodicity. (a) $D = 70$ μm. (b) $D = 270$ μm. (c) $D = 420$ μm.

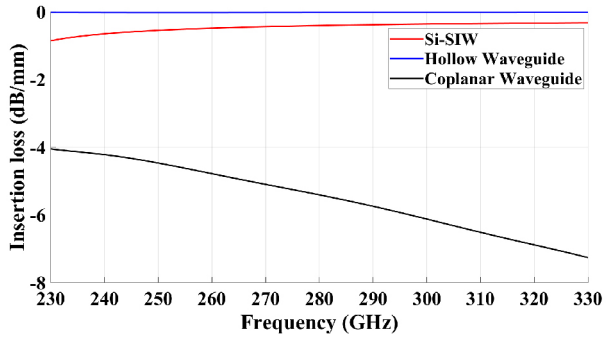

Fig. 3. Simulated IL per millimeter for the novel Si-SIW (red), compared to a hollow micromachined rectangular waveguide (blue) and a CPW (green), assuming a bulk gold conductivity ($\sigma = 1.8e + 007$ S/m).

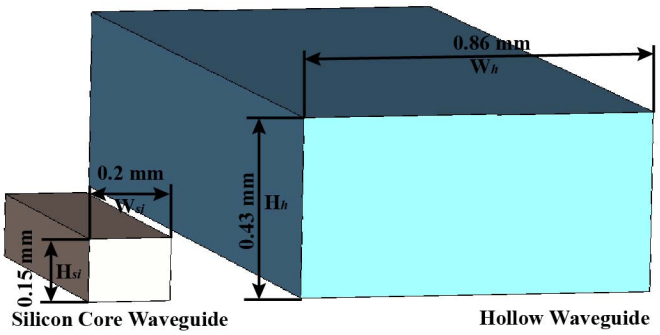

Fig. 4. Comparison of sizes of a silicon-filled to an air-filled waveguide for 220–325 GHz.

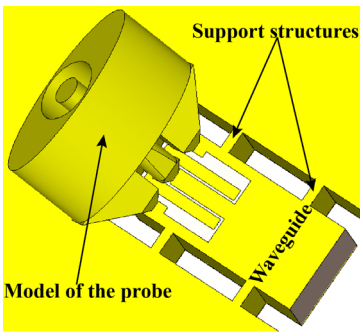

Fig. 6. CST Microwave Studio simulation model of the coplanar probe on the transition to the silicon core micromachined SIW.

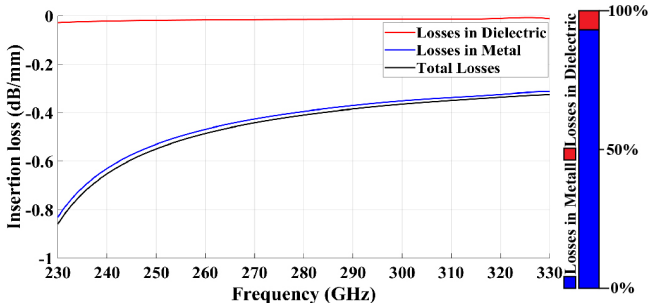

Fig. 5. Simulation results of the contribution of the metallization and the dielectric material to the overall IL of the proposed Si-SIW: the metallization losses contribute by 94%. For dielectric loss only, the metal is set to PEC; for metallization loss only, the tanδ of the dielectric is set to zero.

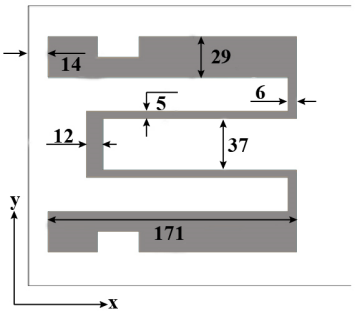

Fig. 7. Layout of the CPW to micromachined-SIW transition, with dimensions in μm.

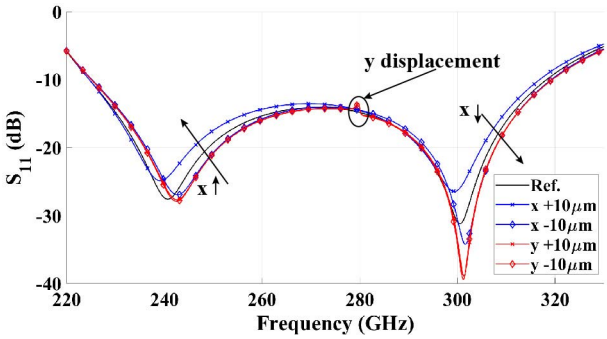

Fig. 8. Probe position sensitivity analysis.

WM-864 sizes $H_h = 864$ μm and $W_h = 432$ μm, and a CPW line with a substrate height of $H_{\text{sub}} = 150$ μm, a signal line width of $W_{\text{cpw}} = 50$ μm and a gap of $G = 32$ μm. Since the same DRIE processing as in [3] was used to fabricate Si-SIW, similar losses model with $\sigma = 1.8 \times 10^7$ S/m is used for the simulations in this article. The thickness of the metal layers was set to 1 μm for all simulation models presented in this article. The CPW line has an IL over 4 dB/mm (1.7 dB/λ_g), the hollow waveguide 0.03 dB/mm (0.03 dB/λ_g) and the proposed Si-SIW 0.33 dB/mm (0.11 dB/λ_g). The Si-SIW thus is expected to have higher losses than a micromachined hollow waveguide, but is more than 3 times smaller in size in all dimension and thus circuits take up to 40 times less volume than in hollow waveguide technology, as illustrated in Fig. 4.

To investigate the contribution of losses in the Si-SIW attributed to the dielectric and the metal circumference, a comparative simulation, shown in Fig. 5, has been performed with lossless or lossy metal (gold, $\sigma = 1.8 \times 10^7$ S/m), and with a silicon resistivity of $\rho_{\text{Si}} = 5000$ Ω·cm or lossless dielectric. To obtain more precise data, the fully 3-D EM simulations with high-density mesh and frequency-dependent parameters were performed. It was found that the metal losses contribute to around 94% of the total insertion loss. The skin depth at 275 GHz is $\delta = 144$ nm, so the total thickness of the metal layer around the silicon core should be at least three times higher, $t_{\text{min}} \geq 450$ nm, so that the metallization thickness starts getting negligible.

B. CPW-to-Si-SIW Transition

Fig. 6 shows the configuration of the CST Microwave Studio simulation model of the CPW-to-Si-SIW transition, including a model of the CPW measurement probe. Fig. 7 shows the layout with optimized dimensions, whose design concept origins from a *W*-band folded slot antenna coupling transition [18]. The transition pattern contains three interdigital coupled lines arranged between side ground planes of a coplanar waveguide (CPW) with various gaps. The ground connection points are moved to the edges of the waveguide which allows fitting a 50-Ω GSG probe with 75-μm pitch size to the transition pattern. The basic principle of operation of the transition was previously described in [22]. Fig. 8 shows the results of the probe's position sensitivity analysis, where the variation of the transition's reflection coefficient is plotted

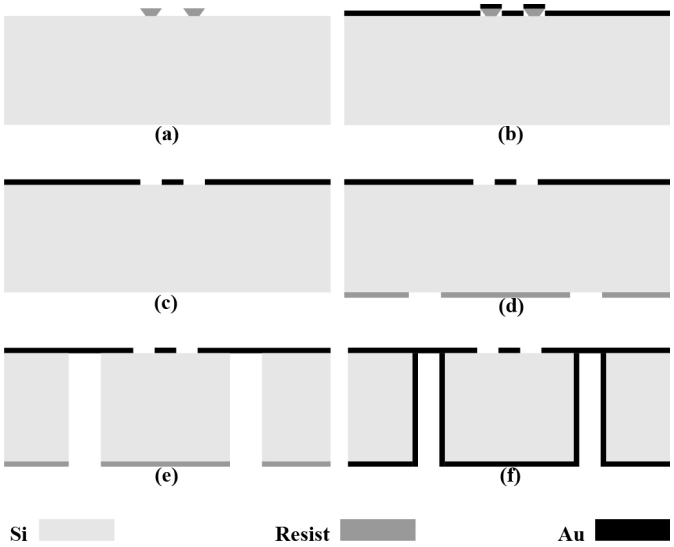

Fig. 9. Fabrication steps. (a) Patterning of the LOR resist. (b) Deposition of the top metal layer to provide the transition pattern. (c) Lift-off process. (d) Soft-mask patterning of the back side for (e) subsequent DRIEtching. (f) Back side metal deposition.

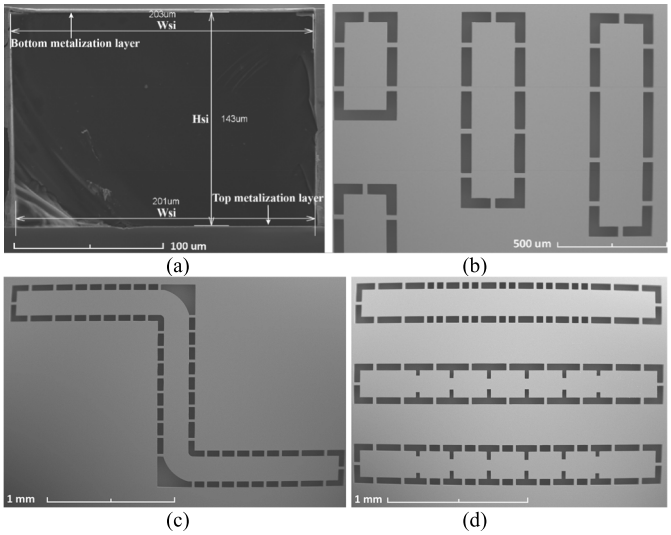

Fig. 10. SEM pictures of fabricated devices. (a) Cross section of the waveguide. (b) Bottom view of waveguides. (c) Waveguide bends. (d) Filters and reference waveguide.

with respect to a probe displacement of 10 μm in x- and y-directions (see Fig 7). Thus, the positioning of the probe is not more critical than for conventional CPW probe pads.

III. Fabrication

Fig. 9 illustrates the process flow, which can be divided into two parts: wafer level processing and chip level processing. To minimize the dielectric losses, high resistivity ($\rho > 5000$ Ω·cm) 150±5 μm thick 100-mm-diameter silicon wafers were used.

The fabrication begins with patterning of the front-side metallization for the CPW-Si-SIW transition structure, by using a lift-off processes with a positive LOR 5A photoresist [see Fig. 9(a)–(c)]. The metallization scheme consists of a 500-nm-thick gold layer on top of a 50-nm chromium adhesion layer. The chromium layer additionally acts as an etch stop for the subsequent deep reactive ion etching (DRIE) step without exposing the gold to the plasma. Then, the back side is patterned [Fig. 9(d)]. Since only 150 μm have to be etched, a soft mask (5 μm) of photoresist is sufficient. Subsequently, to define the trenches of the waveguide walls and separate the wafer into chips, the etching by a DRIE BOSCH process is performed [Fig. 9(e)]. The final step is performed on the chip level and comprises the sputtering of a 2.5-μm-thick layer of gold on the back side, for providing sufficient waveguide sidewall coverage deep into the trenches [Fig. 9(f)].

Fig. 10 shows various SEM pictures of details of the manufactured Si-SIW. The waveguide widths measured on the top and the bottom are 203 and 201 μm, respectively. This difference is attributed to underetching [23], typical for DRIE.

In comparison with previously reported micromachining process flows [18], [19] for substantially lower frequencies, the present solution provides a minimum number of masks and process steps. Moreover, it does not require any bonding, gluing, or substrate transfer steps and is therefore significantly faster, of lower complexity, and more cost efficient.

IV. Measurements

Measurements were performed using a Rohde&Schwarz ZVA24 vector network analyzer with two ZC330 millimeter-wave extenders for 220 to 330 GHz and Picoprobe Model 325B CPW probes.

A. Waveguide

For characterization of the waveguides, an on-chip thru–reflect–line (TRL) calibration kit was designed and implemented. Fig. 11 shows measurement and simulation results of a 5-mm-long ($15.5{\cdot}\lambda_g$) Si-SIW section with distances between the support structures of $D = 270$ and 420 μm. The measured IL for the Si-SIW with $D = 270$ μm at 325 GHz is 0.14 dB/λ_g (0.43 dB/mm), which is only on 30% more than predicted by simulations (0.11 dB/λ_g; 0.33 dB/mm); the corresponding return loss of about 25–30 dB is observed at frequencies not affected by the parasitic resonances. Similar results are observed for $D = 420$ μm. Since it is expected from the simulation results (Section II) that a major part of the losses is attributed to metallic losses, the difference between the simulated and the measured results is assumed to be attributed to the metallization. In particular, the thickness of the side-wall metallization layer is decreasing from top to bottom [12] influenced by the trench width [24], and the surface roughness is increasing close to the bottom part of the side-walls [12]. The quality of metallization can be improved by sputtering a thicker gold layer. Table I compares the measured performance of the proposed Si-SIW platform with other waveguide technology reported in literature. As expected from simulations, for the new Si-SIW platform, the losses per guided wavelength are higher than for any hollow waveguide technology, even though a much higher integration density can be achieved.

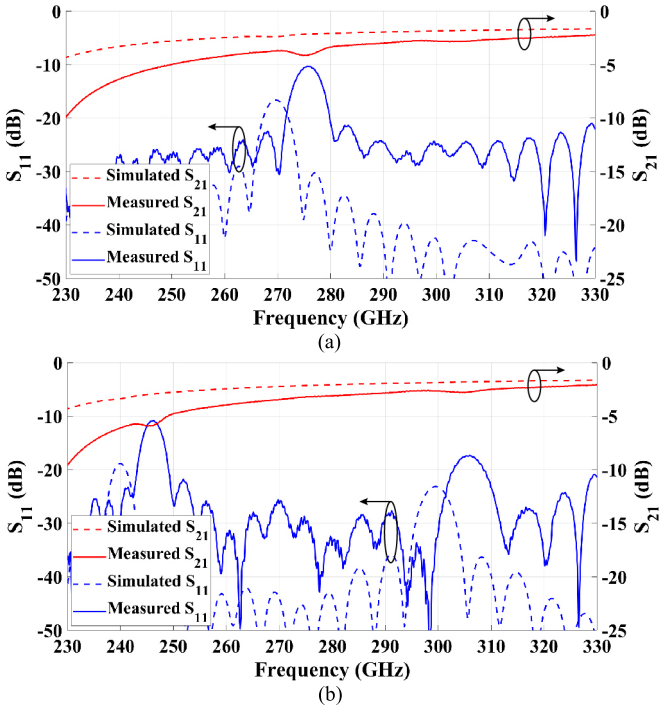

Fig. 11. Measured and simulated S-parameters of 5-mm-long sections of the Si-SIW, after de-embedding the transitions. (a) Support structure periodicity $D = 270$ μm and (b) $D = 420$ μm.

TABLE I

COMPARISON OF MEASURED INSERTION LOSS OF DIFFERENT WAVEGUIDE TECHNOLOGIES

Ref.	Size W×H, μm× μm	Guided wavelength, mm	Freq., GHz	Loss, dB/mm	Loss, dB/λ_g
(this work)	200×150	0.325	325	0.43	0.14
[18]	560×280	1.23	105	0.121	0.15
[3]	864×275	1	325	0.02	0.02
[28]	864×432	1	325	0.03	0.03
[29]	864×432	1	325	0.03	0.03

When comparing the measurement results with the simulations, a clear shift of the resonant frequencies caused by the periodical support structures is visible; this is attributed to the underetching of the width of the waveguide, which is confirmed by the measurements of the manufactured structures. The measured frequency shift can be used for calculation of the actual underetching. Assuming that the distance D between the support structures is uniform, the underetching value can be derived from [21] as follows:

$$\Delta = \frac{c_0}{2 \cdot \sqrt{\varepsilon}} \times \left(\frac{1}{G_1} - \frac{1}{G_2} \right) \tag{1}$$

$$G_k = f_k \cdot \sqrt{1 - \left(\frac{c_0 \cdot n}{2 f_k \cdot D \cdot \sqrt{\varepsilon}} \right)^2}, \quad k = 1, 2 \tag{2}$$

where Δ is the underetching value (see Fig. 12), f_1 is the simulated resonance frequency, f_2 is the measured resonance frequency. The underetching derived for the measured waveguide with $D = 420$ μm is $\Delta = 6$ μm. Furthermore, the fabricated Si-SIWs are subsequently resimulated taking into account the calculated underetching of 6 μm, resulting in a match of the resonances. The presented analytical approach allows estimating the average underetching value with good accuracy and without damaging the devices.

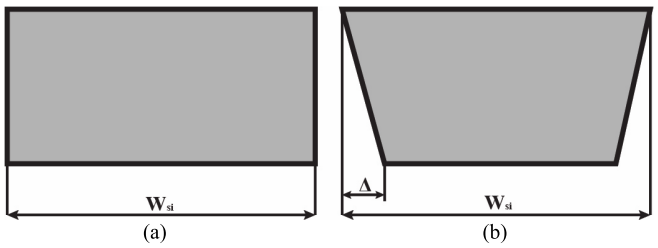

Fig. 12. Cross section of the Si-SIW. (a) Without and (b) with fabrication-induced sidewall underetching.

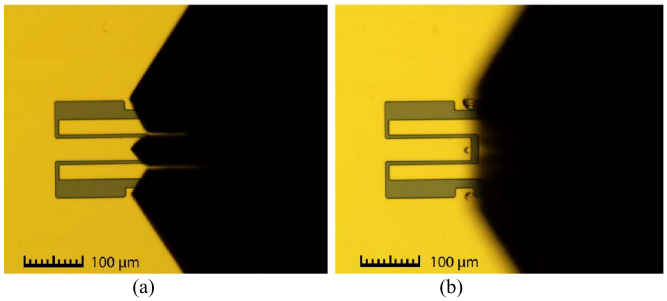

Fig. 13. Microscope pictures. (a) Transition before probing. (b) After probing with a 75-μm pitch GSG probe from GGB industries.

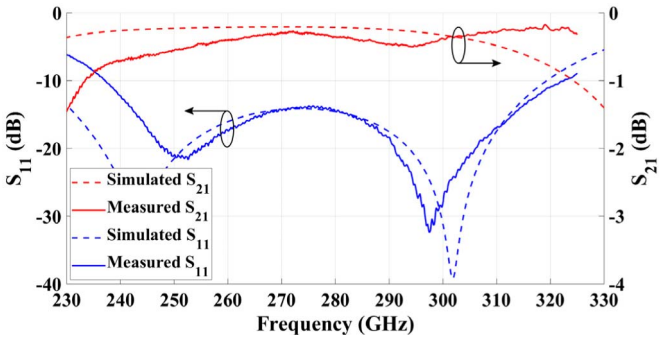

Fig. 14. Measurement results matched to and simulation data of the CPW to waveguide transition alone, measured in a back-to-back configuration and after deembedding the 500-μm-long central waveguide piece.

B. CPW-to-Si-SIW Transition

Fig. 13 shows a photograph of the transition before and after probing. To measure the transitions accurately, the two tier one port calibration method of offset shorts was adopted [25]. The set of offset short standards were manufactured in the same fabrication process and are placed on all chips; hence a high-quality measurement standard was guaranteed.

Fig. 14 shows the measured, compared to the simulated, S-parameters of the CPW-to-Si-SIW transition. The measured IL is better than 0.5 dB for the entire band above 250 GHz (with 250 GHz being 15% above the cut-off frequency, since the waveguide width is narrower than a nominal WM-864 silicon-core waveguide) and averaging to only 0.34 dB over that band. The presented transition has a pole

TABLE II
COMPARISON OF CPW-TO-SIW TRANSITION CHARACTERISTICS

Ref.	Return loss, dB	Frequency range, GHz
(this work)	14	220-330
[18]	15	80-129
[26]	15	40-60
[27]	20	26-40

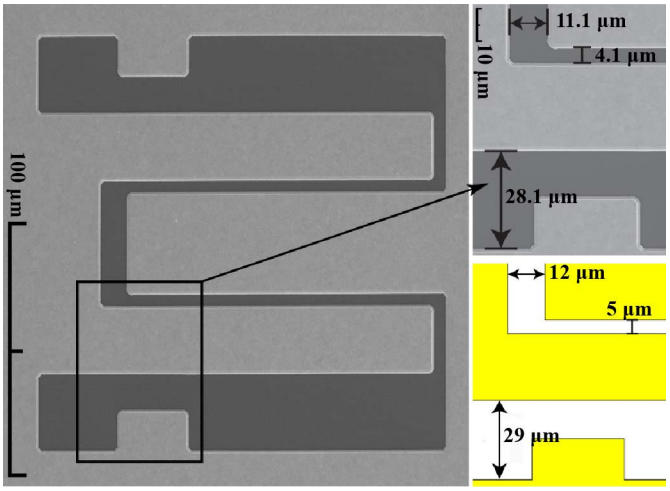

Fig. 15. SEM picture of the fabricated CPW-to-Si-SIW transition; comparison between the measured dimensions as manufactured to the designed dimensions, revealing a feature accuracy of the fabrication process of 0.9 μm.

and a transmission zero at frequencies where the distance from the probe to the back short reaches $\lambda_g/4$ and $\lambda_g/2$ respectively (around 242 GHz and above 330 GHz in the simulated responses in Fig. 14). Due to underetching, the guided wavelengths decreased, so the corresponding frequencies increased by 10–15 GHz. Thus, the measured IL begins to drop towards the transmission zero at about 325 GHz, while the simulated IL drops at lower frequency; this creates the observed difference between the measured and the simulated insertion losses at frequencies over 300 GHz. The measured return loss is below 14 dB for the 240–315-GHz frequency band. Fig. 15 displays an SEM image of the fabricated transition compared to the designed transition. The open areas of the fabricated pattern are approximately 1 μm smaller than expected due to the nonoptimized lift-off process which is assumed to create the small discrepancy between the measured and simulated results in Fig. 13. Table II shows the comparison of the presented CPW-to-Si-SIW transition with previously reported transitions, in any frequency range. It can be seen in the table that the return losses of the transitions are similar. Since the presented transition, based on [15] which was designed for three times lower frequencies, shows a similar return loss and even less insertion loss, it can be concluded that the reported design can be scaled and used at even higher frequencies.

V. INTEGRATED PASSIVE COMPONENTS

A. H-Plane Bends

Fig. 16(a) shows three variations of waveguide bend designs with different outer R_1 and inner R_2 radii in a waveguide

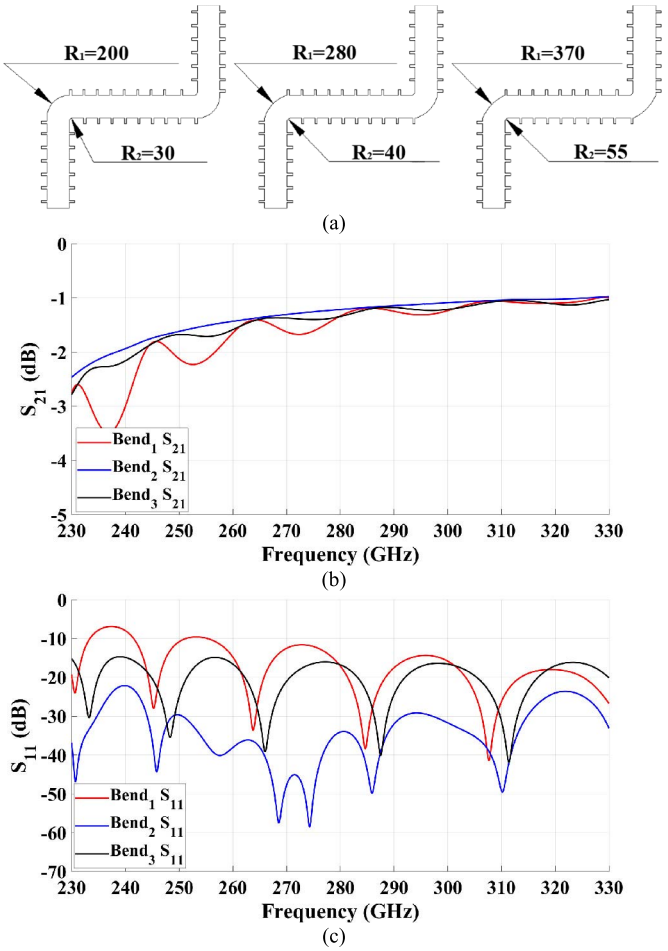

Fig. 16. Parameter variations of the inner and outer radii of waveguide bends, with a support structure periodicity of $D = 120$ μm. (a) Dimensions of the design variations. (b) Simulated insertion loss. (c) Simulated return loss.

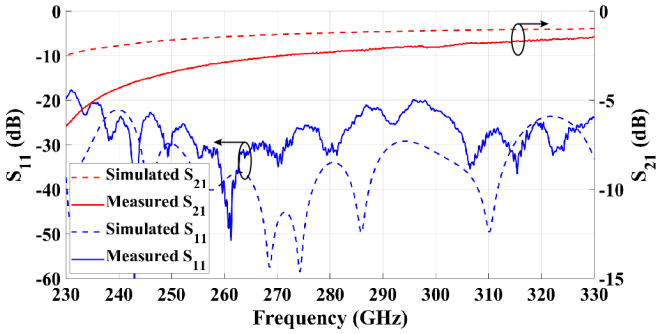

Fig. 17. Measured and simulated S-parameters of a 3-mm-long waveguide piece including two 90° bends of the best-performing bend design with $R_1 = 280$ μm and $R_2 = 40$ μm.

with total length of 3 mm. The distance between the support structures was chosen to be $D = 120$ μm. Fig. 16(b) shows the simulated IL and Fig. 16(c) the return loss for all three configurations. The most promising design, with outer and inner radii $R_1 = 280$ μm and $R_2 = 40$ μm, respectively, was fabricated.

Fig. 17 compares the measured and simulated S-parameters of this design. The measured return loss is 19 dB along

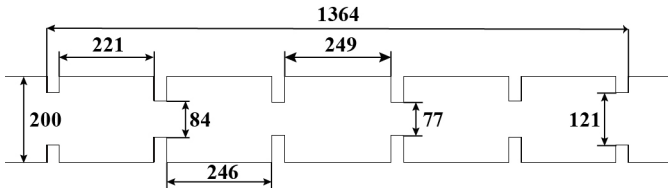

Fig. 18. Configuration of the all-pole fifth-order Si-SIW test filter, with dimensions in μm.

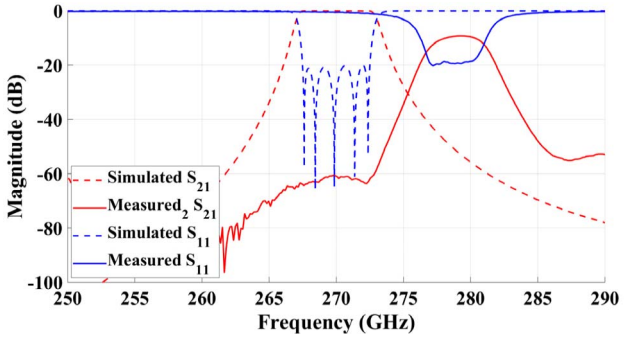

Fig. 19. Simulated and measured S-parameters of the fifth-order Si-SIW's filter.

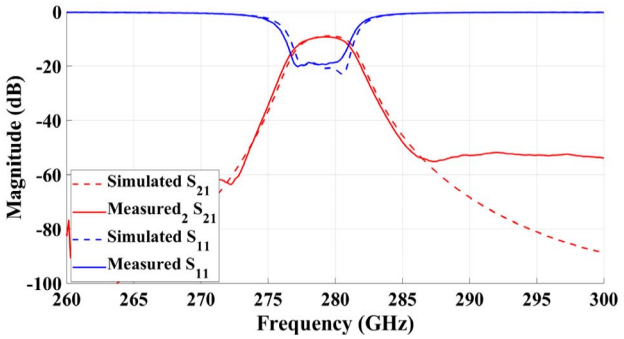

Fig. 20. Experimental response resimulated taking into account the nonverticality of the Si-SIW's sidewalls due to fabrication-induced underetching.

TABLE III

COMPARISON OF Si-SIW FILTER CHARACTERISTICS TO PREVIOUS WORKS ON SIW FILTERS AT SUB-THz FREQUENCIES

Ref.	Technology	f_0, GHz	FBW^*, %	IL, dB	Q^*_U
[33]	LTCC	140	14.3	2.44	70
[34]	TSV	331	15.4	1.5	150
This work	Si-SIW	270	1.85	9.2	200

*FBW – fractional bandwidth, Q_U – unloaded quality factor

the entire band and the IL at 325 GHz is 0.22 dB/λ_g (0.6 dB/mm).

B. Filter

Fig. 18 shows the configuration of an all-pole fifth-order test filter designed for implementation in the proposed fabrication platform. The filter structure is symmetric with respect to the middle point and consists of five waveguide resonators directly coupled through six inductive irises. The filter was designed and optimized through an aggressive space mapping (ASM) procedure [30] using a surrogate model built in MATLAB [31] and a high-fidelity model created in CST Microwave Studio [32] with respect to the following specifications:

1) center frequency: $f_0 = 270$ GHz.
2) bandwidth: BW $= 5$ GHz.
3) maximum return loss in passband: 20 dB.

The experimental results of the filter are compared to the simulation results in Fig. 19. The measured response is shifted in frequency by about 9 GHz with respect to the simulation; the return loss in the passband is slightly decreased from 20.3 to 18.5 dB in the frequency range of 277–280.1 GHz, making the measured bandwidth by 1.9 GHz narrower than simulated; the best IL in the passband is about 9.2 dB. It was estimated from the measured S-parameters that the obtained unloaded quality factor of a single resonator in this filter is about 200. The transmission zeros at 261, 272, and 287 GHz in the experimental response are assumed to appear due to interaction with the probes during the measurement procedure.

The reason for the shifting and shrinking of the passband was found to happen because of nonverticality of the filter's sidewalls due to underetching. This affects the effective width of the waveguide, lengths of the resonators, as well as width of windows in all the irises, thus making them smaller than designed. In order to confirm the reason for the failure, the filter model was updated to account for the nonverticality of the sidewalls, and the results agree very well with the experimental response for the measured underetching value of 6.2 μm in the vicinity of the measured passband (see Fig. 20).

Table III compares the presented filter with other sub-THz SIW filters available in the literature up to date. The present work presents for the first time much more narrow-band filter demonstrators (by a factor of 7.7), even at significantly better unloaded Q-factors than these other SIW technologies.

VI. CONCLUSION

This article has reported on a new technology platform for creating highly integrated sub-THz systems—the micromachined silicon-core SIW. The performance of the platform at 220–330 GHz has been demonstrated by experimental verification of waveguide sections, a CPW-to-Si-SIW transition, and several passive components, including H-plane bends and filters. The obtained measurement results, in particular the IL of the waveguide of 0.14 dB/λ_g (0.43 dB/mm) at 325 GHz and the insertion and return losses of the transitions of 0.34 and 14 dB, are in a reasonable agreement with the simulation results. The influence of the support structures on the performance of the devices was studied and proven by the experimental measurements. Moreover, the presented process flow shows the potential of the platform to high-volume, low-cost, and fast batch fabrication of highly integrated sub-THz frequency systems.

REFERENCES

[1] H.-J. Song and T. Nagatsuma, "Present and future of terahertz communications," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 256–263, Sep. 2011.

[2] A. R. Kerr, C. Litton, G. Petencin, D. Koller, and M. Shannon, "Loss of gold plated waveguide at 210–280 GHz," *Alma Memo*, vol. 585, pp. 1–6, Jan. 2009.
[3] B. Beuerle, J. Campion, U. Shah, and J. Oberhammer, "A very low loss 220–325 GHz silicon micromachined waveguide technology," *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 2, pp. 248–250, Mar. 2018.
[4] K. M. K. H. Leong *et al.*, "WR1.5 silicon micromachined waveguide components and active circuit integration methodology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 998–1005, Apr. 2012.
[5] C. Jung-Kubiak *et al.*, "A multistep DRIE process for complex terahertz waveguide components," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 5, pp. 690–695, Sep. 2016.
[6] J. Svedin, R. Malmqvist, B. Beuerle, U. Shah, and J. Oberhammer, "A 230–300 GHz low-loss micromachined waveguide hybrid coupler," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Oct. 2017, pp. 616–619.
[7] C. A. Leal-Sevillano *et al.*, "Silicon micromachined canonical E-plane and H-plane bandpass filters at the terahertz band," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 6, pp. 288–290, Jun. 2013.
[8] O. Glubokov, X. Zhao, J. Campion, U. Shah, and J. Oberhammer, "Micromachined filters at 450 GHz with 1% fractional bandwidth and unloaded q beyond 700," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 106–108, Jan. 2019.
[9] A. Gomez-Torrent, U. Shah, and J. Oberhammer, "Compact silicon-micromachined wideband 220–330-GHz turnstile orthomode transducer," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 38–46, Jan. 2019.
[10] M. Alonso-delPino, T. Reck, C. Jung-Kubiak, C. Lee, and G. Chattopadhyay, "Development of silicon micromachined microlens antennas at 1.9 THz," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 2, pp. 191–198, Mar. 2017.
[11] A. Gomez-Torrent *et al.*, "A low-profile and high-gain frequency beam steering subterahertz antenna enabled by silicon micromachining," *IEEE Trans. Antennas Propag.*, vol. 68, no. 2, pp. 672–682, Feb. 2020.
[12] U. Shah *et al.*, "A 500–750 GHz RF MEMS waveguide switch," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 3, pp. 326–334, May 2017.
[13] U. Shah *et al.*, "Submillimeter-wave 3.3-bit RF MEMS phase shifter integrated in micromachined waveguide," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 5, pp. 706–715, Sep. 2016.
[14] M. Bozzi, A. Georgiadis, and K. Wu, "Review of substrate-integrated waveguide circuits and antennas," *IET Microw., Antennas Propag.*, vol. 5, no. 8, pp. 909–920, Jun. 2011.
[15] H.-Y. Jin, G.-J. Wen, and Y.-B. Jin, "A novel spatial power combiner based on SIW and HMSIW," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 2008, pp. 233–236.
[16] D. Stephens, P. R. Young, and I. D. Robertson, "Millimeter-wave substrate integrated waveguides and filters in photoimageable thick-film technology," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 12, pp. 3832–3837, Dec. 2005.
[17] M. Bozzi, L. Perregrini, and K. Wu, "Modeling of conductor, dielectric, and radiation losses in substrate integrated waveguide by the boundary integral-resonant mode expansion method," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 3153–3161, Dec. 2008.
[18] G. Gentile *et al.*, "Silicon-filled rectangular waveguides and frequency scanning antennas for mm-wave integrated systems," *IEEE Trans. Antennas Propag.*, vol. 61, no. 12, pp. 5893–5901, Dec. 2013.
[19] V. Jovanovic *et al.*, "Silicon-based technology for integrated waveguides and mm-wave systems," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3153–3159, Oct. 2015.
[20] A. Krivovitca, U. Shah, O. Glubokov, and J. Oberhammer, "Micromachined silicon-core substrate-integrated waveguides with co-planarprobe transitions at 220–330 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 190–193.
[21] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ, USA: Wiley, 2012.
[22] G. Gentile, B. Rejaei, V. Jovanovic, L. K. Nanver, L. C. N. de Vreede, and M. Spirito, "Ultra-wide band CPW to substrate integrated waveguide (SIW) transition based on a U-shaped slot antenna," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Oct. 2013, pp. 25–28.
[23] O. Glubokov, X. Zhao, J. Campion, B. Beuerle, U. Shah, and J. Oberhammer, "Investigation of fabrication accuracy and repeatability of high-Q silicon-micromachined narrowband sub-THz waveguide filters," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3696–3706, Sep. 2019.
[24] C.-G. Kim and W.-J. Lee, "Quantitative study on the enhancement of sidewall coverage of sputter-deposited film by partially tapering the sidewall of via holes," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 29, no. 2, Mar. 2011, Art. no. 020604.
[25] T. J. Reck *et al.*, "Micromachined probes for submillimeter-wave on-wafer measurements—Part II: RF design and characterization," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 2, pp. 357–363, Nov. 2011.
[26] A. Patrovsky, M. Daigle, and K. Wu, "Millimeter-wave wideband transition from CPW to substrate integrated waveguide on electrically thick high-permittivity substrates," in *Proc. Eur. Microw. Conf.*, Oct. 2007, pp. 138–141.
[27] X.-P. Chen and K. Wu, "Low-loss ultra-wideband transition between conductor-backed coplanar waveguide and substrate integrated waveguide," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 349–352.
[28] X. Shang, M. Ke, Y. Wang, and M. J. Lancaster, "WR-3 band waveguides and filters fabricated using SU8 photoresist micromachining technology," *IEEE Trans. THz Sci. Technol.*, vol. 2, no. 6, pp. 629–637, Nov. 2012.
[29] J.-Q. Ding, S.-C. Shi, K. Zhou, Y. Zhao, D. Liu, and W. Wu, "WR-3 band quasi-elliptical waveguide filters using higher order mode resonances," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 3, pp. 302–309, May 2017.
[30] M. H. Bakr, J. W. Bandler, R. M. Biernacki, S. H. Chen, and K. Madsen, "A trust region aggressive space mapping algorithm for EM optimization," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 12, pp. 2412–2425, 1998.
[31] *MATLAB*, MathWorks, Inc, Natick, MA, USA, 2014.
[32] *CST Microwave Studio*, Comput. Simul. Technol. AG, Darmstadt, Germany, 2016.
[33] K. Wang, S.-W. Wong, G.-H. Sun, Z. Ning Chen, L. Zhu, and Q.-X. Chu, "Synthesis method for substrate-integrated waveguide bandpass filter with even-order chebyshev response," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 1, pp. 126–135, Jan. 2016.
[34] F. Wang, V. F. Pavlidis, and N. Yu, "Miniaturized SIW bandpass filter based on TSV technology for THz applications," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 4, pp. 423–426, Jul. 2020.

Aleksandr Krivovitca was born in Stary Oskol, Russia, in 1991. He received the B.S. degree in electronics and nanoelectronics and the M.Sc. degree (Hons.) in electronics and nanoelectronics, nano- and microsystem technology from Saint Petersburg Electrotechnical University "LETI," Saint Petersburg, Russia, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree at the Micro and Nanosystems Group, KTH Royal Institute of Technology, Stockholm, Sweden.

His research interests include substrate integrated waveguide (SIW) platform development at RF/microwave/millimeter-wave/THz frequency ranges, design of passive, and MEMS-based sub-THz devices.

Umer Shah (Member, IEEE) was born in Bannu, Pakistan, in 1981. He received the B.S. degree in engineering from the Ghulam Ishaq Khan Institute of Engineering Sciences and Technology, Topi, Pakistan, in 2003, the M.Sc. degree in wireless engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2007, and the Ph.D. degree in microsystem technology from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2014.

Since May 2014, he has been a Post-Doctoral Researcher with the Micro and Nanosystems Group, KTH Royal Institute of Technology. He has authored or coauthored more than 30 reviewed articles. His research interests include RF MEMS-based filters, phase shifters, matching circuits, and antennas.

Dr. Shah was a recipient of the Best Student Paper Award presented at the Asia–Pacific Microwave Conference 2010, Yokohama, Japan, and the 2014 IEEE MTT-S Graduate Fellowship Award for his research activities.

Oleksandr Glubokov (Member, IEEE) was born in Kiev, Ukraine, in 1985. He received the M.Sc. degree in telecommunications from the National Technical University of Ukraine (KPI), Kiev, in 2007, and the Ph.D. degree in electronic and electrical engineering from the University of Westminster, London, U.K., in 2011.

From 2012 to 2014, he was a Post-Doctoral Research Fellow with Reykjavík University, Reykjavík, Iceland. Since 2015, he has been a Post-Doctoral Researcher of MEMS THz systems project with Micro- and Nanosystems at the KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include filter design at RF/microwave/millimeter-wave/terahertz (THz) frequency ranges, passive sub-THz devices, and their numerical optimization.

Joachim Oberhammer (Senior Member, IEEE) was born in Italy in 1976. He received the M.Sc.EE degree from the Graz University of Technology, Graz, Austria, in 2000, and the Ph.D. degree from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2004.

He was a Post-Doctoral Research Fellow with Nanyang Technological University, Singapore, in 2004, and Kyoto University, Kyoto, Japan, in 2008. Since 2005, he has been leading radio frequency/microwave/terahertz microelectromechanical systems research at the KTH Royal Institute of Technology. In 2010, he was an Associate Professor with the KTH Royal Institute of Technology, where he has been a Professor of microwave and terahertz (THz) microsystems since 2015. He was a Guest Researcher with Nanyang Technological University, Singapore, in 2007, a Guest Researcher with the NASA-Jet Propulsion Laboratory, Pasadena, CA, USA, in 2014, and a Guest Professor with the Universidad Carlos III de Madrid, Madrid, Spain, in 2019. He has authored or coauthored more than 100 reviewed research articles and holds four patents.

Dr. Oberhammer served as a TPRC Member for the IEEE Transducers in 2009, 2015, and 2019, the IEEE International Microwave Symposiums from 2010 to 2018, the IEEE Micro Electromechanical Systems in 2011 and 2012, the IEEE Radio and Wireless Week in 2015 and 2016, and EuMCE in 2019. He has been a Steering Group Member of the IEEE MTT-S and AP-S Chapters Sweden since 2009. He was a Steering Group Member of the Young Academy of Sweden from 2014 to 2016. He received an award by the Ericsson Research Foundation, a grant by the Swedish Innovation Bridge, and a scholarship by the Japanese Society for the Promotion of Science in 2004, 2007, and 2008, respectively. The research work that he is heading received six best paper awards (five of which at IEEE conferences) and four IEEE Graduate Fellowship Awards (by MTT-S and by AP-S) since 2009. In 2013, he received an ERC Consolidator Grant by the European Research Council. He was a Representative of Sweden/Norway/Iceland in the European Microwave Association from 2016 to 2018. He has been an Associate Editor of the IEEE TRANSACTIONS ON TERAHERTZ SCIENCE AND TECHNOLOGY since 2018.