Multi-port Active Load Pulling for mm-Wave 5G Power Amplifiers: Bandwidth, Back-Off Efficiency, and VSWR Tolerance

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***Abstract*— The opening of spectral bands in the millimeter-wave (mm-Wave) spectrum from 26 GHz and extending up to the E-band poses new challenges to the power amplifier (PA) design for spectrally agile radios. They are expected to operate with high energy efficiency at peak and back-off levels to process signals with high peak-to-average power ratio (∼10 dB), while being able to maintain their performance across a wide range of 5G bands. In addition, the PAs can experience strong load impedance mismatch conditions in a user equipment (UE) that pose additional challenges in handling strong voltage-standing-wave-ratio (VSWR) events. In this article, we present a systematic approach to exploit active load pulling in a multi-port network that synthesizes optimal impedance conditions for 1) broadband peak and back-off operation and 2) mitigating VSWR events at peak power. As proofs of concept, we present two PAs in 65-nm bulk CMOS process. The first chip demonstrates P_{sat} between 16.3 and 19.3 dBm across 37–73 GHz, with an improvement in the output drain efficiency (η_{out}) of up to 3.2×/5.8× at 6-/9.6-dB power back-off (PBO) across the frequency range compared to class-A operation. The second chip achieves 26–42-GHz $P_{sat,\,-1\,dB}$ bandwidth with $P_{sat} > 19$ dBm and $PAE_{peak} > 20\%$ across all 28–40-GHz bands and with up to 3.35× and 4.84× enhancement in PAE at the PBO levels of 6 and 9.6 dB over class-A operation, respectively. The PA also demonstrates strong tolerance to VSWR events with only 2 dB degradation over a VSWR 4:1 load circle at a frequency of 33 GHz.**

***Index Terms*— Back-off, broadband, DAC, 5G, load impedance mismatch, load–pull, millimeter wave (mm-Wave), power amplifier (PA), power combining, voltage-standing-wave-ratio (VSWR).**

I. Introduction

FIFTH-GENERATION (5G) communication systems promise a significant amount of data capacity and quality of service to support advanced modulation schemes. The third-generation partnership project (3GPP) has dubbed 5G's new air interface as 5G new radio (NR) that divides the band into two frequency ranges: FR1 that operates below 6 GHz and FR2 that includes bands above 24 GHz and extending into the range above 50 GHz. As of now, the 5G NR specifies numerous bands at mm-Wave frequencies, such as n257, 28-GHz band (26.5–29.5 GHz) and n260, 38-GHz band (37–40) GHz. The proliferation of this spectrum demands new spectrally-agile power amplifiers (PAs) that can support energy-efficient operation at peak and back-off across the broad spectrum, while being tolerant to load impedance mismatches operating in complex electromagnetic environment [1], [2].

For PAs, energy efficiency and bandwidth typically tradeoff with each other [3], [4]. In addition, mm-Wave propagation and antenna properties can be significantly affected by blockage and by the presence of human body [1], [5]. The above-mentioned factors lead to strong tradeoffs among output power generation, back-off efficiency, bandwidth, and voltage-standing-wave-ratio (VSWR) tolerance. While prior works [6]–[33] have shown the capability of broadband and efficient silicon-based PAs enabling multiband operation from 37 GHz and extending up to 73 GHz with high back-off efficiency across the band is still very challenging. In addition, mitigation of load impedance mismatches in a complex near-field environment is nontrivial.

In this article, we propose a systematic method to exploit active load pulling in a multi-port combiner to simultaneously allow broadband and high back-off efficiency operation, and VSWR tolerance at peak power [see Fig. 1(a)]. The tradeoffs between peak power, bandwidth, and achievable back-off efficiency are shown in Fig. 1(b)–(d). Wideband PAs can achieve broadband operation with optimal impedances at the peak power (albeit with less efficient multiorder matching networks), but suffer from low efficiency at back-off due to suboptimality of the presented impedance [see Fig. 1(b)] [21]–[24]. The newly proposed waveform-engineered continuous-mode PAs are promising candidates in terms of achievable bandwidth, but the operation is often limited to peak power levels with a relatively low back-off efficiency [25]–[27]. On the contrary, load modulation architectures can provide high back-off efficiency but suffer from lower fractional bandwidth, as shown in Fig. 1(c). Prior works have demonstrated transformer-based Doherty PAs at mm-Wave, but over a limited frequency range of operation [28]–[34]. A PA architecture that can be reconfigured simultaneously across frequency and power back-off (PBO) levels is, therefore, very challenging [see Fig. 1(d)].

Manuscript received August 10, 2019; revised November 15, 2019; accepted December 30, 2019. Date of publication April 10, 2020; date of current version July 1, 2020. This work was supported by the SRC Global Research Collaboration (GRC), in part by the Texas Analog Center of Excellence (TxAce), Office of Naval Research, Defense Advanced Research Projects Agency (DARPA), and in part by the Qualcomm Innovation Funding (QinF). *(Corresponding author: Tushar Sharma.)*

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Digital Object Identifier 10.1109/TMTT.2020.2977342

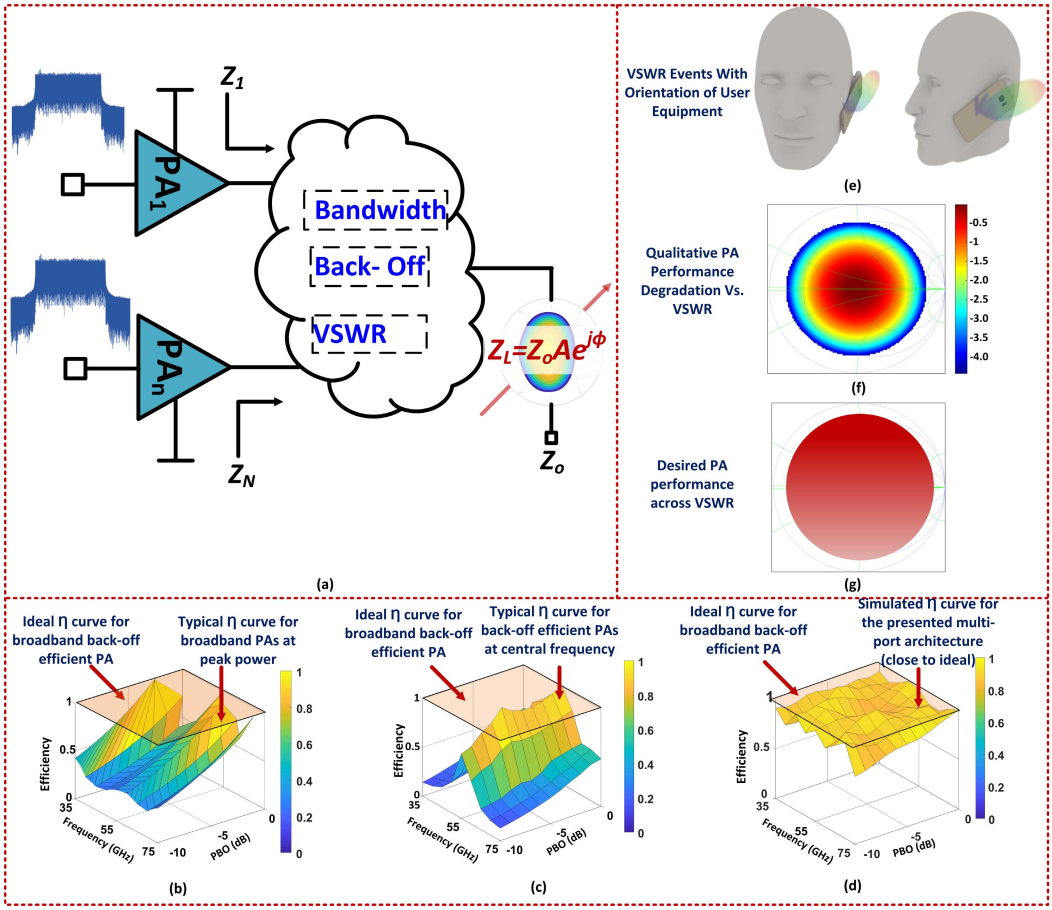

Fig. 1. Multi-port PA architecture for broadband, back-off efficient operation and VSWR tolerance exploiting controlled active loadpulling. (a) $(N+1)$-port PA architecture. Efficiency curve (η) against power and frequency for (b) broadband PA at peak power, (c) back-off efficient PA at center frequency, and (d) presented multi-port architecture. (e) Load mismatch or VSWR event in an UE. (f) Qualitative description of PA performance degradation against VSWR event. (g) Desired VSWR reconfigurability across VSWR events.

In addition to energy and spectral efficiencies, VSWR tolerance is also an important characteristic for 5G mmWave PAs. Various factors, including but not limited to blockage of mm-Wave chipset by the position of the hand in landscape or portrait mode, as shown in Fig. 1(e), impact the loading at the PA output. These load variations present suboptimal impedance at the output of each PA cell, which drastically degrades the performance, as shown in Fig. 1(f). In addition to large-signal performance considerations, to best of our knowledge, no prior work has shown compensation of load mismatch effects along with broadband operation in the mm-Wave band [35], [36]. In an ideal scenario, these mm-Wave front ends desire to be VSWR agile or self-healing where efficiency is immune to load mismatch conditions, as shown in Fig. 1(g) [41].

The key aspect to allow efficient operation across all these three parameters is being able to synthesize the optimal impedances in a controlled fashion. In this article, we present a generalized approach toward this by exploiting active load pulling through controlled interactions among an array of mm-Wave DACs in a systematically designed combiner network. We show that in an N-way combiner, unlike Doherty or our previous work [37], the concept of main and auxiliary PAs can be eliminated to allow a more fine-grained distribution of power across back-off and frequency leading to energy-efficient and spectrally efficient multiband operation.

We present two different prototypes in a 65-nm bulk CMOS technology. For frequency and back-off adaptability, a scalable three-stage, four-way PA with a self-similar Γ-conjugate architecture is implemented. The PA operates across 37–73 GHz generating P_{sat} between 16.3 and 19.3 dBm with an improvement in output drain efficiency (η_{out}) of up to 3.2×/5.8× enhancement at 6-/9.6-dB PBO across the range compared to the class-A operation. The second-level application of the proposed architecture for VSWR agility is demonstrated using a differential two-way combiner that operates across 26–42 GHz. The PA compensates for antenna load variations of up to 4:1 VSWR through active impedance synthesis at a frequency of 33 GHz.

This article is broadly divided into two major parts, one focusing on broadband back-off efficiency enhancement and second part on VSWR tolerance. A simplified two-way combiner example is introduced in Section II to explain the core properties of the proposed architecture. Section III presents the proposed architecture for frequency and back-off reconfigurability. Section IV discusses the analytical framework for the VSWR-agile operation of PA. Thereafter, the implementation of wideband back-off efficiency PA in

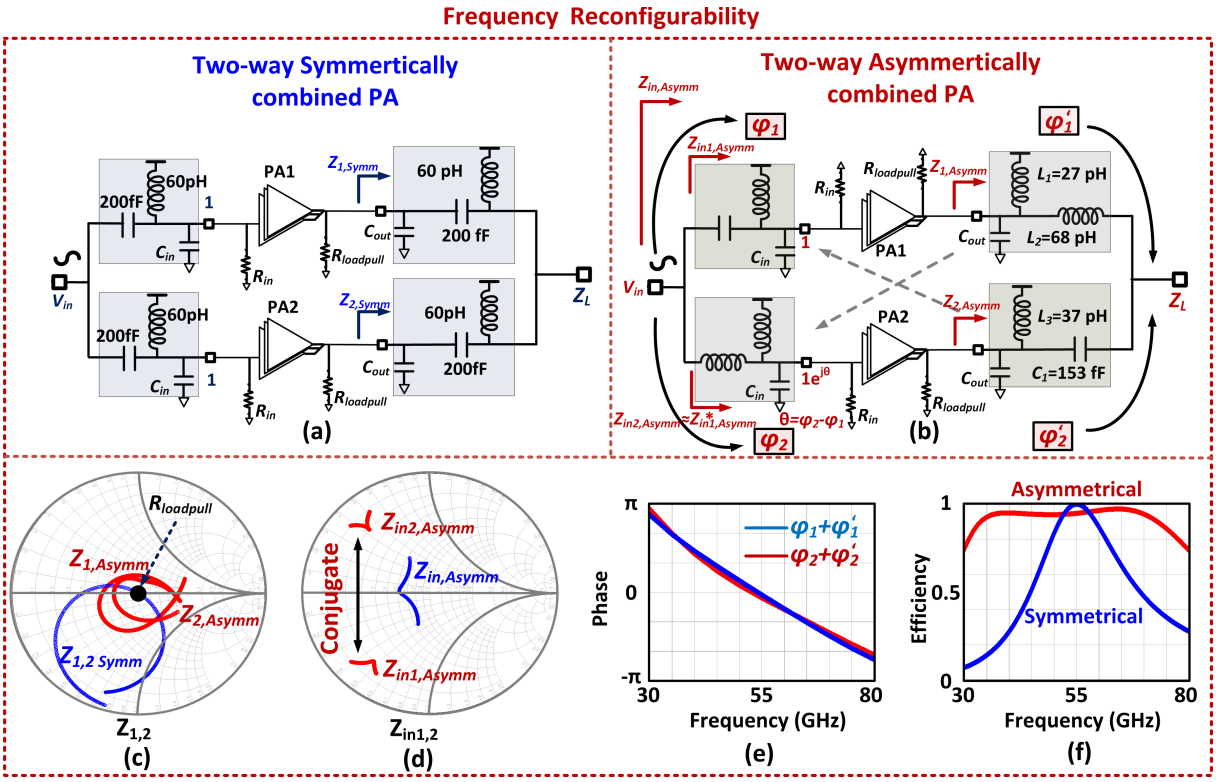

Fig. 2. DAC-based two-way combiner PA for frequency reconfigurability. (a) Symmetrically combined PA. (b) Asymmetrically combined PA. (c) Impedances seen by each PA in the symmetrical and asymmetrical configurations. (d) Input impedances looking into each branch of the asymmetrically combined PA. (e) Phase compensations for the two branches to add coherently at the output load. (f) Efficiency comparison of (a) and (b).

a 65-nm bulk CMOS process is presented in Section V. Section VI presents the VSWR agility of the proposed architecture followed by conclusions in Section VII.

II. Unified Combiner Network Synthesis Approach

Here, in this section, we present an intuitive approach for an example two-way combiner network to illustrate the methodology of exploiting active load pulling for frequency, back-off, and VSWR. While some of our prior works ([37]–[44]) have demonstrated the aspects of this technique, here, we present a unified approach in a step-by-step fashion to synthesize optimal input and output combining networks for bandwidth, back-off efficiency, and VSWR tolerance.

A. Bandwidth: Multi-order Network Synthesis Through Power Combining

Power combining is central to mm-Wave power generation due to the limited output power from a single device. The input and output matching in such a case is typically achieved with passive networks, the order of which determines the bandwidth of the operation. An example of symmetric PA is shown in Fig. 2(a) with input and output combiner comprised of second-order networks (designed with lossless passives) for 65-nm CMOS transistors. The PA produces 20-dBm peak output power at the center frequency of 55 GHz. Due to the symmetry of the network, the impedances seen by the PAs are identical, i.e., $Z_{1,\mathrm{Symm}} = Z_{2,\mathrm{Symm}}$ that represent the optimal load–pull impedances at the designed frequency of 55 GHz. The impedances deviate from R_{loadpull} significantly at other frequencies limiting bandwidth, as shown in Fig. 2(c). Broadband operation where $Z_{1,\mathrm{Symm}} = Z_{2,\mathrm{Symm}}$ closely follows R_{loadpull} can be achieved with multi-order networks at the expense of efficiency.

The symmetry of the network completely overlooks the possibility of establishing a quasi-higher order network through signal combination and active load pulling. An example is shown Fig. 2(b), where two phase-offset PAs combine through two second-order networks designed as an asymmetric Γ-conjugated combiner to produce the same output power of 20 dBm. By breaking the symmetry of the network, the combiner behaves as a quasi-fourth-order network due to active load pulling at peak power. The proposed input and output branch networks have two demonstrative features that establish a foundation for high combining efficiency over a broadband range.

First, the impedance transformation is not achieved individually in each branch of the network to transform 100 Ω to R_{loadpull}, such as in Fig. 2(a). It is through the interactions that the optimal impedance is synthesized. The approach to design the combining network is shown in Fig. 2(b), which shows the conjugate nature of the reflection coefficients at the center frequency of 55 GHz in each branch as observed from the output port. This allows the impedances ($Z_{1,\mathrm{Asymm}}$, $Z_{2,\mathrm{Asymm}}$) to follow closely to R_{loadpull} across 30–80 GHz, even with a second-order in each branch [see Fig. 2(c)].

Second, broadband input matching is also established reciprocally. In a manner similar to the output, the input impedances of PA1 ($Z_{\mathrm{in1,Asymm}}$) and PA2 ($Z_{\mathrm{in2,Asymm}}$) are different (conjugate at the center frequency of 55 GHz), and combines together

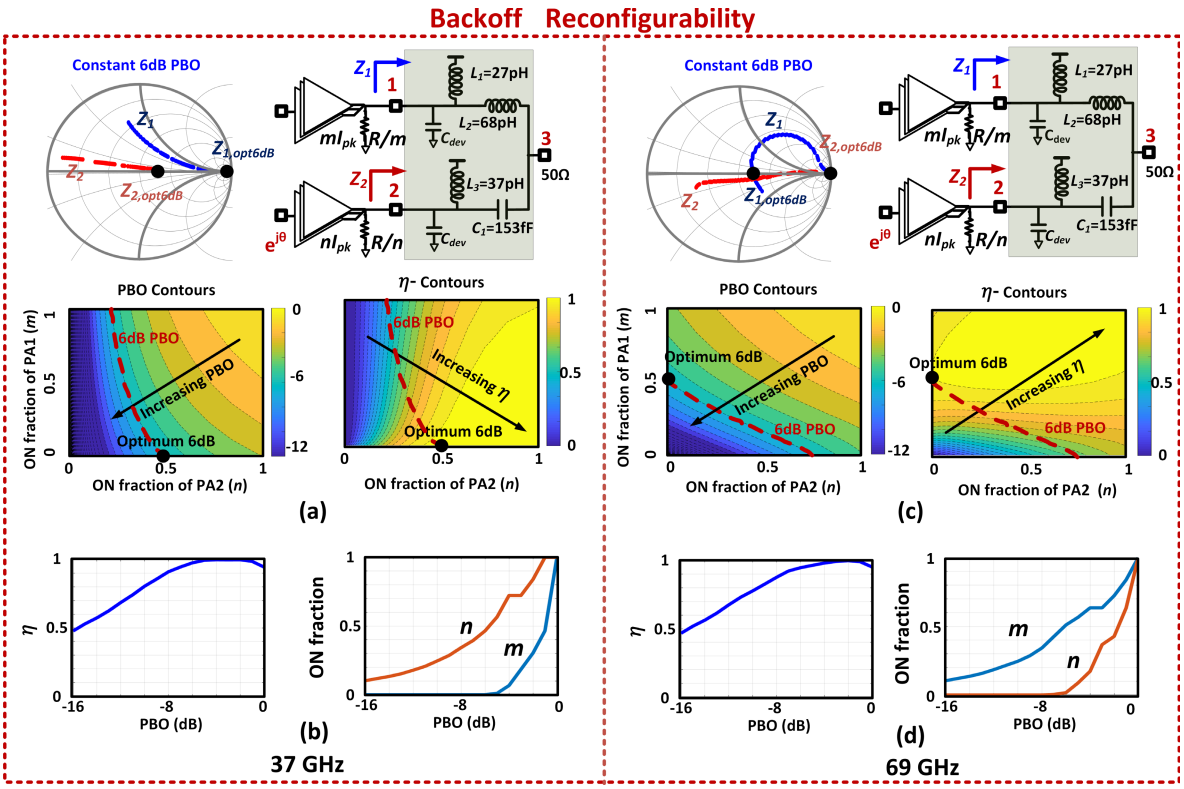

Fig. 3. DAC-based two-way combiner PA for back-off reconfigurability across frequencies. (a) Efficiency and power contours across the combinations of (m, n) at 37 GHz. (b) Achievable efficiency and on-fractions for optimum operation across PBO levels at 37 GHz. (c) Efficiency and power contours for 69 GHz. (d) Achievable efficiency and on-fractions for optimum operation across PBO levels at 69 GHz.

to provide broadband response, as shown in Fig. 2(d). The optimal phase offset for the PAs to combine in the Γ-conjugate combiner is also established at the input by interchanging the topology of the networks from the output to the input. This simultaneously establishes broadband input matching while ensuring optimal phase synthesis (θ) and equality of total phase ($\phi_1 + \phi_1' = \phi_2 + \phi_2'$) across both branches over the frequency range, as shown in Fig. 2(e). The small-signal combining efficiency ($\eta = P_{\text{out, max}}/P_{\text{avs}} = ((||S_{31}| + |S_{32}||^2)/2)$) is plotted in Fig. 2(f) across 30–80 GHz for both symmetric and asymmetric networks. As can be seen, the asymmetric nature of architecture achieves simultaneously high efficiency and high bandwidth when compared with the symmetrical architectures. This provides a strong framework for mm-Wave multi-port network synthesis.

B. Broadband Back-Off Reconfigurability

Keeping the same asymmetric network as explained in the previous section, the back-off reconfigurability is exploited using interaction between mm-Wave asymmetrically coded DAC cells [see Fig. 3(a)]. The various back-off power levels (PBO) are generated through the choice of the codes m and n that represent the fraction of the PA cells switched ON. The efficiency at a given PBO then depends on the optimality of impedance synthesis at that given power level. The goal is to choose optimal codes (m, n) to generate the desired output power with maximum efficiency at different frequency bands. We will demonstrate that, through optimal choices of frequency dependent (m, n), efficient back-off operation can be synthesized by mimicking a frequency reconfigurable Doherty-like operation.

As shown in Fig. 3(a), the two different PA cells can be represented in a simplistic way with load impedances of R/m and R/n, where m and n represent on-fraction of PA1 and PA2, respectively. For ease of analysis, we employ a linear circuit analysis to capture the efficiency degradation as the impedances deviate from optimality. This qualitatively captures the efficiency degradation under voltage and current saturation in a PA operation as well. For a three-port broadband asymmetric combing network, we define the efficiency as $\eta = P_{\text{out}}/P_{\text{avs}}$, where $P_{\text{avs}} = (mI_{\text{pk}}/2)^2 \cdot (R/m) + (nI_{\text{pk}}/2)^2 \cdot (R/n)$, $m \leq 1$ and $n \leq 1$ and I_{pk} is the peak current of the device.

This power transfer efficiency of the network for any back-off level (or code (m, n)), that represents how close the impedances are to the optimal, can also be calculated using the scattering parameters $(S^{m,n})$ of the network defined with the reference impedances R/m, R/n, and Z_o. For any given code (m, n), the efficiency at back-off level (PBO) can be shown to be

$$\eta = f_{\text{PBO}}(m, n, S^{m,n}) = \frac{\left||S_{31}{}^{m,n}|\sqrt{m} + |S_{32}{}^{m,n}|\sqrt{n}\right|^2}{m+n} \quad (1)$$

Similarly, the normalized output PBO level can be derived as

$$\begin{aligned}\text{PBO} = g_{\text{PBO}}(m, n, S^{m,n}) &= (m+n)\, f_{\text{PBO}}(m, n, S) \\ &= \left||S_{31}{}^{m,n}|\sqrt{m} + |S_{32}{}^{m,n}|\sqrt{n}\right|^2\end{aligned} \quad (2)$$

where $g_{\text{PBO}}(m, n, S^{m,n})$ is the achievable output PBO.

Using (1) and (2), the efficiency and power at a given back-off can be plotted as a function of continuously varying m and n, as shown in Fig. 3. There are several codes given by combination of m and n for a given back-off level (say 6 dB), as shown by the red traces in Fig. 3(a) and (c). These code combinations present a wide range of impedances for two different PA cells (noted as Z_1 and Z_2), respectively, some of which are efficient and some are not. The optimal pair (m, n), which provides maximum efficiency for a given back-off level $\text{PBO}_{\text{given}}$, can be solved to be

$$\begin{aligned} \frac{\partial f_{\text{PBO}}}{\partial m} &\approx 0 \\ \frac{\partial f_{\text{PBO}}}{\partial n} &\approx 0 \\ |g_{\text{PBO}}(m, n, S^{m,n}) - \text{PBO}_{\text{given}}| &< \epsilon \end{aligned} \tag{3}$$

where ϵ is the tolerable error bound between the desired back-off level and achieved power level.

As shown in the example in Fig. 3(a), the PBO and efficiency contours are plotted as a function of m and n. Here, the optimum efficiency can be achieved for $m = 0$ and $n = 0.5$. This implies that at 37-GHz, optimal 6-dB PBO is achieved when PA1 is OFF and PA2 is partly switched ON, where it sees the optimum impedance of $Z_{2,\text{opt6dB}}$, thus allowing high back-off efficiency. The achievable efficiency over different PBO levels optimized in the (m, n) plane is plotted in Fig. 3(b). The codes for both PA cells are also plotted as a function of PBO, that clearly illustrates the loadpulling effect in enhancing the back-off efficiency compared to class-A/B operation.

At 69 GHz, the role reversal takes place. Now for back-off, the second PA shuts OFF and part of first PA remains ON for efficient operation, as could be seen from constant 6-dB PBO curve shown by code $m = 0.5$ and $n = 0$, respectively, in Fig. 3(c). Thus, the PA demonstrates 2-D reconfigurability over PBO and frequency by maintaining high efficiency, as shown in Fig. 3(d).

This demonstrates the ability of exploiting active load pulling and code synthesis to allow simultaneously broadband and back-off operation. The granularity of the code synthesis can be increased with an N-way combiner that allows even higher efficiency and back-off operation, as we will demonstrate with a four-way combiner architecture.

C. Reconfigurability for VSWR Tolerance

The ability to allow optimal synthesis in a controlled fashion can be extended to overcome impedance mismatch effects as well. Here, we demonstrate an example of VSWR mitigation at peak power by exploiting the asymmetric-coded interaction between m and n using the asymmetric combiner explained in the previous section. Although this architecture uses the same conjugate output combiner, however, it exploits different load-pulling mechanisms for back-off and VSWR reconfigurability.

To allow VSWR mitigation at peak power, the architecture is designed for optimal code of $(m, n = 0.5)$ for peak operation under a 50-Ω load condition, i.e., the half of each branch (PA1 and PA2) is active for peak operation in a 50 Ω environment. For given impedance mismatch condition and operating code (m, n), the efficiency and output power level are given by $\eta = f_{\text{VSWR}}(S^{m,n}, m, n, \Gamma_L)$ and $P_{\text{out}} = g_{\text{VSWR}}(S^{m,n}, m, n, \Gamma_L)$, respectively. Similar to (3), the optimal operating code (m, n) for a given VSWR load Γ_L can be solved from

$$\begin{aligned} \frac{\partial f_{\text{VSWR}}}{\partial m} &\approx 0 \\ \frac{\partial f_{\text{VSWR}}}{\partial n} &\approx 0 \\ |g_{\text{VSWR}}(m, n, S^{m,n}) - P_{\text{out,given}}| &< \epsilon \end{aligned} \tag{4}$$

where $P_{\text{out,given}}$ is the desirable output power.

It is interesting to note that for maximum efficiency and output power, while PA1 is dominant in certain portions of the VSWR circle, the PA2 is dominant across the others, as shown in Fig. 4. For a VSWR 2:1 ($\Gamma_L = 0.31\angle 61°$) load at 69 GHz, the symmetric-coded operation with half fractions of PA1 and PA2 being ON ($m = 0.5$ and $n = 0.5$), degrades the power and efficiency η by ∼1 dB. This degradation in efficiency can be mitigated by changing the codes to $m = 0$ and $n = 1$, as shown in Fig. 4(a). This optimum combination with first PA turned off and second PA turned on gives us $\eta = 1$ and moves optimum impedance to $Z_{2,\text{opt}}$. Similarly, for VSWR 3.8:1 load ($\Gamma_L = 0.58\angle 23°$), η and power are enhanced by ∼2 dB through optimal code selection with second PA turned off and first PA turned on, i.e., $m = 1$ and $n = 0$, as shown in Fig. 4(b). This methodology demonstrates a PA architecture that exploits controlled mutual interactions through a combination of DAC cells to mitigate VSWR effects.

III. Self-Similar Γ-Conjugated Multi-port Architecture for Frequency and Back-Off Reconfigurability

In Section II, we showed that two-way power combined PA cells when driven with appropriate phases can generate the optimal load–pull impedances for an extensive range of frequencies and back-off levels. For a two-port network synthesis, the conjugate nature of the matching system in each branch could be seen from the design equations presented in [37]–[40], as given by

$$\Gamma_2 = \Gamma_1{}^* \tag{5}$$

$$|\Gamma_1| = \left|\frac{1 - \Gamma_1}{2}\right| \tag{6}$$

where $\Gamma_{1,2} = (Z_{1,2} - Z_o)/(Z_{1,2} + Z_o)$. It is interesting to note that this conjugate nature could be extended for 2^K ports. Such a generalized N-port architecture, due to the nature of asymmetry involved, also improves the efficiency across higher back-off levels as elaborated in this section.

Fig. 5 shows the proposed architecture where 2^K mm-Wave DAC cells combine their power in the 50-Ω load. The impedance seen by these PA cells Z_i are functions of driving conditions of all PA cells. The proposed architecture is divided into several different stages, which are subsequently explained next.

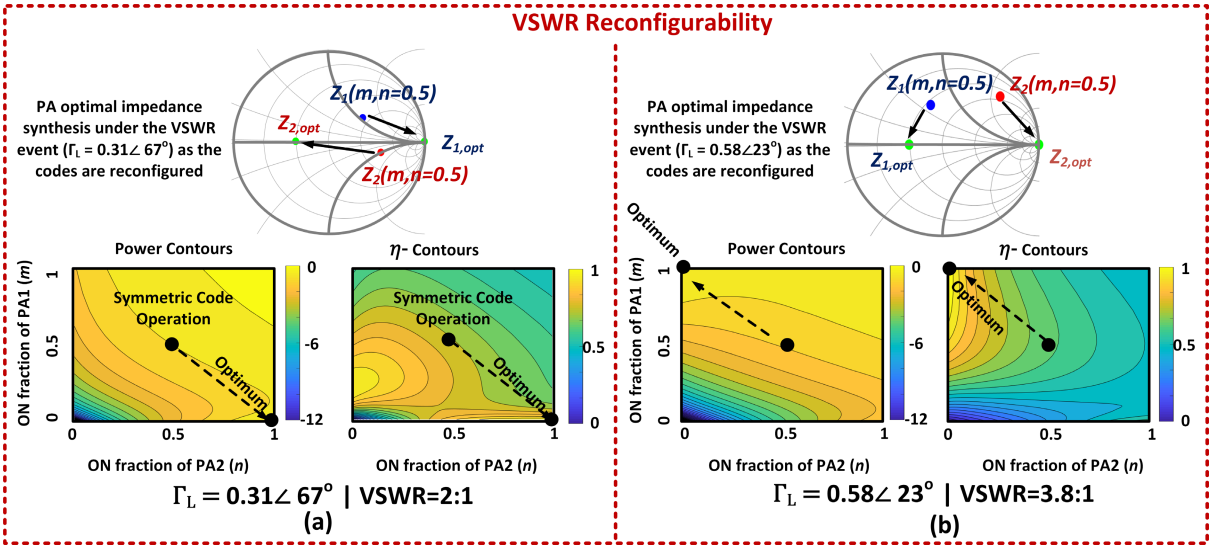

Fig. 4. DAC-based two-way combiner PA for VSWR reconfigurability for (a) VSWR 2:1 load and (b) VSWR 3.8:1 load at 69 GHz.

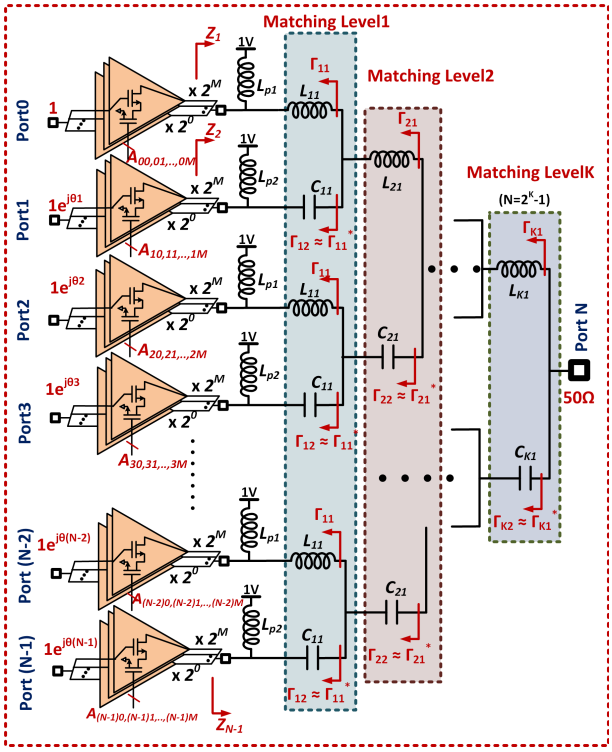

Fig. 5. Proposed self-similar, node-conjugated architecture with $(N+1)$-port network.

1) First Stage: Split the 2^K PA cells into 2^{K-1} groups with each group containing two PAs. First, add the parallel inductor L_p to resonate out the device capacitance of each PA cell at the center frequency. Once the device capacitance is resonated out, an asymmetric combiner synthesis is carried out to maximize the combining efficiency across the broad spectrum. This is accomplished by adding an inductor in one branch (L_{11}) and capacitor in other branch (C_{11}) to create the conjugate condition $\Gamma_{12} \approx \Gamma_{11}{}^*$. This network is replicated for all the groups, resulting in 2^{K-1} outputs from the first stage.

2) Second Stage: Now, split the 2^{K-1} outputs from the first-stage into 2^{K-2} groups with each containing two branches. Then, add inductor in one branch (L_{21}) and capacitor in another (C_{21}) creating $\Gamma_{22} \approx \Gamma_{21}{}^*$ condition, thereby maintaining the asymmetry in the structure. Replicate this for the rest of the groups similar to the first stage.

3) Kth Stage: After the Kth-stage with $\Gamma_{K2} \approx \Gamma_{K1}{}^*$, connect the resulting output to 50-Ω load. The optimal phase driving condition for PAs in each of these branches could be derived from the S-parameter matrix of the $(N+1)$-port combiner, as given by $\theta_i = \angle(S_{N,i}/S_{N,0})^*$.

A. Number of Stages(K)

1) $K = 1$: Fig. 6(a) shows the proposed architecture with $K = 1$ or a two-way combiner with goal to deliver ~200 mW to the load. Γ_{1j}s are conjugate in nature, as shown in Fig. 6(b). Once this condition is achieved, the impedances presented to the PAs in both the branches are close to optimal impedance automatically as we could see from Fig. 6(c). This optimal impedance synthesis ensures peak power combining across wideband and also provides back-off reconfigurability, which is shown in the 3-D plot across the dual axes of frequency and PBO levels in Fig. 6(d). As shown, the efficiency $\eta > 0.7$ at the peak power level and $\eta > 0.5$ at 10-dB PBO over a large frequency range can be achieved.

2) $K = 2$: The proposed architecture can be adapted for $K = 2$ or a four-way combiner, as shown in Fig. 7(a) to deliver ~200 mW to the load. Here, the PAs are denoted as cell A, B, C, and D. Γ_{ij}s at each of the matching levels are nearly conjugate in nature, as shown in Fig. 7(b). After achieving this condition, the impedances presented to the PAs in all the four branches are much closer to optimal impedance as we could see from Fig. 7(c). Fig. 7(d) shows the 3-D plot of near-optimal efficiency across the dual axes of frequency and back-off levels for this four-way combiner. As shown, almost

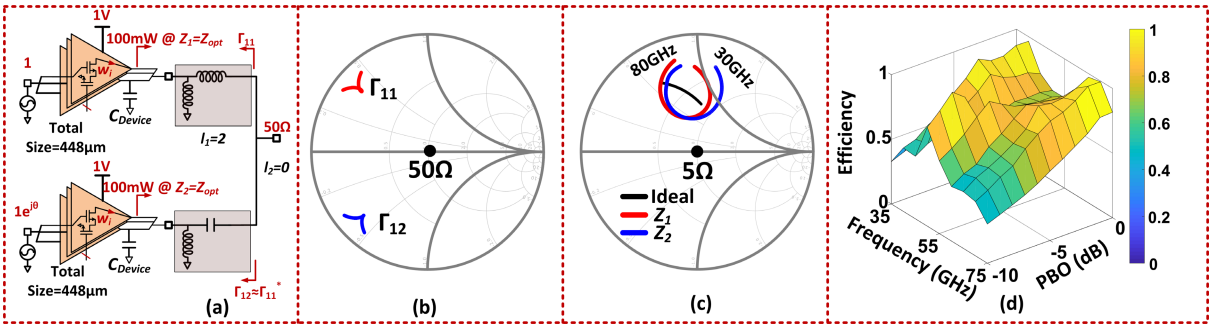

Fig. 6. Γ-conjugated combiner. (a) Combiner design with $K = 1$ delivering 200 mW to the load. (b) $\Gamma_{12} \approx \Gamma_{11}^*$. (c) Impedances seen by PAs in two branches. (d) 3-D plot of efficiency against 2-D axes-frequency and back-off.

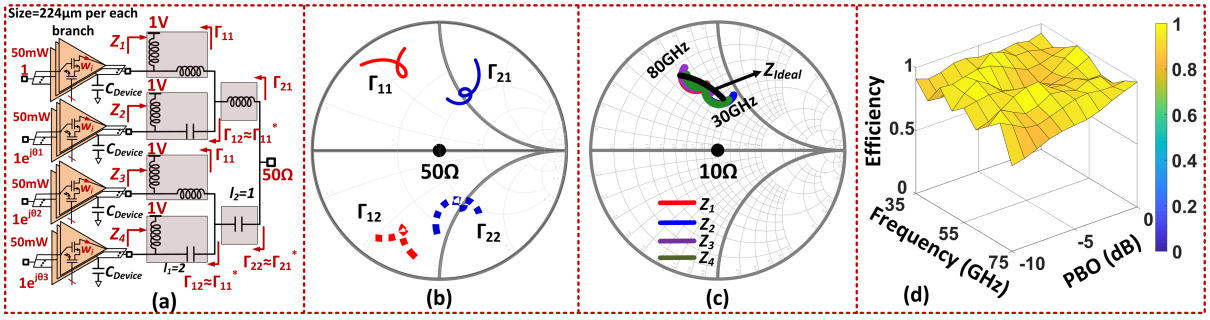

Fig. 7. Scalable Γ-conjugated combiner. (a) Combiner design with $K = 2$ delivering 200 mW to the load. (b) Γs are nearly conjugate-natured, as could be seen at each matching level ($\Gamma_{12} \approx \Gamma_{11}^*$ and $\Gamma_{22} \approx \Gamma_{21}^*$). (c) Impedances seen by PAs in two branches are closer to the optimal impedance. (d) 3-D plot of efficiency against 2-D axes-frequency and back-off shows almost constant optimal efficiency.

a desired flat efficiency could be achieved with $\eta > 0.9$ at the peak power level and $\eta > 0.8$ at 10-dB PBO across the complete frequency span (35–75 GHz).

B. Coding Scheme for the Proposed Architecture

The proposed architecture allows a different combination of codes for controlling the contributions coming from various PA cells for a given level of output power. The codes can be analytically derived based on combining cells and can be stored in a lookup table (LUT) on-chip and even adjusted post-fabrication to compensate for mismatches and process variations. The programmability of the codes is intended to synthesize optimal operating conditions for high efficiency broadband peak and back-off operation. For an ideal two-way Doherty, at peak output power, both PAs are ON and at 6-/9-dB back-off, the main PA is ON, while the auxiliary PA is OFF, as shown in Fig. 8(a). To further explain the coding schemes in the proposed architecture, a block diagram of four-way combining PA architecture is shown in Fig. 8(b) and (c). Different mm-Wave PA-DAC cells are represented as A, B, C, and D. For a given frequency and an output back-off power level, the voltage and current saturation conditions can be maintained with a certain combination of these cells. The selection of codes self-adjusts the load modulation through node-conjugated combiner and is summarized in Fig. 8(d). For example, at the lower end of the band, i.e., 37 GHz, the cell B dominates at 9.6-dB PBO, while the combination of cells B and D achieves optimal performance at 6-dB PBO. At the higher side of spectrum, i.e., 71 GHz, cell C determines the desired power at 9.6-dB PBO, while the combination of A and C dictates 6-dB back-off level, as shown in Fig. 8(d). At the center of the band, i.e., 55 GHz, cells C and A provide the optimal power at 6- and 9.6-dB PBO, thereby ensuring the voltage–current saturation of the two PA cells. The methodology demonstrates that through this self-similar architecture and optimal code synthesis, simultaneously broadband peak and back-off operation can be achieved exploiting active load-pulling.

IV. Active Load-Pulling Architecture for VSWR Agility

The effect of VSWR events on the performance of a PA and the combining cells is shown in Fig. 9. The range of the load variation translates through the combining network into a range of impedance variations that each cell experiences, that results in the degradation of the overall PA performance. Mitigation of this effect requires us to bring back the optimal impedance that each PA sees under such VSWR event. Achieving this through a reconfigurable tuning network is challenging at mm-Wave frequencies due to the low-quality factors of variable passive elements. We will explore if load pulling through a systematically designed network can allow us to resynthesize optimal impedances and overcome VSWR without the need for variable lossy passives.

A. Can VSWR Be Mitigated Through Active Load Pulling? Small-Signal Regime Analysis

For ease of analysis and understanding of the design space, we will start with investigation of the effect of load mismatch in a lossless multi-port network through which a set of small-signal amplifiers combine to drive a load. In such a case,

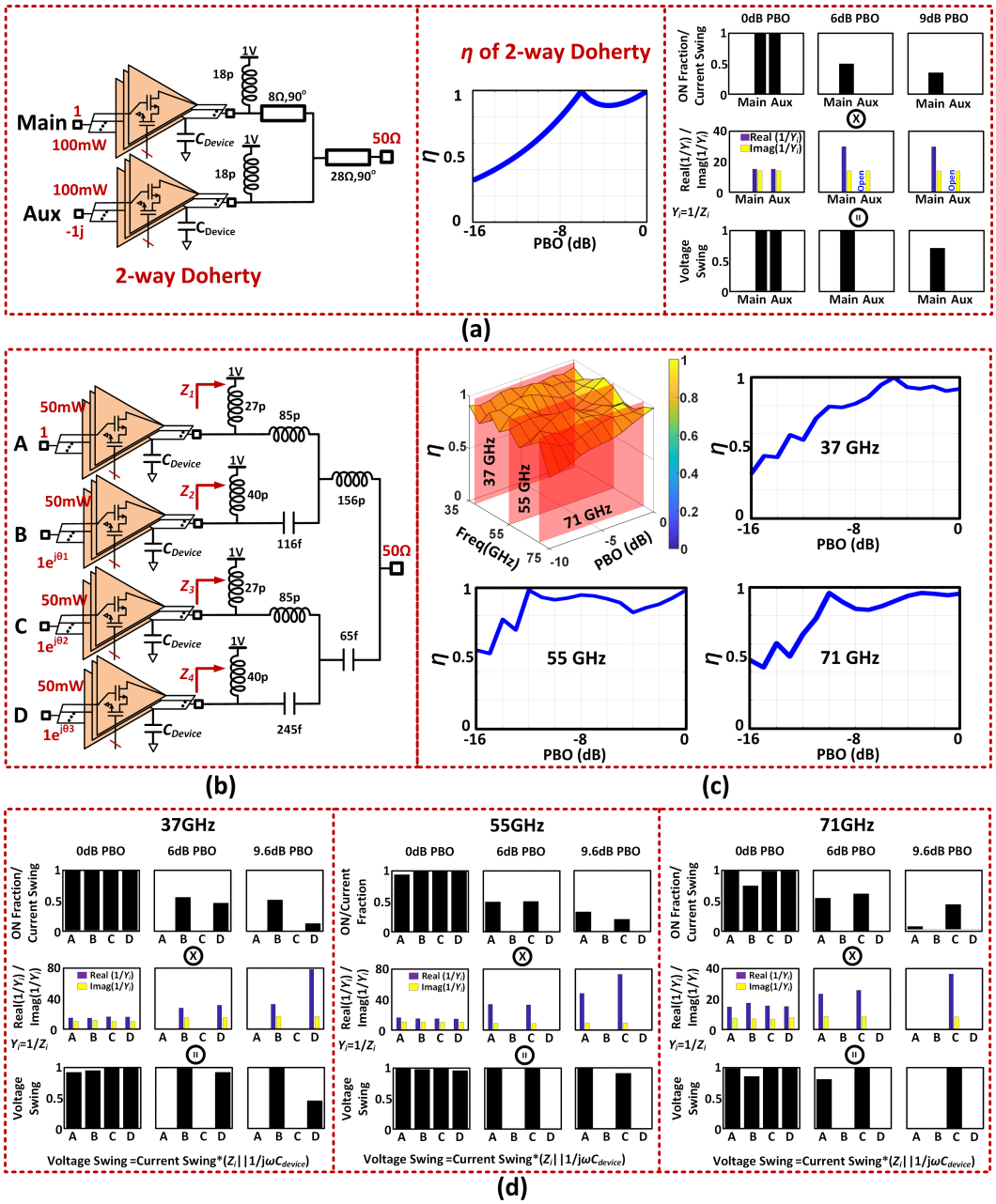

Fig. 8. Γ-conjugated combiner. (a) Doherty design, its efficiency, and DAC codes across PBO levels. (b) Proposed four-way Γ-conjugated design. (c) Efficiency across the frequencies and PBO. (d) Corresponding DAC codes at PBO levels along with the impedance seen by the PA cells ($Z_i = R_i || jX_i$) to achieve simultaneous current–voltage saturation across the frequencies for a near flat efficiency at 37, 55, and 71 GHz.

the amplifiers still would like to see the optimal impedance (conjugate of the their output impedance) that can deviate strongly under a VSWR event. To understand whether active loadpulling can mitigate this effect, the question we address is whether such degradation can be minimized with carefully designed combiner network and with reconfiguration of the amplifier driving conditions?

For such a generalized N-port combining network, the maximum efficiency under optimal driving conditions ($p_i \propto S^*_{N+1,i}$) is given by $\eta_{\text{tot, max}} = 1 - |S_{N+1,N+1}|^2$. Evidently, the combiner is designed in such a way that under optimal load of $Z_L = Z_0$, $\eta_{i\text{th source}} = \eta_{\text{tot, max}} = 1$, and $S_{N+1,N+1} = 0$ for a lossless combiner [38].

When the load impedance (Z_L) is now varied, it can be shown that the optimal driving conditions of the combining cells remain unchanged. Under such VSWR events, the maximum achievable combining efficiency and corresponding efficiency of the ith source can be both shown to be

$$\eta'_{i\text{th source}} = \eta'_{\text{tot, max}} = 1 - |\Gamma_L|^2 \tag{7}$$

where $\Gamma_L = (Z_L - Z_o)/(Z_L + Z_o)$.

The earlier analysis also infers that the achievable combining efficiency is entirely independent of the combining network and active load modulation cannot mitigate the degradation resulting from load mismatches. This is only true if the output impedances of the combining amplifiers are constant, such as in a small-signal amplifier. In a PA though, this can be modified through switching cells in an mm-Wave DAC array. The optimal output impedance of each combining cell can be

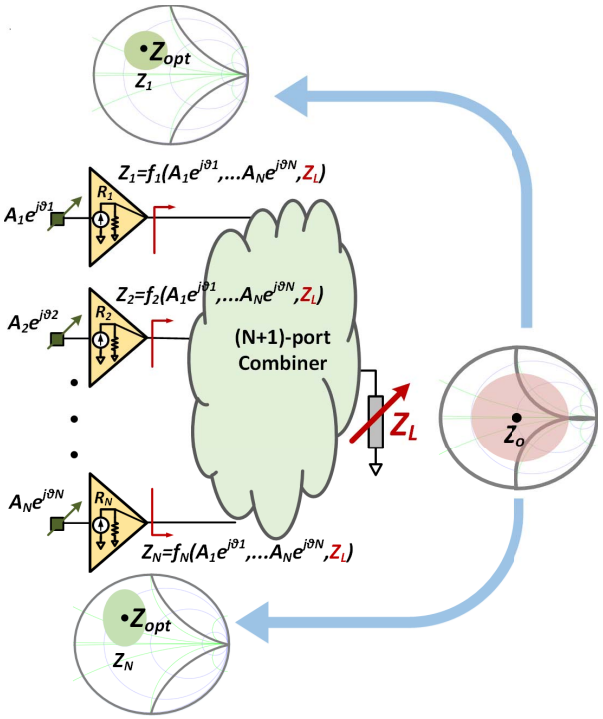

Fig. 9. Impedances seen by PA cells deviate from the optimal impedance Z_{opt} under VSWR events at the load Z_L leading to PA performance degradation.

reconfigured and VSWR mitigation can be achieved through optimal code synthesis.

B. Network Analysis

Here, we present a method to design the combining network that can allow us to overcome VSWR in specified regions of the Smith Chart. Under load mismatch effects, i.e., $Z_L \neq 50\ \Omega$, the performance degrades as a function of VSWR and is shown in Fig. 10(c).

Consider a simplified PA-DAC cell with N number of cells. Assume that under $Z_o = 50\ \Omega$ load, the required output power is delivered equally by both cells at $m = 1/M$, $n = 1/N = 0.5$. Now, each DAC cell can be modeled as a DAC-current source with complex RC impedance $Z_{\text{out}} = Z^*_{\text{opt}}$, where Z_{opt} is the optimal load–pull impedance. When the PA is completely ON, the optimal output impedance is given by $Z_{\text{out}} = R_{\text{opt}}||(1/j\omega C_{\text{d}})$, as shown in Fig. 10(a). Similarly, for $1/M$ fraction of DAC cell, the optimal impedance can be modeled as $Z_{\text{out}} = MR_{\text{opt}}||(1/j\omega C_{\text{d}})$. This is the method to reconfigure the output impedances of the combining DAC cells.

The effect of this in the two-way combiner example can be seen in Fig. 10(c). In addition to the center $Z_o = 50\ \Omega$ load, the PA shows optimal performance when the load impedance assumes two other impedances in the capacitive region of the Smith chart. In the neighborhood of these impedances, the PA demonstrates high-efficiency operation. As shown in Fig. 10(c), this is achieved by optimally increasing one of the PAs to full strength while turning the other one off. This allows a VSWR-agile operation in the capacitive region of the PA in this example. The location of these two additional regions in the Smith Chart is, of course, dependent on the combiner network. We will show that the combiner can be systematically designed to place these two centers at the desired locations in the Smith Chart.

As shown in Fig. 10(b), the combiner network is defined by the four elements x_1, x_2, x_3, x_4. Using the asymmetric nature of combining condition given by (5), a relation between x_i(s) can be established as

$$\frac{2rx_3(x_3 + j2r)}{4r^2 + x_3^2} + jx_4 = \frac{2rx_1(x_1 - j2r)}{4r^2 + x_1^2} - jx_2. \tag{8}$$

On equating real and imaginary parts, we get

$$|x_3| = |x_1| \tag{9}$$

$$\frac{4r^2x_3}{4r^2 + x_3^2} + x_4 = -\frac{4r^2x_1}{4r^2 + x_1^2} - x_2. \tag{10}$$

Equations (9) and (10) give us two solutions depending on relationship between x_3 and x_1 (Cases 1 and 2)

$$\text{Case 1: } x_3 = x_1, x_4 = -x_2 - \frac{8r^2x_1}{4r^2 + {x_1}^2} \tag{11}$$

or

$$\text{Case 2: } x_3 = -x_1, x_4 = -x_2. \tag{12}$$

A third equation can be established using (6) to provide a relationship between x_2 and x_1 given as

$$\left|\frac{2rx_1(x_1 + j2r)}{4r^2 + x_1^2} + jx_2 - 1\right| = 1. \tag{13}$$

Depending on the dominance of PA1 or PA2 or both, there are several possible solutions for load impedance at which $\eta = 1$ in addition to 50 Ω. To simplify analysis, we can assume one of the PAs to be shut OFF, say PA_2 ($m = 1, n = 0$) and the load impedance at which fully ON PA_1 can transfer all its power efficiently is $z_L = z_{L1}$. Similarly, when PA_1 shuts OFF ($m = 0, n = 1$), the entirely ON PA_2 delivers power with maximum efficiency to load $z_L = z_{L2}$. These impedances can be computed to be

$$\begin{aligned} z_{L1} &= ((r||jx_1 + jx_2)||j(x_3 + x_4))^* \\ &= \frac{\left(rx_1^2 - j\left[r^2x_1 + r^2x_2 + x_1^2x_2\right]\right)(x_3 + x_4)}{\left(r^2 + x_1^2\right)(x_1 + x_2 + x_3 + x_4) - x_1^3 + jrx_1^2}. \end{aligned} \tag{14}$$

Similarly

$$\begin{aligned} z_{L2} &= ((r||jx_3 + jx_4)||j(x_1 + x_2))^* \\ &= \frac{\left(rx_3^2 - j\left[r^2x_3 + r^2x_4 + x_3^2x_4\right]\right)(x_1 + x_2)}{\left(r^2 + x_3^2\right)(x_1 + x_2 + x_3 + x_4) - x_3^3 + jrx_3^2}. \end{aligned} \tag{15}$$

So far, there are three independent equations with four variables in the equation set (11) and (13) for Case 1 or (12) and (13) for Case 2. Hence, there is only one independent variable x_1. Using (14) and (15), we can infer $z_{L1} = f(x_1)$ and $z_{L2} = g(x_1)$. The loci of z_{L1} and z_{L2} for these two possible cases are shown in Fig. 10(d). For example, in Case 1, with $x_1 = +0.3$, z_{L1} ($m = 1, n = 0$) and z_{L2}($m = 0$, $n = 1$) are inductive, and hence, efficiency recovery is configured for inductive-VSWR loads in addition to $z_L = 1$ ($m = 1/2$ and $n = 1/2$), as shown in Fig. 10(e). Likewise,

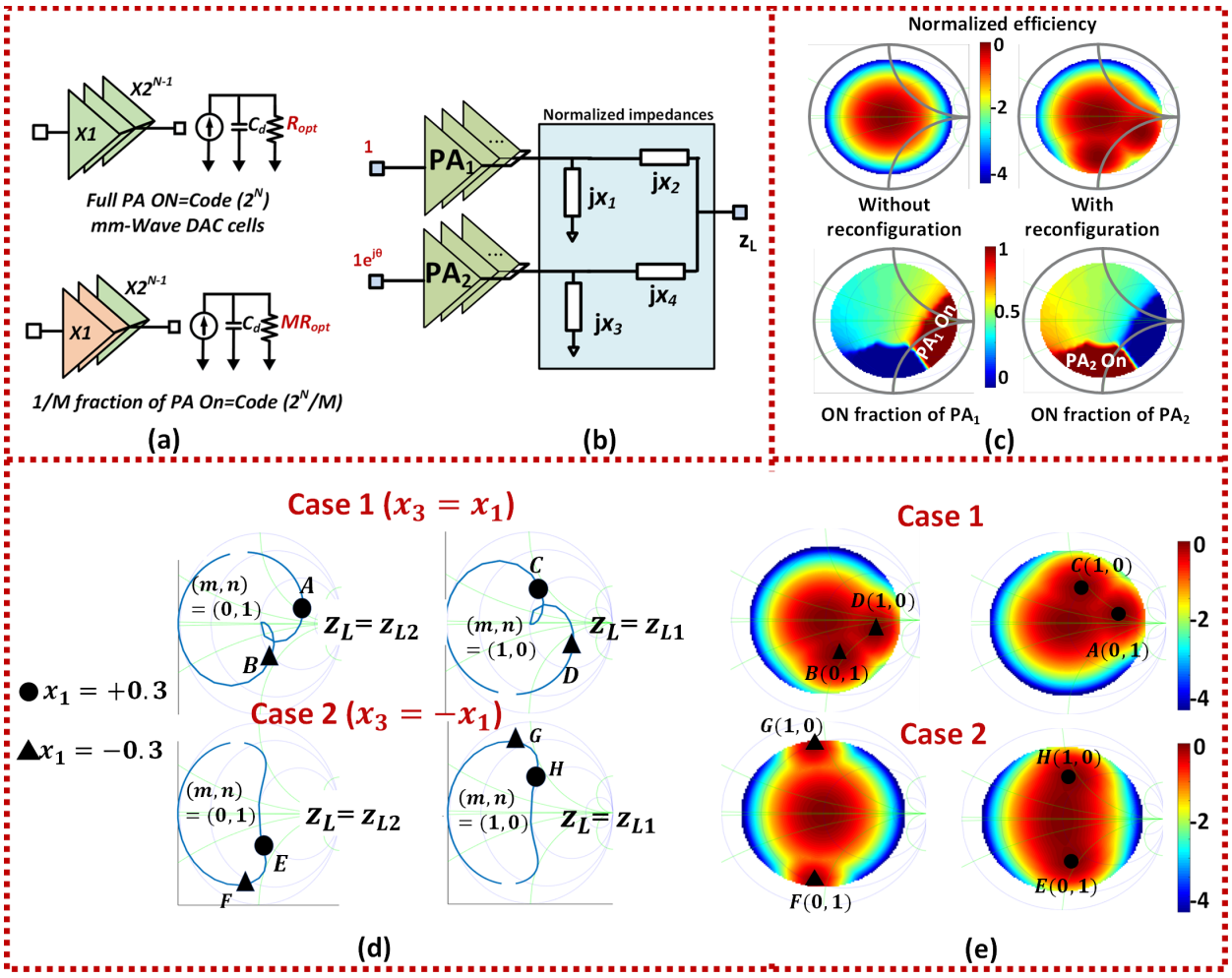

Fig. 10. VSWR reconfigurability. (a) Current model of PA with $1/M$ fraction being turned on. (b) Example two-way combined linear network. (c) Power degradation circle without and with reconfiguration along with the on-fraction of each PA when reconfigured for maximum efficiency. (d) Combiner design to shape the VSWR enhancement regions. The figure shows the loci of two load impedances (z_{L1} and z_{L2}) in (14) and (15) that represent optimal efficiency operation for the two codes ($m = 1, n = 0$) and ($m = 0, n = 1$). This results in appearance of the VSWR tolerance regions around z_{L1} and z_{L2} as shown in part (e) of the figure. (e) Combiner examples showing the η-enhancement in capacitive and inductive portions of the Smith chart corresponding to the impedances highlighted in part (d) of the figure.

the VSWR enhancement could be achieved on the capacitive region (Case 1, $x_1 = -0.3$), inductive region (Case 1, $x_1 = +0.3$), or combination of both (Case 2, $x_1 = +0.3$) [See Fig. 10(d) and (e)].

In the presented two-way combiner, we see that two additional regions of VSWR enhancement are created in a two-way combiner [see Fig. 10(e)]. Expectedly, this can be extended as we move from a two-way to an N-way combiner.

V. Wideband and Back-Off Agile PA Implementation

A codesign process between the constituent PA cells and the output combiner is followed for the optimization of peak power and efficiency across the frequency range. The complete schematic comprises of four-way three-stage PA, as shown in Fig. 11. The input signal splits into two branches driving the first 2-bit thermal-coded predriver stage. It drives the 2-bit driver, which further powers the 3-bit main stage. The broadband interstage matching networks are synthesized to achieve high network efficiency. The input digital bits are sent to each of the branches through a high-speed on-chip serial-to-parallel converter designed with dynamic latches.

A. mm-Wave DAC

A common-emitter stage with control switch at its source is chosen for each of the weighted-PA bits, as shown in Fig. 12(a). When the control bit is high, the switch is turned on with a minimal resistance at the source enabling PA to deliver power. When the control bit is low, the switch is turned off, creating an open-circuit condition at the source of PA and turning off the PA.

The output stage comprises of a 3-bit mm-Wave DAC with the least significant bit (LSB) PA and LSB switch sized $2 \times 16 \times 1$ and $1 \times 32 \times 4$ μm, respectively. In addition, the most significant bit (MSB) PA and MSB switches are sized $8 \times 16 \times 1$ and $4 \times 32 \times 4$ μm, respectively. The layout of MSB cell and its load–pull contours at 37 and 71 GHz are shown in Fig. 12(a) and (b). The layout of the 3-bit DAC is

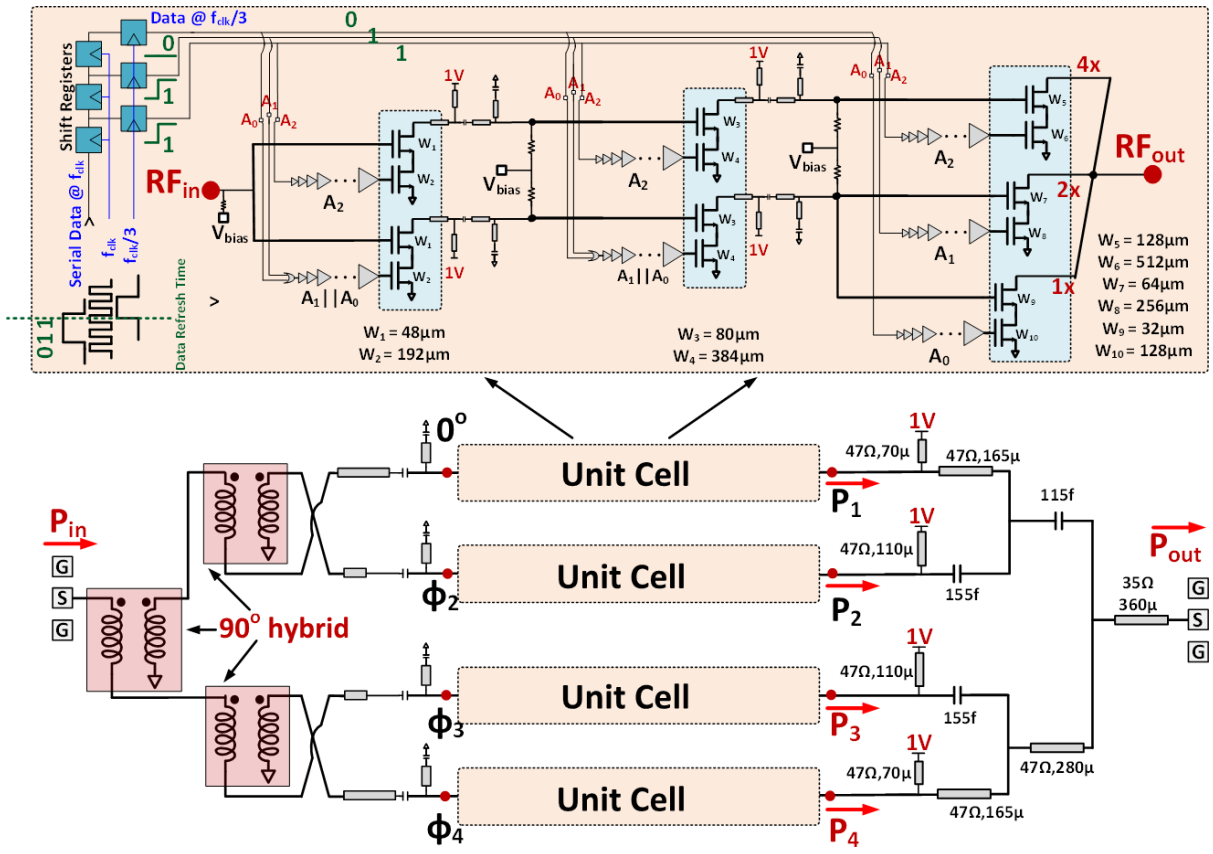

Fig. 11. Circuit schematic of the 37–73-GHz broadband PA with back-off energy efficiency enhancement.

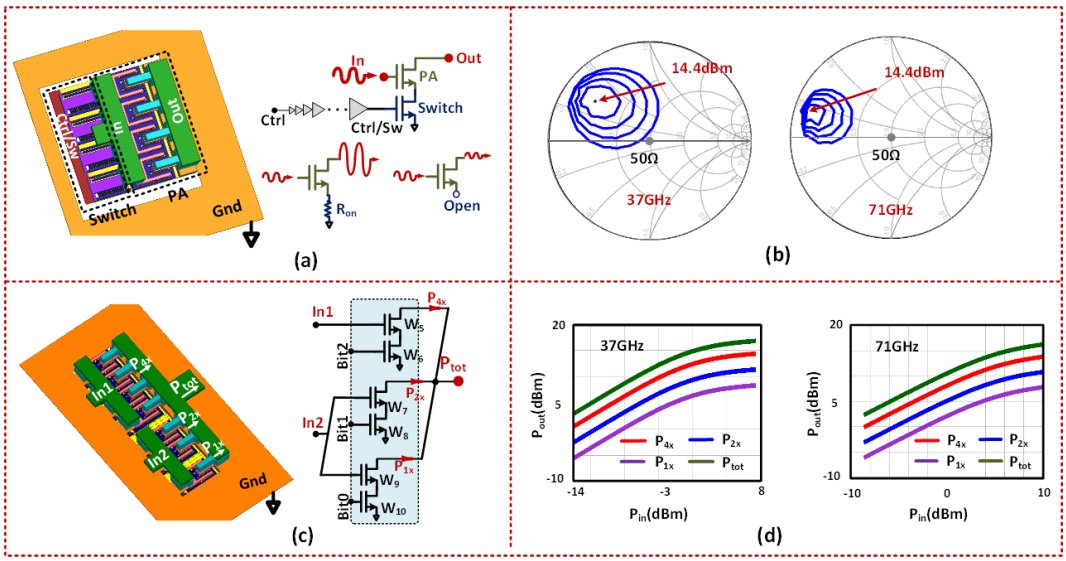

Fig. 12. PA output 3-bit DAC. (a) Layout of MSB along with the switch. (b) Load–pull contours of MSB PA at 37 and 71 GHz. (c) Layout of 3-bit mm-Wave DAC. (d) Power delivered by each of the bits at 37 and 71 GHz.

shown in Fig. 12(c), and the power delivered by each of the cells is shown in Fig. 12(d).

B. Combiner Design

The combiner is designed following the methodology presented in Section III to ensure that the PAs operate efficiently at peak power level and across back-off over targeted bandwidth. The combiner is realized with microstrip transmission lines with the top aluminum (Al) metal layer of 1.45 μm thickness and metal–oxide–metal (MOM) capacitors. It is jointly shown in Figs. 11 and 13(a). As stated, the combiner follows the Γ-conjugated network, which is designed to have the driving phases of approximately $0, -\pi/2, 0, +\pi/2$ at the four branches. Fig. 13(b)–(f) shows the simulated performance of the output PA stage with the combiner across 35–75 GHz, showing the ability to deliver $P_{\text{out}} > 20$ dBm and high

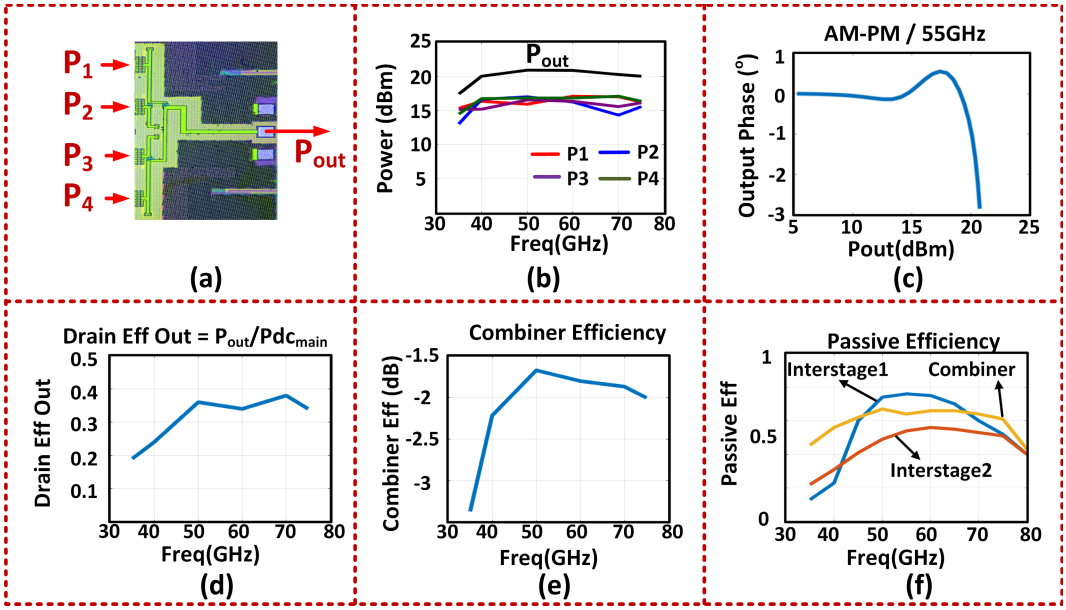

Fig. 13. Simulated PA performance. (a) Micrograph of the output combiner. (b) Output power and individual cell contributions. (c) AM-PM at 55 GHz across frequency. (d) Output drain efficiency across frequency. (e) Output combiner efficiency across frequency. (f) Interstage matching network efficiencies.

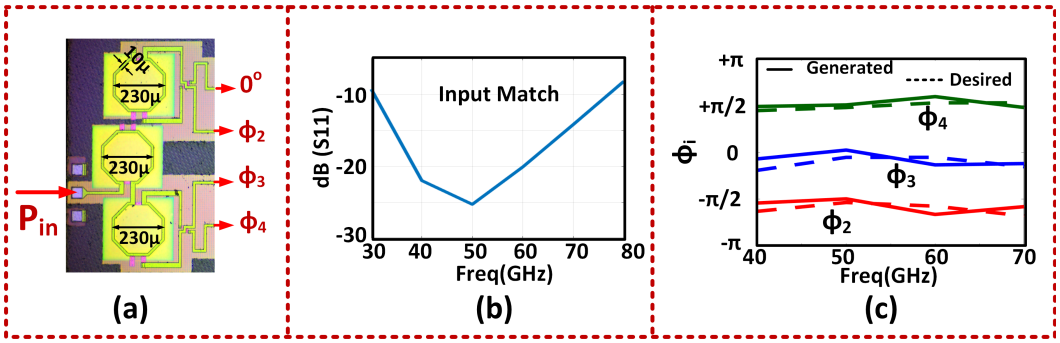

Fig. 14. Simulated PA performance. (a) Micrograph of the input combiner. (b) Input matching. (c) Phase generation across the branches with the input network and comparison with optimal phase profiles.

combining efficiency over 72% fractional bandwidth. In addition, the AM–PM variation is within 3° at 55 GHz across the output power, as shown in Fig. 13(c). To ensure maximum power delivery to the main stage, broadband interstage networks are designed, as shown in Fig. 13(f).

C. Input Match and Phase Generation

The input matching needs to ensure simultaneous maximum power delivery and the synthesis of desired driving phases across frequency. As explained in the previous section, the combiner requires approximate phases of $0, -\pi/2, 0, +\pi/2$ for efficient operation (see Fig. 11). The compact 90° hybrid in [45] along with asymmetrical matching networks in each branch is used to generate the required phases close to $0, -\pi/2, 0, +\pi/2$ across the four paths, as shown in Fig. 14. The dimensions of the input transformers are shown in Fig. 14(a). Fig. 14(b) shows the input return loss to be less than −10 dB across the targeted frequency band of 30–80 GHz. The desired input phase control is achieved using the abovementioned synthesis and is plotted across frequency in Fig. 14(c).

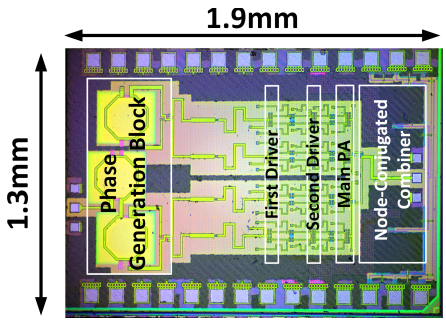

Fig. 15. Chip microphotograph.

D. Measurement Results

The PA is implemented in a 65-nm bulk CMOS process with reported peak f_{max} of 240 GHz for the transistors with the lowest metal contacts. The microphotograph of the chip is shown in Fig. 15 with the dimensions of 1.3×1.9 mm^2. All the PA cells operate from a supply voltage of 1 V and a bias voltage of 0.7 V.

The measured large-signal output stage drain efficiency for the digital codes across 37–71 GHz is shown in Fig. 16.

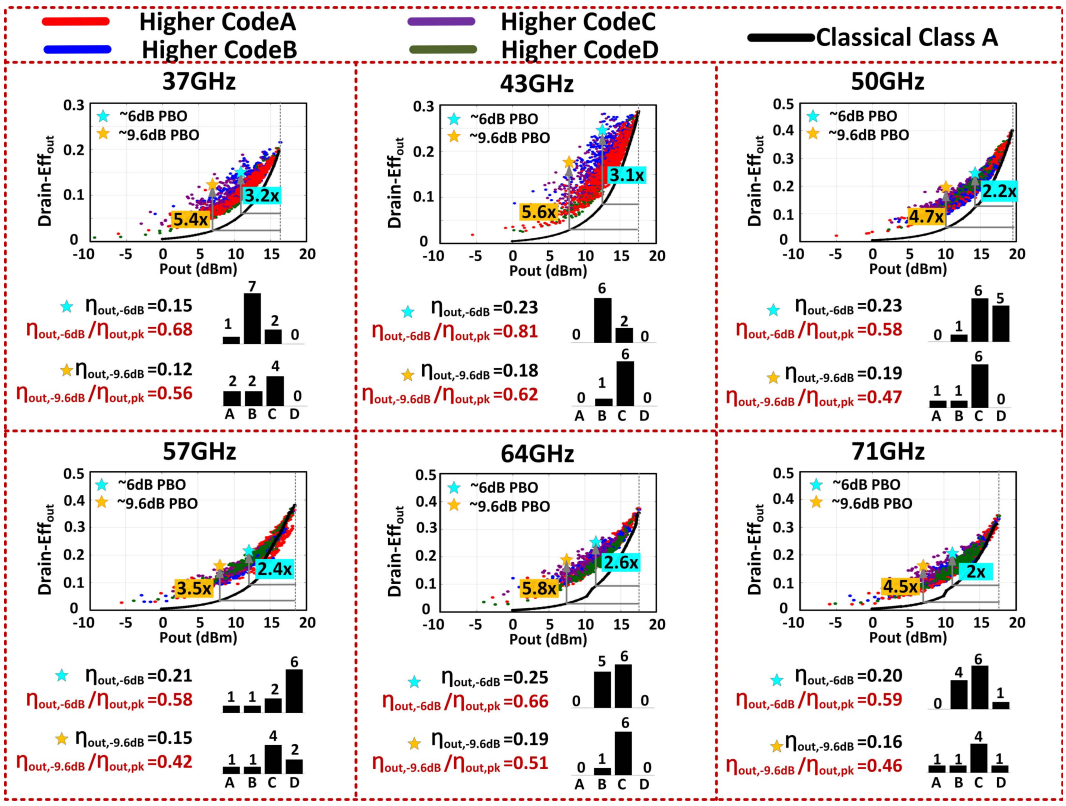

Fig. 16. Measured large-signal performance across the frequencies.

The plots are all color-coded, i.e., each PA cell is represented by a specific color in the measurement chart. The red color implies that, for that specific point, PA_1 dominates in the four-way combining. Similarly, color codes of blue, violet, and green, indicate domination of PA_2, PA_3, and PA_4, respectively. These different curves are compared with respect to the class-A operation.

As can be seen, at the peak power, all the four PAs are fully ON, indicating near-equal contribution of the output power as expected. The codewords at the back-off levels of 6 and 9.6 dB are also shown across each of these frequencies. As can be seen, for higher efficiency at 37 GHz, PA_2 dominates for 6-dB back-off and PA_3 for 9.6-dB PBO. At 71 GHz, PA_3 dominates for 6- and 9.6-dB PBO levels to achieve higher efficiency. We can further see that the degradation in efficiency at the back-off levels over that of the peak is low with the ratio $((\eta_{\text{out, }-6\text{ dB}})/\eta_{\text{out, pk}})$, varying between 0.58 and 0.81, while $((\eta_{\text{out, }-9.6\text{ dB}})/\eta_{\text{out, pk}})$ varies between 0.42 and 0.62. An efficiency enhancement of up to 3.2× over the class-A operation is measured for 6-dB PBO and up to 5.8× is measured for ≈9.6-dB PBO when compared with class-A operation.

The measured P_{sat} varies between 16.3 and 19.3 dBm across 37–73 GHz, as shown in Fig. 17(a). The measured output drain efficiency, total drain efficiency (η_{tot}), and PAE are shown in Fig. 17(b). The sharp decrease at 35 and 75 GHz is due to the bandwidth limitation of the networks between the PA, driver, and predriver stages. A peak P_{sat} of 19.3 dBm is measured at 50 GHz with η_{out} of 40.1% and PAE of 16.2%. The drop in PAE over η_{out} is due to the overdesign and significant dc power consumption in the driver and predriver stages (∼235 mW at 50 GHz) when compared with the main stage PA cells (∼212 mW at 50 GHz). The PA has a small-signal gain of 15.6 dB and a large-signal gain of 8.5 dB at 50 GHz. The measured η_{out} values at PBO levels of 3, 6, and 9.6 dB are shown in Fig. 17(c) with the peak values of 0.3 at 50 GHz for 3-dB PBO, 0.25 at 64 GHz for 6-dB PBO, and 0.19 at 64 GHz for 9.6-dB PBO. The measured P_{sat} and η_{out} values across the four different chips are shown in Fig. 17(d) and (e). We can see that P_{sat} varies by ≤1 dB across the frequencies except at 50 GHz where the maximum variation is 1.9 dB.

Fig. 18 summarizes the measured performance of the chip and shows the comparison with the recent state-of-the-art mm-Wave PAs in CMOS/SiGe processes. As can be seen, the reported PA maintains high P_{sat} with high efficiency across a dual combination of wider PBO and wider frequency range.

VI. VSWR-Agile PA Implementation

For practical validation of VSWR agility explained in Section IV, a differential two-way combined two-stage PA with neutralization capacitances is realized in 65-nm CMOS. The schematic of the PA is shown in Fig. 19(a), where the driver stages are sized to be one-third of the main stage cells. The differential input is fed through a GSGSG port and converted into differential-quadrature signals with an on-chip differential hybrid [34]. The input is designed to simultaneously achieve the required broadband input matching with simulated $S_{11} < -10$ dB across 26–42 GHz and generate the required phases across the range of operation, as shown

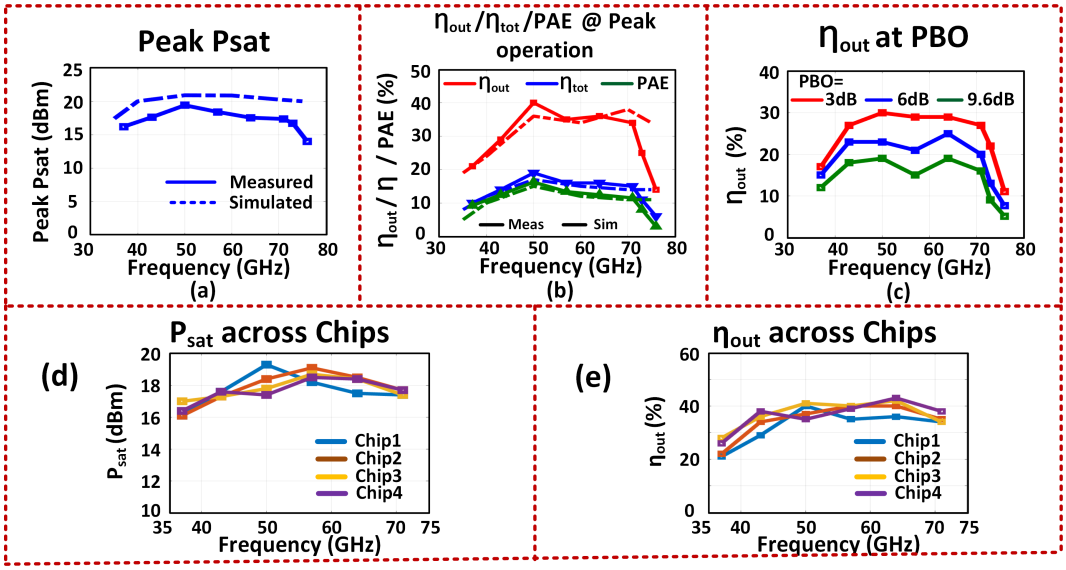

Fig. 17. Measured PA performance. (a) Measured P_{sat}. (b) Measured η_{out}, η_{tot}, and PAE. (c) Measured η_{out} at PBO levels of 3, 6, and 9.6 dB. (d) P_{sat} across multiple chips. (e) η_{out} across multiple chips.

	This Work	H.-T.Nguyen ISSCC '19	T.Li RFIC'18	S.Hu ISSCC'17	M. Vigilante RFIC'17	A.Agah JSSC'13
Frequency of Operation (GHz)	37-73	57	23.5-41	26-44	29-57	45
Technology	65nm bulk CMOS	45nm CMOS SOI	45nm CMOS SOI	0.13µm SiGe	28nm bulk CMOS	45nm CMOS SOI
Architecture	4-way Self Similar Node-Conjugated Architecture	Antenna-based Doherty	Hybrid of Continuous Class F/F^{-1}	Multiband Doherty	Broadband Series Power Combiner	SlowWave-CPW Doherty
Supply (V)	1	2	-	1.5	0.9	2.5
P_{sat} (dBm)	19.3 @50G	21.2	18.6@28G	17.1@37G	16.6@43G	18
$\frac{\eta_{out}(-6dB\ PBO)}{\eta_{out}(pk)}$	0.68 @37G ,0.81@43G, 0.66 @64G ,0.59@71G	-	-	0.86@28G, 0.94@37G, 0.73@39G	-	0.77@45G*
$\frac{\eta_{out}(-9.6dB\ PBO)}{\eta_{out}(pk)}$	0.56 @37G ,0.62@43G, 0.51 @64G ,0.46@71G	-	-	0.54@28G*, 0.69@37G*, 0.57@39G*	-	0.52@45G*
Peak η_{out} (%)	40.1 @50G	>23*	55*@28G	27.6@37G	>34*@43G	31
Peak η_{out} at 6dB back-off (%)	24.7 @64G	>20*	20*@28G	26@37G	>15*@43G	24 *
Peak η_{out} at 9.6dB back-off (%)	19.3 @64G	>16*	10*@28G	19@37G*	>5*@43G	16*
Peak PAE (%)	16.2 @50G	21.8	45.7@28G	22.6@37G	24.2@43G	21
Area (mm^2)	2.47	3.61	0.14**	1.76	0.16**	0.45

*Estimated from the plots. **Active chip Area.

Fig. 18. Comparison with the state-of-the-art mm-Wave PAs.

in Fig. 19(b). The interstage networks are transformer coupled and are designed to cover the broad frequency range. Each branch of the PA operates from a 1.1-V dc supply voltage. The combiner network allows efficient back-off operation, with frequency-dependent codes of the combining cells at the back-off. In this RF-in/RF-out design, the back-off operation is permitted through an adaptive biasing that is broadband enough to allow high-speed envelope tracking with multi-Gb/s modulation. The biasing values are tolerant to process variations (measured across two chips) and, therefore, can be stored in an LUT for repetitive use after one-time calibration. The objective of the design is to demonstrate broadband peak power, high back-off efficiency, and VSWR tolerance. The simulated performance of PA is plotted in Fig. 19(b), in which PA delivers nearly 20 dBm with PAE > 20%. The transmission-line-based combiner allows efficient back-off and broadband performance, as shown in the simulated results in Fig. 19(b).

A. Measurement Results

The PA is implemented in a 65-nm bulk CMOS process. The die photograph of the silicon chip measuring 1.5 × 0.9 mm^2 is shown in Fig. 20.

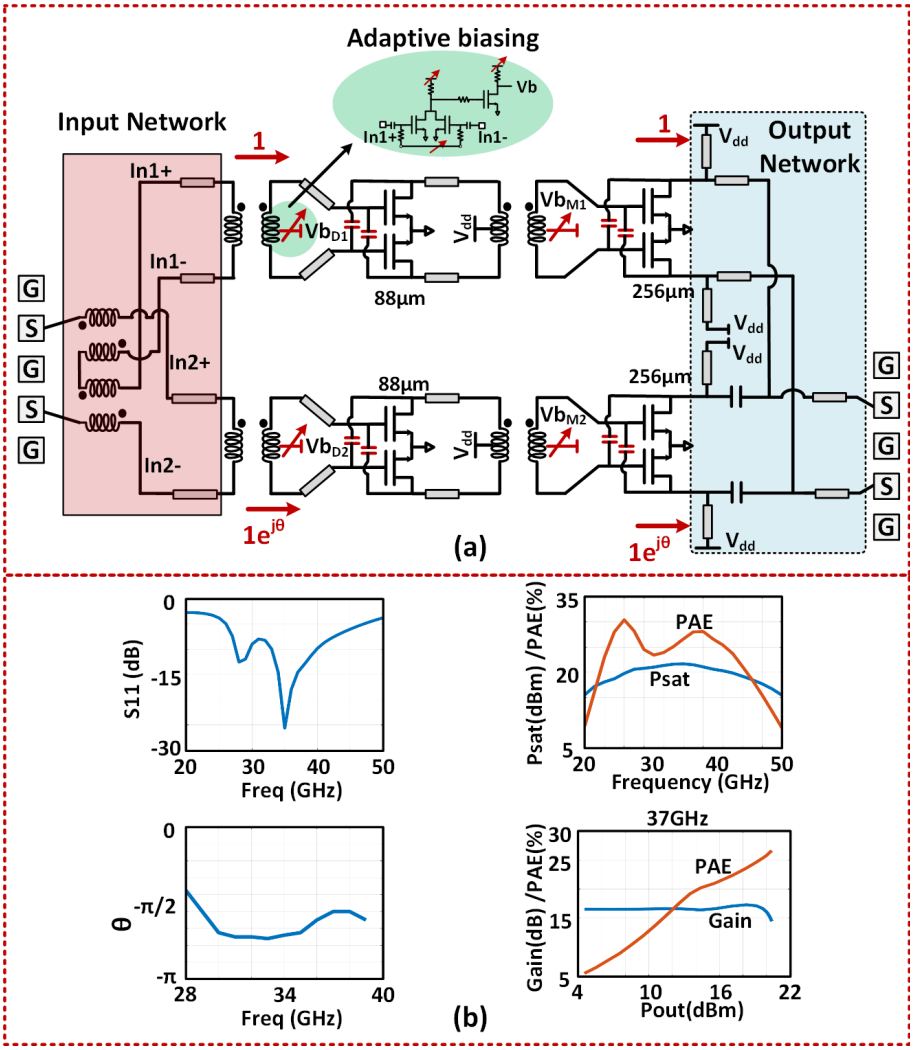

Fig. 19. VSWR-agile PA. (a) Complete circuit schematic. (b) Simulated performance.

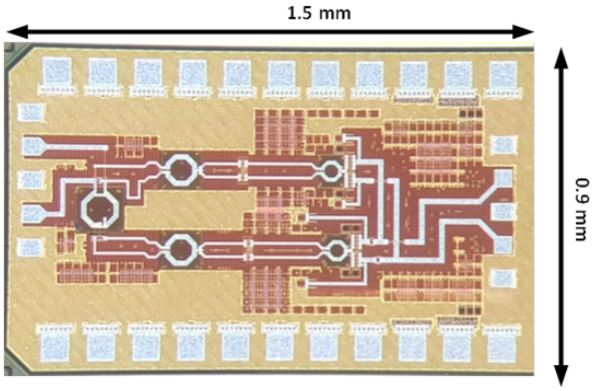

Fig. 20. Die photograph of the VSWR-agile PA.

1) Continuous-Wave Measurement: The PA achieves the peak PAE of 24% at 33 GHz and a $P_{\text{sat, }-1\text{ dB}}$ bandwidth span 26–42 GHz (47%), as shown in Fig. 21. The measured large-signal performance of the PA across 26–42 GHz (including 5G bands of 28/37/39 GHz) is shown in Fig. 21. The PA delivers P_{sat} of 19/19.6/19.2 dBm with the PAE of 21.6%/21.9%/21.7% and $P_{1\text{ dB}}$ of 19/16/18.1 dBm at 28-/37-/39-GHz bands, respectively. The performance of the PA across the 6 dB and 9.6 dB PBO levels is also shown in Fig. 21(a).

The architecture allows Doherty-like operation over the band. As the back-off is varied by more than 9.6 dB (PAPR for 64-QAM OFDM), linearity is maintained and efficiency is enhanced considerably, as shown in Fig. 21. As shown in the figure, the PA also achieves high PAE at PBO levels, with up to 3.35× and 4.84× enhancement in PAE at the PBO levels of 6 and 9.6 dB over the class-A operation (with PAE at the peak power levels remaining the same) across the frequency range. Fig. 21 also shows the measured AM–PM distortion across the various bands. The high AM–PM degradation at 28 GHz is due to the limited dynamic range of the predriver amplifier used in the measurement setup. The measurements are carried out for two different chips, which shows a similar performance, demonstrating the robustness of the design.

2) Modulation Measurement: The measured PA performance with 64-QAM OFDM modulation with the 2-GHz

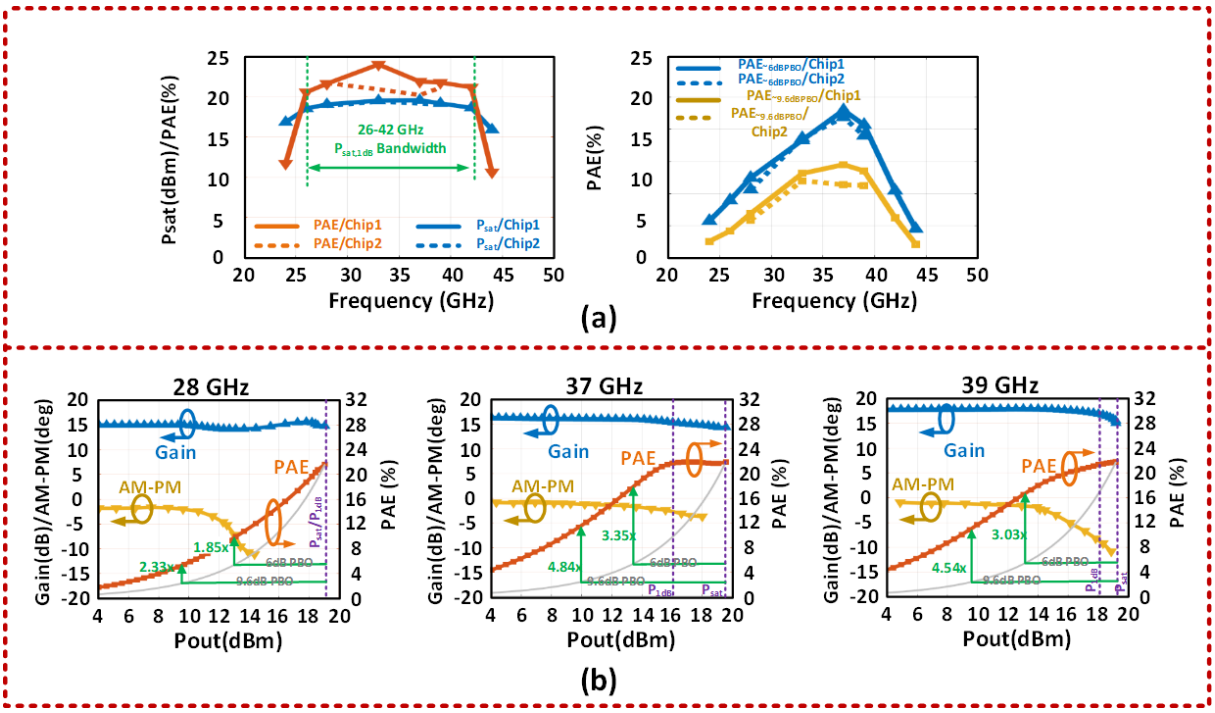

Fig. 21. Large-signal measurements. (a) Performance across 26–42 GHz for the two measured chips. (b) Performance at 28/37/39 GHz with a 50-Ω load. The class-A curve with PAE similar to the measured chip at peak power level is shown in gray for each of these plots for comparison.

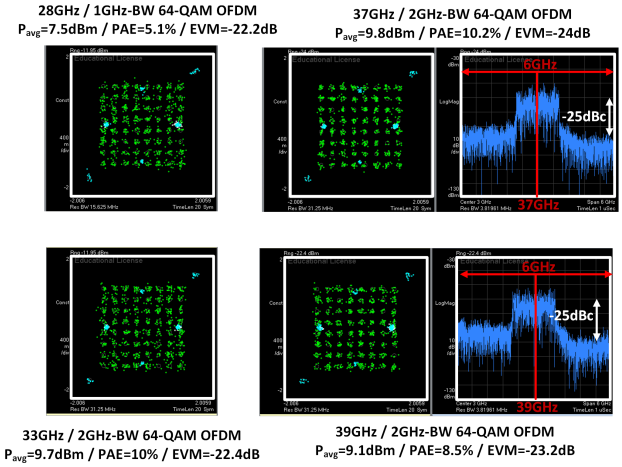

Fig. 22. Modulation measurement with 64-QAM OFDM across 26–42-GHz bands.

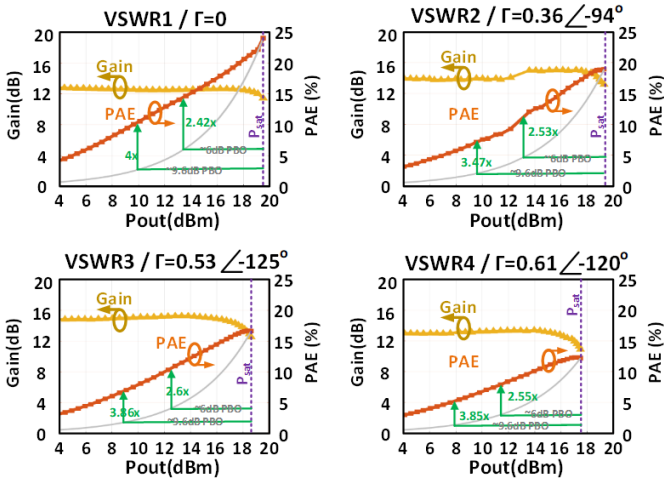

Fig. 23. Performance across VSWR loads up to VSWR 4:1 at 33 GHz. Class-A curve is shown in gray.

bandwidth across the 5G bands 28–40 GHz is shown in Fig. 22. At 37 GHz, the PA achieves 9.8-dBm average output power at a high PAE of 10.2% and an EVM of −24 dB.

3) VSWR Tolerance: To evaluate the VSWR tolerance of the architecture, measurements are carried out using a fundamental load tuner from Focus-Microwaves. Since the PA is differential, we use an external balun to convert the differential output to single-ended output for VSWR measurements. The performance of PA under load mismatch is shown in Fig. 23. The PA is tested across different loads with VSWR 1:1, 2:1, 3:1, and 4:1. The PA shows robust performance across all of them with ∼2-dB power degradation at the VSWR 4:1 load. The PA also maintains a Doherty-like performance at the back-off even when operated with up to VSWR 4:1 loads. For the load with $\Gamma = 0.36\angle -94°$ (VSWR 2:1), PA shows the efficiency improvement of 2.53× at 6-dB PBO and 3.47× at 9.6-PBO, compared to classical class-A PA. Even with load mismatch up to a VSWR of 4:1, i.e., $\Gamma = 0.61\angle -120°$, the PA demonstrates PAE improvement of 2.55× and 3.85× over class-A operation at 6- and 9-dB PBO, respectively. The loss and the phase mismatch between the two paths of the external balun restricted the points of measurement on the Smith chart. The results are in well accordance with the theoretical efficiency improvement analysis presented in Section III.

The measurements demonstrate a robust PA performance maintaining high linearity and back-off efficiency

	This Work	S.Hu ISSCC'17	S.Shakib ISSCC'17	S.N.Ali ISSCC'18	T.Li RFIC'18
Frequency of Operation (GHz)	26-42	26-44	28	28	23.5-41
Technology	65nm CMOS	0.13µm SiGe	28nm CMOS	65nm CMOS	45nm CMOS SOI
Architecture	Broadband Doherty like operation across frequencies	Multiband Doherty	Dual Resonance Transformer Matching	Transformer-based AM-PM Correction	Hybrid of Continuous Class F/F^{-1}
Supply (V)	1.1	1.5	1.1	1.1	
Peak P_{sat} (dBm)	19.6 @33G	17.1@37G	15.1	15.6	18.6@28G
P1dB (dBm)	19.1 @33G	15.5 @37G	13.7	14	16.6 @28G
Degradation at VSWR=4:1 load	2dB (after reconfiguration)	-	-	-	-
Peak PAE (%)	24 @33G	22.6@37G	33.7@27G	41	45.7
P_{sat} 1dB bandwidth	26-42 (47%)	28-42 (40%)	below27G to above30G *	26-31*	23.5-41 (54%)
$\frac{PAE_{-6dB\ PBO}}{PAE\ (pk)}$	0.84 @37G	0.73@37G	0.45*	0.41*	0.44*
$\frac{PAE_{-9.6dB\ PBO}}{PAE\ (pk)}$	0.54 @37G	0.44 @37G*	0.24*	0.17*	0.22
Modulation/ Bandwidth/Pout/ PAE	64-QAM OFDM/ 2GHz / 10dBm/ 10.2% @ 37G	64QAM/ 0.5GSps/ 9.2dBm/- @37G	64-QAM OFDM/ 800MHz/ 6.7/11	64QAM/ 340MSps/ 9.8/18.2	-
Area (mm^2)	1.35	1.76	0.23**	0.24	0.14**

*Estimated from the plots. **Active chip Area.

Fig. 24. Comparison table with state-of-the-art mm-Wave PAs with VSWR agility.

enhancement against VSWR events at 33 GHz up to 4:1 variations. The comparison table with the recent mm-Wave PAs is shown in Fig. 24, in which this works demonstrates VSWR agility in comparison to other reported works.

VII. Conclusion

In this article, we present a generalized multi-port network synthesis approach for enabling reconfigurability across frequency, back-off, and VSWR in a PA architecture. The method presents a general treatment of exploiting mutual interactions of an array of mm-Wave DACs in an asymmetric mm-Wave combiner synthesizing the optimal impedances for efficient operation across the aforementioned variations. As proofs of concept, two silicon-based PAs are presented in a 65-nm bulk CMOS process across 26–73 GHz. The first chip operates across 37–73 GHz demonstrating peak P_{sat} of 19.3 dBm with η_{out} of 40% at 50 GHz and peak $\eta_{\text{out, 6 dB}}$ of 25% at 64 GHz. The second chip operates across 26–42 GHz with $P_{\text{sat}} > 19$ dBm and PAE $> 20\%$ and with up to $3.35\times/4.84\times$ enhancement in PAE at 6-/9.6-dB PBO levels, even under varying VSWR conditions.

Acknowledgment

The authors would like to thank Krishnanshu Dandu (Texas Instruments), Kaushik Dasgupta (Intel), Saeid Daneshgar (Intel), and Khurram Wahid (NXP) for technical discussions. The authors would also like to thank Vince Mallette from Focus Microwaves for high-frequency harmonic load–pull tuner, and Jeremy Dunworth, Qualcomm, for technical discussions.

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