# Versatile Dual-Receiver 94-GHz FMCW Radar System With High Output Power and 26-GHz Tuning Range for High Distance Applications

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***Abstract*— Airborne applications demand exceptional overall radar system performance and eminently high output power for high range target detection. The frequency modulated continuous wave (FMCW) radar system presented in this article is capable of achieving this task due to its high output power at 94-GHz center frequency with over 26-GHz tuning range. Nevertheless, the radar still provides a small form factor and low power consumption of 4.25 W at 5 V single Universal Serial Bus (USB) supply. The key system component is a Silicon Germanium (SiGe) bipolar complementary metal-oxide-semiconductor (BiCMOS) monolithic microwave integrated circuit (MMIC) that contains a 94-GHz voltage-controlled oscillator (VCO), and a 27-GHz VCO for dual-loop phase-locked loop (PLL) stabilization, a power amplifier (PA), and two receive mixers. It generates frequency ramps between 83- and 109-GHz with a maximum output power of 19.7 dBm at its output after the bond wires on the printed circuit board (PCB) and 14.8-dBm output power at the radar's transmit (TX)-waveguide WR-10-flange. The sensor was also tested in a temperature range from −40 °C to +70 °C with menial deviation. Thus, the system offers high system dynamic range and far distance target detection range. Following a detailed system description, we finally present the FMCW range and Doppler measurements performed with the presented radar sensor as well as the application on unmanned aerial vehicles (UAVs) for flight altitude control and as airborne collision avoidance system (ACAS).**

***Index Terms*— Airborne, BiCMOS, Doppler, FMCW, high range, monolithic microwave integrated circuit (MMIC), passive components, phase-locked loops (PLLs), power amplifiers (PAs), radar, radar transceivers, silicon germanium (SiGe), substrate integrated waveguide (SIW), unmanned aerial vehicle (UAV), vertical take-off and landing (VTOL), waveguides (WVGs), W-band, WR-10.**

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## I. Introduction

ACHIEVING sufficient output power of the transmitted electromagnetic wave in radar systems is, besides other key characteristics such as high transmitter-receiver (TX–RX)-isolation, high receiver sensitivity, or low total receiver noise factor, one of the essential attributes to reach high system dynamic range and thus high detection range. In particular, in SiGe bipolar technologies producing high output power is more challenging than in modern III-V technologies due to its lower transistor breakdown voltages [1], [2]. However, SiGe technologies offer a higher level of integration, lower cost, very little performance variation between chip samples, and in this case, also CMOS integration [3].

For high detection range in airborne applications, this work demonstrates a quasimonostatic 94-GHz FMCW radar system with one transmitter and two receivers with 14.8-dBm output power at the radar's TX-waveguide port and over 26 GHz of phase-locked loop (PLL)-stabilized frequency modulation. By deembedding the passive components on the front end, the monolithic microwave integrated circuit (MMIC) output power behind the bondwires on the printed circuit board (PCB) was determined to be 19.7-dBm indicating a power added efficiency (PAE) of the PA of over 19% with less than 500 mW of power dissipation.

The presented radar system was developed to address the challenging demands for high detection range and overall system performance for airborne radar. One possible application is operation as a landing assistance radar in severe weather conditions for vertical take-off and landing (VTOL)-aircrafts. Another fielding scenario that we demonstrate in Section VI-A is as a flight altitude control radar and airborne collision avoidance system on unmanned aerial vehicles (UAVs).

The two coherent receiver channels are used to improve the system's signal-to-noise ratio (SNR) by up to 3 dB (depending on measurement scenario and calibration) and for target angular estimation.

For the implementation of the transceiver MMIC, the automotive qualified production technology B11HFC by Infineon Technologies AG was used, which is a 130-nm-BiCMOS

Fig. 1. Photograph of the dual-receiver 94-GHz radar system (right) with high output power and high bandwidth for high detection range and a small form factor realization with one transmitter- and one receiver-channel (left).

TABLE I
TECHNICAL SPECIFICATIONS OF MMW-RADAR SENSOR

| | |
|---|---|
| Radar sensor type | PLL-stabilized W-band FMCW |
| Stabilized frequency range | 83 GHz to 109 GHz |
| FMCW ramp width | 26 GHz (27 %) |
| Phase noise (in-loop) | -81 dBc/Hz @ 10 kHz |
| Phase noise | -87 dBc/Hz @ 1 MHz |
| Output power | 19.7 dBm @ PCB Bond-Landing Pads |
| Output power | 14.8 dBm @ WR-10 Flange |
| System dynamic range | 82 dB† |
| Antenna ports | 1TX/2RX – WR-10 |
| MMIC power consumption | typ. 850 mW |
| Sensor power consumption | typ. 4.25 W |

† The system dynamic range was measured as the difference between target peak and noise floor using a 10 $m^2$ @ 94 GHz corner at 5 m distance with a 1 GHz FMCW-chirp over 8 ms.

SiGe:C technology with an $f_T/f_{max}$ of 250/370 GHz [3], respectively.

Fig. 1 shows the complete radar system in two form factors, both with one TX-antenna and the left one with one RX-antenna and the right one with two RX-antennas. The key performance parameters of the presented system are listed in Table I. The antennas are implemented as dielectric lenses for a high antenna gain and a small half power beamwidth (HPBW).

## II. RADAR SYSTEM ARCHITECTURE

### A. Overview

The dual receiver FMCW radar at 94 GHz consists of three building blocks as shown in Fig. 2. On the left, the digital back-end contains the radar control features and power supply, such as the microcontroller ($\mu$C), Universal Serial Bus (USB) interface, direct current (dc)–dc converters, low-dropout (LDO) regulators, low phase noise (PN) reference oscillator (VCXO) for the $\mu$C and the PLLs, antialiasing filters with variable gain, and analog-to-digital converters (ADCs) for intermediate frequency (IF)-signal sampling.

On the right-hand side of the block diagram, the front-end includes the PLLs for the radar MMIC's voltage-controlled oscillators (VCOs), the 94 GHz radar MMIC, IF-amplifiers for both receiver channels with bandpass behavior, a digital-to-analog converter (DAC) that controls the radar's output power, and transitions for the 94-GHz signals between the MMIC and the WR-10 waveguide ports for antenna connection.

The third key component is the radar MMIC, which consists of VCOs for signal synthesis and PLL stabilization, a local oscillator (LO)-distribution network, two receiving mixers, a PA in its TX-path, followed by bond wire compensation networks (see Fig. 6(a) in [4]), and also static frequency dividers and mixer for PLL-stabilization. Section III presents the transceiver MMIC in more detail.

The complete radar system is powered by a single USB 3.0 port, consuming 5 V and 850 mA or 4.25 W. The implemented personal computer (PC) communication uses a high-speed USB 2.0. No additional cables for power supply or communication are required.

Particular emphasis was laid on the design of the power supply for the different system components in terms of low noise supply voltages [5]. A similar system architecture was realized in [4], [6], [7] with an 80-GHz MMIC fabricated in the predecessor technology of B11HFC named B7HF200 with one receive channel and also in [5] for a monostatic D-band radar sensor with the MMIC also fabricated in B7HF200. With similar systems as in [8], [9], micrometer accuracy and nanometer stability were demonstrated. For this work, the knowledge and experience from those previous projects were enhanced and transferred from Infineon's predecessor technology B7HF200 into their current technology B11HFC in which all on-chip components had to be redeveloped. Furthermore, in this work, the recent system concepts were improved by shrinking the MMIC die size while adding additional functionality like a second RX-channel and a PA on the MMIC, and also a DAC for output power control and new passive components for low loss high-frequency signal routing between MMIC and antennas on the PCB.

The radar sensor must be connected to a USB 3.0 host device, e.g., a PC or field programmable gate array (FPGA), which triggers the FMCW radar operation and receives and processes the radar's data. When the radar sensor is powered up, the microcontroller $\mu$C initializes the sensor and programs the PLL ICs for stable and low phase noise operation. After initialization, the USB host device triggers an FMCW measurement which leads to the $\mu$C sending a trigger signal to the fractional-N PLL of the 94-GHz VCO to produce a frequency sweep of a given bandwidth. The received IF-signals of both RX-channels are amplified, filtered, and sampled by the two-channel 16-bit/2 MSPS differential ADCs on the back-end. The acquired data are finally transmitted to the host device by the $\mu$C with USB-interface for further processing using MATLAB or other proprietary software, or in hardware by an FPGA.

The 100-MHz reference crystal oscillator CVSS-945 was chosen to provide extremely low phase noise combined with a small form factor. It is used as the $\mu$C-clock (divided-by-2), as reference-clock for both PLL ICs, and for the ADC (managed by the $\mu$C), so that the radar represents a completely coherent system. An HMC704 IC, which is a fractional-N PLL IC without sweeper functionality and with low phase

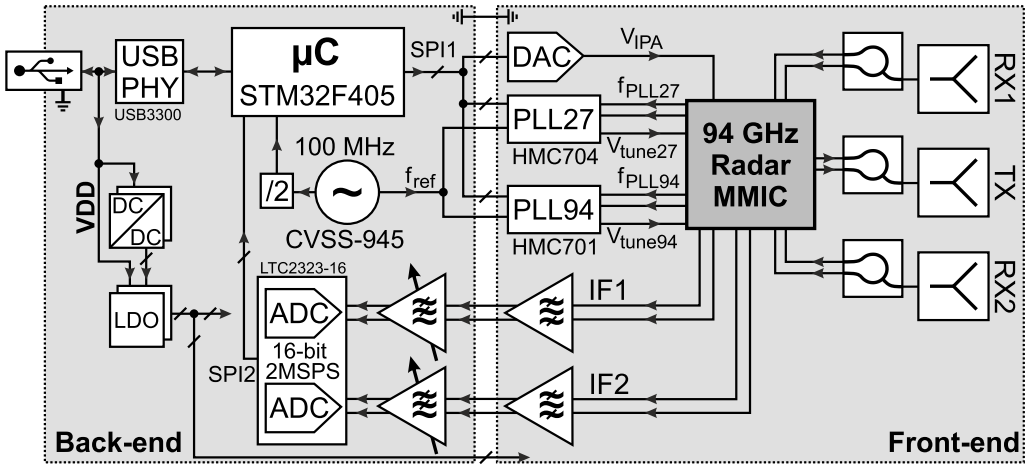


Fig. 2. Block diagram of the multistatic 94-GHz transceiver MMIC with PA and two receiver channels used in a dual-loop PLL for frequency stabilization.

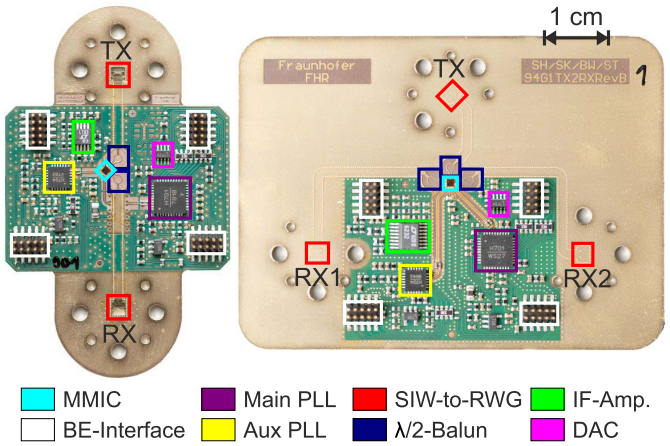


Fig. 3. Photograph of the multistatic 94-GHz FMCW front-end boards with transceiver MMIC, $\lambda/2$-Balun, SIW-to-RWG-transitions, PLL circuits for the 94-GHz VCO and for the 27-GHz-auxiliary-VCO and IF-amplifier, DAC, and back-end (BE)-interface. Left: compact front end with one RX-channel. Right: larger front-end version with two RX-antennas and channels, respectively.

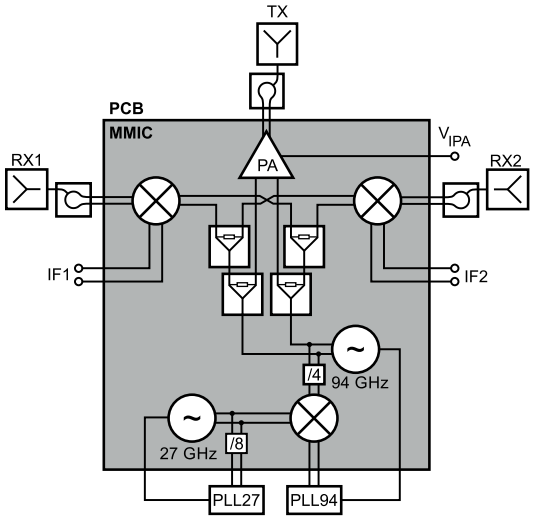


Fig. 4. Block diagram of the bistatic 94-GHz transceiver MMIC with PA and two receiver channels together with dual-loop PLL concept for frequency stabilization.

noise, was chosen to stabilize the constant 27 GHz-VCO. Here, no sweeper functionality is required. For the 94 GHz-VCO, that modulates the linear frequency ramps an HMC701 was implemented, which is also a fractional-N PLL with low phase noise together with sweeper functionality for linear FMCW ramps.

The routing of the millimeter-wave signals is done with highly optimized wideband structures with an additional focus on low loss, feasibility, low cost, and versatility. Both realized front-ends are shown in Fig. 3. For maximum flexibility the standardized WR-10 interface is used [10], [11]. Thus, the flange of the TX- and one/two RX-channels are milled into the front-end. The spacing of the flanges needs to be large enough for sufficient spacing between high gain dielectric lens antennas which results in long transmission lines (TRLs) connecting the antennas to the MMIC. To couple from the PCB into the rectangular waveguide (RWG) of the antennas a substrate integrated waveguide (SIW)-to-RWG transition was developed, which is directly fabricated into the PCB substrate. Low cost and low manufacturing effort are maintained with this solution. It is clearly visible by the orientation of the screw holes and dowel pins of the dual-RX front end that the angle of polarization is tilted by $\pm 45°$ with respect to the TX channel for polarization-dependent measurements on the cost of reduced system dynamic range (see Fig. 3). The SIWs are connected to the MMIC by $\lambda/2$-Baluns that are located as close to the MMIC as possible. The position of both PLL ICs and the IF-amplifier is given by the back-end interface that was kept from previous radar systems for good interoperability.

## III. Transceiver MMIC

### A. Architecture

Fig. 4 shows the block diagram of the transceiver MMIC and the photograph of the fabricated MMIC is given in Fig. 5. The MMICs signal-routing and circuit blocks are fully differential.

The 94-GHz VCO (1) is generating output signals between 83 and 109 GHz with an output power between 10 and 14 dBm. An LO-distribution network made of Wilkinson dividers (6) distributes its LO-output signal to the

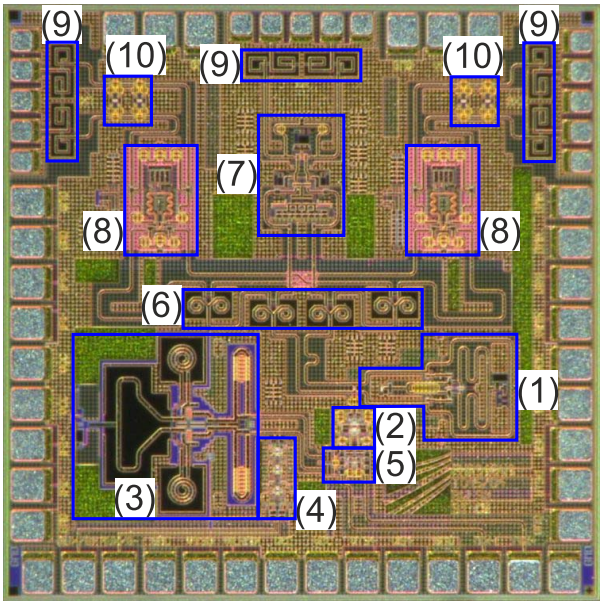


Fig. 5. Chip photograph of the bistatic 94-GHz transceiver MMIC (1.5 × 1.5 mm$^2$). (1) 94-GHz VCO, (2) Static by-4-divider, (3) 27-GHz VCO, (4) Static by-8-divider, (5) PLL-mixer, (6) LO power distribution network, (7) 94-GHz PA, (8) RX-mixers, (9) Bond compensation network, (10) RX-attenuators (2 × 6 dB per RX-channel).

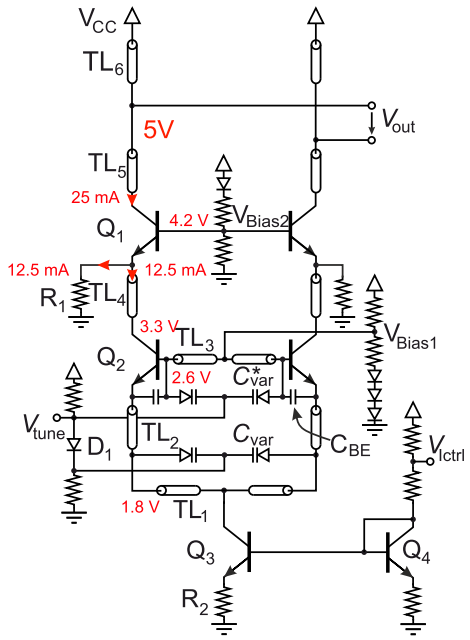


Fig. 6. Schematic of the 94-GHz VCO dual-varactor concept for high bandwidth.

receiving Gilbert-mixers of the two RX-channels (8) and the PA (7) in the TX-channel. The Wilkinson divider network is designed with unequal power split, so that the VCOs differential output signal is attenuated by 3 dB until it reaches the PAs input and 6 dB to each LO-input of the RX-mixers. This asymmetrical LO-distribution helps to provide sufficient input power for the PA to be saturated and hence delivering its maximum output power. All 94-GHz MMIC-to-PCB interfaces include compensation networks for the bondwires and pads (9), which also provide ac-coupling for the 94 GHz signals and an electrostatic discharge (ESD)-path to ground. The compensation network topology can be seen in [4, Fig. 6(a)]. A differential bondwire transition was chosen because of lower series resistance and inductance of the two slightly coupled parallel bondwires compared to a single wire in a single-ended (SE) configuration and thus easier matching and lower loss. Of course the differential-to-SE coupler/balun could also be realized on-chip with lower loss than the realization shown on the PCB but was not integrated due to limited chip area and easier differential bondwire compensation. Furthermore, radiation losses and crosstalk between TX- and RX-channels is reduced by differential bondwire transition compared to a SE transition. To improve TX-RX-isolation the TX-path lies orthogonally to the two RX-paths. Larger spacing between the MMICs RX-channels and the TX-channel would be desirable but the bottom part of the MMIC together with the bond pad frame is needed for PLL-/IF-/power- and control-interfacing because a single layer PCB with 1-mm copper backside cladding was used for good thermal management which means that signal crossings of radio frequency (RF)-signal-paths and PLL-/dc-signals is not advisable. Measurements showed no false target appearance due to low TX-RX-isolation, indicating proper channel separation.

The 94-GHz LO-signal is frequency-divided by four (2) and then mixed upside down by a down-conversion mixer (5) with the signal of a 27-GHz auxiliary-VCO (3). The mixer feeds its output signal to the PLL that stabilizes the 94-GHz VCO by producing a regulated tuning voltage $V_{\text{tune94}}$ (compare Fig. 2). By mixing in reverse frequency position of the 94/4-GHz signal with the signal of the 27-GHz VCO, the PLL's loop gain variation is reduced by which the PLL is capable of stabilizing the complete 26-GHz bandwidth of the 94-GHz VCO [4].

The 27-GHz VCO is also stabilized by a dedicated PLL that generates the VCOs tuning voltage $V_{\text{tune27}}$. Therefore, its output signal is frequency-divided by eight (4) and then fed to the respective PLL (see Fig. 2).

The MMIC also contains two times 6-dB attenuators in each RX-channel for low range applications (large RX-signal levels). The attenuators can be activated or deactivated by cutting aluminum fuses with a laser cutter, which helps to increase the input compression point of the receiving mixers that might be exceeded by close targets or high RX-input power, respectively. For a high detection range, the attenuators were deactivated. The TX-output power can be adjusted by controlling the PAs current with the analog control voltage $V_{\text{IPA}}$, which is provided by a DAC on the front-end board (compare Fig. 2). The VCOs, RX-mixers, and PAs can be shut down by setting their dc-current to nearly zero by external control voltage pins.

All circuits and RF-/IF-signals on the MMIC are differential unless otherwise mentioned. In addition, some OFF-chip components like the IF-amplifier chain and the ADC are differential for superior interference immunity.

### *B. Voltage-Controlled Oscillator*

The ultra-wideband VCO architecture with 94-GHz center frequency is based on the architecture shown in Fig. 6.

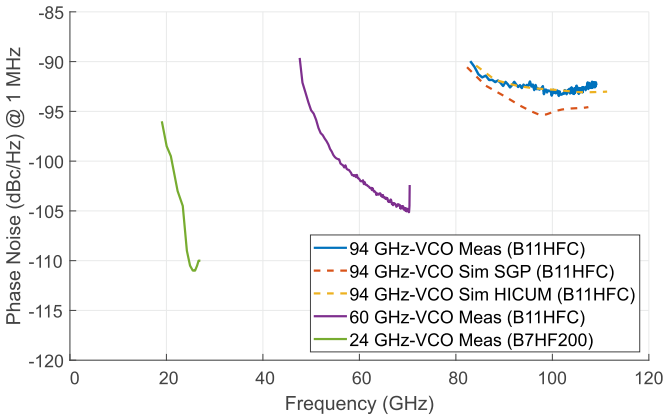


Fig. 7. Phase noise measurement of the 94-GHz VCO compared to measurements of an 24-GHz VCO [16] and 60 GHz [17] in the same and predecessor SiGe technology, respectively.

The differential Colpits-VCO uses two differential varactor-pairs at the VCO-core's base and its emitter of $Q_2$ for improved bandwidth [12], [13]. It generates frequencies between 83 GHz, with an output power of 14 dBm, up to 109 GHz with 11 dBm. By varying the tuning voltage $V_{\text{tune}}$, the junction capacitance of the varactors, which are reverse biased, changes, resulting in a change of the VCO core resonance impedance and thus in a change of frequency. The resonance impedance is mainly given by $\text{TL}_3$, $C_{\text{BE}}$, $C_{\text{var}}$, and $C^*_{\text{var}}$. The VCO-core uses 12.5 mA of current per side while the cascode stage $Q_1$ that decouples the output from the core against load—pull effects [14] is biased with additional 12.5 mA adding up to 25 mA for the output cascode stage. This serves the purpose of better linearization of the VCO-core because its load impedance decreases for higher current of the cascode-stage and also load—pull effects can be stronger reduced with this technique [12], [15]. The minimum phase noise at 1 MHz offset is $-92.5$ (dBc/Hz) at 102 GHz.

In Fig. 7, the measured phase noise of the 94-GHz VCO is shown in comparison with the phase noise measurements of a comparable 60-GHz VCO [16] which was also realized in the B11HFC technology and a 24-GHz VCO [17] in the B7HF200 technology which is the predecessor of B11HFC. All measurements were taken at the SE divide-by-4 section output and 50-Ω match at the VCOs' RF-outputs with an Rohde & Schwarz FSW67 and then calculated back to the VCO's output by adding 12 dB from the by-4-division. The VCO's outputs were not measured directly because of load—pull effects due to long cabling influences the phase noise. As can be seen in the plotted graph, the phase noise of the 24- and 60-GHz VCOs rises for their lower frequencies limits, whereas in comparison the phase noise curve of the 94-GHz VCO is notably flat.

Particularly in long range measurements where low phase noise for high autocorrelation is mandatory, a low and flat phase noise curve helps to receive good system measurement performance over a large frequency range compared to the 24- and 60-GHz VCOs where a rise in phase noise of about 15 dB would limit system performance and utilizable bandwidth.

The main influence for flat phase noise behavior over frequency of the 94-GHz VCO compared to the previous designs of the 24- and 60-GHz VCOs is the relationship between the bias current of the tuning network and the junction area of $D_1$. This relationship of current density has to be in a comparable region as for the emitter area of $Q_2$ together with its bias current of 12.5 mA in this case. If the forward voltage drop of $D_1$ is significantly different from the base–emitter voltage $V_{\text{BE}}$ of $Q_2$ either the varactor $C_{\text{var}}$ or $C^*_{\text{var}}$ starts reaching its forward-active region first for low tuning voltages. This leads to an immense decrease of the VCO-core's quality factor due to the changing varactors small-signal resistance and thus to a substantial phase noise increase as can be seen in Fig. 7 for the 24- and 60-GHz VCOs especially for low frequencies which correspond to low tuning voltages where one of the varactors comes close to its active region. This is due to the voltage drop over the shift-diode $D_1$ being unequal to the voltage drop over the base–emitter diode of $Q_2$.

Also, the bias network of the tune voltage $V_{\text{tune}}$ with bias current through the diode $D_1$ and the two resistors in series against $V_{\text{CC}}$ and ground influence the VCO's PN. There exists a tradeoff between thermal noise of the diode and the two resistors which is determined by (2) and the diode's shot noise from (3). The thermal noise at this node is high for small bias currents or large resistors and the shot noise rises for high bias currents and low resistor values. With an open tune voltage node at $V_{\text{tune}}$ (high impedance due to no PLL or loop filter connected), the influence of the thermal noise on the VCO's phase noise is stronger than for a low impedance tune voltage node

$$r_{\text{Diode}} = \frac{\partial V_D}{\partial I_D} \approx \frac{nV_T}{I_{\text{D,Bias}}} \tag{1}$$

$$v_{\text{Noise,eff}} = \sqrt{4k_B \cdot T \cdot r_{\text{Diode}} \cdot BW} \tag{2}$$

$$i_{\text{Noise,eff}} = \sqrt{2I_{\text{D,Bias}} \cdot e \cdot BW}. \tag{3}$$

However, if the PLL with its loop filter is connected to the tune voltage potential of the VCO, the influence of the noise voltage of the two resistors gets filtered because of the now low impedance of this node and does not start to be relevant until the resistors reach several 100 kΩ (less than 10 $\mu$A of bias current through $D_1$). But the shot noise which influences the potentials of the two varactors differentially, still affects the total noise that is modulated on the 94-GHz carrier signal and results in high PN. Also the differential thermal noise from the diode $D_1$ can influence the differential voltage over the two varactors if its small signal resistance gets too large for very low bias currents (1, 2). In conclusion, the current of the bias network should be chosen in a way, in which the influence of both differential noise sources of $D_1$, the shot noise and the thermal noise, are at their common minimum, and also in which the thermal noise of the resistors is negligible.

Including bias networks, the VCO's power consumption is 300 mW at 5-V supply voltage and 60-mA bias current.

### *C. Power Amplifier With Load Line Matching by Transistor Dimensioning*

The PA design is based on the architecture in [18]. Here, the PA's operating frequency of 24 GHz is lower compared to

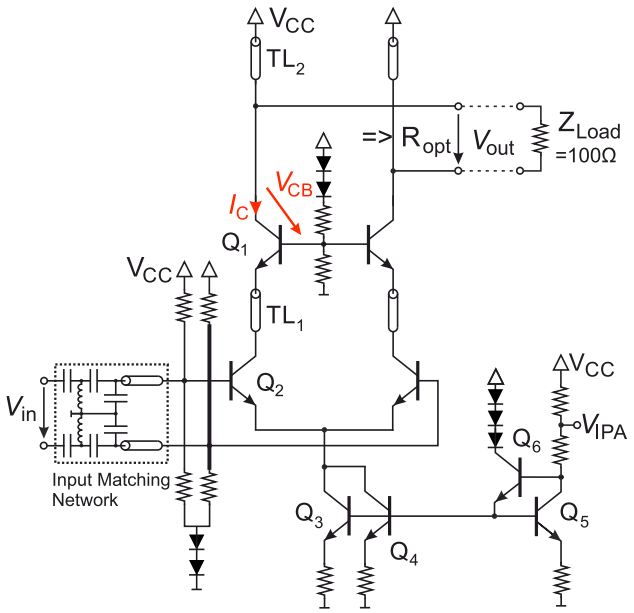


Fig. 8. Schematic of the 94-GHz PA with optimized load line matching by transistor dimensioning.

94 GHz in this work, meaning that insertion loss of passive elements, matching-, and bonding-networks are less critical than at 94 GHz. Thus, the design was modified to counteract the problems that are accompanied by operating close to very high frequencies, like higher loss and less gain.

The PA's schematic is given in Fig. 8. It operates with a 98-mA supply current at 5 V or 490 mW, respectively. It is based on a differential common-emitter stage with a wideband LC-matching network providing proper input matching over the complete frequency range given by the 94-GHz VCO. The differential cascode output stage is the most critical part of the PA. Its purpose is to generate the maximum current and voltage amplitude to be delivered to the load impedance $Z_{\mathrm{Load}}$ or $R_{\mathrm{opt}}$, respectively.

Considering the dynamic load line for the cascode stage's output and its limits from [18], the optimal load impedance has to be resistive. As a result, the dynamic load line gets linear, which reduces the risk of running into the high current or avalanche breakdown regions of $Q_1$ by staying in the transistors' safe operating area (SOA). Therefore, $\mathrm{TL}_2$ is used with inductive behavior that compensates the collector-base capacitance $C_{\mathrm{CB}}$ of $Q_1$ at 94 GHz. $\mathrm{TL}_2$ represents a 137 $\mu$m long 50 Ω TRL which has a low simulated loss of around 0.14 dB and is a very compact way of resonating with the $C_{\mathrm{CB}}$. The low loss together with proper transistor layout induce a high quality factor of the PA's resonant output which helps to generate and transmit maximum output power in context to the description in [18] Section II-C.

The optimum load resistance $R_{\mathrm{opt}}$ for the cascode stage is determined by the maximum voltage and current limits shown in the dynamic load line and thus by the high current and avalanche breakdown limits. The linear dynamic load line also implies that the cascode transistor generates $\hat{V}_{\mathrm{CB,max}}$ and $\hat{I}_{\mathrm{C,max}}$ in phase or at the same time with its resistive load conditions.

The maximum voltage amplitude $\hat{V}_{\mathrm{CB,max}}$ that can be generated by the cascode transistors is limited by the avalanche breakdown limit of the collector-base diode of $Q_1$ and the maximum current amplitude $\hat{I}_{\mathrm{C,max}}$ is limited by the high current limit. Besides that, $\hat{I}_{\mathrm{C,max}}$ equals the maximum current amplitude $\hat{I}_{\mathrm{out,max}}$ through the load impedance $Z_{\mathrm{Load}}$ or $R_{\mathrm{opt}}$, respectively.

The high current limit starts at currents that relate to current densities higher than the transistor's current density $j_{\mathrm{C,opt}}$ for maximum $f_T$, which means that the transistor's dc-collector current $I_{\mathrm{C,dc}}$ for $Q_1$ and $Q_2$ must be chosen below the optimum current density $j_{\mathrm{C,opt}}$ because the peak collector-current through $Q_1$ and $Q_2$ for the dynamic large-signal rises to $2I_{\mathrm{C,dc}}$ or $2\hat{I}_{\mathrm{C,max}}$. Previous PA designs showed that dc-current values that correspond to 50–75% of $j_{\mathrm{C,opt}}$ result in stable operation of the PA even at harsh environment condition like 120 °C chuck temperature $\vartheta$. The shown PA in this work is dc-biased with 44.5 mA per side of the differential architecture or 89 mA at the current source $Q_{3,4}$. The transistors of the common-emitter input stage $Q_2$ and the cascode stage $Q_1$ each consist of 4 fingers with 10 $\mu$m length. The optimum current density $j_{\mathrm{C,opt}}$ for maximum $f_T$ equals 1.5 (mA/$\mu$m), which means that the transistors are dc-biased at 74.1% of $j_{\mathrm{C,opt}}$.

Because of the differential architecture and the virtual ground at the cascode base, the base can be assumed to be ac-shorted to the ground. Therefore, the avalanche breakdown limit for the B11HFC's high-speed transistors with base shorted to the ground is typically $\mathrm{BV}_{\mathrm{CES}}$ of 5.3 V. Hence, the maximum output voltage of one side of the differential cascode output is determined through the avalanche breakdown voltage $\mathrm{BV}_{\mathrm{CES}}$ and the base–emitter voltage in the PA's operating point $V_{\mathrm{BE}}$, shown in (4) and (5). Resulting from this limit the maximum output voltage that can be transferred to the load impedance is twice the maximum amplitude of the collector-base voltage $\hat{V}_{\mathrm{CB,max}}$ of one side of the differential PA's cascode stage, shown in (6). The maximum collector-base voltage $V_{\mathrm{CB,max}}$ of $Q_1$ implies that the maximum voltage amplitude of one side of the cascode stage is half as much

$$V_{\mathrm{CB,max}} = \mathrm{BV}_{\mathrm{CES}} - V_{\mathrm{BE}} \tag{4}$$

$$V_{\mathrm{CB,max}} = 5.3\,\mathrm{V} - 0.85\,\mathrm{V} = 4.45\,\mathrm{V} \tag{5}$$

$$\Rightarrow \hat{V}_{\mathrm{out,max}} = 2\frac{V_{\mathrm{CB,max}}}{2} = 2\hat{V}_{\mathrm{CB,max}} = 4.45\,\mathrm{V}. \tag{6}$$

For this purpose, the collector-base diode is biased at $V_{\mathrm{CB,max}}/2$. Because of the cascode base that is shorted to virtual ground for high-frequency signals but not for the dc-biasing, $\mathrm{BV}_{\mathrm{CES}}$ cannot be expected for dc-conditions. This fact must be considered in simulation because this leads to a negative dc-base current (around 2 mA per side of the cascode stage) that is capable of shifting the bias-voltage of the cascode base of $Q_1$. For this reason, the high current model (HICUM), which models among other parameters such as high current, avalanche, and self-heating effects, was used for all PA simulations.

In [18] the 100-Ω load impedance of the PA is converted by a load line matching network to the optimum load impedance $Z_{\mathrm{Load}}$ or $R_{\mathrm{opt}}$ of about 55 Ω. Even though the load line

matching network was realized by as few passive components as possible, it causes insertion loss to the PA's output, which is an even bigger problem in this work at 94 GHz.

For this reason, the load line matching network was omitted, meaning that the optimum load resistance $R_{\text{opt}}$ is chosen to be 100 Ω. By that, no additional insertion loss is added to the PA's output, but the possible output power, respectively, output current/voltage, that can be generated is now limited by $\text{BV}_{\text{CES}}$ or $\hat{V}_{\text{CB,max}}$, and $R_{\text{opt}}$ as shown in (7)

$$\hat{I}_{\text{C,max}} = \frac{2\hat{V}_{\text{CB,max}}}{R_{\text{opt}}} = \frac{4.45\,\text{V}}{100\ \Omega} \tag{7}$$

$$\hat{I}_{\text{C,max}} = 44.5\ \text{mA}. \tag{8}$$

The maximum collector current amplitude $\hat{I}_{\text{C,max}}$ of each side of the cascode stage $Q_1$ is identical with the maximum output current amplitude $\hat{I}_{\text{out,max}}$. This also predefines the maximum output power of the PA which is calculated using (9)

$$P_{\text{out,max}} = \frac{\left(\frac{2\hat{V}_{\text{CB,max}}}{\sqrt{2}}\right)^2}{R_{\text{opt}}} = \frac{(4.45\ V)^2}{2 \cdot 100\ \Omega} \tag{9}$$

$$= 99.01\ \text{mW} \tag{10}$$

$$\hat{=}\ 19.95\ \text{dBm}. \tag{11}$$

The architecture of the PA results in enhanced efficiency because additional losses at the amplifier's output can be avoided and also a high output bandwidth can be achieved (see Section V-A) without the conventional resonant load line matching networks in PA designs. However, the drawback is the limitation of output voltage and current by the differential 100-Ω interface and the transistor's SOA. To win back the freedom to choose output voltage and current, transformer-based matching is commonly used ON-chip but would result in additional chip area, insertion loss, and bandwidth limitations due to its resonant behavior. Also, the OFF-chip Balun could directly be integrated in the ON-chip transformer of the PA to save space on the PCB front end, but the SE bondwire transition would introduce higher insertion loss than the used differential bondwire interface with its slightly coupled bondwires as mentioned in Section III-A. Overall, the demonstrated approach of load line matching using transistor dimensioning is suitable if the chip area is limited and the produced output power from the given SOA of the transistors is sufficient for the desired application.

The PA does not exist as a breakout circuit, meaning that its performance parameters can solely be extracted from measurements of the radar system. However, the saturated output power and gain are derived from system measurements in Section V to the MMIC output behind the bondwires on the PCB-bondwire landing pads.

### *D. Down-Conversion Gilbert-Mixer*

The Gilbert-cell topology builds the foundation of the down-conversion receiving mixer that was matched with wideband LC-networks at the LO- and RF-ports. Even though the lower common-emitter stage of the Gilbert-mixer is often omitted for operation at very high frequencies as discussed in [19], a full Gilbert-cell like in [20] was used for the receiving mixer because the operating frequency at 94 GHz is far enough from $f_T$ of 250 GHz, thus offering higher gain and lower noise figure (NF). The used Gilbert-cell schematic can be found in [20]. It consumes 20 mA at 5-V supply voltage or 100 mW, respectively. The maximum level of the 94-GHz LO signal with approximately 4 dBm and about 0 dBm at 107 GHz is large enough to operate the upper four transistors of the Gilbert-cell as switches. This ensures a high conversion gain and good NF performance of the Gilbert-cell.

The received RF-signal is connected to the differential common-emitter stage of the mixer because the switching-quad operates as a cascode stage for the common-emitter input stage below, which reduces its Miller-effect and leads to better high-frequency performance. This performance enhancement is especially crucial for the RF-signal with its lower signal levels and leads to higher RF-to-IF-conversion gain. The simulated conversion gain and single-sideband (SSB) NF are at around 14 and 12.5 dB, respectively.

## IV. Passive Components

In order to achieve the maximum output power and low receiver NF, high effort was invested into the design of low loss passive interconnects between the MMIC's TX-output/ RX-inputs and the antennas on circuit board level. The front end is fabricated on a Rogers RT/duroid 5880 substrate with a $\varepsilon_r$ of 2.20 and $\tan\delta$ of 0.0009 at 10 GHz to ensure good RF-performance of the passive components. The substrate is coated with rolled copper (which provides low loss due to reduced surface roughness compared to electro-deposited copper) as the top-layer metal and a thick copper cladding with 1 mm thickness on the bottom side for bare die mounting of the MMIC inside a cavity which is milled from the topside. Because of the cavity, the MMIC's top surface is at the same level with the PCB's top surface for minimum bondwire length. The 1-mm backplane also allows milling the PCB-to-antenna interface directly into the board. The surfaces have been gold plated using an electroless nickel electroless palladium immersion gold (ENEPIG) process for high bond strength of bondwires and to achieve a high surface conductivity between the bottom side metal and the waveguide of the flanged antenna. This high-quality process and materials are chosen to compensate the long TRLs on the PCB, which were necessary for sufficient spacing between the TX- and RX-antennas. The long TRLs are solely mandatory due to antenna dimension. Usually, TX- and RX-antenna separation is increased to improve TX–RX-isolation, but the coupling of the dielectric lens antennas is sufficiently low even for minimal spacing due to differential and orthogonal TX- and RX-channels in the presented radar architecture. Also, the high gain or low HPBW of the antennas helps to reduce antenna coupling. Additionally, the TRL of choice is the SIW [21] for less insertion loss compared to microstrip lines or coplanar waveguides. The dispersive behavior of the waveguide does not affect the system for small bandwidth applications or can be corrected by post-processing (compare Section V-B).

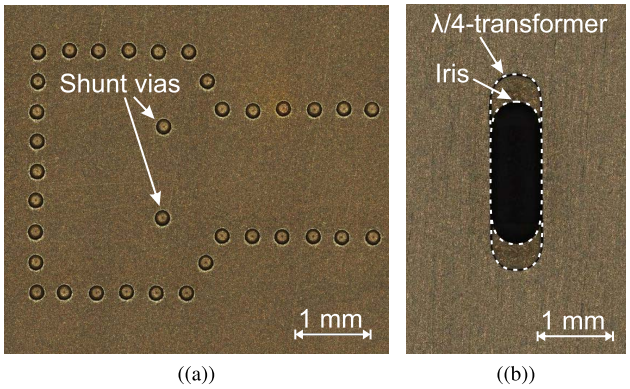


Fig. 9. (a) Top and (b) bottom view of SIW-to-RWG transition.

As can be seen in Fig. 3, passive wideband couplers were used as connection between the differential pads on the MMIC and the WR-10 flange for the antennas. The couplers were designed using full-wave electro-magnetic simulation in CST Microwave Studio and carefully optimized for the center frequency of the MMIC.

### A. SIW-to-RWG Transition

To couple from the SIW into the RWG, a wideband transition based on a dual-mode cavity resonator combined with a $\lambda/4$-transformer similar to [10] is used. The transition can be integrated in a RF PCB manufacturing process, and therefore, no additional assembly steps or components are necessary.

As can be seen in Fig. 9, the cavity is realized by via fences drilled as blind vias from the top layer into the thick-metal cladding and bottom layer of the substrate Fig. 9(a).

Additionally, two via-posts as inductive shunt elements are drilled [see Fig. 9(a)] from the top side and a waveguide iris is milled into the substrate from the bottom side [see Fig. 9(b)] to compensate the otherwise capacitive overall behavior of the waveguide bend. Since for equivalent cutoff frequencies the characteristic impedance for the fundamental mode, which is proportional to the respective waveguide height [22], a high impedance ratio must be matched for thin single-layer substrates with a WR-10 waveguide flange. Thus, a section of intermediate characteristic impedance which acts as an additional $\lambda/4$-transformer is milled into the backside copper [see Fig. 9(b)] from the bottom side on top of the iris. This waveguide-transformer allows matching the low characteristic impedance SIW to a standard WR-10 waveguide over a wide frequency range. By proper tuning of the length and width of the cavity, the resonant modes $TE_{120}$ and $TE_{310}$ with resonance frequencies

$$f_{lm0} \approx \frac{c_0}{2\pi\sqrt{\varepsilon_r}}\sqrt{\left(\frac{l\pi}{W}\right)^2+\left(\frac{m\pi}{L}\right)^2} \tag{12}$$

for $W, L \gg$ height $h$ are coupling from SIW into RWG within the passband. The measurement results are shown and compared to the simulation results in Fig. 10. The insertion loss of the back-to-back (B2B)-arrangement is less than 3 dB between 82 and 107.8 GHz. Here, the insertion loss of the long SIW is also included.

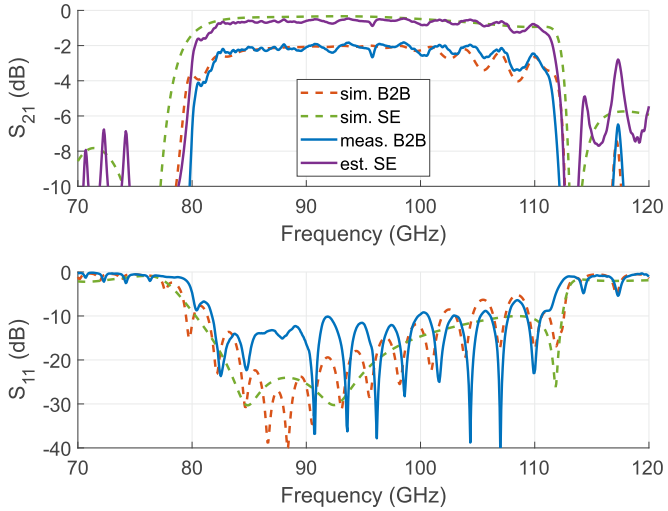


Fig. 10. Measurement results of the back-to-back (B2B)-configuration of SIW-to-RWG transition with compensated loss of feed lines on PCB due to necessity of WG-adapter spacing.

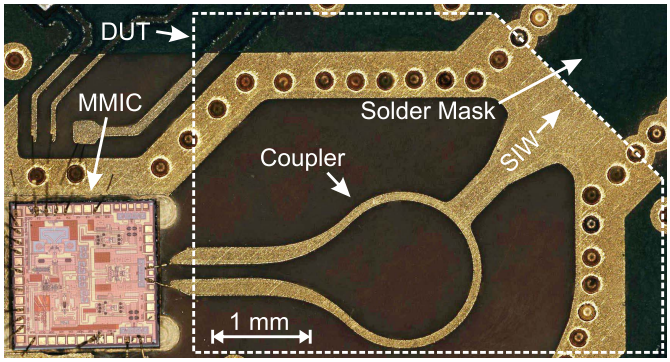


Fig. 11. Fabricated layout of the $\lambda/2$-Balun/Coupler combined with microstrip-to-SIW transition and MMIC in cavity with bondwires.

To estimate the insertion loss of the SE transition, the attenuation of the SIW feed line connecting the transitions on the PCB is deembedded by measuring B2B-arrangements with SIW lines of different lengths. Measurements indicate an insertion loss of 0.06 dB/mm for the SIW feed line. The insertion loss of a single transition has been estimated by subtracting the SIW feed line losses and dividing the remaining insertion loss by 2. This results in an insertion loss of less than 0.7 dB in a frequency range of 82–107.8 GHz, or 27% of relative bandwidth. This estimation is in good agreement with the SE-simulation (see Fig. 10, purple and green curve). The return loss of the B2B transition has a minimum of 9 dB within this range, which corresponds to around 12 dB for the single transition. During the design process a minimal return loss toward lower frequencies was rated with greater importance to reduce load—pulling effects from high VSWR since here, the output power of the MMIC is at its peak. Overall, the measured results match the simulations.

### B. $\lambda/2$-Balun

Consider Fig. 11, which shows the RF-coupler from differential microstrip line to SIW. A $\lambda/2$-Balun is combined with a SIW-to-microstrip transition for minimum space occupation.

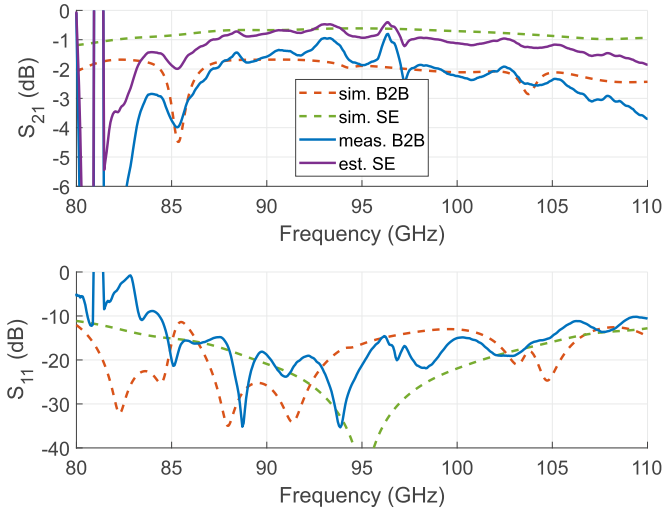


Fig. 12. Measurement and simulation results of the B2B-configuration of the $\lambda/2$-Balun combined with microstrip-to-SIW transition from Fig. 11.

The radius of the Balun corresponds to a circle with a circumference of $2\lambda$ with both legs having an offset of $\lambda/2$ to combine the power of the differential microstrip lines odd mode at its SE port in phase. For this topology [device under test (DUT)], simulations showed that a total of $2\lambda$ is a good compromise of bandwidth and bending radius. Higher circumferences would result in lower bandwidth because of higher frequency dependence of its true time delays, and lower order circumferences result in higher radiation losses of the bends. The line widths are chosen equal to 70.7 Ω for the microstrip line within the circle, 100 Ω for the odd mode of the differential and 50 Ω for the SE microstrip line, respectively. Additionally, a spline-like taper is used for lower return loss at the differential microstrip lines. At the SE port, a tapered transition from microstrip line to SIW with 59-GHz cutoff frequency for the fundamental mode is used.

The simulation results are verified by measurements of a B2B-arrangement of this transition. To measure the calibrated S-Parameter, a TRL-set for SIW was designed with the previously described SIW-to-RWG transition. Thus, the reference planes are the SIW inputs of the coupler with its differential microstrip ports connected back-to-back. Because of the bandpass behavior of the SIW-to-RWG transition, the calibration is only valid around 83–110 GHz.

The measurement results (see Fig. 12) show that the insertion loss ranges from 1 to 4 dB for the B2B-arrangement. The substantial increase of loss below 84 GHz is expected to be a result of insufficient manufacturing accuracy, which results in a frequency shift of the bandpass frequency of the calibration standards. Additionally, resonances occur in the B2B-arrangement. Comparing half of the insertion loss to the simulation of the SE transition, one can see that simulation and measurement match well. The return loss is more than 9 dB from 83.5 to 110 GHz and more than 15 dB from 84.5 to 105 GHz.

### C. Dielectric Lens Antennas

Two types of high gain dielectric lens antennas [23] that differ in size and thus in HPBW or gain G, respectively, are shown in Fig. 1. They cover a full waveguide band with good input matching. The opening angle, and thus antenna gain, depends on the size and permittivity $\varepsilon_r$. The form $x$, $y$ for the ellipsoid of maximum radius $R$ and the corresponding gain can be calculated by (13) and (14) with $\eta_{\text{ap}}$ being the aperture efficiency and $A_{\text{ap}}$ being the physical aperture size

$$1 = \left(\frac{x - R/\sqrt{\varepsilon_r - 1}}{R/\sqrt{1 - 1/\varepsilon_r}}\right)^2 + \left(\frac{y}{R}\right)^2 \tag{13}$$

$$G = \eta_{\text{ap}} \cdot A_{\text{ap}} \cdot \frac{4\pi}{\lambda^2}. \tag{14}$$

It is obvious that for identical antennas and for the same radiation efficiency the gain scales with frequency. According to the desired measurement scenario, antennas with different beamwidth can be attached to the radar sensor by mounting them on the two or three WR-10-flanges, respectively. The standard WR-10-flange makes the radar sensor also compatible with other types of antennas like horn antennas, etc.

In the presented measurements in Section VI, we used dielectric lenses milled from Teflon because of their low loss ($\tan\delta$). However, modern additive manufacturing can be used to 3-D-print antennas, which makes it easy to develop the best suitable antenna for every operational scenario, but often with higher loss than Teflon depending on the material.

Additive manufacturing gives a broad variety of materials that can be used and printed which is easier and cheaper than manufacturing complex metal structures as antennas. This is beneficial in antenna design, because material, permittivity $\varepsilon_r$, and the loss factor $\tan\delta$ must be chosen depending on application and frequency.

## V. System Measurement Results

For characterization of the W-Band radar several measurements are carried out and are presented in this section.

### A. Signal Generation and PLL Design

For the results presented in this publication, the auxiliary-VCO's (27 GHz) frequency is PLL-stabilized at exactly 28.8 GHz. Together with the tuning range of the 94-GHz VCO, this leads to a frequency configuration that is best suited to the frequency limitations given in the datasheet of the PLL ICs.

The frequency range of the breakout main-VCO (94 GHz) was measured directly at its output, and also at the output of its by-4-divider, respectively (see Fig. 13). As can be seen, the tuning curves differ slightly depending on the load conditions presented to the 94-GHz VCO [14]. When the output of the breakout VCO is left open and the frequency is measured at the divide-by-4 output and then multiplied by 4 (point-dashed curve) for better comparability with the other curves, the maximum frequency is reduced to 106 GHz due to load—pull effects of the unloaded VCO. The measurements directly at the 94 GHz-output of the MMIC show a maximum frequency of oscillation of 109 GHz. This differs slightly from the simulation with an ideal 50-Ω load since the pad capacitance was not compensated on the breakout chip. Additionally, one can see a small ripple of high frequency on the orange

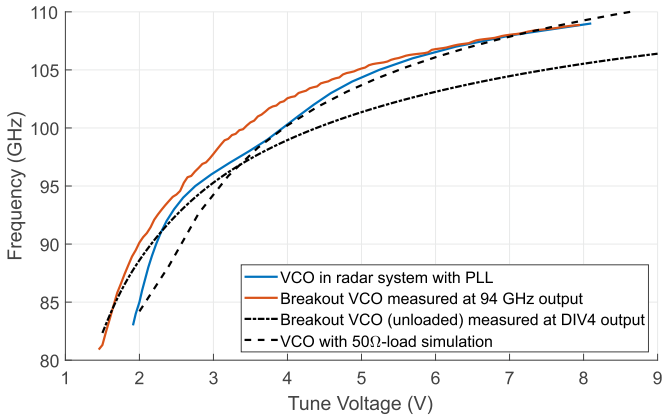


Fig. 13. Measurement of the radar system's PLL-stabilized tune curve in comparison to the tune curves of the breakout VCO measured at the VCO's output and behind the divided-by-4 output together with the simulated tune curve.

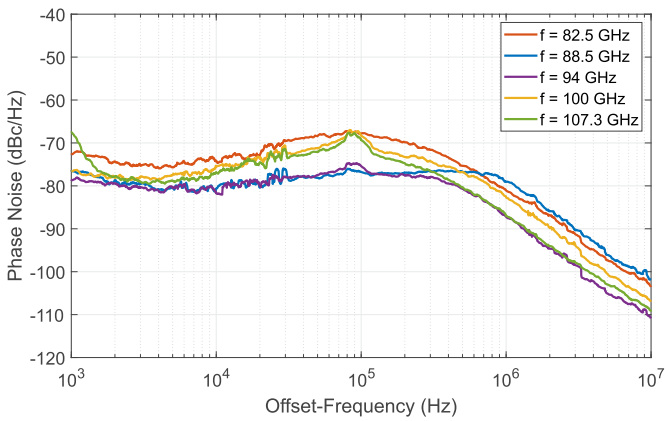


Fig. 14. Measurement of the radar system's PLL-stabilized phase noise at the WR-10-WG-flange for different frequencies.

curve measured at the 94-GHz output, resulting from long coaxial cable to measurement equipment [14] which results in load—pull effects that also influence the phase noise behavior. On the MMIC of the 94 GHz radar transceiver, the Wilkinson-dividers', the receiving mixers', and the PA's input impedance present a frequency-dependent load to the VCO resulting in load—pull effects. Therefore, there is a linear region at around 4 V in the tuning curve of the PLL-stabilized VCO. But overall, minimum and maximum frequency are close to simulation.

Considering the tuning curve measured at the 94-GHz output, the tuning sensitivity $K_{\mathrm{VCO}}$ of the VCO ranges from 22 to 2 GHz/V (11:1) which directly correlates to the loop gain variation. A high loop gain variation makes the loop filter design difficult for a wide tuning range because it results in reduced phase margins toward the frequency limits and thus in instability and reduced locking range of the PLL. By using the offset-PLL concept for loop gain linearization [4], the loop gain

$$H_{\mathrm{loop}} \propto \frac{K_{\mathrm{VCO}}}{N} \tag{15}$$

with N being the divider for ramp generation of the PLL IC can be reduced to a range of 2.9:1, making it possible to stabilize the full 26 GHz of bandwidth of the 94-GHz VCO.

Fig. 14 shows the measured phase noise of the PLL-stabilized 94-GHz VCO at different frequencies. The phase noise is measured with a WR-10 harmonic mixer flanged to the systems antenna interface with an additional 10-dB attenuator for input power protection. At the design frequency of 94 GHz and slightly lower at 88.5 GHz the in-loop phase noise is below −75 (dBc/Hz) with a minimum phase noise of −81 (dBc/Hz) at 10 kHz. Toward the limits of the frequency range, the in-loop phase noise increases to −68 (dBc/Hz).

The measured output power of the system measured at the WR-10 antenna interface is shown in Fig. 15 (blue curve). The output power ranges from 14.8 to 6 dBm. The measured output power is 6.5 to 12.6 dB lower than the simulated saturated output power of the PA on the MMIC which has a maximum of 20.9 dBm at 81 GHz. The passive RF components on PCB level that are characterized in the sections IV-A and IV-B,

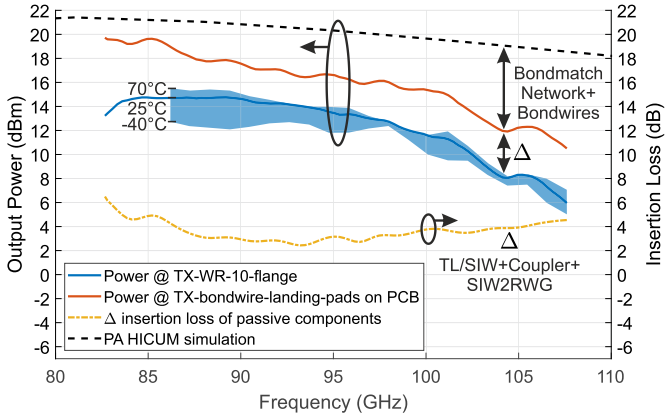


Fig. 15. Measurement results of radar systems output power at the TX waveguide port and at the TX MMIC output behind the bondwires compared to the simulated output power of the PA. The graph also shows the sensor's variation over temperature as an envelope around the output power at the WR-10-flange from measurements in a climate chamber between −40 °C and +70 °C.

in conjunction with the 13 mm SIW with 0.06 (dB/mm) in the TX-path contribute 6 dB to 2.4-dB insertion loss, which is represented by the graph as the yellow dot-dashed curve (Δ insertion loss of passive components, yellow curve). This is the measured insertion loss of all passive structures between the WR-10-flange and the MMIC. De-embedding the combined passive component insertion loss from the measurement of the output power at the waveguide flange (blue curve) results in the calculated output power at the bond landing pads on the PCB side (orange curve) with a maximum of 19.7 dBm at 82.5 GHz and minimum of 10.5 dBm at 107.6 GHz. The de-embedded power also shows that the decrease of power below 83 GHz matches well with the increase of insertion loss of RF passives. The remaining 2–7.7 dB difference from the orange curve to the simulated PA output power can be explained by the bondwires and their matching network. The stronger decrease of output power to high frequencies might result from the decreasing output power of the 94-GHz VCO for these frequencies which means that the VCO is not able to saturate the PA in this region.

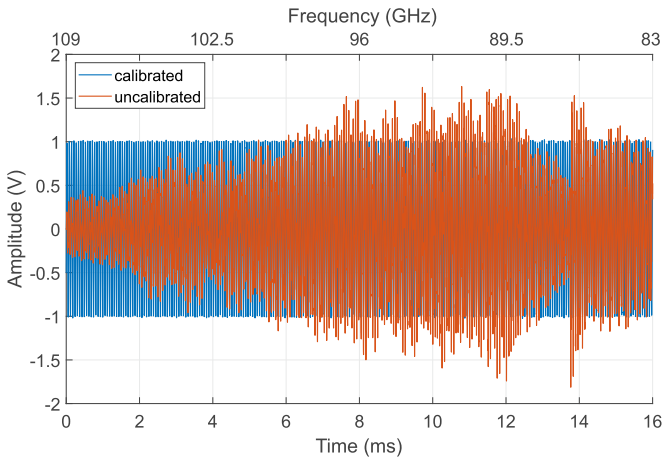


Fig. 16. Transient representation of uncalibrated and calibrated IF-signal with single target in 1.5 m distance for a down-chirp of 26-GHz bandwidth in 16 ms.

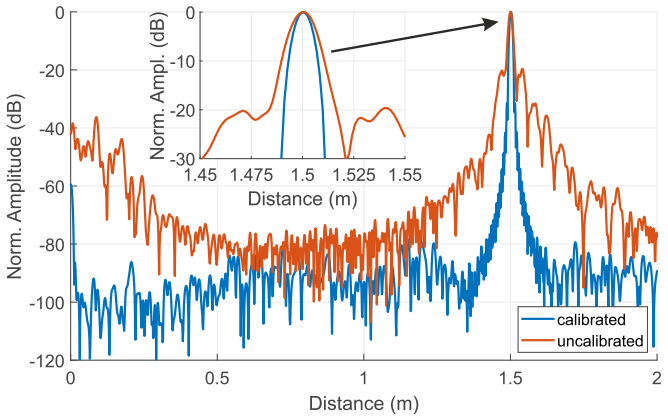


Fig. 17. Frequency-domain representation of uncalibrated and calibrated IF-signal with a single target in 1.5 m distance for a down-chirp of 26-GHz bandwidth in 16 ms and magnification of the target's peak. The calibration increases the effective bandwidth from 18.6 up to 26 GHz, leading to an increased spatial resolution from 16.1 to 11.4 mm (with a factor of 2 for the Hann window). For decreased sidelobe level a Hann window is applied.

The PA's PAE referred to the power at bondwire landing pads is at least 19% consuming 98 mA at 5 V producing 19.7 dBm and being driven by about 10 dBm from the 94-GHz VCO. By adding 1.4 dB (rather more) to the output power from the simulated loss of the bondwires and the bond compensation network the PAE of the PA itself can be conservatively estimated to 26%.

The radar sensor's output power was also measured in a climate chamber between −40 °C and +70 °C leading to the blue envelope area around the measured output power of the radar sensor at room temperature. The sensor operates reliably under those temperature conditions with less than 3 dB of deviation of the measured output power.

### *B. IF-Signal*

Fig. 16 shows the received IF-signal of a frequency chirp from 109 GHz down to 83 GHz in 16 ms with a strong reflector at roughly 1.5 m distance. One can observe a reduction of amplitude toward the frequency limits with significant reduction at higher frequencies (top-axis), which coincide with the system's output power (see Fig. 15). Additionally, the envelope shows an amplitude modulation of rather high frequency coming from mismatch at RF passives and long SIW transmission on the PCB as well.

Fig. 17 shows the corresponding frequency domain representation of the signal, which is re-normalized to 0 dB (see [5] Fig. 22). For sidelobe reduction, a Hann window function with bandwidth correction factor $B_w$ of 2 is used. Thus, the smallest achievable range resolution of an FMCW radar with modulation bandwidth $BW$ is given by

$$\Delta r = \frac{c_0 \cdot B_w}{2 \cdot BW} = \frac{c_0}{BW}. \tag{16}$$

The measured range resolution for 26-GHz ramp bandwidth from the uncalibrated IF-signal in Fig. 16/17 is 16.1 mm, which corresponds to the 6 dB-width of the target peak. The smallest possible range resolution for a frequency chirp of 26 GHz is 11.4 mm. In reality, the range resolution decreases with amplitude modulation $m(t)$ and phase modulation $\phi(t)$ of the IF-signal resulting in

$$s_{\text{real}}(t) = m(t) \cdot \cos\left(\omega_{\text{ideal}}(t) + \phi(t)\right). \tag{17}$$

The main contributors are the modulation due to frequency-dependent output power, and insertion loss of RF passive components as well as a mismatch at the different interfaces as discussed earlier. Furthermore, the group velocity inside the waveguide results in a sweep-time-dependent delay and thus phase modulation $\phi(t)$ in the IF-band. While this is of less severity for narrowband applications like applications presented in this publication, for wideband measurements like radar imaging, inline production monitoring, or nondestructive testing, a calibration can be applied [24], [25] resulting in the blue curves from Fig. 16/17. For an increased range resolution a complex calibration factor which characterizes the system's transfer function is used to harmonize future measurements. This results in a close-to-perfect IF-spectrum and the range resolution increases to 11.4 mm (5.7 mm without Hann window). Furthermore, one can see that the SNR in the calibrated case is increased to more than 80 dB. The increase of SNR after calibration shows that in the uncalibrated measurement, the system is not limited by noise but by modulation and clutter.

For orientation, the SSB NF of one RX-channel from the WR-10-flange can be estimated by adding the simulated insertion loss of the passive components (SIW-to-RWG-transition, SIW, coupler, bondwires with on-chip compensation network, and on-chip TRLs) to the simulated SSB NF of the Gilbert-mixer of 12.5 dB. This results in around 19.5 dB (12.5 dB + 7 dB). Due to a mixer conversion gain of 12.5 dB the following filters and amplifiers have negligible influence on the RX-channel NF.

## VI. Application and Fielding Measurement Campaigns

In order to investigate the usability of the system in real applications, several measurements were carried out to

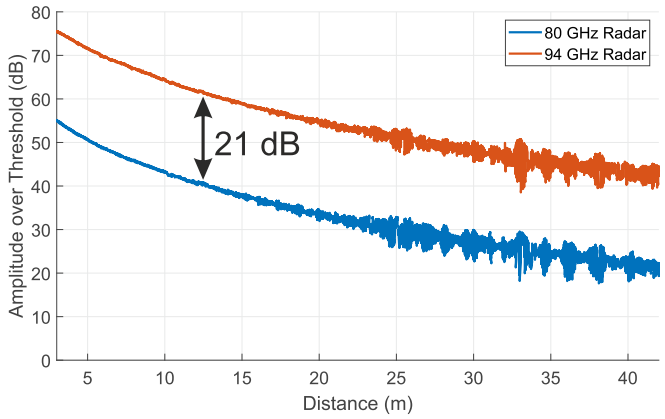


Fig. 18. Comparison of the system dynamic range of the bistatic 94-GHz FMCW radar system (with PA) with the monostatic 80-GHz FMCW radar system (without PA).

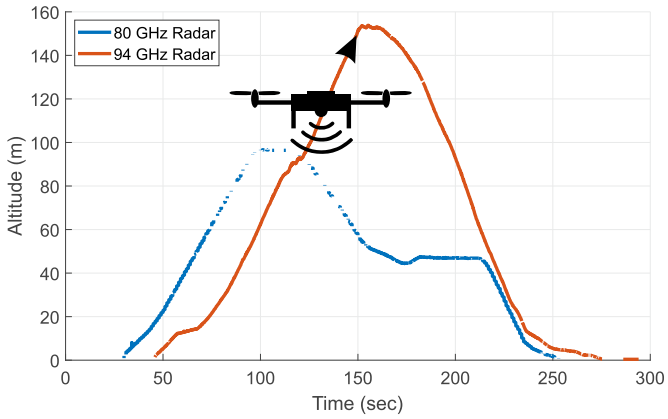


Fig. 19. Comparison of the system dynamic range of the bistatic 94-GHz FMCW radar system (with PA) with the monostatic 80-GHz FMCW radar system (without PA) in an altimeter scenario on a UAV with measurement against ground surface. Through the lower system dynamic range of the 80-GHz radar, the blue curve shows measurement blackouts over 60 m of altitude while the 94-GHz radar is capable of measuring at altitudes of over 150 m.

simulate the radar conditions in airborne systems and in long range scenarios.

### *A. System Dynamic Range Comparison in Flight Altitude Control and Landing Assistance Scenarios*

The first measurement scenario is with the radar mounted at a fixed position and a 10 $m^2$ (at 94 GHz) corner reflector mounted on a rail cart. Fig. 18 shows the resulting target amplitude over the measured distance between corner on rail cart and radar. The intention here is to have a controlled single-target environment to measure the signal level above a threshold that is 10 dB higher than the noise floor when no target is present (dynamic range). We compare the 94-GHz radar presented in this publication to a similar monostatic 80-GHz radar without PA (designed in B7HF200) to show the dynamic range increase due to the PA. Both systems were used in their respective frequency range of best performance under otherwise identical conditions. The modulation bandwidth is 1 GHz with a triangle modulation with 4-ms modulation duration in upward and downward direction each.

The modulation bandwidth had to be reduced from 26 GHz of possible bandwidth to 1 GHz because higher modulation bandwidth at constant ramp length results in higher ramp slope of the FMCW-chirp which causes IF-frequencies that are higher in frequency. The IF-signal frequency is limited due to the ADCs which sample the IF-signal with 1 MSPS. This results in a Nyquist-frequency of 500 kHz for which the corner frequency of the 8. order active antialiasing filter was set to be 400 kHz. For IF-signals that can be sampled under those conditions, the modulation bandwidth has to be reduced in case of scenarios with targets that are far away.

For both systems the same W-band dielectric lens antennas were used. A dielectric lens antenna with a diameter of 22 mm was used. Thus considering the center frequency of both systems the gain at 94 GHz is 1.6 dB higher than that at 80 GHz (see (14)). The aperture angle is around 8° with 24.4 dBi and 26-dBi gain, respectively.

One can see that the signal levels of the 94-GHz radar in Fig. 18 is around 21 dB higher. At 40 m, which is the end of the test range, the signal level is still 40 dB above the threshold for proper detection. Considering −12 dB per distance doubling one can estimate that for this corner reflector distances above 300 m are possible. At distances above 20 m, the beamwidth of the antenna is also detecting reflections from the rail cart, which result in clutter and overall noisier curves.

Because of the system's high dynamic range and its compact size, the system is suitable for flight altitude control and altimeter applications on small UAVs and helicopters. Radar supported landing assistance is especially useful in white-out or brownout scenarios with poor visibility conditions.

Therefore, the system was tested with a flight over a dry meadow, which is expected to have a low radar cross section (RCS) compared to wet meadow or asphalt. Again the 94-GHz system is compared with the 80-GHz sensor to show the advantages of high system dynamic range for this application. Both systems were mounted underneath a small UAV. The UAV was manually controlled to vertically fly up and down. Its height profile can be seen over time in Fig. 19. This figure shows that the 94 GHz system was able to measure the altitude up to at least 150 m (limited by UAV capabilities) at any measurement time, which is represented as a continuous graph. Here a measurement was considered successful only if a signal was detected above a given threshold. At an altitude of 150 m, the signal level was still 22 dB above the detection threshold. The 80 GHz system was able to detect the UAV's altitude up to 60 m. At larger distances, this system was not able to reliably detect the height with each consecutive measurement resulting in an intermittent line.

### *B. Obstacle Detection for Collision Avoidance*

In the second scenario, the system's performance was tested under real conditions in a collision-avoidance scenario. Two different power grids with four and six cable bundles, respectively, are located consecutively, as shown in Fig. 20(a). The radar pointed in the direction of an electricity pylon of the first grid from a distance of 630 m. At that distance the bright spot from the HPBW of the antennas is at around 55 m.

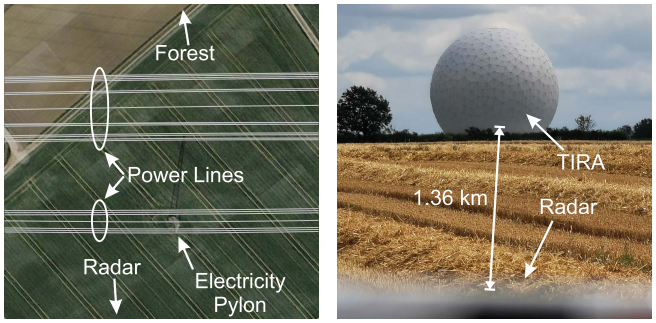


Fig. 20. (a) Top view of measured scene of power lines and electricity pylon and (b) measured radome and the satellite dish (rear side) inside of Fraunhofer FHR's TIRA [26].

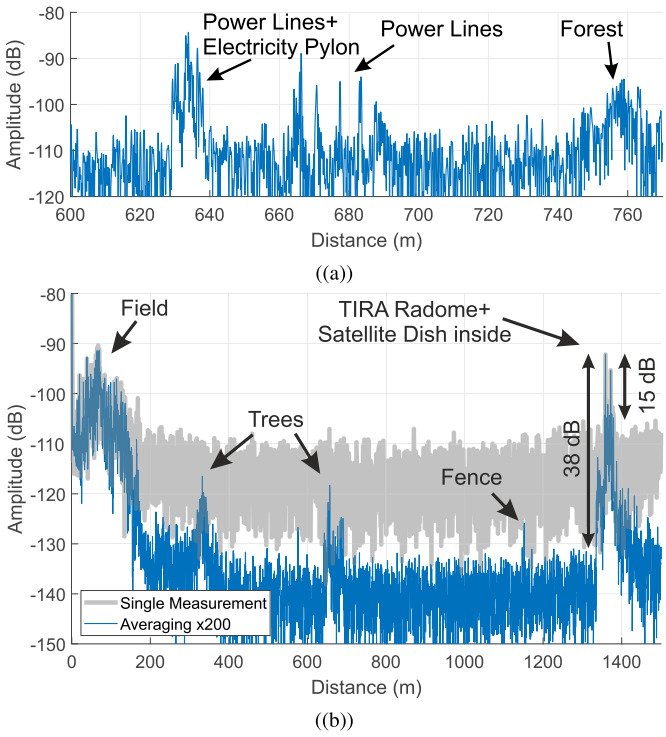


Fig. 21. (a) Distance measurement results of power lines and electricity pylon from Fig. 20(a) and (b) Fraunhofer FHR's TIRA [26] from Fig. 20(b).

While in the spectrum [Fig. 21(a)] the electricity pylon and power lines are represented as an allocation of multiple targets, the bundles of the power lines behind the pylon can be clearly separated. The RCS of the targets is sufficient at 94 GHz to detect them at distances above 600 m with at least 10 dB above the noise floor. Additionally, the forest starting at 760 m can also be detected. Here no signal processing or averaging algorithms were used. Under these conditions the system achieves measurement rates up to 30 Hz.

For stationary targets, the detection range of the system can be further extended by averaging multiple measurements. In order to demonstrate the benefits of the averaging process, the *Tracking and Imaging Radar* (TIRA) [26] [Fig. 20(b)] at Fraunhofer FHR's premises is used as a radar target from a distance of 1.4 km. For this measurement, the modulation

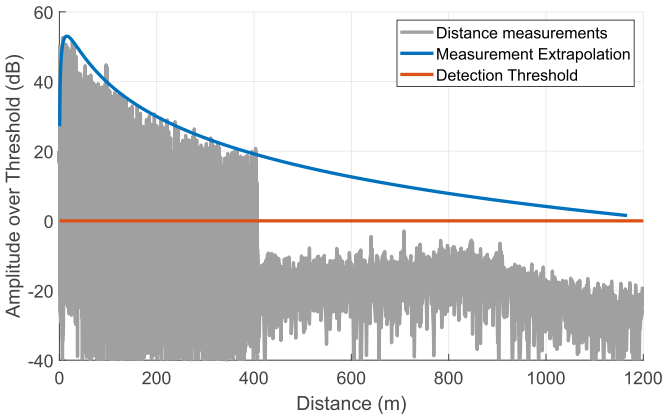


Fig. 22. Distance measurement of a corner on a motorcycle up to 400 m and calculated extrapolation including free space loss.

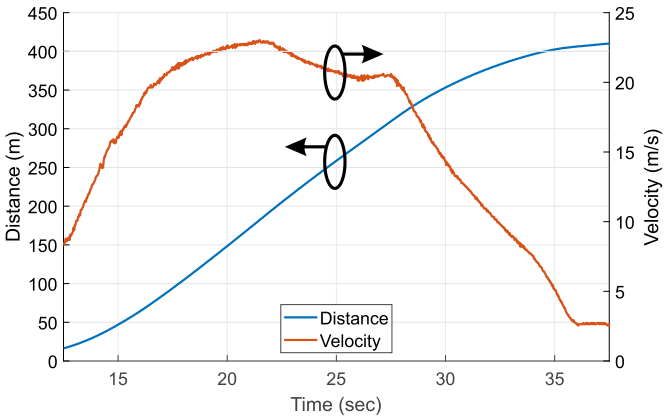


Fig. 23. Distance measurement of a corner on a motorcycle up to 400 m together with the Doppler extraction from the FMCW radar's up/down-chirps.

bandwidth was set to 500 MHz due to the abovementioned limitations from the IF-filtering and sampling. The picture shows the white radome with a diameter of 47.5 m which covers a satellite dish with a diameter of 34 m. At the time of measurement the antenna was facing with its back toward the radar, so that the metallic supporting structures were pointing in the direction of the radar. Even for a single measurement of a 16 ms FMCW-chirp, the radome and antenna could be detected and distinguished as two separate targets [radome and satellite dish (rear side)] in the expected distances with about 15-dB SNR. This is shown in Fig. 21(b). By increasing the sensitivity by 23 dB by correlating 200 measurements [equals $10 \cdot \log_{10}(200)$] at a rate of 30 Hz, which equals 6.7 s measurement duration, even reflections from the building with the radome on top could be detected additionally. There are also target peaks from reflections from trees in the scenery and the fence around the premises, which only become apparent through measurement correlation. This proves the exceptional stability of the PLL circuit, which is needed for detection of high range targets by averaging.

### C. Doppler Measurements

In order to test the system in a dynamic scenario with a moving target, the capability of range and velocity detection

TABLE II
COMPARISON OF SIMILAR STATE-OF-THE-ART W-BAND FMCW RADAR SENSORS

| Ref | TX-/RX-Channels[#] | Freq. (GHz) | Tuning Range (GHz) | $P_{\text{out}}$ (dBm) | SSB PN (dBc/Hz) @ 1 MHz | SSB PN (dBc/Hz) @ 10 kHz | SSB NF (dB) | System Dynamic Range (dB) | Power Supply (W) | Technology |
|---|---|---|---|---|---|---|---|---|---|---|
| This work | 1/2 | 83-109 | 26 | 14.8/ 19.7* | -87 | -81 | ≈19.5 (sim) | 82† | 4.25 | SiGe BiCMOS |
| [6], [27] | 1 | 68-92.5 | 24.5 | -4 | -97 | -88 | - | 61† | 2.9 | SiGe |
| [5] | 1 | 122-170 | 48 | -1* | -94 | <-80 | 19.3* | - | 3.75 | SiGe |
| [28] | 1/1 | 92.2-96 | 3.8 | 20* | - | - | - | 60* | - | III-V |
| [29] | 1/1 | 77-85 | 8 | 11.5* | -99 | -90 @ 100 kHz | 3.85 DSB | - | 0.78 | SiGe |
| [30], [31] | 1 | 85.8-99.9 | 14.1 | 3* | -100 | -72 | - | - | 5 | mHEMT InGaAs |
| [32] | 1/1 | 122-123 | 1 | -4 | - | - | - | - | < 2.5 | SiGe |
| [33] | 2/4 | 74.1-81.1 | 7 | 7* | - | -75.3 @ 100 kHz | 17.7* | - | 3.3* | SiGe |
| [34] | 1/1 | 73.5-77.1 | 3.6 | 6.3* | -86 | - | 6.8* | - | 0.92* | 90 nm CMOS |
| [35] | 4 | 91-97 | 6 | 6.5 | -88 | - | 12 | - | 1.584* | SiGe |
| [36] | 4 | 68-78 | 10 | -7.8 | -70 | -100 | - | - | - | SiGe |
| [37] | 1/1 | 76-81 | 5 | 10.5 | -100.4 | - | 8* DSB | - | 0.61* | SiGe BiCMOS |
| [38] | 4/4 | 89-95 | 6 | 7.7* | -78 | -60 @ 100 kHz | 12.5 | - | 0.804* | SiGe BiCMOS |

[#]Single digit values represent channel number of monostatic systems and the dash-separated numbers represent channel count of quasi-monostatic/bistatic/multi-static systems with first digit being number of TX-channels and second digit number of RX-channels (TX/RX).
*Parameter that refers to the MMIC or parts of the radar system but not to the complete sensor or unexplicitly described.
†The system dynamic range was measured as the difference between target peak and noise floor using a 10 $\text{m}^2$ @ 94 GHz corner at 5 m distance with an 1 GHz FMCW-chirp over 8 ms.

was tested using a motorcycle with a corner reflector mounted on the rear seat. The size was chosen to be 1000 $\text{m}^2$ for sufficient contrast to clutter from lane markers. For a high distance measurement with limited IF-frequency bandwidth, the modulation bandwidth was set to 500 MHz with 8 ms up and down ramp duration, respectively. The IF-signal spectra of multiple measurements during which the motorcycle moved away from the radar at approx. 80 km/h top speed are overlaid in one graph. This is shown in Fig. 22. It can be clearly seen that the signal level is detectable up to a distance of 400 m with high SNR under these conditions. An interpolation of the measurement results with a graph $\propto (1/R^4)$ shows that the measured results follow the theoretical expected decrease at the signal level. Extrapolating the results, the detection threshold is reached at around 1200 m, though this would yield IF-frequencies above the antialiasing filters cutoff, which is at 400 kHz or 960 m, respectively, and thus a further decrease of modulation bandwidth is required. Also, for measurement results below 100 m the far-field condition of the corner reflector is not fulfilled leading to divergence from the fit interpolation-curve. Consider Fig. 23, which shows the distance and velocity of the same measurement series determined by the radar. Range and velocity are extracted from the triangle modulation, allowing the frequency components of the IF-signal to be distinguished in the components resulting from the velocity-dependent Doppler shift and the range-dependent component. A more detailed view of the measured velocity shows that it varies slightly. This curve is less smooth than the range curve. This is due to the fact that the frequency resolution is limited by the measuring rate when determining the Doppler-frequency. However, the fact that it was not possible to keep the speed in direction of the radar beam constant over a longer period due to the bumpy road surface has a larger influence on the noisy velocity curve. This means that significant parts of the velocity variations reflect the reality of the measurement conditions.

## VII. STATE-OF-THE-ART COMPARISON

Table II lists the recently developed state-of-the-art radar systems at around 100 GHz for a comparison with the presented 94-GHz radar. It provides a high relative bandwidth of 27%, only the radar systems from [6], [27] and [5], which were fabricated in the predecessor technology B7HF200, provide higher relative bandwidth with 30.5% and 32.8%, respectively. Although, the in-loop phase noise at 10 kHz offset from carrier is limited to $-81$ (dBc/Hz) compared to [6], [27] and [36], but it is sufficient to detect targets in several hundreds of meters away as demonstrated in Section VI. In fact, the radar was able to detect tall buildings in over 1.4 km distance by correlating multiple measurements to achieve sufficient SNR.

Primarily responsible for the high detection range is the used PA of the TX-channel, resulting in a system dynamic range that is improved by 21 dB compared to a similar radar

system at 80 GHz from [6], [27]. The system dynamic range was determined to be 82 dB for the difference between the target peak of a 10 $m^2$ at 94-GHz corner at a distance of 5 m for an 8-ms FMCW-chirp and the noise floor level of the sampled and fast Fourier transform (FFT)-processed IF-signal. The measured maximum output power at the WR-10-flange is 14.8 dBm, which is the highest of all compared SiGe radar sensors from Table II. By deembedding the passive structures that are located between the radar MMIC and the WR-10-flange of the TX-channel, the output power behind the MMIC-bond wires on the PCB's bondwire landing pads could be extracted to be 19.7 dBm at its peak. Only the radar system from [28] which uses a high PA in a III-V-technology produces a higher output power of 20 dBm.

The presented radar is very compact but does not include signal processing inside of the sensor itself like the system in [30], [31], but, therefore, no additional fan for active cooling is needed. The power consumption of 4.25 W is high compared to the other systems, but, on the other hand, it is needed to generate the 14.8-dBm output power at the WR-10-flange with limited PA efficiency around 94 GHz. Also the two used Hittite PLL ICs consume most of the sensor's power. It is planned to replace them with newer and more power efficient PLL ICs from the automatic direction finder (ADF) series from analog devices.

The comparison to modern state-of-the-art radar systems shows the excellent overall performance in terms of output power, bandwidth, phase noise, system dynamic range, compactness, and power dissipation, leading to a very high detection range suitable for airborne and other high range applications.

## VIII. Conclusion

We presented a quasimonostatic FMCW radar system with one TX- and two RX-channels at 94 GHz. The achieved output power at the WR-10 flange of the radar sensor is over 14.5 dBm from 84 up to 89 GHz. The MMIC output power at the bond wire landing-pads on the PCB directly behind the MMIC was calculated to 19.7 dBm in its peak at 85.2 GHz by measuring and de-embedding the passive structures between the MMIC and the WG-flange. The radar sensor provides 26 GHz or 27% of PLL-stabilized bandwidth. Compared to a similar 80 GHz radar sensor without PA and thus lower output power from [6], [27], the presented 94-GHz radar sensor could demonstrate 21 dB higher system dynamic range or 82 dB in total, which nearly directly correlates to the 20 dB higher output power from less than $-4$ dBm at the WG-flange of the 80-GHz sensor compared to 14.8 dBm at the WR-10-flange of the 94-GHz system.

The easy-to-use and compact system architecture with its sole USB interface for power supply and data transfer makes this sensor applicable for a wide range of usage scenarios. We showed a variety of versatile applications, e.g., for high range obstacle detection up to 1.4 km distance, for range-Doppler measurements of moving targets or as flight altimeter on UAVs.

Through the radar system's high output power and thus high dynamic range many other scenarios can be addressed, such as airborne collision avoidance system (ACAS) in which high range target detection is demanded. Additionally, target angular estimation would be possible because of its two receive channels.

To the best of the authors' knowledge, no quasimonostatic radar system with one TX-channel and two RX-channels at around 94 GHz has demonstrated a higher detection range or dynamic range together with its small form factor.

The radar sensor was also tested in a climate chamber between $-40$ °C and $+70$ °C. It was found to be fully operational within a maximum deviation of output power of less than 3 dB over the frequency range from 87 to 107 GHz and with an absolute frequency shift of less than 2.5 MHz for this tested frequency range.

Previous radar architectures from [4]–[6], [27] served as foundation but were significantly enhanced in this work by nearly keeping the small sensor form factor (limited by two/three antennas/WR-10-flanges) while severely increasing the output power with a sophisticated and compact way of output matching of the PA together with a DAC on the front end for output power regulation. Furthermore, an additional receive channel was added on the MMIC with a die size of $1.5 \times 1.5$ $mm^2$ which is even smaller than the radar MMICs from [4]–[6]. Besides the improvements on the MMIC, we replaced previously used passive structures by a low loss interface on the PCB front-end between the MMIC and the WR-10-flanges based on a SIW-to-RWG transition to reduce output loss and maximize output power of the radar sensor.

All the above shows an exceptional overall sensor performance in relation to output power, dynamic and detection range, temperature stability, power consumption, and compactness.

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