Design for Cost: The Key of Success for 5G and Beyond

5G IS coming and it will change our lives. Now, 6G is under discussion too. The multiple-in–multiple-out (MIMO) technique is a critical technique for 5G and beyond. Additional element transceivers and antennas are usually required for supporting the beamforming configuration and MIMO communication. If one just simply puts many transceivers in parallel to drive the antennas, the system size will increase tremendously and the manufacturing cost will also increase significantly. How to reduce the overall system cost becomes one of the key factors of success for 5G and beyond.

There have been many different attempts to reduce the system costs, for instance, by optimizing the multiple front ends and so on. One of the best ways is to share the subbuilding blocks and components for different RF signal chains from the beginning of designing an entire MIMO system, Design-for-Cost (DfC) to minimize the chip sizes occupied.

The article published in this issue by Pang *et al.* [item 1) in the Appendix] introduces a CMOS two-element transceiver chip based on the area-efficient bidirectional architecture. The gain-boosted bidirectional amplifier proposed in the article further allows the sharing of interstage passive components. With the help of the designed power amplifier-low-noise amplifier (PA-LNA), the required area for a single-element transceiver reported in the article is 0.96 mm^2 with excellent performances at 60 GHz.

Since the early publication in IEEE Xplore, the article has drawn much attention and received the highest numbers of "Full Text Views" in IEEE Xplore among all the articles presented in this issue. The article [item 1) in the Appendix] demonstrates the concept of DfC that might become the mainstream for designing MIMO systems with high performances and low costs.

JIANGUO MA, *Editor-in-Chief*
School of Computers
Guangdong University of Technology
Guangzhou 510006, China

APPENDIX
RELATED WORK

1) J. Pang *et al.*, "A 28.16-Gb/s area-efficient 60-GHz CMOS bidirectional transceiver for IEEE 802.11ay," *IEEE Trans. Microw. Theory Techn.*, to be published, doi: 10.1109/TMTT.2019.2938160.

Digital Object Identifier 10.1109/TMTT.2019.2961249