High-Efficiency Bias Stabilization for Resonant Tunneling Diode Oscillators

Andrei Catalin Cornescu, Razvan Morariu, Afesomeh Ofiare, Abdullah Al-Khalidi, Jue Wang, José M. L. Figueiredo, *Member, IEEE*, and Edward Wasige, *Member, IEEE*

***Abstract*— We report on high-efficiency, high-power, and low-phase-noise resonant tunneling diode (RTD) oscillators operating at around 30 GHz. By employing a bias stabilization network, which does not draw any direct current (dc), the oscillators exhibit over a tenfold improvement in the dc-to-RF conversion efficiency (of up to 14.7%) compared to conventional designs (∼0.9%). The oscillators provide a high maximum output power of around 2 dBm, and low phase noise of −100 and −113 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. The proposed approach will be invaluable for realizing very high efficiency, low phase noise, and high-power millimeter-wave (mm-wave) and terahertz (THz) RTD-based sources.**

***Index Terms*— Bias stabilization, high-frequency oscillators, negative differential resistance (NDR), resonant tunneling diode (RTD).**

I. Introduction

HIGH-FREQUENCY sources are a key building component of many modern electronic systems, and therefore, their design is of paramount importance. For millimeter wave (mm-wave) and terahertz (THz) oscillators, those based on the resonant tunneling diode (RTD) are being actively researched for a variety of applications including short-range multigigabit wireless links and imaging [1]–[4]. They are also being deployed in mm-wave radar sensors for a variety of applications [5]. Advantages of RTDs include the facts that they are extremely broadband with fundamental oscillations up to 1.98 THz recently reported [6], operate at room temperature, are compact, consume low power, and the output power is easily modulated through the bias network.

In our recent work, we have reported RTD oscillators with record output powers in the 0.5–1 mW range up to 300 GHz [7]–[10]. We have used this technology to demonstrate 15 Gb/s wireless links using W-band RTD oscillators [4], and now developing such links for future wireless data centers [11]. The technology has the potential to underpin emerging new applications requiring short-range high-capacity wireless links such as virtual gaming, wireless memory sticks, and so on. Part of the appeal for RTDs is in their simplicity, e.g., a 1 mW J band source requires only a single RTD device realized using just photolithography [10], while transistor technologies such as CMOS require an array of eight or more (active) devices, sub 100 nm high-resolution lithography, and advanced circuit design techniques [12]. Also, RTDs can provide highly efficient electronic sources beyond about 300 GHz, frequencies that cannot generally be easily covered by any transistor technologies today [13].

The basis of the RTD oscillator is the negative differential resistance (NDR) region of its current–voltage (I–V) characteristic. Since the NDR exists right from dc, RTDs are affected by instability when biased in this region resulting in unwanted parasitic bias oscillations. If present, these reduce oscillator output power [14], [15]. The conventional approach to eliminate the bias oscillations in planar RTD oscillators uses a shunt resistor across the RTD so that the combined I–V characteristic remains positive in the NDR region of the device [16]. Using this method in RTD oscillators, however, greatly reduces the dc-to-RF conversion efficiency to under 1% by providing a dc path to ground through the usually low-value resistance, typically ∼10 Ω) [7], [17]. Many earlier RTD oscillators were implemented in rectangular waveguide technology and used a lossy section of the transmission line to minimize bias oscillations, and so had limited efficiency [19]. Therefore, approaches to improve efficiency could have a major impact with regards to the adoption of the technology, especially for portable devices where battery capacity is at a premium.

To improve the dc-to-RF conversion efficiency of NDR (tunnel diode) oscillators, a nonlinear resistor (Schottky diode) was used instead of a linear resistor to reduce the dc power consumption of the stabilizing resistor [18]. The dc power consumption was reduced by a factor of 3–6 using this approach. In [15], an integrated Schottky diode was used, but this approach is limited to only RTD epitaxial designs for which the forward voltage drop of the Schottky diode lies within the NDR of the device, which is often not the case and so the approach has limited applicability. Another approach to providing dc stabilization of an RTD is the use of large shunt capacitance [19]. Even though this would not impact the dc current consumption, its implementation in an oscillator circuit is not always possible due to the large capacitor value required

Manuscript received March 14, 2019; accepted April 24, 2019. Date of publication June 12, 2019; date of current version August 16, 2019. This work was supported in part by the European Commission through the iBROW and TERAPOD projects under Grant 645369 and Grant 761579. The work of A. C. Cornescu was supported by the Engineering and Physical Sciences Research Council (EPSRC) through a Ph.D. studentship. *(Corresponding author: Edward Wasige.)*

A. C. Cornescu, R. Morariu, A. Ofiare, A. Al-Khalidi, J. Wang, and E. Wasige are with the High Frequency Electronics Group, School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K. (e-mail: edward.wasige@glasgow.ac.uk).

J. M. L. Figueiredo is with the Department of Physics, Faculty of Sciences, University of Lisbon, 1649-004 Lisbon, Portugal.

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Digital Object Identifier 10.1109/TMTT.2019.2916602

TABLE I
RTD EPI-LAYER DESIGN

Layer number	Thickness (Å)	Composition	Doping (cm^{-3})	Description
1	450	$In_{0.53}Ga_{0.47}As$	3E19 : Si	Collector
2	800	$In_{0.53}Ga_{0.47}As$	3E18 : Si	Sub-Collector
3	500	$In_{0.53}Ga_{0.47}As$	5E16 : Si	Space II
4	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
5	11	AlAs	Un-doped	Barrier
6	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
7	14	InAs	Un-doped	Sub-Well
8	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
9	11	AlAs	Un-doped	Barrier
10	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
11	500	$In_{0.53}Ga_{0.47}As$	5E16 : Si	Spacer II
12	800	$In_{0.53}Ga_{0.47}As$	3E18 : Si	Sub-Emitter
13	200	InP	1E19 : Si	Etch Stop
14	4000	$In_{0.53}Ga_{0.47}As$	3E19 : Si	Emitter
15	2000	InP	Un-doped	Buffer
		SI : InP		Substrate

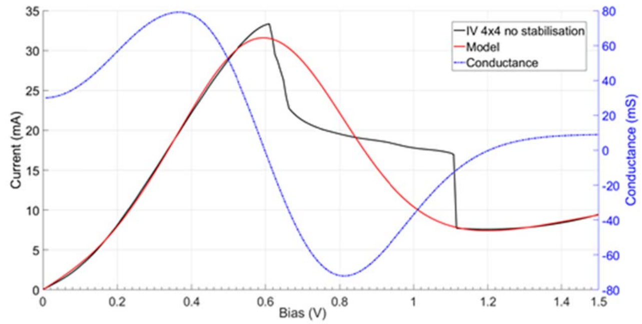


Fig. 1. Measured and modeled I–V characteristic of the 4 μm $\times$ 4 μm RTD device from the epistructure in Table I. The peak voltage is at (0.62 V, 33 mA), the valley voltage at (1.27 V, 6 mA). The device conductance derived from the modeled I–V is also shown (blue trace).

(typically in the picofarad–microfarad range) as this would take up a large chip area in an integrated circuit realization. Nonetheless, this approach has been employed in an RTD wavelet generator circuit in which a gated RTD oscillator works in pulsed mode [20], with the technology forming the basis of commercially available mm-wave radar sensors [5].

In this paper, we report a new RTD oscillator implementation that enables over a tenfold increase in dc-to-RF conversion efficiency. In particular, conventional RTD oscillator designs exhibiting less than 1% efficiency are redesigned to achieve over 10% efficiency, with this being only limited by the employed RTD epitaxial design. The new approach replaces the shunt bias stabilization resistor in the conventional designs with a shunt series resistor–capacitor (RC) network, thereby sharply reducing the dc power requirements but without compromising the oscillator performance. Therefore, the proposed approach could lead to very-high-efficiency high-frequency oscillators.

The paper is organized as follows. Section II describes the RTD epitaxial design, the device characteristics and discusses the new bias stabilization approach. Section III describes the oscillator design and fabrication, while Section IV the oscillator characterization and a discussion of the achieved results. Conclusions are given in Section V.

II. RTD DEVICE

A. RTD Device Structure and Characteristics

The RTD epitaxial layer structure, in this work, consisted of a very-low-energy bandgap (E_g) material, InAs (indium arsenide, $E_g = 0.36$ eV), sandwiched between a low-bandgap material, $In_{0.53}Ga_{0.47}As$ (indium–gallium–arsenide, $E_g = 0.71$ eV), which was, in turn, sandwiched between two high bandgap barriers AlAs (aluminum arsenide, $E_g = 2.15$ eV), making up a double-barrier quantum well (DBQW) structure. The structure is completed by an undoped and/or lightly doped $In_{0.53}Ga_{0.47}As$ spacer layer, an n-type emitter/collector layer and a highly doped contact layer. The complete epitaxial layer structure is shown in Table I and was adapted from [21]. It provides a large peak-to-valley current ratio (PVCR) and low peak voltage, which are essential device characteristics for high-performance oscillator design.

The epitaxial wafer was grown by a commercial supplier using molecular beam epitaxy (MBE) on a semi-insulating InP substrate. The RTD device sizes were chosen as large as possible for high-RF output power and to meet bias stability requirements as described in [22]. Micrometer-sized 4×4 μm^2 RTD devices were fabricated by optical lithography techniques. The mesa size was defined by H_3PO_4:H_2O_2:H_2O wet etching, while the passivation was done using polyimide PI-2545, a low dielectric constant material. The measured I–V characteristic is shown in Fig. 1. From the figure, it is seen that the peak current density and the PVCR of the RTD are 2.18 mA/μm^2 and 5.83, respectively, and the voltage span of the NDR region, ΔV, is approximately 0.65 V, while the peak-to-valley current difference, ΔI, is 27 mA. The maximum RF power of an oscillator using this device can be estimated using the equation [(3/16) $\Delta V \Delta I$)] [23] and is approximately 3.3 mW. The device self-capacitance, C_n, comprises the geometrical capacitance and the quantum well capacitance and was estimated using the approach in [4] to be 125 fF.

The measured I–V characteristic in the NDR region is distorted into the typical plateaulike feature due to the presence of parasitic oscillations during measurement. An analytical model of the I–V was derived by fitting the measured data in the positive differential resistance (PDR) regions using a large signal-based model [24], with the NDR region approximated with a smooth trace as shown in Fig. 1. From the modeled I–V, the device's differential conductance was computed and is also shown in Fig. 1 (blue trace). The device has a maximum negative differential conductance G_n value of -70 mS. The series resistance of the RTD can be estimated from the standard transmission line method (TLM) measurements. The measured ohmic contact resistance was 128 Ω μm^2 for the collector (top) contact layer. Therefore, for the 4×4 μm^2 RTD, the device resistance is approximately 9 Ω. The cutoff frequency of the device was estimated from the device equivalent circuit parameters (C_n, G_n, and contact resistance) [19] and/or from the electron dwell time within the quantum well and the electron transit time through the spacer layer [25], which, for this structure, is around 480 GHz.

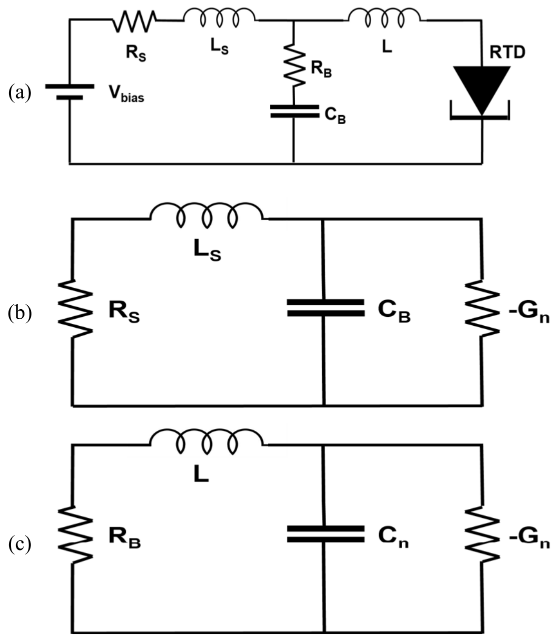


Fig. 2. (a) Proposed stabilization circuit for RTD device, where V_{bias} is the bias voltage, R_S and L_s are the parasitics introduced by the biasing network, R_B and C_B are the shunt stabilizing resistor and capacitor, and L is the inductance of the CPW line. (b) Low-frequency equivalent circuit, L is considered a short and the impedance of R_B is ignored. (c) High-frequency equivalent circuit, L_S is considered an open circuit and the capacitance C_B is a short circuit.

B. Stabilizing Circuit and Its Characterization

The RTD bias stabilization network approach presented in this paper employs the addition of a shunt capacitor C_B connected in series with the stabilizing resistance, to eliminate the dc path to ground. The circuit is shown in Fig. 2(a), where V_{bias} is the bias voltage to set the device in the NDR region, R_S and L_S are the resistance and inductance introduced by the biasing cable, R_B and C_B are the shunt resistor and capacitor, respectively, and L is the series inductance of the contact pads of the device. This stabilization network was used earlier by the authors for the direct characterization of the NDR region of tunnel diodes under stable nonoscillatory conditions [26]. It is being employed in high-efficiency RTD oscillator realization for the first time in this paper.

For low frequencies (megahertz range), the circuit shown in Fig. 2(a) can be simplified to the equivalent circuit shown in Fig. 2(b), where the RTD is represented by its negative differential conductance ($-G_n$) and self-capacitance (C_n). In this case, the inductance L is considered a short circuit, R_B is ignored since the impedance of capacitor C_B becomes dominant and the device capacitance C_n (typically tens of femtofarads) is considered negligible when compared with C_B (typically tens of picofarads). On the other hand, at high frequencies (gigahertz range), the circuit in Fig. 2(a) can be simplified to the equivalent circuit in Fig. 2(c), where the inductance L_B is considered an open circuit and the capacitance C_B is a short circuit. Note that the circuits in Fig. 2(b) and (c) are identical, only with different element values. We analyze the circuit shown in Fig. 2(b) using nodal analysis by applying Kirchoff's current law to give

$$\frac{V}{R_S + sL_S} + sC_BV - G_nV = 0 \tag{1}$$

where V is the voltage across the parallel circuit and s the complex frequency. From (1), we obtain the following characteristic equation:

$$C_BL_ss^2 + (C_BR_S - L_sG_n)s + 1 - G_nR_s = 0. \tag{2}$$

The solutions to (2) are given by

$$s = \frac{(L_sG_n - C_BR_S) \pm \sqrt{(C_BR_S - L_sG_n)^2 - 4C_BL_s(1 - G_nR_s)}}{2C_BL_s}. \tag{3}$$

The roots of (3) can be classified into two possible cases.

Case 1: the solutions are complex and, therefore,

$$(C_BR_S - G_nL_s)^2 - 4C_BL_s\,(1 - G_nR_s) < 0. \tag{4}$$

For the circuit to be stable, the solutions of (3) must fall on the left half of the complex frequency plane. As a result, the circuit is stable if

$$R_S > \frac{L_sG_n}{C_B} \quad \text{or} \quad C_B > \frac{L_sG_n}{R_S}. \tag{5}$$

Case 2: the solutions are real and so

$$(C_BR_S - G_nL_s)^2 - 4C_BL_s(1 - G_nR_s) > 0. \tag{6}$$

For these solutions to fall in the left half of the complex frequency plane, the magnitude of the term under the square root sign of (3) must be smaller than the magnitude of the first term, so

$$R_s < \frac{1}{G_n}. \tag{7}$$

Combining the conditions derived from case 1 and 2, the condition to achieve low-frequency circuit stability is

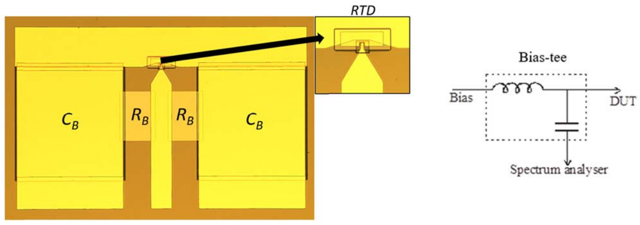
$$\frac{L_sG_n}{C_B} < R_s < \frac{1}{G_n}. \tag{8}$$

Since the circuits shown in Fig. 2(b) and (c) are identical, (8) can be rewritten with the corresponding elements to provide the condition for stability at high frequencies as

$$\frac{LG_n}{C_n} < R_B < \frac{1}{G_n}. \tag{9}$$

From (5), (8), and (9), the chosen values of the R_B and C_B were 10 Ω and 144 pF, respectively. Here, R_S and L_S were approximated to be 2 Ω and 900 pH, respectively. L_S was assumed to be dominated by the bias-T inductance. C_n was 125 fF and G_n was −70 mS as earlier noted.

To determine the efficacy of the proposed bias stabilization approach, devices with and without bias stabilization were fabricated. The resistor R_B was realized with thin film nichrome (NiCr) deposition. The integrated capacitor ($C_B = 140$ pF) was realized as a metal-insulator metal (MIM) capacitor with a thin 75nm Si_3N_4 dielectric layer deposited by inductively coupled plasma (ICP) chemical vapor deposition (CVD), while the RTD was realized as earlier described.



(a) (b)

Fig. 3. (a) Micrograph of a fabricated 4 μm × 4 μm RTD device with an integrated stabilizing network. Inset: actual RTD. The capacitor C_B and resistance R_B are each realized from two parts and are placed in parallel with the RTD. (b) Setup for measuring bias oscillations using a bias tee. DUT is either an unstabilized or stabilized RTD device.

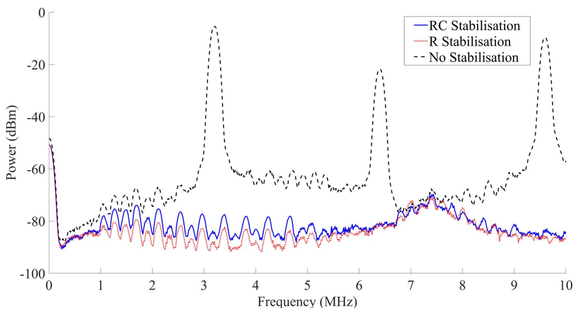
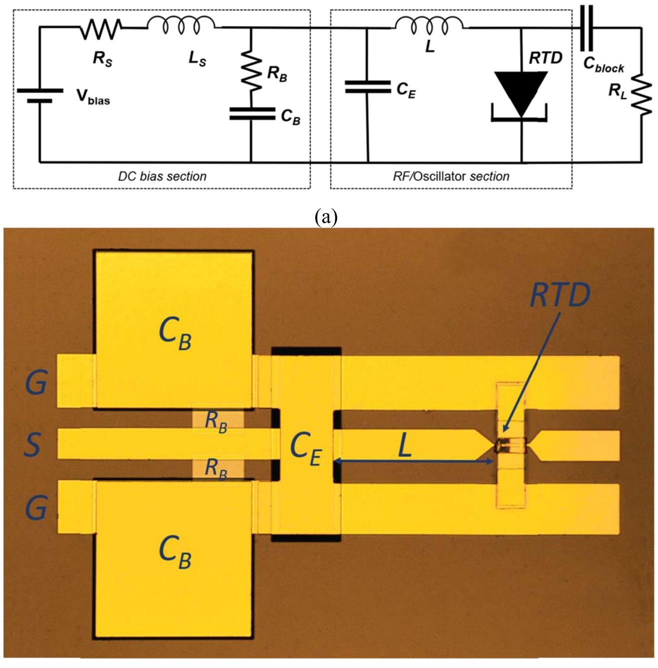


Fig. 4. Measured spectrum on bias lines at $V_{\text{bias}} = 0.8$ V, i.e., in the NDR region for 4 × 4 μm^2 RTD devices with and without stabilization (dashed black line). No bias oscillations detected for both shunt resistor (red trace) and shunt series resistor–capacitor stabilization (blue trace).



(a)

(b)

Fig. 5. (a) Schematic circuit of an oscillator employing a resistor and capacitor stabilization network (R_B, C_B). The section in the dashed rectangle as realized as MMIC. (b) Micrograph of the fabricated RTD oscillator with an integrated stabilizing network. For measurement, a GSG probe is used. The capacitor C_B and resistance R_B are split in two and placed in parallel with the RTD. The capacitor C_E acts as a short to ground for the RF signal.

A micrograph of the fabricated device having the RC stabilizing network is shown in Fig. 3. Due to the used coplanar waveguide (CPW) pad configuration, both R_B and C_B were realized from two identical parts connected in parallel.

Bias oscillations for an individual unstabilized RTD device were first characterized using a spectrum analyzer [see Fig. 3(b)]. The device was biased in the NDR region through the dc port of the bias tee with the spectrum analyzer connected to the RF port and the device under test (DUT) to the dc + RF port. Fig. 4 shows the measured bias oscillations whose frequency is determined largely by the connecting coaxial cable, bias tee inductance, and the device capacitance, and lie in the 2–3 MHz range for fundamental oscillations (black trace). This experiment was then repeated for RTD devices with the conventional shunt resistor bias stabilization (red trace) and the other with the shunt series RC bias stabilization (blue trace). No bias oscillations are observed for the stabilized devices.

III. RTD Oscillator Design and Fabrication

The schematic of the oscillator circuit employing the high-efficiency bias stabilization network is shown in Fig. 5(a). It also employs a decoupling capacitor C_E (30 pF) which was added to create a short circuit path for the RF oscillator signal, and so avoid the loss of RF power in the stabilizing network. At low frequencies, C_E and C_B are in parallel (R_B is ignored) and can be combined, and so the analysis described in Section II is applicable. The inductance L is realized as a short-circuited CPW and along with the device capacitance determines the oscillation frequency. The value for L was 140 pH in our design for the ∼30 GHz oscillators. This was realized with a CPW transmission line that was terminated with capacitor C_E (which acts as an RF short circuit at the oscillation frequency). The choice of the oscillation frequency of around 30 GHz was to facilitate easier circuit realization and characterization to demonstrate the proposed bias stabilization concept.

The RTD and passive components were fabricated as earlier described. The complete monolithic microwave integrated circuit (MMIC) fabrication process is described in [8]. R_L is the load resistance introduced by the spectrum analyzer which is 50 Ω with a coaxial dc block in between. A micrograph of the fabricated oscillator circuit is shown in Fig. 5(b). The overall size of the oscillator circuit was around 1000 × 700 μm^2.

The same measurements that are described in Fig. 4 were carried out on the oscillator circuit and no low-frequency parasitic oscillations were observed.

IV. Measurement Results

The MMIC RTD oscillator frequency was measured on-wafer using an Agilent E4448A spectrum analyzer (3 Hz–50 GHz). The measured spectrum is shown in Fig. 6(a). When the bias voltage is 0.94 V, the RTD oscillates at 34 GHz with an output power of 3.95 dBm. The dc current was 18 mA and so the dc-to-RF conversion efficiency was 14.7%. This compares well to the estimated maximum oscillator

(a)

(b)

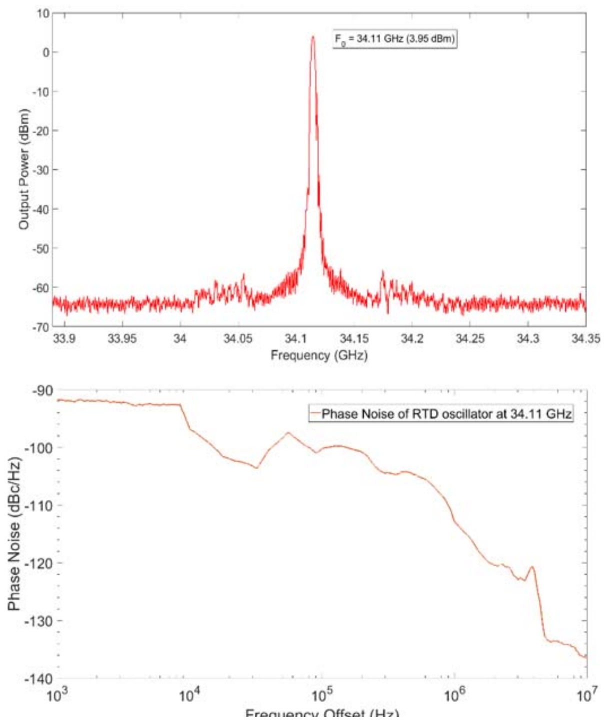


Fig. 6. (a) Measured output spectrum of RTD oscillator with capacitor and resistor stabilizing network at $V_{\mathrm{BIAS}} = 0.94$ V, $I_{\mathrm{BIAS}} = 18$ mA. (b) Measured SSB phase-noise performance at the 34.1 GHz carrier frequency.

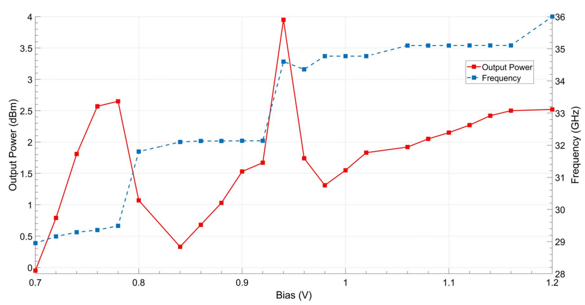


Fig. 7. Measured oscillator output power and frequency as a function of bias voltage.

power from the device's NDR region of 3.3 mW (5.18 dBm), i.e., theoretical dc-to-RF efficiency of around 19.5%. For this measurement setup, the insertion loss of the probe, dc block, and cable between the oscillator and the spectrum analyzer was measured to be 3.4, 5.4, and 5.46 dB at 25, 30, and 35 GHz, respectively, and was corrected from the reported results. For an RTD oscillator employing only a 10-Ω shunt resistance for stabilization, the dc current was 100 mA and the dc-to-RF conversion efficiency was 0.93 %. This low efficiency is clearly due to the dc power that is dissipated through the low-value shunt resistance.

The phase noise of the RTD oscillators was also measured and a typical result is plotted in Fig. 6(b). At 100 kHz and 1 MHz offset frequencies, the phase noise values were -100.2 and -112.9 dBc/Hz, respectively. The values are comparable with an RTD oscillator stabilized with a shunt resistor realized on the same wafer. The measured low phase noise is consistent with our earlier results [7] and is key to applications such as wireless communications or radar. Fig. 7 shows the oscillator spectrum and output power measurements at different bias levels for the high-efficiency oscillator. It has a tuning range of about 7 GHz and high output power of around 1–2 dBm across most of this range, corresponding to efficiencies of around 6%–10%.

V. Conclusion and Discussion

Highly efficient mm-wave RTD oscillators with a tunable frequency between 29 and 36 GHz were presented in this paper. They employ a bias stabilization network that does not consume dc power resulting in over a tenfold improvement in dc-to-RF conversion efficiency. The oscillators also exhibit low phase noise. For further higher dc-to-RF oscillator efficiencies, a reduction of the peak voltage and of the valley current is necessary. Compared to other semiconductor electronic technologies, RTD oscillators provide a simple, low-cost solution for future short-range high-capacity wireless communication systems and other applications, and as such improvements need to be made to increase their output power ($\sim$10 mW at $>$100 GHz) and efficiency ($>$20%). For high-RF output power, increasing the span of the NDR region is required. Therefore, future work will, thus, focus on designing advanced RTD epitaxial layer structures and optimally loaded mm-wave and THz oscillators using this high-efficiency bias stabilization approach.

Acknowledgment

The authors would like to thank the staff of the James Watt Nanofabrication Center (JWNC), University of Glasgow, for helping in the fabrication of the devices reported in this paper.

References

[1] S. Diebold *et al.*, "High-speed error-free wireless data transmission using a terahertz resonant tunnelling diode transmitter and receiver," *Electron. Lett.*, vol. 52, no. 24, pp. 1999–2001, Nov. 2016.

[2] T. Miyamoto, A. Yamaguchi, and T. Mukai, "Terahertz imaging system with resonant tunneling diodes," *Jpn. J. Appl. Phys.*, vol. 55, no. 3, 2016, Art. no. 032201.

[3] N. Oshima, K. Hashimoto, S. Suzuki, and M. Asada, "Wireless data transmission of 34 Gbit/s at a 500-GHz range using resonant-tunnelling-diode terahertz oscillator," *Electron. Lett.*, vol. 52, no. 22, pp. 1897–1898, Oct. 2016.

[4] J. Wang, A. Al-Khalidi, L. Wang, R. Morariu, A. Ofiare, and E. Wasige, "15-Gb/s 50-cm wireless link using a high-power compact III–V 84-GHz transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4698–4705, Nov. 2018.

[5] *A1 Radar Sensor*. Accessed: Jun. 6, 2019. [Online]. Available: https://www.acconeer.com/products

[6] R. Izumi, S. Suzuki, and M. Asada, "1.98 THz resonant-tunneling-diode oscillator with reduced conduction loss by thick antenna electrode," in *Proc. 42nd Int. Conf. Infr., Millim., THz Waves (IRMMW-THz)*, Aug./Sep. 2017, pp. 1–2.

[7] J. Wang, L. Wang, C. Li, B. Romeira, and E. Wasige, "28 GHz MMIC resonant tunnelling diode oscillator of around 1mW output power," *Electron. Lett.*, vol. 49, no. 13, pp. 816–818, Jun. 2013.

[8] J. Wang *et al.*, "High performance resonant tunneling diode oscillators for THz applications," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2015, pp. 1–4.

[9] J. Wang *et al.*, "High performance resonant tunneling diode oscillators as terahertz sources," in *Proc. 46th Eur. Microw. Conf. (EuMC)*, Oct. 2016, pp. 341–344.

[10] A. Al-Khalidi, J. Wang, and E. Wasige, "Compact J-band oscillators with lm RF output power and over 110 GHz modulation bandwidth," in *Proc. 43rd Int. Conf. Infr., Millim., THz Waves (IRMMW-THz)*, Sep. 2018, pp. 1–2.

[11] A. Al-Khalidi, K. Alharbi, J. Wang, and E. Wasige, "THz Electronics for data centre wireless links—The TERAPOD project," in *Proc. 9th Int. Congr. Ultra Mod. Telecommun. Control Syst. Workshops (ICUMT)*, Nov. 2017, pp. 445–448.

[12] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.

[13] R. Lachner, "Overview of new Si-based mm-wave technologies and packaging solutions and their potential impact on future mm-wave sensing in automotive and industrial applications," in *Proc. Workshop Future Automot. Radar Towards Auto. Driving, Eur. Microw. Week*, Sep. 2018.

[14] C. Kidner, I. Mehdi, J. R. East, and G. I. Haddad, "Bias circuit instabilities and their effect on the d.c. current-voltage characteristics of double-barrier resonant tunneling diodes," *Solid-State Electron.*, vol. 34, no. 2, pp. 149–156, Feb. 1991.

[15] M. Reddy *et al.*, "Bias stabilization for resonant tunnel diode oscillators," *IEEE Microw. Guided Wave Lett.*, vol. 5, no. 7, pp. 219–221, Jul. 1995.

[16] M. Q. Bao and K. L. Wang, "Accurately measuring current-voltage characteristics of tunnel diodes," *IEEE Trans. Electron Devices*, vol. 53, no. 10, Oct. 2006, pp. 2564–2568.

[17] S. Suzuki, K. Hinata, M. Shiraishi, M. Asada, H. Sugiyama, and H. Yokoyama, "RTD oscillators at 430–460 GHz with high output power (200 μW) using integrated offset slot antennas," in *Proc. 22nd Int. Conf. Indium Phosph. Rel. Mater. (IPRM)*, May/Jun. 2010, pp. 1–4.

[18] J. T. Wallmark and A. H. Dansky, "Nonlinear biasing resistors for microwave tunnel-diode oscillators," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-11, no. 4, pp. 260–262, Jul. 1963.

[19] C. Kidner, I. Mehdi, J. R. East, and G. I. Haddad, "Power and stability limitations of resonant tunneling diodes," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 7, pp. 864–872, Jul. 1990.

[20] M. Egard, M. Ärlelid, E. Lind, and L.-E. Wernersson, "Bias stabilization of negative differential conductance oscillators operated in pulsed mode," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 672–677, Mar. 2011.

[21] T. Broekaert, W. Lee, and C. Fonstad, "Pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs/InAs resonant tunneling diodes with peak-to-valley current ratios of 30 at room temperature," *Appl. Phys. Lett.*, vol. 53, no. 16, p. 1545, Aug. 1988.

[22] L. Wang, "Reliable design of tunnel diode and resonant tunnelling diode based microwave and millimeterwave sources," Ph.D. dissertation, Univ. Glasgow, Glasgow, U.K., 2011.

[23] C. S. Kim and A. Brändli, "High-frequency high-power operation of tunnel diodes," *IRE Trans. Circuit Theory*, vol. CT-8, no. 4, pp. 416–425, Dec. 1961.

[24] S. F. Nafea and A. A. S. Dessouki, "An accurate large-signal SPICE model for resonant tunneling diode," in *Proc. Int. Conf. Microelectron. (ICM)*, Cairo, Egypt, Dec. 2010, pp. 507–510.

[25] M. Asada, S. Suzuki, and N. Kishimoto, "Resonant tunneling diodes for sub-terahertz and terahertz oscillators," *Jpn. J. Appl. Phys.*, vol. 47, no. 6R, p. 4375, Jun. 2008.

[26] L. Wang, J. M. L. Figueiredo, C. N. Ironside, and E. Wasige, "DC characterization of tunnel diodes under stable non-oscillatory circuit conditions," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 343–347, Feb. 2011.

Andrei Catalin Cornescu received the B.Eng. degree in electronics and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2015, where he is currently pursuing the Ph.D. degree in the design and characterization of resonant tunneling diode (RTD)-based terahertz oscillators and detectors.

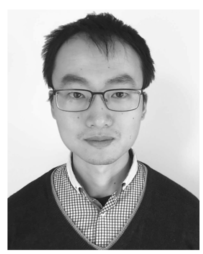
Razvan Morariu received the M.Eng. degree in electronics and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2016, where he is currently pursuing the Ph.D. degree in the design and characterization of RTD-based terahertz oscillators and detectors.

Afesomeh Ofiare received the B.Eng. degree in electrical and electronic engineering from Madonna University, Okija, Nigeria, in 2005, and the M.Sc. and Ph.D. degrees in electronic and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2009 and 2016 respectively.

He is currently a Research Assistant with the University of Glasgow. His current research interests include high-frequency device characterization, antennas for millimeter-wave and terahertz applications, and wireless communications.

Abdullah Al-Khalidi received the B.Eng., M.Sc. and Ph.D. degrees from the University of Glasgow, Glasgow, U.K., in 2010, 2011, and 2015, respectively.

He is currently a Post-Doctoral Researcher with the University of Glasgow. His current research interests include terahertz resonant tunneling diodes (RTDs) and gallium nitride (GaN) transistor technologies.



Jue Wang received the Ph.D. degree in electronics and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2014.

Since 2014, he has been a Post-Doctoral Researcher with the University of Glasgow, where he is involved in resonant tunneling diode-based terahertz oscillator design. His current research interests include high-power terahertz devices and terahertz applications including wireless communications, imaging, and so on.

José M. L. Figueiredo (M'09) received the B.Sc. degree in physics and the M.Sc. degree in optoelectronics and lasers from the University of Porto, Porto, Portugal, in 1991 and 1995, respectively, and the Ph.D. degree in physics from the University of Porto in "co-tutela" with the University of Glasgow, Glasgow, U.K., in 2000.

His work at the University of Glasgow was on the optoelectronic properties of resonant tunneling diodes (RTDs). He is currently with the Department of Physics, Faculty of Sciences, University of Lisbon, Lisbon, Portugal. His current research interests include applications of RTDs and RTD-based optoelectronic devices, and neural-inspired photonic circuits.

Edward Wasige (S'97–M'01) received the B.Sc.Eng. degree in electrical engineering from the University of Nairobi, Nairobi, Kenya, in 1988, the M.Sc.Eng. degree from the University of Liverpool, Liverpool, U.K., in 1990, and the Ph.D. degree in electrical engineering from Kassel University, Kassel, Germany, in 1999.

He was a Lecturer at Moi University (Kenya), up to 2001, and a UNESCO Postdoctoral Fellow at the Technion–Israel Institute of Technology, from 2001 to 2002. He has been a Lecturer at the University of Glasgow, Glasgow, U.K., since 2002. His current research interests include compound semiconductor micro/nanoelectronics and applications with a focus on GaN electronics and RTD-based terahertz electronics.