Synchronization-Phase Alignment of All-Digital Phase-Locked Loop Chips for a 60-GHz MIMO Transmitter and Evaluation of Phase Noise Effects

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***Abstract*— A phase-coherent technique for multiple all-digital phase-locked loops (ADPLLs) is presented and developed in this paper to target a 57–63-GHz multiple-input multiple-output (MIMO) transmitter (TX) with a digital beam-steering capability. The ADPLL TX chains are first fabricated in nanoscale CMOS and then time-synchronized and frequency–phase locked by a field-programmable gate array (FPGA) evaluation board. The calibration approach for phase alignment is carried out using a cancellation method to acquire the out-of-phase state within two ADPLLs. The accuracy of beam steering and phase alignment is investigated and analyzed based on a time-domain model for ADPLL to consider the impact of phase noise. The analysis results offer the required values of the ADPLL parameters to allow a millimeter-wave (mm-wave) MIMO TX with a highly accurate digital beam-steering capability.**

***Index Terms*— All-digital phase-locked loop (ADPLL), beamforming, cancellation method, digital beam steering, highly accurate beam steering, phase coherence, phase noise, phase-alignment accuracy, 60-GHz multiple-input multiple-output (MIMO).**

I. Introduction

MULTIPLE-INPUT multiple-output (MIMO) communications at millimeter-wave (mm-wave) frequencies (e.g., in the 60-GHz band) are a modern technology recently considered for various applications, such as emerging 5G services for multiuser MIMO (MU-MIMO) [1]–[5] and high-resolution frequency-modulated continuous-wave (FMCW) MIMO radars [6]–[9] to support multigigabit throughputs in the short-range environments via spatial multiplexing and diversity. For these reasons, the IEEE 802.11ay standard is being proposed and is now under significant considerations as the extension of IEEE 802.11ad with throughput capabilities up to 100 Gb/s utilizing MIMO features. This standard is supposed to be finalized in 2019 [10]–[12]. Nevertheless, the impairments of communication channels in this frequency band, including significant propagation loss and severe blockage effect, are quite challenging to allow an efficient communication link. Hence, beamforming/beam steering can play a crucial role in 60-GHz MIMO systems to overcome the destructive influence of the communication channel by supporting sufficient antenna gain and tilting the antenna beam to the desired direction. Numerous antenna array topologies have been reported to realize the MIMO beam steering [13]–[17], and diverse techniques have been applied to implement the beamforming method involving digital baseband [18], purely radio-frequency (RF) digital phase shifter [19], hybrid RF analog phase shifter/digital baseband [20]–[22], antenna selection [23], and precoding algorithms such as code booking [24], QRD [25], and SVD [26]. The beamforming mechanism is built either at both transmitter (TX)–receiver of the link [27] or only at the TX [28]. This is specified by the status of the channel state information (CSI) known only by the TX or both. In fact, beam steering is much more practical and advantageous at the TX side than at the receiver side. The beamforming operation yields considerable improvements in the channel budget and capacity of the MIMO communications [29], [30]. As mm-wave antenna arrays are directive with very narrow beams, the accuracy of beam steering is so vital in ensuring suitable wireless communication.

All-digital phase-locked loops (ADPLLs) have been employed extensively [31]–[33] in recent years, because their precise control of the loop functionality is feasible in a fully digital manner with resolution often limited only by the digital word length. Having this ability, the ADPLL can be utilized as a variable phase-steering element to develop a 60-GHz MIMO TX [34]. The all-digital blocks enable the exact control of the array beam, which is currently realized by analog components or less accurate digital phase shifters. Principally, the ADPLL can provide a full-range (0°–360°) phase tuning with the resolution of much better than 1° at 60 GHz (limited only by the digital word length and phase noise), which is comparable with the best state-of-the-art CMOS phase shifters [35], [36].

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Moreover, a more compact and cost-effective V-band MIMO TX can be exploited by using the CMOS ADPLL technology instead of upconverter MIMO structures (either superheterodyne or direct conversion) [18], [37]–[40] and along with a 60-GHz frequency multiplier [41], where more complex hardware and costs are imposed. Additionally, further flexibility and reconfigurability are achievable with regard to the digitally intensive characteristics of the TX to fulfill a highly accurate digital beam-steering capability. It is worth mentioning that an mm-wave ADPLL-based beam-steering TX has been described but not investigated in the previous works [42].

Concerning the accurate adjustment of phase shift for this system and very directional mm-wave antennas, a calibration procedure is required to align the output amplitude and phase of the different ADPLL elements very precisely before applying the desired phase weights to each chain [43]–[46]. In this paper, a highly accurate phase-alignment calibration approach is proposed and developed for the intended 57–63-GHz ADPLL MIMO TX to serve with a strict digital beam-steering capability. Our calibration procedure is based on a cancellation method to acquire the equiamplitude and out-of-phase conditions in two ADPLL elements using signal combining [45]. This technique is exploited by several applications, including the phase coherence of multielement systems, such as MIMO (e.g., our proposed TX) and phased arrays, interferometry for phase noise reduction of an oscillator, suppression of the local oscillator (LO)-to-RF leakage for direct converters, and adaptive cancellation for full-duplex transceivers and FMCW radars [47], [48]. In all these systems, only a single oscillator is taking part in the calibration mechanism; however, two ADPLLs with independent noise sources are present in our chosen cancellation method. Thus, phase noise is a key concern in the combining process of the two signals, which could degrade the phase-alignment performance (contrary to an upconverter MIMO system in which only a single LO is adopted). Owing to the importance of phase noise for this calibration, the influence of the ADPLL phase noise on the cancellation method is studied both theoretically and numerically in this paper using the ADPLL time-domain model to reach the appropriate ADPLL specifications for highly precise beam pointing. It is noteworthy that any such analysis of the phase noise impact on the phase-alignment process has not been conducted elaborately in the literature since the proposed MIMO topology is quite novel.

Section II introduces the ADPLL MIMO TX architecture and explains the theory of operation. The proposed calibration procedure is implemented, a validation experiment is performed using the existing CMOS ADPLL chips, and the measurement results are presented in Section III. In Section IV, the ADPLL phase noise sources are identified and the phase noise effect on the calibration phase alignment is evaluated by the mathematical formulation and numerical simulation.

II. MIMO TX Architecture and Theory of Operation

The construction of the proposed 60-GHz MIMO TX is shown in Fig. 1 [34]. This paradigm of an MIMO scheme

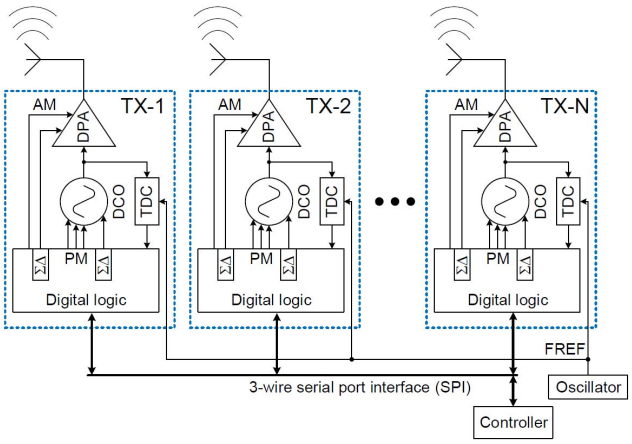

Fig. 1. Proposed 60-GHz MIMO TX with a digital beam-steering capability, from [34].

is formed upon an array of ADPLL-based TXs and antennas whereby each TX chain is dedicated and in close proximity to an individual antenna unit. The antenna elements are normally spaced by half-wavelength in order to offer maximum beam-steering coverage. This system is realized either as an RF system-on-chip (RF-SoC) with the dedicated antenna array element nearby or as a system-in-package (SiP) in which each ADPLL, as an integral part of RF-SoC, is integrated with the antenna array element inside the package; hence, for both topologies (RF-SoC and SiP), the TX-antenna separation can be a small fraction of the interelement spacing (a fraction of millimeter). Recent advancements in the CMOS technology and digitally intensive mm-wave front-end architectures provide a quite dense and cost-effective MIMO solution compared with the other MIMO structures, specifically upconverters. Our proposed solution avoids drawbacks arising from high power losses of mm-wave interconnects, since each CMOS integrated circuit (IC) chip can be placed very close to its antenna element. In this topology (see Fig. 1), all ADPLL chains are phase-locked at a single-frequency reference by a common reference crystal oscillator that controlled digitally by a host controller, i.e., a field-programmable gate array (FPGA) or a microcontroller (depending on the control sophistication) via a simple serial peripheral interface (SPI) bus. This digital control gives a remarkable flexibility to configure each ADPLL in terms of the loop operating mode and disable/enable certain functionalities and adjust various parameters consisting of RF/analog, digital loop, modulation, and test/debug. Furthermore, all ADPLL chains are time-synchronized and frequency-locked through this mechanism. For beam-steering purposes, the system is monitored via the main 60-GHz output and a test 2-GHz output (a replica of the 60-GHz output divided by 32) per chain. Once all the TX chains are frequency-/phase-locked and time-synchronized, the calibration approach (discussed in Section III) is performed to compensate the unwanted amplitude–phase mismatch of the ADPLLs and align the amplitude and phase of the whole elements. Afterward, the intentional phase offsets are numerically entered to the chains to achieve a V-band highly accurate beam-steering unit (BSU).

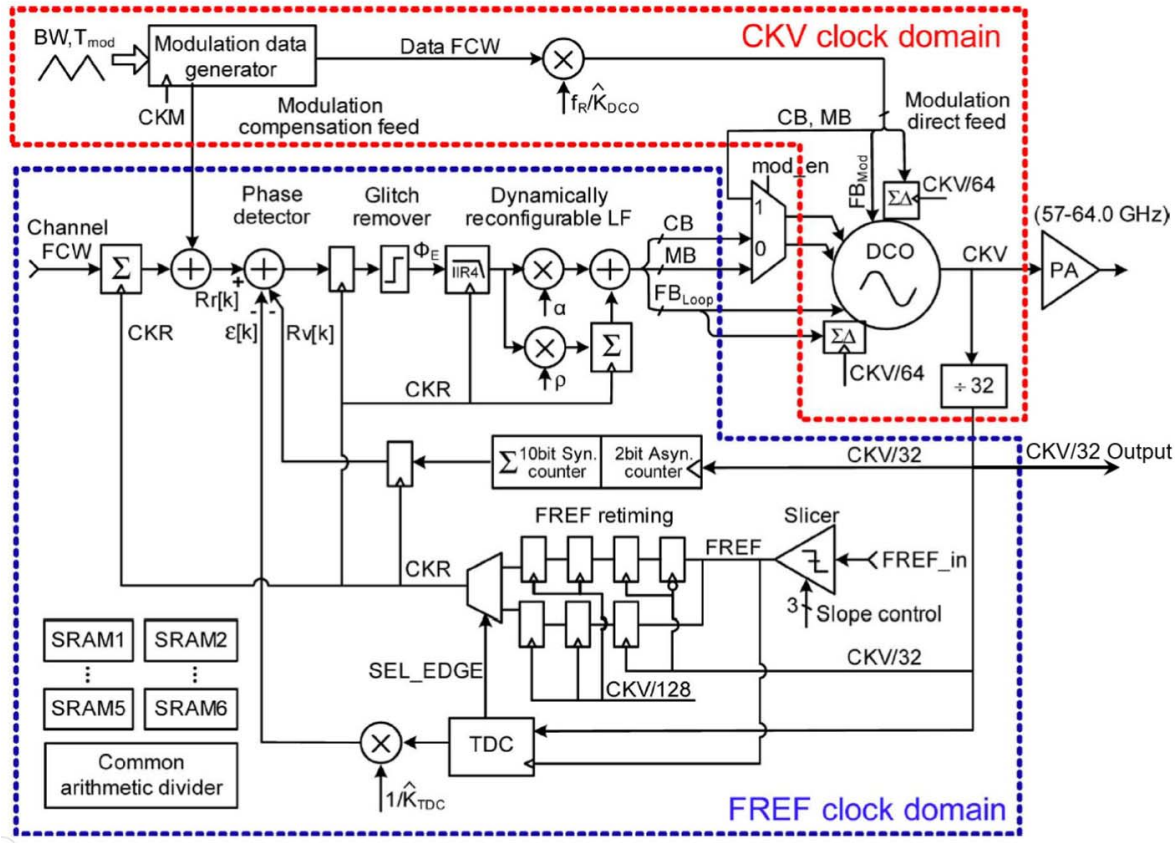

Fig. 2. Block diagram of the employed 60-GHz ADPLL with controllable phase, from [49].

Fig. 2 shows the detailed block diagram of the utilized ADPLL chip realized in the 65-nm CMOS technology aimed for 60-GHz FMCW radar applications [49]. The ADPLL is a digitally synchronous fixed-point phase-domain architecture. The building blocks are classified into analog and digital domains. On the one hand, the fundamental analog blocks comprise a 60-GHz digitally controlled oscillator (DCO), a frequency divider (to procure a divide-by-32 (CKV/32) signal at 2 GHz for monitoring purposes as a feedback output (shown in Fig. 2) and for the loop operations), an FREF slicer (to create a square-wave FREF signal from the external crystal oscillator), a time-to-digital converter (TDC) (to calculate the fractional part of the CKV/32-to-FREF ratio $\varepsilon[k]$), and an output power amplifier (PA) (to deliver enough RF output power at 60 GHz). On the, other hand, the digital portion contains a variable phase accumulator consisting of a 2-bit asynchronous and a 10-bit synchronous counters (to count the number of rising clock transitions of the CKV/32 clock signal and compute $R_V[k]$ as the integer variable phase); an FREF retiming circuit including a couple of flip-flops (to oversample the FREF signal by both rising (top four flip-flops) and falling (bottom three flip-flops) edges of the CKV/32 signal simultaneously to reduce metastability in FREF retiming) and a multiplexer (to select either the rising or the falling edge generated clock using the SEL_EDGE edge-selection signal derived from the TDC delay chain that chooses the path furthest away from the metastable region and, ultimately, to produce a retimed clock CKR as a synchronous system clock for the low-speed-digital circuitries of the loop); a reference phase integrator (to accumulate the channel frequency command word (FCW) with every rising edge of CKR and build the reference phase $R_r[k]$); a synchronous arithmetic-phase error detector (to estimate the digital phase error term $\phi_E[k] = R_r[k] - R_V[k] - \varepsilon[k]$); a simplified glitch removal circuit (to compare the absolute value of the ϕ_E jump with a half-integer threshold and correct potential misalignment between $R_V[k]$ and $\varepsilon[k]$ coming from the TDC); a digital reconfigurable loop filter involving a proportional attenuator α (for fast frequency/phase acquisition during the locking process) together with an integration factor ρ (to offer better filtering of the DCO noise within the loop bandwidth) and a fourth-order infinite-impulse-response (IIR) filter (to suppress the TDC and reference noise outside the loop bandwidth and improve the overall phase noise performance and, finally, to condition and convert the phase error ϕ_E into a digital tuning word with a three-bank format (coarse bank (CB), mid bank (MB), and fine bank (FB) with 400-, 35-, and 1.8-MHz frequency resolution, respectively) for the DCO and amend the frequency-phase error of the loop; a sigma–delta ($\Sigma\Delta$) operating at about 1-GHz clock (to enhance the ADPLL frequency resolution up to 400 Hz by dithering). The output power of the PA is 5 dBm ± 1 dB on 50-Ω load in the entire tuning range of 56.4–63.4 GHz. The whole ADPLL can be configured by 128 8-bit programmable registers through the SPI port.

The modulating data are injected by a two-point modulation scheme to support wide bandwidth for MIMO and FMCW radar systems. The modulation data generator synchronized by a high-speed modulation clock (CKM) feeds both the reference phase accumulator (with low-pass characteristics) and the DCO tuning word banks (with high-pass properties) with exactly the same signal called data FCW to create an all-pass response and meet a wideband modulation behavior. A multiplexer is embedded to select the FB either from the loop (FB_{Loop} in the continuous-wave mode) or through the modulation path (FB_{Mod} in the modulation mode). To synchronize the digital modulating streams precisely (1° resolution is equivalent to 46 fs at 60 GHz) for the different ADPLLs which is quite vital for both the beam-steering and MIMO modes, the CKM clock is always synchronized with the retimed system clock CKR via resampling of the FREF signal by the CKV/128 signal from which the CKM clock is created (viewed in Fig. 2 in the FREF retiming circuit). Owing to using a single reference oscillator for all the ADPLLs, all CKR, all CKM, and, hence, all the modulation streams will be synchronized. To target a digital BSU, the output phase of the digital loop can be adjusted either by means of a direct phase offset register or via a two-point single-pulse frequency modulation. In the former, the phase error term (ϕ_E in Fig. 2) is altered by an intentional phase offset applied on the digital loop filter, whereas in the latter, the FCW in the two-point modulation path (data FCW) is varied for a short duration to yield a phase change of the overall loop governed by

$$\Delta\varphi_0 = 2\pi f_r M \int_{t_0}^{t_0+\Delta t} \Delta(\mathrm{FCW}) d\tau \tag{1}$$

where f_r is the reference frequency and $M = 32$ is the frequency division factor of the DCO divider. Fig. 3 shows these two phase-tuning approaches. To simplify the implementation, the first solution (the phase offset register) is chosen.

III. Calibration Implementation and Experimental Results

Following the antenna array theory, the beam-steering angle of a uniform linear array is stated by the following equation [50]:

$$\sin\theta_{\max} = -\frac{\alpha}{kd} \tag{2}$$

where $k = (2\pi/\lambda_0)$ is the wavenumber, d is the interelement spacing (usually $d = (\lambda_0/2)$), and α is the progressive phase shift among the elements. The required accuracy of the phase offset can be calculated as

$$\partial\alpha = -kd(\cos\theta_{\max})\partial\theta_{\max}. \tag{3}$$

To attain the beam tilting precision of $\partial\theta_{\max} = 1°$ for an array of half-wavelength distance with the maximal beam-steering coverage of 60°, the needed accuracy for the phase shift will be

$$|\partial\alpha| = \pi \times 0.5 \times 1° = 1.57°. \tag{4}$$

This implies an error of less than 2° for the phase-steering component, which is really challenging in the 60-GHz band.

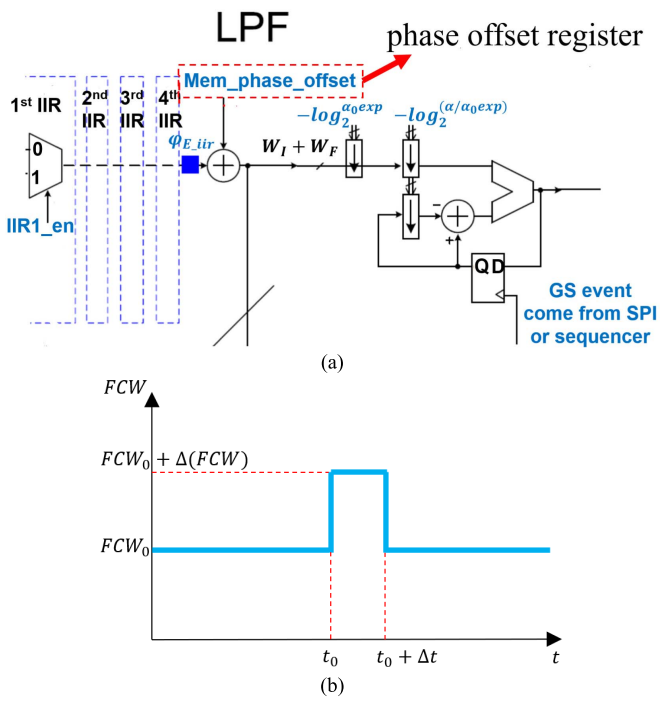

Fig. 3. Digital phase adjustment of the ADPLL TX. (a) Phase offset register. (b) Two-point single-pulse frequency modulation.

Consequently, the digitally intensive approach is selected for the proposed mm-wave MIMO-beam-steering TX by the usage of the ADPLL technology to supply the above-mentioned accuracy. Therefore, the beam-steering precision is just confined by the accuracy of the phase-alignment calibration, and subsequently, a highly accurate calibration is crucial to eliminate the amplitude–phase imbalance of the ADPLL elements due to either static factors, such as imperfections from process strength (P) and fabrication-assembly tolerances, or dynamic issues, such as voltage–temperature (VT) variations of CMOS circuitry.

A. Calibration Procedure

The primary calibration of the intended MIMO TX should synchronize and amplitude and phase align all the TX elements, including the ADPLLs, the feeding lines, and the antenna array, to account for all the contributors within each TX element. Note that there is no dedicated feeding network in the proposed architecture (see Fig. 1) since the interconnects' length can be very short (as short as a fraction of millimeter) and this interconnection is merely a simple and very short one-to-one feed line. This introduces an over-the-air calibration, which can be implemented by the round-robin strategy [45], for which one system chain is taken as the reference and the other ones are amplitude-phase aligned with this element. Assume that *element (1)* is the reference, and *element (i)* under test is calibrated by tuning its amplitude and phase, while these parameters remain fixed for the reference to acquire the equal-amplitude and out-of-phase conditions. This is accomplished by spatial combining of the output signals of the two elements by means of radiation pattern measurement. The radiation pattern of the 2×1 integrated antenna array (consisting of

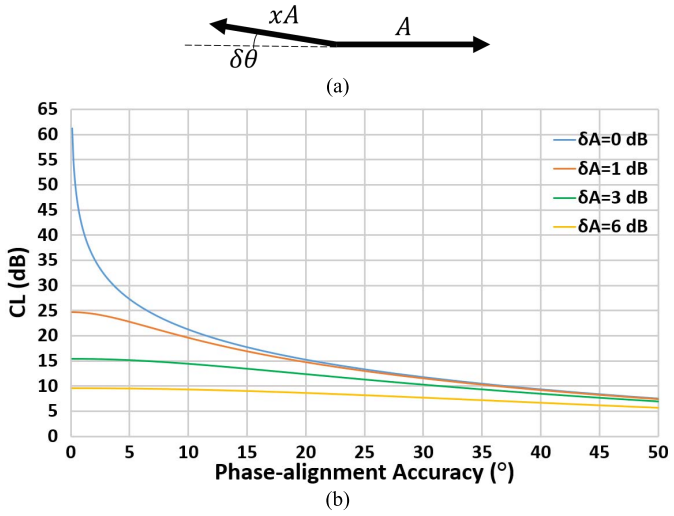

Fig. 4. Cancellation method for calibration. (a) Phasor diagram. (b) Graphs of the CL versus the phase-coherence accuracy for different values of the amplitude mismatch $\delta A = 0, 1, 3, 6$ dB.

the reference and the under-test elements) creates a null at broadside direction as the cancellation point. Prior to this step and to verify that the ADPLL concept can provide the required accuracy for this calibration, the synchronization mechanism can be explored by a simpler validation method without the antennas, since the antenna system does not contribute to the ADPLLs' synchronization verification and is rather static with geometry-defined characteristics. Therefore, the adopted validation scheme is developed based on the power combining of the two standalone ADPLL chains (excluding the antenna system) using a power combiner and monitoring the output power of the combiner to observe a null at the cancellation point with the same procedure as the over-the-air calibration. Note that this power combiner is preferred to have high isolation between the two input arms to minimize the interaction (e.g., injection locking or injection pulling) between the two ADPLLs.

Fig. 4(a) shows the phasor diagram of the cancellation method. If $\delta\theta$ and δA denote the phase-alignment error (°) from the 180° mark and the amplitude mismatch (dB), respectively, the cancellation level (CL) can be computed by

$$A_{\max} = (1+x)A \tag{5}$$

$$A_{\min} = A\sqrt{(1-x\cos\delta\theta)^2 + x^2\sin^2\delta\theta} \tag{6}$$

$$\begin{aligned}\mathrm{CL(dB)} &= 20\log_{10}\left(\frac{A_{\max}}{A_{\min}}\right) \\ &= 20\log_{10}\left(\frac{1+x}{\sqrt{1+x^2-2x\cos\delta\theta}}\right)\end{aligned} \tag{7}$$

where $x = 10^{-(\delta A/20)}$ is the linear amplitude misalignment. Clearly, when this variable is decreasing from unity (ideal amplitude-balance) to zero, the logarithm argument in (7) is dropping uniformly from $(1/\sin(\delta\theta/2))$ to 1 implying the degradation of the CL in the presence of amplitude imbalance, as expected. The graphs of the cancellation amount versus the phase-alignment accuracy are shown in Fig. 4(b) for $\delta A = 0, 1, 3, 6$ dB ($x = 1, 0.89, 0.71, 0.5$). For instance,

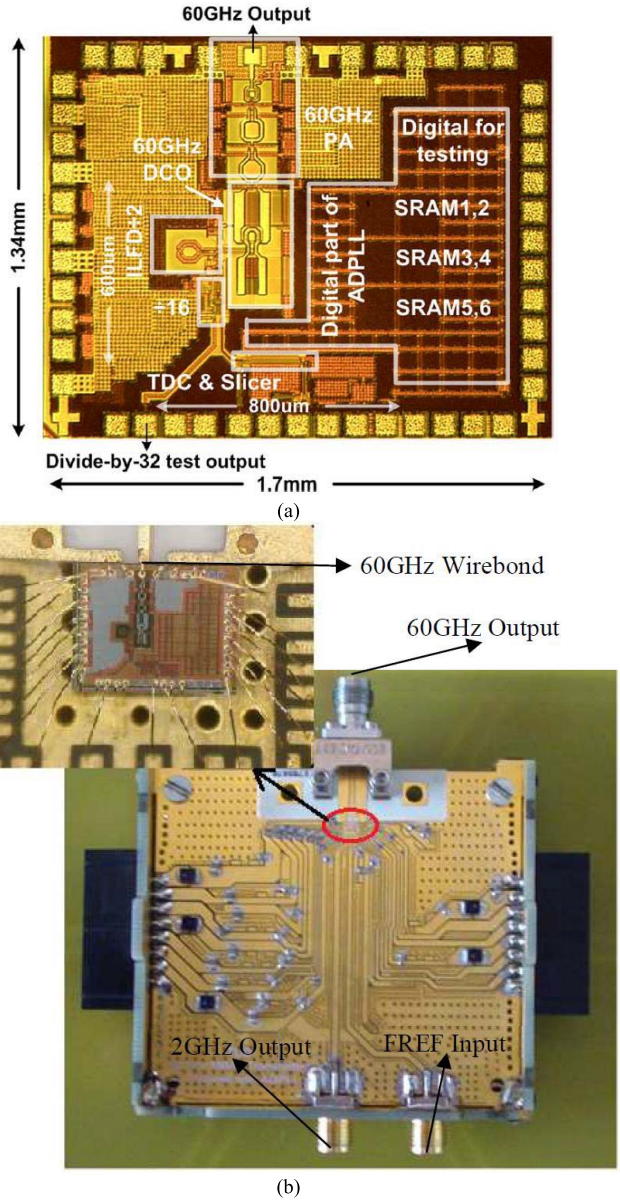

Fig. 5. (a) Die micrograph of the 60-GHz CMOS ADPLL chip from [49]. (b) Fabricated ADPLL board with the IC directly wire bonded, from [34].

35-dB power cancellation in the ideal case ($\delta A = 0$ dB) corresponds to about 2° phase-alignment accuracy. It is noticeable that the better the phase-alignment accuracy, the larger the delta of CL (for different values of the amplitude mismatch), which implies that a highly accurate phase-alignment calibration is so vulnerable to amplitude deviation and must be taken into account seriously.

B. Fabrication and Measurement of Single Chain

To aim, for a demonstration system, for the intended MIMO TX and to facilitate the fabrication/assembly process, each ADPLL chip is assembled on a separate printed circuit board (PCB) as the single chain of the 60-GHz MIMO BSU. The die micrograph of the utilized CMOS ADPLL IC and the fabricated board of the single chain are shown in Fig. 5. The RF bond pads consist of a ground-signal-ground (GSG)

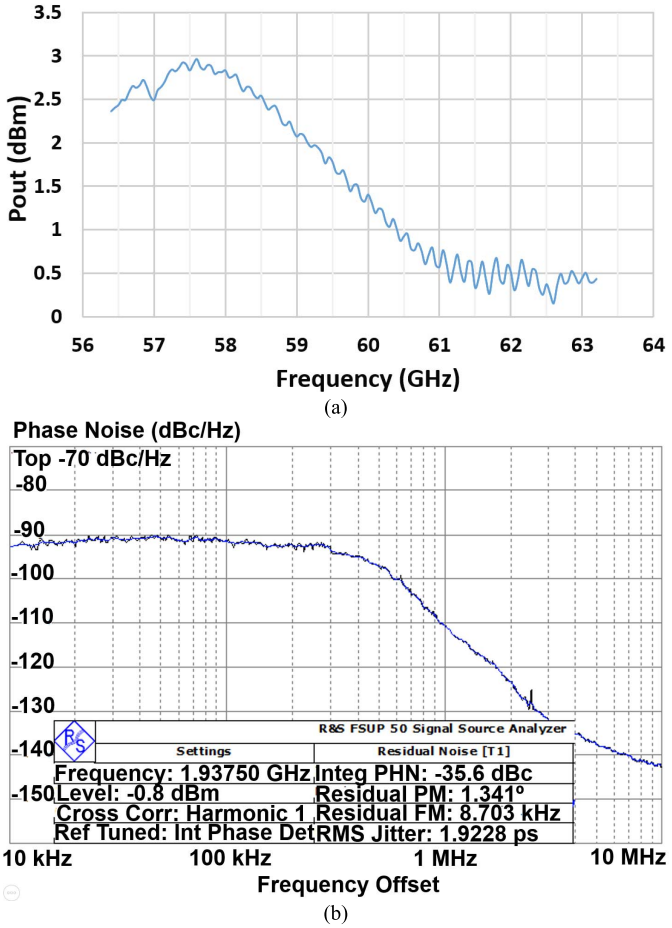

Fig. 6. Measurement results of the single ADPLL chain. (a) 60-GHz output power. (b) Phase noise profile at the 2-GHz output for $f = 62$ GHz.

60-GHz output, a test 2-GHz output (CKV/32), and a reference input from an external oven-controlled crystal oscillator (OCXO). As shown in Fig. 5(b), the ADPLL IC chip is wire bonded on the FR4 fabricated board and interconnected to the output V-connector via a matching network manufactured on the high-frequency laminate RO4350B (whiteboard). This matching circuit is characterized by measuring the output power of the board together with the large-signal analysis of the ADPLL PA [51] and is expected to have a 1-dB maximum loss including the 60-GHz wire bonding, over the frequency band of interest. In addition, two SMA connectors are mounted to provide access to the 2-GHz output and the reference input (FREF). Fig. 6 shows the measured 60-GHz output power of one ADPLL element across the locking band (56.4–63.4 GHz) and the phase noise profile at the 2-GHz output for $f = 62$ GHz (at $62/32 = 1.9375$ GHz). It should be noted that the phase noise characteristics at the 60-GHz output have the same behavior given but with only $20\log_{10}32 = 30.1$ dB higher level than the 2-GHz subharmonic as the 2-GHz output is merely a divide-by-32 version of the 60-GHz one. The output power is in the range of 0–3 dBm, which increases to 4–7 dBm after deembedding the V-band matching network, connector, and cable. This value agrees well with the expected output power of the ADPLL chip. The phase noise graph points out that the ADPLL is locked correctly.

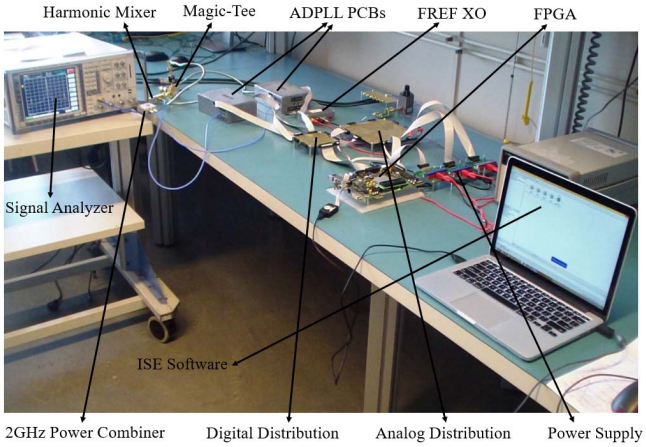

Fig. 7. Measurement setup to verify the phase-alignment calibration of the two ADPLL elements, from [34].

C. Measurement Results of Cancellation Method

The calibration approach is implemented by an experimental setup and the cancellation method is evaluated at the two outputs. To realize this implementation, the two ADPLL chains must be synchronized in time and locked at a single frequency [52]. Then, the output amplitude and phase are swept for one element, while the other one is fixed, to obtain the cancellation graph. The output amplitude of all ADPLL elements is constant, and thus, just the phase parameter is tuned. To accomplish the above-mentioned steps, an FPGA evaluation board from Xilinx ML50X Virtex-5 family is used to control all digital registers of the ADPLL chip either by writing the data into it or reading the data from it via the SPI port. The SPI_WRITE command sets different parameters to configure the chip, including main control, RF and analog subblocks, low-speed and high-speed digital, loop filter, DCO and TDC gains, locking steps, modulation (FMCW and FSK), frequency, and phase. The system status and internal results (estimated TDC and DCO gains) can be monitored through SPI_READ. The Verilog code of the ADPLL control/synchronization is designed and synthesized by Xilinx ISE design suite software to generate a bitstream (BIT) file for the FPGA programming. First, the two ADPLL chips are time-synchronized by a common serial clock (SPI clock) from the FPGA board to apply all digital commands synchronously as well as the same reference clock (CKR in Fig. 2) produced by a single crystal oscillator to be the counter of the digital part. After that, the same desired data are written into the registers of both ADPLLs to configure them identically, e.g., locking at a single frequency. Finally, the PHASE_OFFSET register for one of the chips is varied by a counter controlled via a couple of push buttons on the FPGA board, to sweep the phase difference. Since the phase resolution at the 60-GHz output is almost 2° (LSB bit change equals 2° in this particular implementation), a multiplication factor of about 16 is assigned for the 2-GHz output to enable 1° phase resolution at this output.

The photograph of the validation experiment setup is shown in Fig. 7. The two ADPLL PCBs are embedded in two separate metal boxes to alleviate any possible radiation coupling and

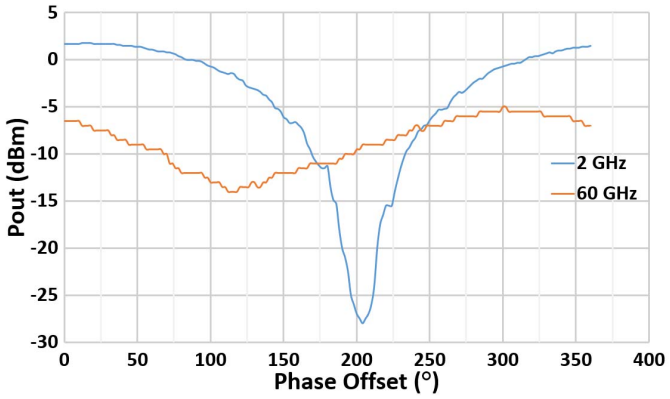

Fig. 8. Measured cancellation graphs at the two combined outputs for $f = 62$ GHz, from [34].

prevent from injection pulling or locking, particularly between the 60-GHz circuits. Both IC chips are locked by the 40-MHz OCXOV microcrystal with HC-MOS compatible output for better performance of the digital loop. Note that the digital circuitry of the current ADPLL chip functions properly up to $f_r = 50$ MHz. The bias voltages are supplied by supply regulating boards via an analog distribution board to distinguish the voltages between the two ADPLL PCBs. The regulated voltages reduce the power supply noise yielding lower phase noise. The FPGA board prepares the SPI digital commands for the ADPLLs through a digital distribution board. This FPGA is programmed by a master computer (PC) with ISE software. The cancellation method is established by adding up the main 60 GHz and the test 2-GHz outputs of the two ADPLL PCBs by means of a V-band magic tee (waveguide 180° hybrid to have more isolation between the two input ports) and a stripline power combiner, respectively. It should be mentioned that two extra waveguide isolators are located at the two inputs of the magic tee to boost the isolation and prohibit injection pulling. Both the outputs are monitored on a signal analyzer to read the output power. A V-band harmonic mixer is embedded for the 50-GHz signal analyzer to extend the frequency measurement range. When the FPGA synchronizes the two chips and locks them at an arbitrary frequency, the phase difference is swept, and the output power is measured to obtain the cancellation graph. This curve is drawn for the 60- and 2-GHz combined outputs in Fig. 8 at $f = 62$ GHz. Notice that the 2-GHz clocks are always amplitude-balanced, because the auxiliary 2-GHz output of the ADPLL chip (CKV/32 output in Fig. 2) is clipped at the VDD/GND supply rails. However, the 60-GHz outputs could be amplitude-mismatched due to the static–dynamic variations (discussed in Section III) and the impairments of the antenna system in case of the over-the-air calibration. This imbalance can be compensated up to at least ±1 dB by altering the bias voltage of the output 60-GHz PA slightly to change the gain and, hence, the 60-GHz output power of the chip. Indeed, the residual misalignment leads to more deviation in the 60-GHz cancellation curve and reduces the CL at this output, as shown in Fig. 4(b). The CLs are reported as 9 and 30 dB for the 60- and 2-GHz outputs, respectively. Fig. 4(b) points out that the amplitude mismatch does not influence the 60-GHz curve significantly because of low obtained CL at this output unless this imbalance is more than 6 dB [yellow graph in Fig. 4(b)], which is not the case for this validation (the residual amplitude mismatch between the two ADPLL PCBs could be 1∼2 dB worst case after compensation). This implies that the phase coherence of the two ADPLL ICs at 60 GHz is much less accurate than at 2 GHz [i.e., accuracy better than 3.5° and 35°∼40° for the 2- and 60-GHz outputs, respectively, in accordance with Fig. 4(b)]. As a matter of fact, it is very crucial to implement a more suitable amplitude-tuning (preferably, digital) mechanism with a wider adjustment range once the issue of poor phase-alignment precision is resolved at 60 GHz, as Fig. 4(b) shows the sensitivity of the cancellation method to amplitude deviation when the phase-balance error is small.

To explore the reason for this degradation, two experiments were carried out. First, the two ADPLL PCBs are replaced by two 60-GHz synthesized signal generators with the same V-band combining mechanism. The two generators are synchronized by connecting the reference output of one to the reference input of the other. Then, the phase difference between the two synthesizers is swept by enabling the simple phase modulation of one of the generators

$$S(t) = A\cos[2\pi f_0 t + \Delta\varphi\cos(2\pi f_m t)]. \tag{8}$$

If $\Delta\varphi = \pi$ with a very slow variation of phase (very small modulating frequency $f_m < 1$ Hz), the phase offset between the two instruments is swept slowly in full range. Having performed that, a CL better than 40 dB is observed, confirming the 60-GHz power combining validation procedure. In the next test, the 2-GHz outputs of the two boards are upconverted to 60 GHz by two V-band fundamental mixers and then combined by the same setup. The measured cancellation amount is 30 dB, just like in the original 2-GHz output, which also proves the 60-GHz calibration strategy. Since the output amplitudes of the ADPLLs are approximately the same and the only difference between the 2- and 60-GHz outputs is the division ratio 32 (the divided signal does not pass through the 60-GHz PA, which has a linear transmission phase response without any PM–to–PM conversion), the solely remaining factor is the phase noise degraded by $20\log_{10}32 = 30.1$ dB factor at the 60-GHz output with respect to the 2-GHz one. Fig. 6(b) shows the residual PM value of 1.3° at 2 GHz that will rise to $1.3° \times 32 = 41.6°$ at 60 GHz. Obviously, this phase deviation destroys the phase-alignment performance and accuracy severely. This establishes the clear need for an mm-wave ADPLL with a better phase noise performance.

IV. Analysis and Evaluation of ADPLL Phase Noise Effect on Phase-Alignment Calibration

As concluded by the experimental validation, the ADPLL phase noise is recognized as the main deviation factor of the phase-alignment accuracy at 60 GHz. Therefore, it is essential to find out the noise sources of an ADPLL and to assess the effect of the phase noise on the calibration procedure both analytically (mathematical formulations) and numerically (modeling and simulations). The objective behind is to come up with a solution for the ADPLL redesign in

terms of optimizing ADPLL key specifications to achieve the required phase-coherence performance (at least at the same performance level as at the 2-GHz output).

A. ADPLL Phase Noise Sources

The major sources of phase noise in an ADPLL-based TX are the phase noise of the reference crystal oscillator (L_{REF}) and the DCO (L_{DCO}) together with the quantization noise introduced by the TDC (L_{TDC}) as a function of the reference clock frequency (f_r) and the TDC time resolution (Δt_{TDC}) to extract the fractional portion of the loop phase error. Besides these factors, the digital loop filter configuration impacts the phase noise profile via alteration of the loop transfer function and is subjected to optimization once the above-mentioned effective parameters are settled down. All these effects have been addressed in detail [53]. To summarize the effect of these parameters mathematically, the relationship of the ADPLL phase noise and those factors can be formulated by the following expressions:

$$L_{\delta\varphi}(f_m) = |H_{\mathrm{cl,DCO}}(f_m)|^2 L_{\mathrm{DCO}}(f_m) + |H_{\mathrm{cl,REF}}(f_m)|^2 \left[L_{\mathrm{REF}}(f_m) + \frac{L_{\mathrm{TDC}}(f_m)}{N^2} \right] \quad (9)$$

$$L_{\mathrm{TDC}}(f_m) = \frac{\pi^2}{3} \left(\frac{f_0 \Delta t_{\mathrm{TDC}}}{M} \right)^2 \frac{1}{f_r} \quad (10)$$

which is derived through the low-frequency-domain analysis of the ADPLL loop. Basically, the ADPLL phase noise spectrum is the sum of the closed-loop responses [H_{cl} in (9)] to the DCO phase noise (L_{DCO}), the reference phase noise (L_{REF}), and the TDC quantization flat noise (L_{TDC}) spectra (in the linear and not in the dB scale). The closed-loop transfer functions depend on f_r, M ($M = 32$) and the digital loop filter specifications. These transfer functions behave as high-pass and low-pass filters for the DCO and the REF-TDC, respectively. The only difference between the REF and the TDC closed-loop responses is the factor $N = (f_0/Mf_r)$ as the ratio of the CKV/32 frequency to the reference one (channel FCW in Fig. 2). The TDC quantization noise has a flat response calculated by (10). Note that this noise is proportionally increasing with the square of the carrier frequency in the 60-GHz band (f_0) and the TDC time resolution (Δt_{TDC}) and decreasing with the reference frequency (f_r).

The current values of these variables for the measured ADPLL chip are

$$\begin{aligned} L_{\mathrm{REF}} &= e - 135 \text{ dBc/Hz} \\ L_{\mathrm{DCO}} &= -115 \text{ dBc/Hz@}\, f_m = 10 \text{ MHz} \\ f_r &= 40e \text{ MHz} \\ \Delta t_{\mathrm{TDC}} &= 12 \text{ ps}. \end{aligned} \quad (11)$$

Owing to the low-pass response of the loop to both the reference and TDC quantization noise and high-pass response to the DCO noise, the in-band phase noise is determined by the reference oscillator and the TDC specifications, whereas the out-of-band phase noise is established by the DCO phase noise. The values in (11) lead to the phase noise profile in Fig. 6(b). This curve can be regulated through varying the digital loop filter configuration, which results in a change of the loop bandwidth. For example, in Fig. 2, type-1 filter (only the multiplication factor α) dictates wider bandwidth than in type-2 (α along with the integration factor ρ), and adding some IIR stages procures extra reduction in the loop bandwidth profile that ends in the phase noise improvement. The basic disadvantage of the type-1 filter is the lack of zero phase-error forcing (the phase error is a function of the difference between the desired and free-running frequencies). However, the type-2 filter resolves this difficulty and supports a PLL that is suited to our intended application. The phase noise level of the presented 60-GHz ADPLL in the 65-nm CMOS process technology is compared to a typical commercial frequency synthesizer in a dedicated, non-CMOS technology as a reference criterion for the LO of a 60-GHz upconverter TX [54].

ADPLL [See Fig. 6(b)]:

$$\begin{aligned} L_{\delta\varphi}(10 \text{ kHz}) &= -90 + 20\log_{10}32 = -60 \text{ dBc/Hz} \\ L_{\delta\varphi}(1 \text{ MHz}) &= -110 + 20\log_{10}32 = -80 \text{ dBc/Hz}. \end{aligned}$$

Upconverter (20-GHz Synthesizer With 3× Frequency Multiplier):

$$\begin{aligned} L_{\delta\varphi}(10 \text{ kHz}) &= -110 + 20\log_{10}3 = -100 \text{ dBc/Hz} \\ L_{\delta\varphi}(1 \text{ MHz}) &= -140 + 20\log_{10}3 = -130 \text{ dBc/Hz}. \end{aligned} \quad (12)$$

As noticed, the phase noise performance of a typical instrumentation quality, but very bulky and costly, upconverter TX is much superior to the presented low-cost ADPLL system at 60 GHz. This fact points out the importance of the ADPLL phase noise investigation and the phase noise influence should be analyzed elaborately in the ADPLL MIMO TX either for calibration phase-alignment in beam-steering mode or for data rate augmentation with phase modulations (PM or N-PSK) in the MIMO mode.

B. Analytical Formulation of Phase Noise Effect

The output signal of an ADPLL can be described by

$$S(t) = [A + \delta A(t)] \cos[2\pi f_0 t + \varphi_0 + \delta\varphi(t)] \quad (13)$$

where $\delta A(t)$ and $\delta\varphi(t)$ stand for amplitude noise and phase noise random processes, respectively. The average power of the signal is ($|\delta A(t)| \ll A$)

$$P_{\mathrm{avg}} = E\left\{ \frac{1}{T_0} \int_{t_0}^{t_0+T_0} S^2(t) dt \right\} = \frac{1}{2} A^2 \quad (14)$$

where $E\{\cdot\}$ denotes the expected value of a random process. To model the calibration procedure, two signals of the form (13) are assumed

$$\begin{aligned} S_1(t) &= [A_1 + \delta A_1(t)] \cos[2\pi f_0 t + \varphi_{01} + \delta\varphi_1(t)] \\ S_2(t) &= [A_2 + \delta A_2(t)] \cos[2\pi f_0 t + \varphi_{02} + \delta\varphi_2(t)]. \end{aligned} \quad (15)$$

The two ADPLLs are locked at a single frequency f_0, but the output amplitude and initial phase are different associated with the static–dynamic issues (fabrication/assembly tolerances, process strength, and VT variations). Having stated that, the amplitude noise and phase noise of the two TXs

are uncorrelated and should be treated as independent random processes. In other words, although the two devices are fed by a single reference oscillator, both the in-band and out-of-band phase noise characteristics do not exhibit a strong correlation for the two ADPLLs due to the employment of independently distinct TDCs and DCOs, respectively. The sole correlation between the phase noise profiles of the two signals is the reference phase noise affecting the in-band region. Nonetheless, the dominant in-band cause is the TDC quantization noise, and thus, no enhancement in the correlated portion of phase noise is possible, e.g., by increasing the loop bandwidth so that the in-band characteristic would dominate the out-of-band part and govern the total phase noise profile. The same theoretical analysis has been discussed for the phase noise coherence of two signals with different frequencies at the output of a mixer (rather than a combiner which is our case) [55]. The average power of the combined signal is

$$P_{\text{avg}} = E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}[S_1(t)+S_2(t)]^2dt\right\} = E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}\left[S_1^2(t)+S_2^2(t)+2S_1(t)S_2(t)\right]dt\right\}. \quad (16)$$

Substituting (14) for the first two terms in the inner bracket will result in

$$P_{\text{avg}} = \frac{1}{2}\left(A_1^2+A_2^2\right) + E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}2S_1(t)S_2(t)dt\right\}. \quad (17)$$

The integral expression is simplified as follows:

$$\begin{aligned}&2S_1(t)S_2(t)\\ &=[A_1+\delta A_1(t)][A_2+\delta A_2(t)]\{\cos[\varphi_{01}-\varphi_{02}+\delta\varphi_1(t)-\delta\varphi_2(t)]\\ &\quad+\cos[4\pi f_0 t+\varphi_{01}+\varphi_{02}+\delta\varphi_1(t)+\delta\varphi_2(t)]\}. \end{aligned}\quad (18)$$

Ultimately, the average power of the combined output signal (displayed on the spectrum analyzer) is attained as

$$\begin{aligned}P_{\text{avg}} &= \frac{1}{2}\left(A_1^2+A_2^2\right)\\ &\quad+E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}[A_1+\delta A_1(t)][A_2+\delta A_2(t)]\right.\\ &\quad\left.\times\cos[\Delta\varphi_0+\delta\varphi_1(t)-\delta\varphi_2(t)]dt\right\}\end{aligned}\quad (19)$$

where $\Delta\varphi_0 = \varphi_{01} - \varphi_{02}$ is the phase offset value between the two ADPLLs. It should be mentioned that the last term in (18), $\cos(4\pi f_0 t)$, produces zero for the integral over one signal period. For simplicity and according to our case, the two ADPLL chains are supposed to be amplitude-balanced with negligible amplitude noise. The normalized power (divided by the peak value for which $\Delta\varphi_0 = 0$) would be

$$P_{\text{norm}} = \frac{P_{\text{avg}}}{2A^2} = \frac{1}{2}\left\{1+E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}\cos[\Delta\varphi_0+\delta\varphi_1(t)-\delta\varphi_2(t)]dt\right\}\right\} \quad (20)$$

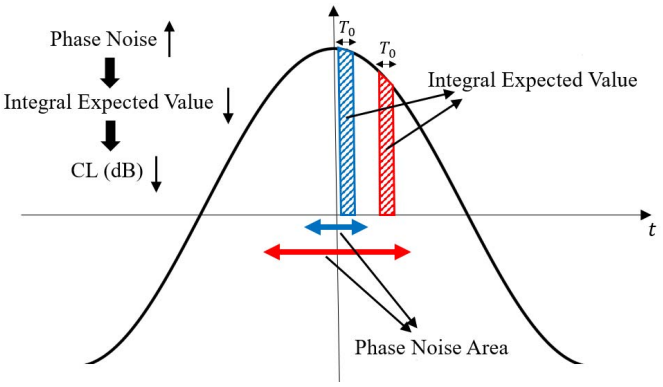

Fig. 9. Quantitative interpretation of (21) for the two scenarios, low phase noise (blue) and high phase noise (red), to compare their cancellation levels.

At the cancellation point, where $\Delta\varphi_0 = \pi$, the mean CL is computed

$$\begin{aligned}\text{CL} &= \frac{1}{2}\left\{1-E\left\{\frac{1}{T_0}\int_{t_0}^{t_0+T_0}\cos[\delta\varphi_1(t)-\delta\varphi_2(t)]dt\right\}\right\}\\ \text{CL(dB)} &= -10\log_{10}\text{CL}.\end{aligned}\quad (21)$$

Equation (21) establishes that the phase noise profile of the ADPLL directly contributes to the cancellation depth at the output. If the two ADPLL chains have fully correlated phase noise characteristics, the expected value of the integral argument is unity and the cancellation is ideal. Otherwise, the cancellation value is an analytically complicated function of the phase noise profile revealed by (21). As a rough and qualitative interpretation, when the phase noise level is rising, the amplitudes of the random processes $\delta\varphi_1(t)$ and $\delta\varphi_2(t)$ are elevated. The cosine function will always exhibit here a positive value, because the mean value of the phase noise is zero and, hence, the cosine value is around but less than unity. This implies that more noise (i.e., variability) will result in a reduction in the cosine function value under integral and, as a result, the positive expected value of the integral will decrease. As a consequence, the CL (dB) will drop as absolutely agreed in Fig. 8 (60-GHz graph compared with 2-GHz one). Fig. 9 (the cosine function versus integration time) shows the two scenarios, i.e., the low phase noise and high phase noise and interprets the integral term in (21) quantitatively to compare the CLs for these two cases. As clarified, higher phase noise level introduces smaller value for the expected integral and, subsequently, lower CL in the dB range. Because further analytical investigation of (21) is rather sophisticated, the exploration of the phase noise impact is performed in Section IV-C via the numerical simulations.

C. Numerical Simulations of Phase Noise Effect

To analyze the phase noise contribution on the phase-alignment calibration in more detail and to obtain the required specifications of each ADPLL chain for a highly accurate beam-steering MIMO TX, a numerical simulation of the cancellation method is conducted using the ADPLL time-domain model in the MATLAB software. The main inputs of this model consist of the carrier and reference frequencies (f_0 and f_r), the phase noise level of the reference and the DCO (L_{REF} and L_{DCO} at f_m = 10 MHz), the digital loop

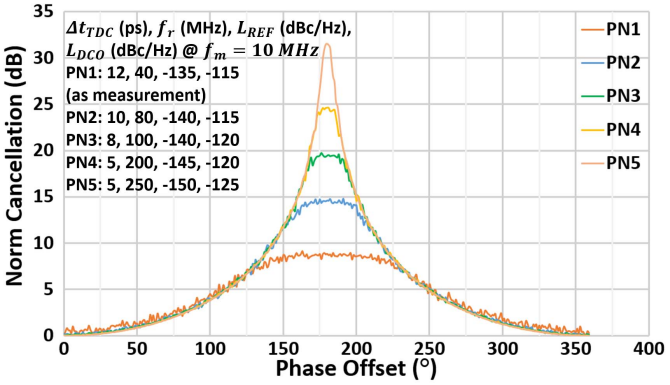

Fig. 10. Simulated normalized cancellation graphs at the ~60-GHz output ($f = 62$ GHz) for various ADPLL settings (computed by the ADPLL time-domain model in MATLAB), from [34].

filter parameters (α, ρ, and λ vector of IIR stages), the TDC time resolution (Δt_{TDC}), the phase offset of the loop, and the modulation mode if required (either FSK or QPSK). The time-domain operations of the digital loop are applied on these parameters to output the carrier signal and its phase noise profile at 60 and 2 GHz. The model is repeated twice with the same inputs other than the phase offset to generate two ADPLL signals with the relative phase difference. Then, this phase difference is swept 0°–360° and the average power of the two-signal sum is computed in the frequency domain [fast Fourier transform (FFT) method by (14)] for each phase offset. To gain a precise mean value, the calculated power is averaged a number of times (e.g., 20) similar to the operation of a spectrum analyzer. Complying with the noise sources of ADPLL, the effective parameters of the two identical ADPLL elements are altered and the normalized cancellation [$P_{\mathrm{norm}}(\mathrm{dB}) = -10\log_{10} P_{\mathrm{norm}}$ in (20)] graphs are plotted at $f = 62$ GHz (the same frequency as measurement) in Fig. 10 for various settings of the ADPLL. Fig. 10 affirms that the following configuration for the ADPLL chains will offer at least 32-dB CL at $f = 62$ GHz to satisfy the phase-alignment and beam-steering accuracy better than 3° [see Fig. 4(b)] and 2° [see (3) and (4)], respectively:

$$\begin{aligned} L_{\mathrm{REF}} &= -150 \text{ dBc/Hz} \\ L_{\mathrm{DCO}} &= -125 \text{ dBc/Hz@}\, f_m = 10 \text{ MHz} \\ f_r &= 250 \text{ MHz} \\ \Delta t_{\mathrm{TDC}} &= 5 \text{ ps}. \end{aligned} \tag{22}$$

The behavior of the CL versus the integrated phase error (created by phase noise) of the ADPLL at $f = 62$ GHz is shown in Fig. 11(b). Fig. 4(b), for the ideal case ($\delta A = 0$ dB), is also replotted on top of that for better comparison as in Fig. 11(a). It is quite clear that the cancellation will not be effective for the ADPLL phase error levels approaching 40°. Fig. 11(b) is well in agreement with Fig. 11(a) to relate a specific beam-steering and phase-alignment accuracy to the level of the ADPLL integrated phase noise. In principle, these two figures can assist to optimize the ADPLL design and succeed in the required beam-steering accuracy for the MIMO TX. Nevertheless, a discrepancy is observed between these two figures in terms of x-axis comparison. For the same CL, the integrated phase noise [see Fig. 11(b)] is smaller

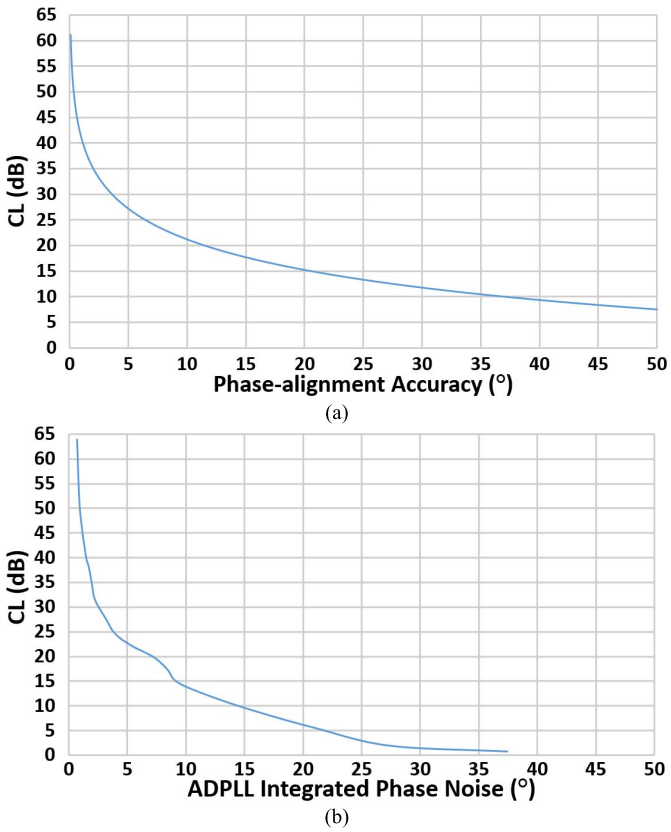

Fig. 11. Simulated cancellation level versus (a) phase-alignment accuracy from Fig. 4(b) for $\delta A = 0$ dB and (b) ADPLL integrated phase noise at $f = 62$ GHz.

than the phase mismatch [see Fig. 11(a)]. As an example, CL = 10 dB is equivalent to 15° integrated phase noise and 35° phase mismatch. This inconsistency arises from different translations of CL versus these two parameters (i.e., stochastic and deterministic). This difference can easily be interpreted in the quantitative form via (20), from which both (7) and (21) would be derived. Fig. 11(a) corresponds to (7) in a deterministic case without phase noise [$\delta\varphi_1(t) = \delta\varphi_2(t) = 0$] and only with phase-alignment error ($\delta\theta = 180° - \Delta\varphi_0$), whereas Fig. 11(b) is acquired by (21) in a stochastic scenario with phase noise and $\Delta\varphi_0 = 180°$ ($\delta\theta = 0$). Therefore, the integrated phase noise introduces an rms parameter for which the peak value could reach three times more while the phase mismatch is constant. As a rule of thumb, this implies that the integrated phase noise is expected to be less than the phase mismatch by a factor of 2~3 for the same CL as observed by the above-mentioned example. When the CL is decreasing, the phase mismatch is increasing, and therefore, the delta between the phase mismatch and the integrated phase noise gets more significant. Actually, the lower the CL, the larger the difference. As a subsequence, for low CL, this difference is considerable, whereas for high CL, the difference is negligible.

In summary, the future activities to fulfill an mm-wave highly accurate beam-steering MIMO TX are listed as follows [as mentioned by (22)].

1) Design a TDC with time resolution better than 5 ps.

2) Design a 60-GHz DCO with $L_{\mathrm{DCO}} = -125$ dBc/Hz at $f_m = 10$ MHz.
3) Redesign the digital part of the loop to be working with f_r up to 250 MHz.
4) Feed the 60-GHz loop by an OCXO with $f_r = 250$ MHz and $L_{\mathrm{REF}} = -150$ dBc/Hz.
5) Reoptimize the digital loop filter configuration with the new 60-GHz loop (new TDC, DCO, digital part, and OCXO).
6) Implement a proper mechanism for digitally adjusting the output power of the ADPLL to meet a highly accurate amplitude balance during the system calibration (step 9).
7) Redesign the modulation part to support the required modulation schemes for mm-wave applications such as 5G (QPSK, QAM, and so on).
8) Fabricate the new redesigned ADPLLs, integrated with the antenna system to build the new 60-GHz MIMO TX in the spirit of the proposed architecture of Fig. 1 (RF-SoC or SiP).
9) Perform the overall system calibration, fundamentally, by a two-step mechanism. The first is the major over-the-air synchronization performed only once (at the system creation in the factory or in the field) to account for all static mismatch sources (fabrication-assembly imperfections such as wire bond interconnection-packaging mismatch, PCB tolerances, and imbalance of the antenna array elements as well as process strength of CMOS for the ADPLLs) and calibrate the whole TX as described in Section III-A. It is noteworthy that the interconnection of the ADPLLs and the antenna array should not cause any dynamic variability compliant with the proposed architecture of Fig. 1 (RF-SoC or SiP) since, for both topologies, the interconnects' length is very short up to a fraction of millimeter and will not impose any dynamic variations. The dynamic deviations (mainly VT variations of the CMOS process) should be naturally compensated by the closed-loop ADPLL operations.
10) Apply the desired phase shifts to the different elements to offer the beam-steering capability for different use-cases, including CW and various modulation types exploited by mm-wave communication systems such as QPSK, QAM, and so on.

In order to support the main claim of this paper, which is to achieve the 60-GHz CMOS ADPLL with the required phase noise performance, it is worthy to mention that a 60-GHz digital frequency synthesizer with ultralow in-band phase noise characteristics has already been attained in the CMOS technology [56]. The proposed 60-GHz ADPLL provides a 1-dBm PA realized in 28-nm CMOS and occupies 0.4 mm^2.

V. Conclusion

In this paper, a novel mm-wave MIMO architecture comprising of the low-cost CMOS ADPLL chips has been introduced and a highly accurate calibration strategy has been proposed to provide a precise digital beam steering. The calibration procedure has been implemented by the fabricated ADPLL chains using a cancellation method to align the output phases of all TX elements for beam tilting goals. The experimental results have demonstrated that the phase-coherence accuracy at the main 60-GHz output is much worse than that at the test 2-GHz output arising from 30-dB higher phase noise level at 60 GHz. Hence, the phase noise effect on the cancellation method and phase-alignment accuracy has been assessed and analyzed by the exploitation of the ADPLL time-domain model. This analysis has been executed through the analytical formulation and numerical simulations that have verified the measurement outcomes. Finally, the required values of the ADPLL parameters have been derived through this analysis and the essential ADPLL specifications have been determined to allow a 60-GHz ADPLL MIMO TX with highly accurate digital beam-steering capabilities demanded for mm-wave communications and 5G emerging technology.

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References

[1] A. Maltsev *et al.*, "Partially adaptive arrays application for MU-MIMO mode in a mmWave small cells," in *Proc. IEEE PIMRC*, Hong Kong, Aug./Sep. 2015, pp. 315–319.
[2] A. Maltsev, I. Bolotin, A. Pudeyev, G. Morozov, and A. Davydov, "Performance evaluation of the isolated mmWave small cell," in *Proc. IEEE PIMRC*, Hong Kong, Aug./Sep. 2015, pp. 2354–2358.
[3] A. Maltsev *et al.*, "Performance evaluation of interference mitigation techniques in the overlaying mmWave small cell network," in *Proc. IEEE CSCN*, Tokyo, Japan, Oct. 2015, pp. 130–136.
[4] J. Lota, S. Sun, T. S. Rappaport, and A. Demosthenous, "5G uniform linear arrays with beamforming and spatial multiplexing at 28, 37, 64, and 71 GHz for outdoor urban communication: A two-level approach," *IEEE Trans. Veh. Technol.*, vol. 66, no. 11, pp. 9972–9985, Nov. 2017.
[5] O. Jo, J.-J. Kim, J. Yoon, D. Choi, and W. Hong, "Exploitation of dual-polarization diversity for 5G millimeter-wave MIMO beamforming systems," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6646–6655, Dec. 2017.
[6] C. Pfeffer, R. Feger, C. Wagner, and A. Stelzer, "FMCW MIMO radar system for frequency-division multiple TX-beamforming," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4262–4274, Dec. 2013.
[7] D. Bleh *et al.*, "W-band time-domain multiplexing FMCW MIMO radar for far-field 3-D imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3474–3484, Sep. 2017.
[8] H. J. Ng, M. Kucharski, W. Ahmad, and D. Kissinger, "Multi-purpose fully differential 61- and 122-GHz radar transceivers for scalable MIMO sensor platforms," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2242–2255, Sep. 2017.
[9] H. J. Ng and D. Kissinger, "Highly miniaturized 120-GHz SIMO and MIMO radar sensor with on-chip folded dipole antennas for range and angular measurements," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 6, pp. 2592–2603, Jun. 2018.
[10] A. Maltsev, A. Pudeyev, A. Lomayev, and I. Bolotin, "Channel modeling in the next generation mmWave Wi-Fi: IEEE 802.11ay standard," in *Proc. IEEE EuWC*, Oulu, Finland, May 2016, pp. 1–8.
[11] Y. Ghasempour, C. R. C. M. da Silva, C. Cordeiro, and E. W. Knightly, "IEEE 802.11ay: Next-generation 60 GHz communication for 100 Gb/s Wi-Fi," *IEEE Commun. Mag.*, vol. 55, no. 12, pp. 186–192, Dec. 2017.
[12] P. Zhou *et al.*, "IEEE 802.11ay-based mmWave WLANs: Design challenges and solutions," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 3, pp. 1654–1681, 3rd Quart., 2018.
[13] A. P. Toda, F. de Flaviis, and J. Castaneda, "60GHz waveguide array design for MIMO channel characterization," in *Proc. IEEE ICUWB*, Vancouver, BC, Canada, Sep. 2009, pp. 12–16.
[14] X. Li, B.-B. Xu, and H.-L. Peng, "A 60 GHz antenna array with heatsink considerations for massive-MIMO applications," in *Proc. IEEE EDAPS*, Honolulu, HI, USA, Dec. 2016, pp. 79–81.

[15] A. Dadgarpour, M. S. Sorkherizi, T. A. Denidni, and A. A. Kishk, "Passive beam switching and dual-beam radiation slot antenna loaded with ENZ medium and excited through ridge gap waveguide at millimeter-waves," *IEEE Trans. Antennas Propag.*, vol. 65, no. 1, pp. 92–102, Jan. 2017.

[16] M. Salarpour, F. Farzaneh, and R. B. Staszewski, "Design procedure of a U-slot patch antenna array for 60 GHz MIMO application," in *Proc. IEEE TCSET*, Slavske, Ukraine, Feb. 2018, pp. 612–615.

[17] M. Salarpour, F. Farzaneh, and R. B. Staszewski, "Design and calibration procedure of a proposed V-band antenna array on fused silica technology intended for MIMO applications," *Int. J. Microw. Opt. Technol.*, vol. 13, no. 4, pp. 317–329, Jul. 2018.

[18] J.-Y. Park, Y. Wang, and T. Itoh, "A 60 GHz integrated antenna array for high-speed digital beamforming applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Philadelphia, PA, USA, Jun. 2003, pp. 1677–1680.

[19] E. Pisek, S. Abu-Surra, J. Mott, T. Henige, and R. Sharma, "High throughput millimeter-wave MIMO beamforming system for short range communication," in *Proc. IEEE CCNC*, Las Vegas, NV, USA, Jan. 2014, pp. 537–543.

[20] G. Wang and G. Ascheid, "Hybrid beamforming under equal gain constraint for maximizing sum rate at 60 GHz," in *Proc. IEEE VTC Spring*, Glasgow, U.K., May 2015, pp. 1–5.

[21] G. Wang, P. Karanjekar, and G. Ascheid, "Beamforming with time-delay compensation for 60 GHz MIMO frequency-selective channels," in *Proc. IEEE PIMRC*, Hong Kong, Aug./Sep. 2015, pp. 387–391.

[22] S.-H. Wu, L.-K. Chiu, and J.-W. Wang, "Reconfigurable hybrid beamforming for dual-polarized mmWave MIMO channels: Stochastic channel modeling and architectural adaptation methods," *IEEE Trans. Commun.*, vol. 66, no. 2, pp. 741–755, Feb. 2018.

[23] S. Ranvier, C. Icheln, and P. Vainikainen, "Measurement-based mutual information analysis of MIMO antenna selection in the 60-GHz band," *IEEE Antennas Wireless Propag. Lett.*, vol. 8, pp. 686–689, 2009.

[24] L. Zhou and Y. Ohashi, "Efficient codebook-based MIMO beamforming for millimeter-wave WLANs," in *Proc. IEEE PIMRC*, Sydney, NSW, Australia, Sep. 2012, pp. 1885–1889.

[25] K. J. Kim, S. J. Bae, and K. S. Kwak, "A new beamforming for 60GHz wireless system with reduced feedback overhead," in *Proc. IEEE ISCIT*, Icheon, South Korea, Sep. 2009, pp. 1517–1521.

[26] S. Tiraspolsky, B. Jeon, J. Kim, A. Rubtsov, A. Flaksman, and V. Ermolayev, "mmWave SVD-based beamformed MIMO communication systems," in *Proc. IEEE CCNC*, Las Vegas, NV, USA, Jan. 2010, pp. 1–5.

[27] J. Nsenga, W. Van Thillo, F. Horlin, V. Ramon, A. Bourdoux, and R. Lauwereins, "Joint transmit and receive analog beamforming in 60 GHz MIMO multipath channels," in *Proc. IEEE ICC*, Dresden, Germany, Jun. 2009, pp. 1–5.

[28] P. Shanmugam, H.-G. Yeh, J. Lee, and D. Chang, "Transmitter beamforming techniques for indoor millimeter wave communication," in *Proc. IEEE SYSCON*, Montreal, QC, Canada, Apr. 2017, pp. 1–5.

[29] M. Kyro, S. Ranvier, C. Icheln, and P. VainiKainen, "Measurement based mutual information analysis of beam steering in the 60 GHz band," in *Proc. IEEE EuCAP*, Berlin, Germany, Mar. 2009, pp. 332–335.

[30] J. Ahmadi-Shokouh, R. Rafi, A. Taeb, and S. Safavi-Naeini, "Empirical MIMO beamforming and channel measurements at 57–64 GHz frequencies," *Trans. Emerg. Telecommun. Technol.*, vol. 26, no. 6, pp. 1003–1009, Jun. 2015.

[31] A. Hussein, S. Vasadi, M. Soliman, and J. Paramesh, "A 50-to-66GHz 65nm CMOS all-digital fractional-N PLL with 220fs$_{rms}$ Jitter," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 326–327.

[32] F.-W. Kuo *et al.*, "An all-digital PLL for cellular mobile phones in 28-nm CMOS with −55 dBc fractional and −91 dBc reference spurs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 3756–3768, Nov. 2018.

[33] C.-C. Li, M.-S. Yuan, C.-C. Liao, Y.-T. Lin, C.-H. Chang, and R. B. Staszewski, "All-digital PLL for Bluetooth low energy using 32.768-kHz reference clock and =0.45-V supply," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3660–3671, Dec. 2018. doi: 10.1109/JSSC.2018.2871632.

[34] M. Salarpour, R. B. Staszewski, and F. Farzaneh, "A mm-wave MIMO transmitter with a digital beam steering capability using CMOS all-digital phase-locked loop chips," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dublin, Ireland, Aug. 2018, pp. 1–3.

[35] B. Wang, H. Gao, M. K. Matters-Kammerer, and P. G. M. Baltus, "A 60 GHz 360° phase shifter with 2.7° phase resolution and 1.4° RMS phase error in a 40-nm CMOS technology," in *Proc. IEEE RFIC*, Philadelphia, PA, USA, Jun. 2018, pp. 144–147.

[36] W. Lee *et al.*, "Fully integrated 94-GHz dual-polarized TX and RX phased array chipset in SiGe BiCMOS operating up to 105 °C," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2512–2531, Sep. 2018.

[37] S. Ranvier, J. Kivinen, and P. Vainikainen, "Millimeter-wave MIMO radio channel sounder," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 1018–1024, Jun. 2007.

[38] C. Sheldon, E. Torkildson, M. Seo, C. P. Yue, M. Rodwell, and U. Madhow, "Spatial multiplexing over a line-of-sight millimeter-wave MIMO link: A two-channel hardware demonstration at 1.2Gbps over 41m range," in *Proc. IEEE EuWiT*, Amsterdam, The Netherlands, Oct. 2008, pp. 198–201.

[39] C. Sheldon, M. Seo, E. Torkildson, M. Rodwell, and U. Madhow, "Four-channel spatial multiplexing over a millimeter-wave line-of-sight link," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, Jun. 2009, pp. 389–392.

[40] W. Keusgen *et al.*, "An NLOS-capable 60 GHz MIMO demonstrator: System concept & performance," in *Proc. IEEE NEWCAS*, Bordeaux, France, Jun. 2011, pp. 265–268.

[41] S. Salous, S. M. Feeney, X. Raimundo, and A. A. Cheema, "Wideband MIMO channel sounder for radio measurements in the 60 GHz band," *IEEE Trans. Wireless Commun.*, vol. 15, no. 4, pp. 2825–2832, Apr. 2016.

[42] M. Houdebine *et al.*, "An 85-GHz fully integrated all digital fractional frequency synthesizer for e-band backhaul and radar applications in 55-nm BiCMOS," in *Proc. IEEE ESSCIRC*, Lausanne, Switzerland, Sep. 2016, pp. 381–384.

[43] D. Hall, A. Hinde, and Y. Jia, "Multi-channel phase-coherent RF measurement system architectures and performance considerations," in *Proc. IEEE MILCOM*, Baltimore, MD, USA, Oct. 2014, pp. 1318–1323.

[44] W. Li, J. Lin, W. Wang, Y. Wang, and Z. Chen, "Method of multi-channel calibration for digital array radar," in *Proc. IEEE EuRAD*, Paris, France, Sep. 2015, pp. 533–536.

[45] A. Visweswaran, C. de Martino, E. Sirignano, and M. Spirito, "An IQ-steering technique for amplitude and phase control of mm-wave signals," in *Proc. IEEE ARFTG Microw. Meas. Conf.*, Atlanta, GA, USA, Dec. 2015, pp. 1–4.

[46] S. Chaudhary and A. Samant, "Characterization and calibration techniques for multi-channel phase-coherent systems," *IEEE Instrum. Meas. Mag.*, vol. 19, no. 4, pp. 44–50, Aug. 2016.

[47] A. Kiayani *et al.*, "Adaptive nonlinear RF cancellation for improved isolation in simultaneous transmit–receive systems," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 5, pp. 2299–2312, May 2018.

[48] T. Zhang, C. Su, A. Najafi, and J. C. Rudell, "Wideband dual-injection path self-interference cancellation architecture for full-duplex transceivers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1563–1576, Jun. 2018.

[49] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May 2014.

[50] R. J. Mailloux, *Phased Array Antenna Handbook*, 2nd ed. Norwood, MA, USA: Artech House, 2005, pp. 63–108.

[51] M. Salarpour, F. Farzaneh, and R. B. Staszewski, "A low cost-low loss broadband integration of a CMOS transmitter and its antenna for mm-wave FMCW radar applications," *Int. J. Electron. Commun.*, vol. 95, pp. 313–325, Oct. 2018.

[52] D. J. Jörg *et al.*, "Synchronization of mutually coupled digital PLLs in massive MIMO systems," in *Proc. IEEE ICC*, London, U.K., Jun. 2015, pp. 1716–1721.

[53] W. Wu, "Millimeter-wave digitally-assisted frequency synthesizer in CMOS," Ph.D. dissertation, Dept. Elect. Eng. Math. Comput. Sci., Dept. Microelectron., Delft Univ. Technol., Delft, The Netherlands, 2013.

[54] Datasheet. *Agilent E8257D PSG Microwave Analog SignalGenerator*. Accessed: Dec. 1, 2017. [Online]. Available: https://literature.cdn.keysight.com/litweb/pdf/ 5989-0698EN.pdf

[55] D. Rönnow, S. Amin, M. Alizadeh, and E. Zenteno, "Phase noise coherence of two continuous wave radio frequency signals of different frequency," *IET Sci. Meas. Technol.*, vol. 11, no. 1, pp. 77–85, Jan. 2017.

[56] Z. Zong, P. Chen, and R. B. Staszewski, "A low-noise fractional-N digital frequency synthesizer with implicit frequency tripling for mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 755–767, Mar. 2019.

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