Lumped-Element Wilkinson Power Combiners Using Reactively Compensated Star/Delta Coupled Coils in 28-nm Bulk CMOS

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Abstract— This paper presents four compact lumped-element Wilkinson power combiners (WPC) operating at 5 GHz in 28-nm bulk CMOS. To minimize the chip area, the inductances in the designs are implemented using mutually coupled coils. Two designs use star inverting coupled coils (SICC), while the other two employ delta noninverting coupled coils (DNICC). One of the two SICC-based designs (and similarly for the DNICC-based designs) incorporates a second harmonic $(2f_0)$ trap to lower the total harmonic distortion and reduce the required inductances by 25%, further reducing the circuits footprint. A design methodology for effectively exploiting the mutual coupling and nullifying the coupling parasitics is presented. The coupling parasitic in the DNICC-based design is exploited to provide the WPC isolation resistance, resulting in a lumped-element WPC requiring only three components: a coupled coil and two capacitors. The measurement and simulation results are presented to confirm the theory validity. The SICC-based WPC with an area of 0.13 mm^2 achieved input return losses (RL) >17.5 dB, output RL > 11.8 dB, isolation >11.2 dB, and insertion losses (IL) <1.5 dB across 3.5–5.4-GHz frequency range. Its variant with a $2f_0$ trap achieved, from 3.5–5.35 GHz, input RL >18.2 dB, output RL >11.6 dB, isolation >11 dB, IL <1.4 dB, and peak $2f_0$ rejection of 18 dB at 10.2 GHz in an area of 0.13 mm^2.The DNICC-based WPC with an area of 0.11 mm^2 achieved input RL and isolation >10 dB, output RL >15.3 dB, and IL <1.2 dB across 4.1–5.45-GHz frequency range. Its variant with a $2f_0$ trap achieved, from 4.3–5.3 GHz, input RL and isolation >10.1 dB, output RL >14.6, IL <1.2 dB, and peak $2f_0$ rejection of 23 dB at 10.4 GHz in an area of 0.09 mm^2.

Index Terms— CMOS, coupled coil, impedance matching, lumped element, mutual coupling, power combiners, reactive compensation, Wilkinson.

I. INTRODUCTION

THE demand for low-cost system-on-chips (SOC), which integrate digital, analog, and radio frequency (RF) circuitry on the same die, can only be met by CMOS processes
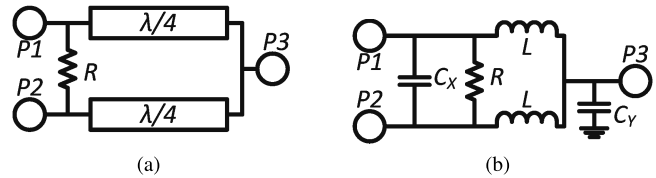
Fig. 1. Ideal WPCs. (a) Distributed. (b) Lumped-element.

due to their extremely small feature size [1]. Smaller feature sizes are being aggressively pursued to meet the demand for faster circuitry and higher levels of integration, but this presents increasing challenges for RF designers. One major challenge in designing the RF transmitter of a CMOS SOC is that the output power of the power amplifier (PA) is constrained by the low transistor oxide breakdown voltages, which limits the usable supply voltages [2], [3]. To prevent oxide damage and achieve the desired output power, multiple PA unit cells can be used together with power combiners such as the Wilkinson power combiner (WPC) [4], quarter-wave transmission lines (QWTL) [5], and transformer-based power-combining structures [6], [7].

The WPC, shown in distributed and lumped-element forms in Fig. 1, is popular due to its simple circuit topology and high performance, e.g., low insertion loss (IL), excellent return losses (RL), and high input isolation [4]. WPCs allow PAs to operate in isolation and ensure that they do not interfere with each other. In the classical distributed WPC, the QWTL match the input ports to the output port and the isolation resistor dissipates antiphase input power. Although QWTLs are too large for use in CMOS integrated circuits (IC) at low microwave frequencies, they can be replaced with lumped-element *LC* networks as in [8]–[17], as lumped components require much less circuit area than QWTLs.

On a CMOS process, inductors are typically implemented using large, lossy spiral coils, and thus, their size is minimized wherever possible. The high inductor losses on CMOS are due to the thin metal layers and eddy currents caused by the coil electromagnetically (EM) coupling with the conductive silicon substrate [18]. The inductance density can be increased through the appropriate use of mutual coupling between two or more coils. Mutual coupling has been used in [12]
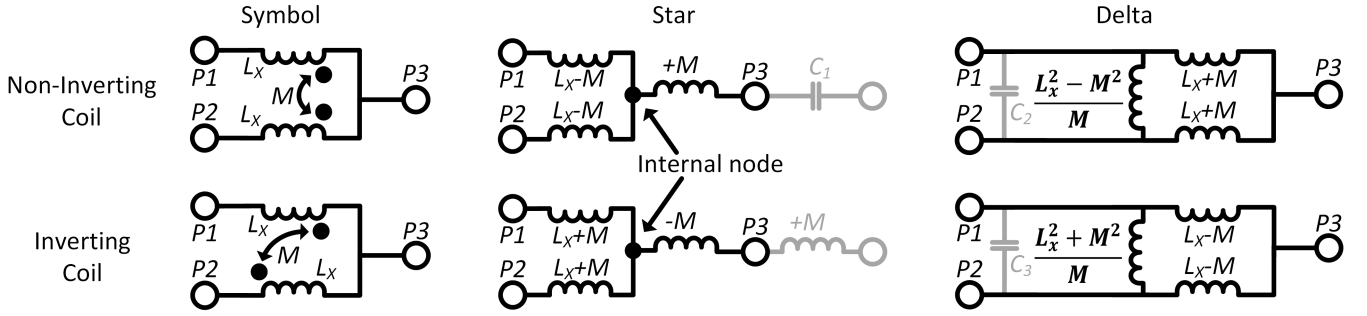
Fig. 2. Equivalent circuit models of inverting and noninverting coupled coils in star and delta configurations (external compensation elements in gray).

and [14]–[17] to create compact lumped-element WPCs, but the reported methodology for correctly using the technique has been insufficient. One critical deficiency in the literature is that the parasitic coupling reactances, which degrade the matching and isolation significantly and hence must be compensated, have not been given sufficient attention. Park and Wang [15] acknowledge the parasitics but state that they were absorbed into the design without giving a thorough explanation of their operation. The WPC design in [17] utilizes four bridged-T coupled coils with each representing a QWTL. Since the bridged-T coil has similar electrical characteristics to QWTLs, the resulting circuit bandwidth is similar to that of the conventional WPC.

This paper will provide a thorough and concise methodology for correctly utilizing mutual coupling in order to design compact lumped-element WPCs based on the circuit topology shown in Fig. 1(b). Furthermore, the analysis of mutual coupling will show that the parasitics of coupled coils can be exploited to provide the shunt isolation resistance resulting in a lumped-element WPC requiring only three components: a coupled coil and two capacitors. Two circuits have been designed that use inverting and noninverting coupling, each with a variant containing a second harmonic trap to lower the total harmonic distortion (THD) and the required inductance value in the circuit. The four WPCs were designed at 5 GHz and have been fabricated on TSMC's 28-nm bulk CMOS process.

The key design challenge is to achieve reasonable levels of RL at both input and output ports, IL, isolation, amplitude/phase balance, and operating bandwidth while keeping the overall circuit footprint minimal. The designs in this paper target 5-GHz WLAN (IEEE 802.11ac/n) applications with the ultimate goal being to integrate the power combiners with high-efficiency switched-mode PAs wherein isolation of at least 10 dB is needed to prevent one PA from loading the other.

The remainder of this paper is organized as follows. Section II introduces the star- and delta-equivalent circuit models of the inverting and noninverting coupled coils including reactance compensation techniques, Section III presents the working principles of four WPC variants designed using coupled coils, Section IV covers the implementation of the four circuits on 28-nm bulk CMOS, Section V discusses the circuit measurement results against simulation predictions, and finally, Section VI concludes the paper.

II. STAR-/DELTA-EQUIVALENT CIRCUITS OF COUPLED COILS

The two inductances shown in Fig. 1(b) can be implemented with a single three-port coupled coil comprised of two windings with one side of each connected to a common node. Mutual coupling occurs when the magnetic fields of the two windings interact, which alters the windings net inductances and, thus, can be used to design inductors with higher inductances than the winding self-inductance alone. The windings net inductances are determined by the coupling type and the coupled coil circuit model. The coupling type can be inverting or noninverting and these are respectively caused by antiparallel and parallel current flow in the windings. Coupled coils are commonly represented with dot notation as shown in Fig. 2, where L_x is the self-inductance of each winding, $M = L_x k$ is the mutual inductance between the windings, and k is the coupling factor, ranging from 0 to 1 which represent no coupling and maximum coupling, respectively. The coupled coil can be modeled as a star or delta network. The star and delta models are derived using the transmission (ABCD) parameters of the inverting/noninverting coupled coils. Alternatively, once one model has been derived, the other can be obtained using a star–delta or delta–star transformation. In the literature, the star model is the most commonly used coupling model, but it will be shown that the delta model can enable the design of an even more compact WPC. Fig. 2 shows that the star inverting coupled coil (SICC) and the delta noninverting coupled coil (DNICC) have larger net inductances than the star noninverting coupled coil (SNICC) and the delta inverting coupled coil (DICC), i.e., $L_x + M$ versus $L_x - M$, and, therefore, are favorable for a compact WPC design.

In addition to changing the windings net inductances to $L_x \pm M$, mutual coupling results in the creation of parasitic reactances, i.e., $\mp M$ in the star configuration and $(L_x^2 \mp M^2)/M$ in the delta configuration, which must be removed as they degrade the WPC performance in terms of impedance matching and isolation. The parasitic reactances and their compensation components are shown in Fig. 2. In the SICC, the negative inductance $-M$ can be canceled with an equally sized inductor M. The other three models have positive inductive parasitics which can be resonated out with a capacitor at the fundamental frequency f_0, with the capacitor
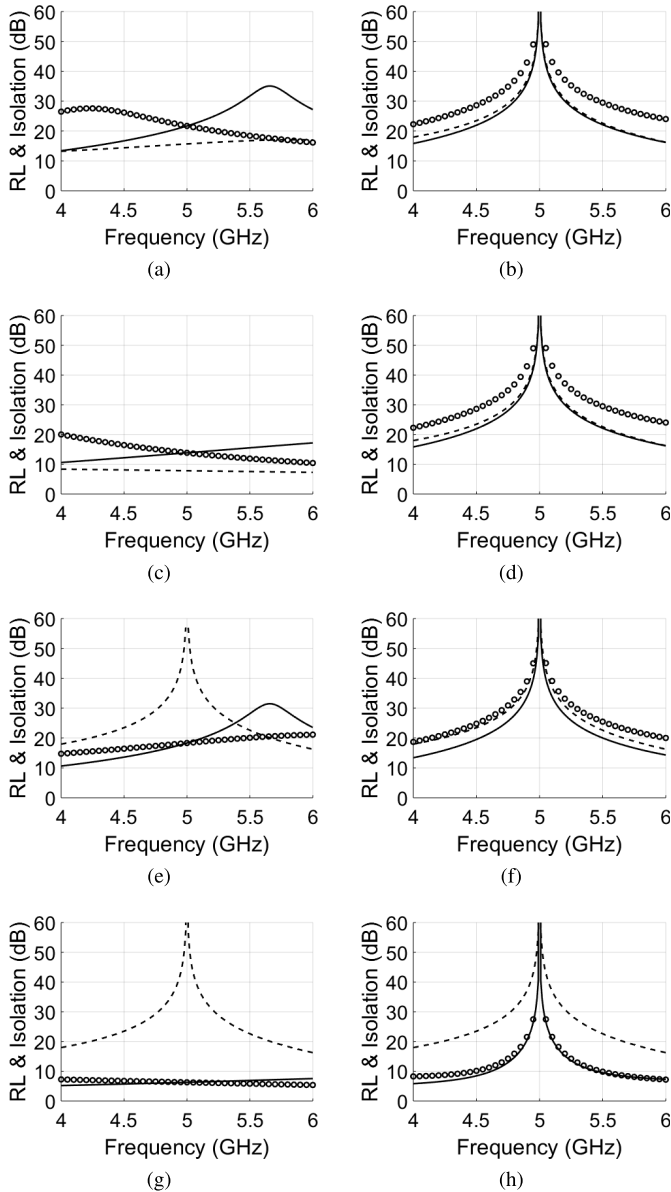
Fig. 3. Effects of the SICC's and DNICC's parasitics on the WPC performance. Circles: input RL. Dashed lines: output RL. Solid lines: isolation. (a) SICC with $k = 0.2$. (b) Compensated SICC with $k = 0.2$. (c) SICC with $k = 0.8$. (d) Compensated SICC with $k = 0.8$. (e) DNICC with $k = 0.2$. (f) Compensated DNICC with $k = 0.2$. (g) DNICC with $k = 0.8$. (h) Compensated DNICC with $k = 0.8$.

values given in the following equation:

$$(C_1, C_2, C_3) = \left(\frac{1}{\omega_0^2 M}, \frac{1}{\omega_0^2 \frac{L_x^2 - M^2}{M}}, \frac{1}{\omega_0^2 \frac{L_x^2 + M^2}{M}} \right). \quad (1)$$

The detrimental effects of the SICC's and DNICC's parasitics on the performance of the lumped-element WPC shown in Fig. 1(b) are demonstrated in Fig. 3 for two different coupling factor values with circuit values given in Table I and derivations given later in Section III. When $k = 0$, there would be no coupling and, thus, no parasitics, and compensation would not be needed. As the coupling factor increases, the RL and isolation of the SICC-based circuit are increasingly degraded [Fig. 3(a) and (c)], and similarly,

TABLE I
CIRCUIT COMPONENT VALUES USED TO PLOT 3

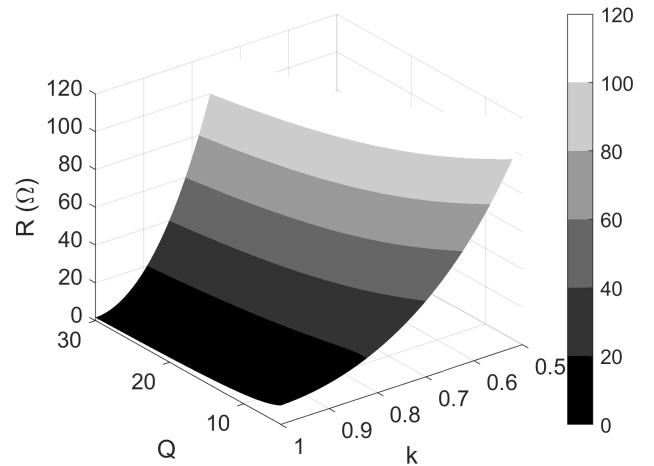|	SICC		DNICC	
$k = 0.2$	$k = 0.8$	$k = 0.2$	$k = 0.8$	
$L_{A1} = 1.59\,\text{nH}$	$L_{A1} = 1.59\,\text{nH}$	$L_{C2} = 1.59\,\text{nH}$	$L_{C2} = 1.59\,\text{nH}$	
$L_{A2} = 0.27\,\text{nH}$	$L_{A2} = 0.71\,\text{nH}$	$R_C = 100\,\Omega$	$R_C = 100\,\Omega$	
$C_{A1} = 0.32\,\text{pF}$	$C_{A1} = 0.32\,\text{pF}$	$C_{C1} = 0.48\,\text{pF}$	$C_{C1} = 2.87\,\text{pF}$	
$C_{A2} = 0.64\,\text{pF}$	$C_{A2} = 0.64\,\text{pF}$	$C_{C2} = 0.64\,\text{pF}$	$C_{C2} = 0.64\,\text{pF}$	
$R_A = 100\,\Omega$	$R_A = 100\,\Omega$			

Fig. 4. DNICC shunt resistance versus quality factor and coupling factor for $L = 1.59$ nH.

in the DNICC-based circuit, the input RL and isolation are increasingly degraded, while the output RL is unaffected [Fig. 3(e) and (g)]. Higher coupling factors in compensated DNICC-based WPCs result in more narrowband performance [Fig. 3(h)], giving a tradeoff between the coupling factor and the circuit bandwidth. As k approaches unity, an issue arises with the DNICC-based WPC as the shunt parasitic inductance $(L_x^2 - M^2)/M$ tends to 0 (forming a short-circuit between the inputs) and the compensating capacitance C_2 tends to ∞.

The delta coils have an additional property that is extremely useful for designing compact WPCs. When the winding IL are included in a star–delta conversion, as in Appendix A, the real part of the parasitic impedance (7) increases as the coupling factor is decreased. This relationship means that R in Fig. 1 can be implemented without a discrete resistor by tuning k so that the parasitic resistance equals R. The value of k for a desired parallel parasitic resistance R_{PA} is obtained by solving (10) in Appendix A. The value of the shunt resistance, R_{PA}, given by (9) in Appendix A, is plotted against k and the quality factor Q for $L = 1.59$ nH in Fig. 4. For a given Q value which is largely dictated by the IC process, k must be tuned to achieve the desired R_{PA}, i.e., if R_{PA} is not sufficiently high, then the coupling factor will have to be reduced. In addition, it can be seen that $(dR_{PA})/(dk)$ increases with Q, meaning that k does not need to be reduced as much for higher-Q coils. It can be deduced from (4) that the value of k cannot be set as high as possible in order to maximize the mutual inductance and, hence, minimize the circuit size,
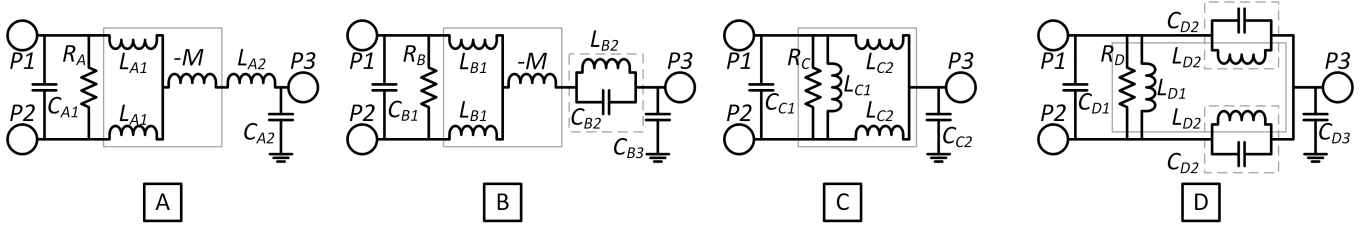
Fig. 5. Fig. 5. Lumped-element WPCs using coupled coils. Design A: star configuration. Design B: star configuration with harmonic trap. Design C: delta configuration. Design D: delta configuration with harmonic trap. The coupled coils and second harmonic traps are bounded with solid and dashed gray boxes, respectively.

TABLE II
WPC DESIGN EQUATIONS

Fig. 1b	Design A	Design B	Design C	Design D
$L = Z_0/\omega_0$	$L_{A1} = L$	$L_{B1} = L$	$L_{C2} = L$	$L_{D2} = 3L/4$
$R = 2Z_0$	$L_{A2} = M$	$L_{B2} = 3M/4$	$R_C = R$	$R_D = R$
$C_X = 1/(2\omega_0 Z_0)$	$R_A = R$	$R_B = R$	$C_{C1} = 1/(\omega_0^2 L_{C1}) + C_X$	$C_{D1} = 1/(\omega_0^2 L_{D1}) + C_X$
$C_Y = 1/(\omega_0 Z_0)$	$C_{A1} = C_X$	$C_{B1} = C_X$	$C_{C2} = C_Y$	$C_{D2} = 1/(3\omega_0^2 L)$
	$C_{A2} = C_Y$	$C_{B2} = 1/(3\omega_0^2 M)$		$C_{D3} = C_Y$
		$C_{B3} = C_Y$		

since high k values result in small R_{PA} values. This shunt parasitic resistance of the delta model allows the construction of a lumped-element WPC with only three components as will be explained in the following section.

III. NOVEL WILKINSON POWER COMBINERS USING COUPLED COILS

Four lumped-element WPCs using coupled coils, labeled Designs A–D, are shown in Fig. 5, with design equations given in Table II, where Z_0 is the port impedance. The design equations for the WPC shown in Fig. 1(b) are derived using even–odd-mode analysis. In the even mode of Fig. 1(b), L and $C_Y/2$ match port 1 to port 3 (and also port 2 to port 3), whereas in the odd mode, $2C_X$ resonates out L so that all the antiphase input power is dissipated in R. Designs A and B use SICCs to implement the series inductances shown in Fig. 1(b) while C and D use DNICCs. Designs B and D include second-harmonic traps to lower the output THD and reduce the required inductance of the corresponding resonated inductor by 25%, i.e., $L_{B2} = 0.75L_{A2}$ and $L_{D2} = 0.75L_{C2}$. Although the DNICC-based circuits require only a single coil, the SICC-based circuits require two coils, i.e., one coupled coil and one compensating coil L_{A2}, L_{B2}. The latter provides a good benchmark as they are similar to the traditional lumped-element WPCs, which are typically implemented with two coils, while also demonstrating the effectiveness of the proposed negative inductance compensation technique.

The specifics of the four designs will now be covered. Design A is similar to the WPC circuit shown in Fig. 1(b) with the two inductances L replaced with a compensated SICC. Design B is a variant of A and includes a second-harmonic trap by replacing L_{A2} with a parallel resonator $L_{B2}C_{B2}$ which presents $+M$ at f_0, with L_{B2} being 25% smaller than L_{A2}. Design C requires only three components as R_C is provided by the coil parasitics and C_{C1} is formed from the combination of C_X in Fig. 1(b) and compensating capacitor C_2 in Fig. 2.

Finally, Design D is a variant of C and includes a second-harmonic trap by replacing L_{C2} with a parallel resonator $L_{D2}C_{D2}$ which presents L at f_0, with L_{D2} being 25% smaller than L_{C2}.

The use of a second-harmonic trap benefits DNICC-based WPCs more than SICC-based WPCs as will be explained below. SICC-based WPCs employ two coils, the SICC and the compensating coil, whereas DNICC-based WPCs only use one coil (Fig. 5). By incorporating a second-harmonic trap into an SICC-based WPC, the inductance value of the compensating coil is reduced by 25% from $L_{A2} = M$ to $L_{B2} = 0.75\,M$ (Table II) while the inductance value of the SICC remains the same, i.e., $L_{A1} = L_{B1} = L$. Hence, the 25% reduction in the compensating coil's inductance does not translate into 25% overall circuit size reduction, especially since the size of the compensating coil is smaller than that of the SICC due to $M < L$. On the other hand, by incorporating a second-harmonic trap into a DNICC-based WPC, the inductance value of the solely employed coil is reduced by 25% from $L_{C2} = L$ to $L_{D2} = 0.75\,L$ (Table II), and therefore, the overall circuit size reduction will also be close to 25%.

IV. IMPLEMENTATION OF WPCs ON 28-nm CMOS

Designs A–D, designed with port impedances $Z_0 = 50\ \Omega$, were fabricated on TSMC's 28-nm bulk CMOS process with the annotated chip layouts and chip micrographs shown in Figs. 6 and 7, respectively. The coils were implemented on the 2.8-μm-thick aluminum redistribution layer to minimize the IL. The coils and interconnects were EM simulated using Keysight's "Momentum RF" solver while TSMC circuit models were used to simulate the metal–oxide–metal capacitors and polysilicon resistors. To reduce the simulation time, the vias were merged using the "merge vias keeping boundaries" option in Momentum. The designs were created in Cadence Virtuoso and simulated with SpectreRF. Keysight's
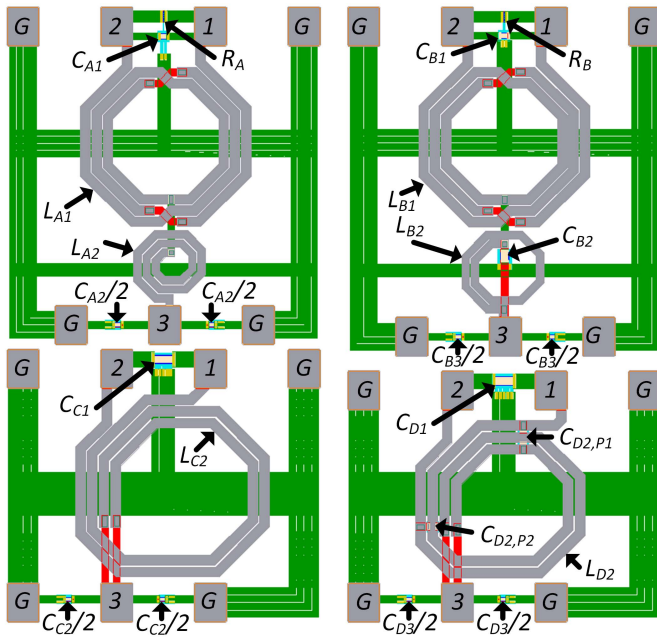
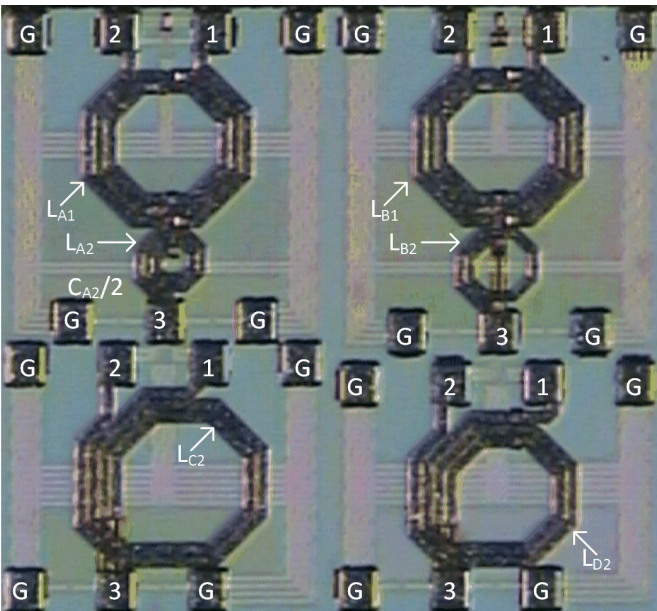Fig. 6.   Circuit layouts for Designs *A–D*.

Fig. 7.   Test chip micrograph with coils and ports annotated.

GoldenGate was used to access Momentum from within Virtuoso. The simulated component values at 5 GHz are given in Table III.

The SICC was implemented with a symmetric center-tapped spiral inductor and the compensating inductor was implemented with a standard spiral inductor. The spacing between the metal traces of the SICC should be as small as possible to maximize the magnetic coupling. The SICC and compensating inductor experience mutual coupling, and thus, there is a tradeoff between the coil separation distance and the interconnect losses. Increasing the coil separation distance lowers the

TABLE III
OPTIMIZED COMPONENT VALUES AT 5 GHz (INDUCTANCES IN NANOHENRY, CAPACITANCES IN PICOFARADS, AND RESISTANCES IN OHMS)

Design *A*		Design *B*		Design *C*		Design *D*	
L_{A1}	1.48	L_{B1}	1.48	L_{C2}	1.7	L_{D2}	1.32
$k_{L_{A1}}$	-0.66	$k_{L_{B1}}$	-0.67	$k_{L_{C2}}$	0.7	$k_{L_{D2}}$	0.66
L_{A2}	0.53	L_{B2}	0.44	C_{C1}	1.52	C_{D1}	1.56
C_{A1}	0.33	C_{B1}	0.33	C_{C2}	0.45	$C_{D2,P1}$	0.46
C_{A2}	0.51	C_{B2}	0.66	R_C	96	$C_{D2,P2}$	0.34
R_A	120	C_{B3}	0.51			C_{D3}	0.44
		R_B	117			R_D	90

coupling factor (meaning that the SICC and the compensating coil can be designed and optimized individually) but increases the interconnect losses. To minimize the interconnect losses, the SICC and the compensating inductor were placed close together and an iterative approach was used to fully cancel the negative SICC leakage inductance. The design methodology for Design *A* is as follows.

1) Design the SICC and evaluate by grounding Port 3 (Fig. 2) and simulating the two-port Z-parameters.
2) Design the $+M$ compensating coil.
3) Connect the two coils and simulate their Z-parameters.
4) Adjust the SICC layout to compensate for the mutual coupling between the SICC and $+M$ coil.
5) Adjust the compensating coil to nullify the new $-M$.
6) Repeat steps 4 and 5 until the specification is satisfied.
7) Use the design equations in Table II to get values for the remaining components and add to the simulation.
8) Evaluate the combiner using three-port S-parameters.
9) Tune noninductive passives to account for circuit nonidealities.

To lower the IL in Design *B*, L_{B2}'s inner diameter was increased and its turn count was decreased relative to L_{A2} resulting in similar areas for L_{A2} and L_{B2} despite $L_{B2} = 0.75L_{A2}$. Increasing the inner diameter of a spiral inductor can lower the IL as it reduces the effects of eddy currents which are concentrated in the center of the coil [19]. The EM-simulated SICC inductances of L_{A1} and L_{B1} are lower than that given in Table II (1.48 nH vs. 1.59 nH) as the coils were simulated in isolation with only the ground lines included. When additional circuitry such as routing lines and the compensating inductance are included, the inductances of L_{A1} and L_{B1} are much closer to 1.59 nH. R_A and R_B are $\sim$20 Ω higher than that given in Table II (100 Ω) as the simulated isolation was $\sim$1.5 dB higher at 5 GHz.

The DNICC was implemented with a custom octagonal version of the Shibata coil, which is primarily a single-layer structure, hence enabling both of its windings to be realized on the thick aluminum layer [20]. As the Shibata coil is an edge-coupled structure, it can easily provide the shunt resistance R as the coupling factor can be tuned by varying the spacing between the metal traces. The design methodology for Design *C* is as follows.

1) Design an initial DNICC and evaluate it by grounding port 3 (Fig. 2) and simulating its two-port Y-parameters.
2) Revise the layout until the specifications are satisfied.
3) Add the resonating capacitance and simulate to confirm that L_{C1} has been nullified.
4) Obtain the remaining component values from Table II and add them to the simulation.
5) Evaluate the combiner using three-port S-parameters.
6) Tune the capacitances to account for circuit nonidealities.

When implementing the $L_{D2}C_{D2}$ resonator in Design D, the capacitors were connected directly across the windings to avoid long routing lines from port 1 to port 3 (and port 2 to port 3) while still resonating the majority of the winding inductance.

L_{C2} and L_{D2} slightly deviate from their theoretical values in Table II, i.e., 1.7 nH versus 1.59 nH and 1.32 nH versus 1.2 nH, as they were tuned to obtain better overall circuit performance in terms of RL, IL, and isolation.

To increase the layout symmetry, the single-ended capacitor at port 3 ($C_{A2}, C_{B3}, C_{C2}, C_{D3}$) was divided in two and connected between port 3 and the two adjacent ground pads (Fig. 7). All four coil designs achieve good levels of coupling ($\sim$0.7) which show that edge coupling is an effective technique for the design of coupled coils.

V. SIMULATION AND MEASUREMENT RESULTS

The S-parameters measurements were performed using an Agilent E8361C PNA with a 40A-GS-150/40A-SG-150-D-150-N Picoprobe connected to ports 1 and 2, and a 40A-GSG-150-p-n Picoprobe connected to port 3 of each circuit. Three sets of two-port measurements were required to assemble the full three-port S-parameters with the unused port terminated to 50 Ω. A Picoprobe CS-3-150 impedance standard substrate (ISS) was used for each two-port short-open-load-thru (SOLT) calibration. For each two-port calibration, the short, open, and load calibration procedures are illustrated in Fig. 8, where the GSG probe would have one of its two ground pins touch the bare ceramic of the ISS. For Thru #1 (ports 1 and 3) and Thru #2 (ports 2 and 3) shown in Fig. 8, the GSG probe would have both ground pins connected to the ground pad while one half of the GSSG probe would not be included in the calibration. Finally, in Thru #3 (ports 1 and 2), the GSG probe would have all the three pins grounded while the GSSG probe would be connected to the fixture.

The simulation and measurement results of the four circuits, with the bond pads deembedded using EM-simulated S-parameters, are plotted in Figs. 9–12, summarized in Table IV, and compared with [9] and [12]–[14] in Table V. The bandwidths in Table V are defined as the range in which the RL and isolation are $\geq$ 10 dB. The upper bounds of Designs A–D's bandwidths have been set to keep the IL to acceptable levels. All four designs have an excellent agreement between the measurements and simulations. The results will now be compared and discussed.

1) All Designs: The difference in measured and simulated IL can be attributed to a number of factors. The high-density
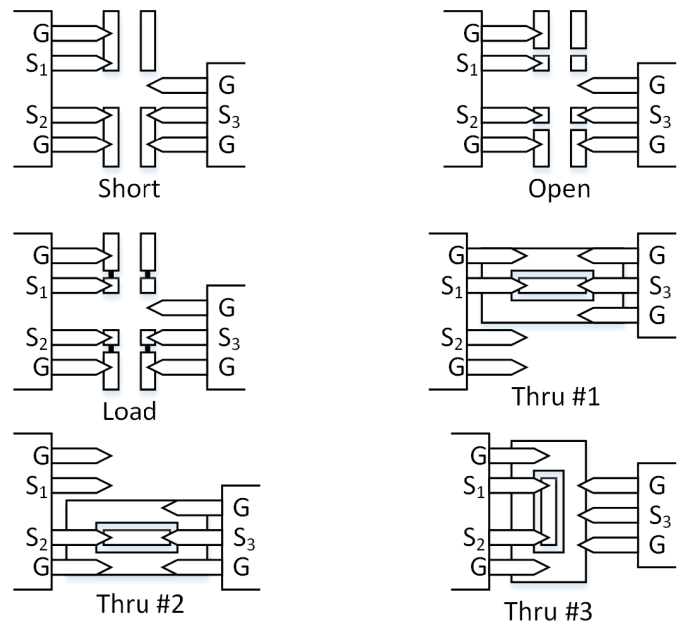

Fig. 8.   Two-port SOLT probe calibration with GSSG and GSG probes.

dummy metal fill, used to meet metal density requirements, was not included in the simulations and is found to decrease the quality factor and self-resonant frequency of integrated inductors due to eddy current flow and increased capacitive coupling, respectively [21]–[24]. A low-density dummy metal fill was available for inductors but was restricted to $\leq$ 5% of the layout area and so could not be used. Furthermore, the TSMC MOM capacitor models used in the simulations may be inaccurate. Via merging was used in Momentum to speed up the EM simulations and reduce the memory requirements. This could have resulted in an underestimate of the via resistances.

2) A and B: The SICC-based designs have high fractional bandwidths of 42%–43% with the lower and upper bounds constrained by the isolation and IL, respectively. The wider bandwidths compared with C and D are aligned with the simulation predictions in Fig. 3, wherein unlike the DNICC-based WPC, the bandwidth of the SICC-based WPC is shown to be unaffected by the level of coupling factor.

A and B have the best input RL with a minimum value of 17.5 and 18.2 dB across a 3.5–5.4 GHz and 3.5–5.35 GHz bandwidth, respectively. The isolation is excellent with peak values of 28.3 and 27.6 dB, respectively. As can be seen from Figs. 9 and 10, there is a variance in the frequency of the peak RL and isolation, with the peak input RL occurred at frequencies below 5 GHz, while the peak output RL and isolation occurred at frequencies above 5 GHz. This variance was inevitable as tuning the capacitances to optimize one parameter to have a peak value at 5 GHz would diminish the other parameters.

The amplitude error, $|S_{13} - S_{23}|$, is relatively constant over the bandwidth and the variation can be partly attributed to measurement noise. Part of the amplitude and phase error, $|\angle S_{13} - \angle S_{23}|$, may be attributed to the asymmetric magnetic
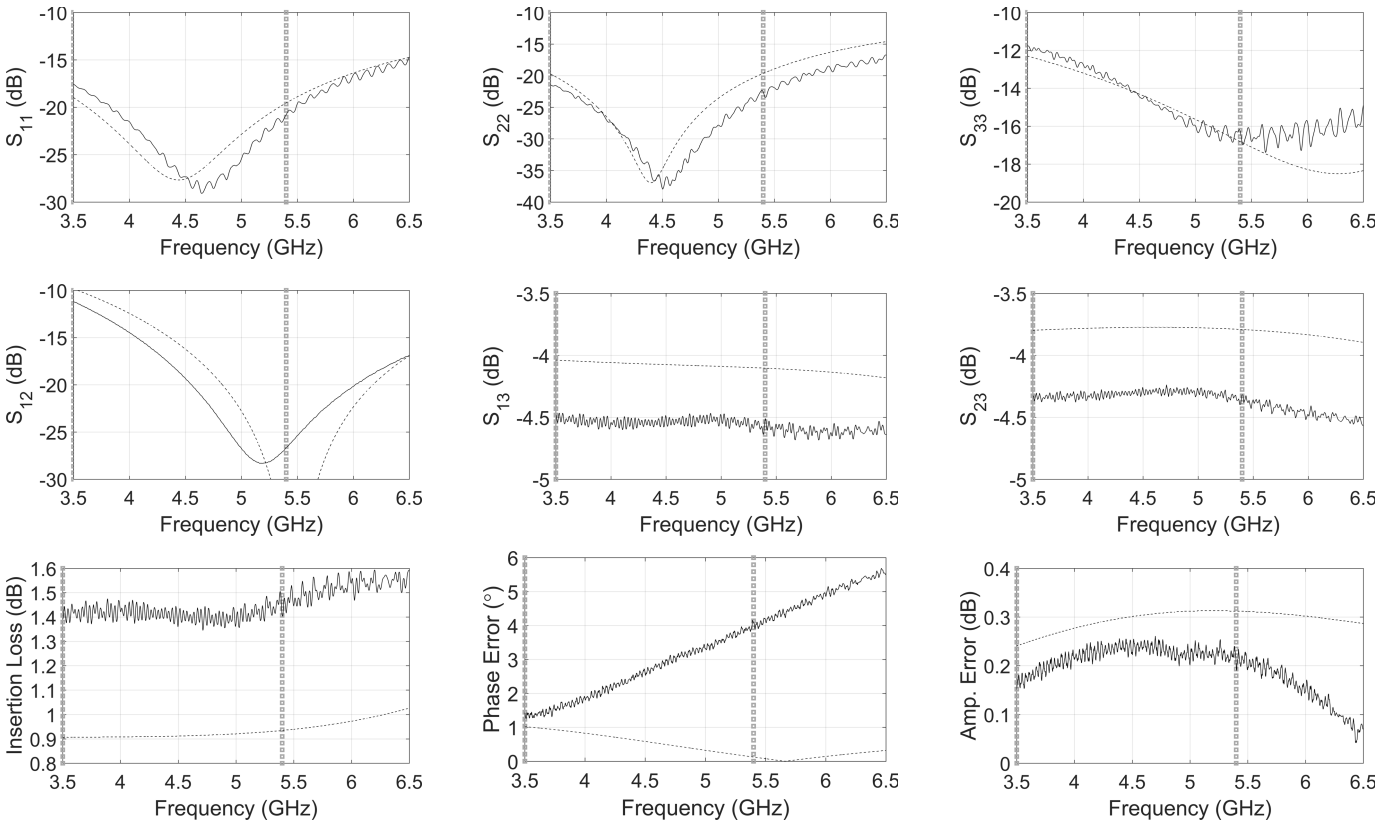
Fig. 9.   S-parameters results of Design *A*. Solid line: measurement. Dashed line: simulation. Squares: f_0 bandwidth.
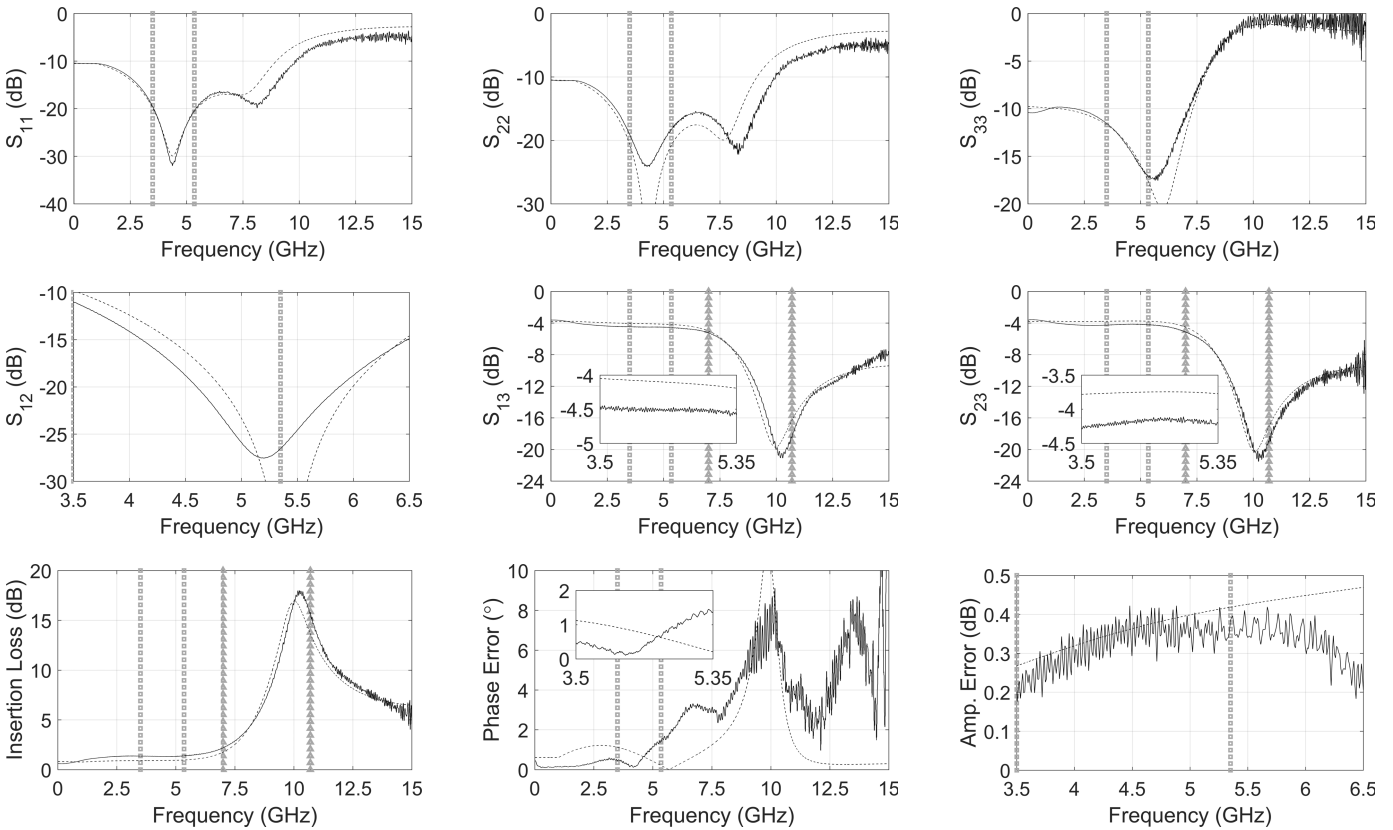

Fig. 10.   S-parameters results of Design *B*. Solid line: measurement. Dashed line: simulation. Squares: f_0 bandwidth. Triangles: $2f_0$ bandwidth.

coupling between the SICC and the asymmetric compensating coil. The amplitude and phase error could be reduced by using a more symmetric compensating coil or moving the two coils further apart to reduce the coupling factor. To confirm
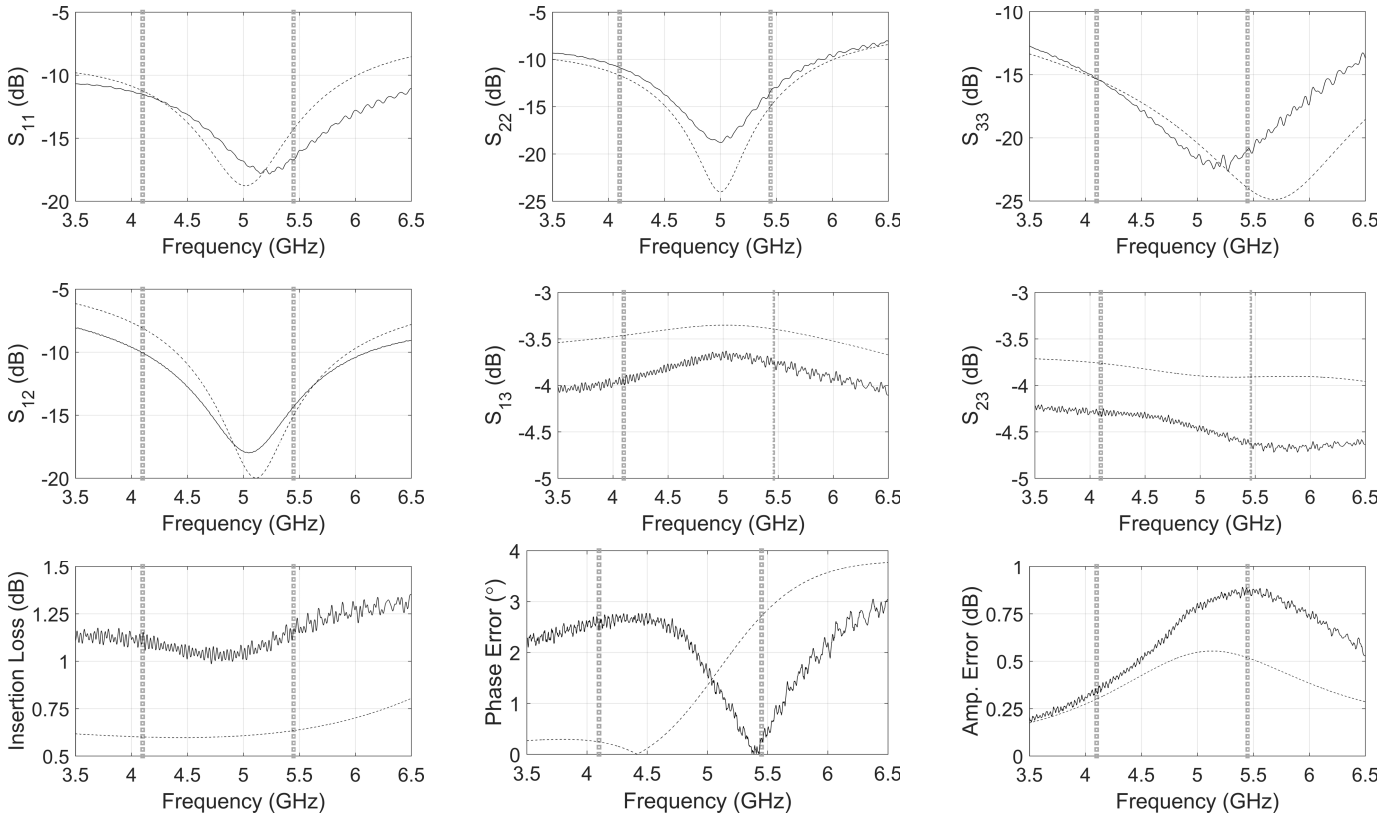
Fig. 11.   S-parameters results of Design *C*. Solid line: measurement. Dashed line: simulation. Squares: f_0 bandwidth.
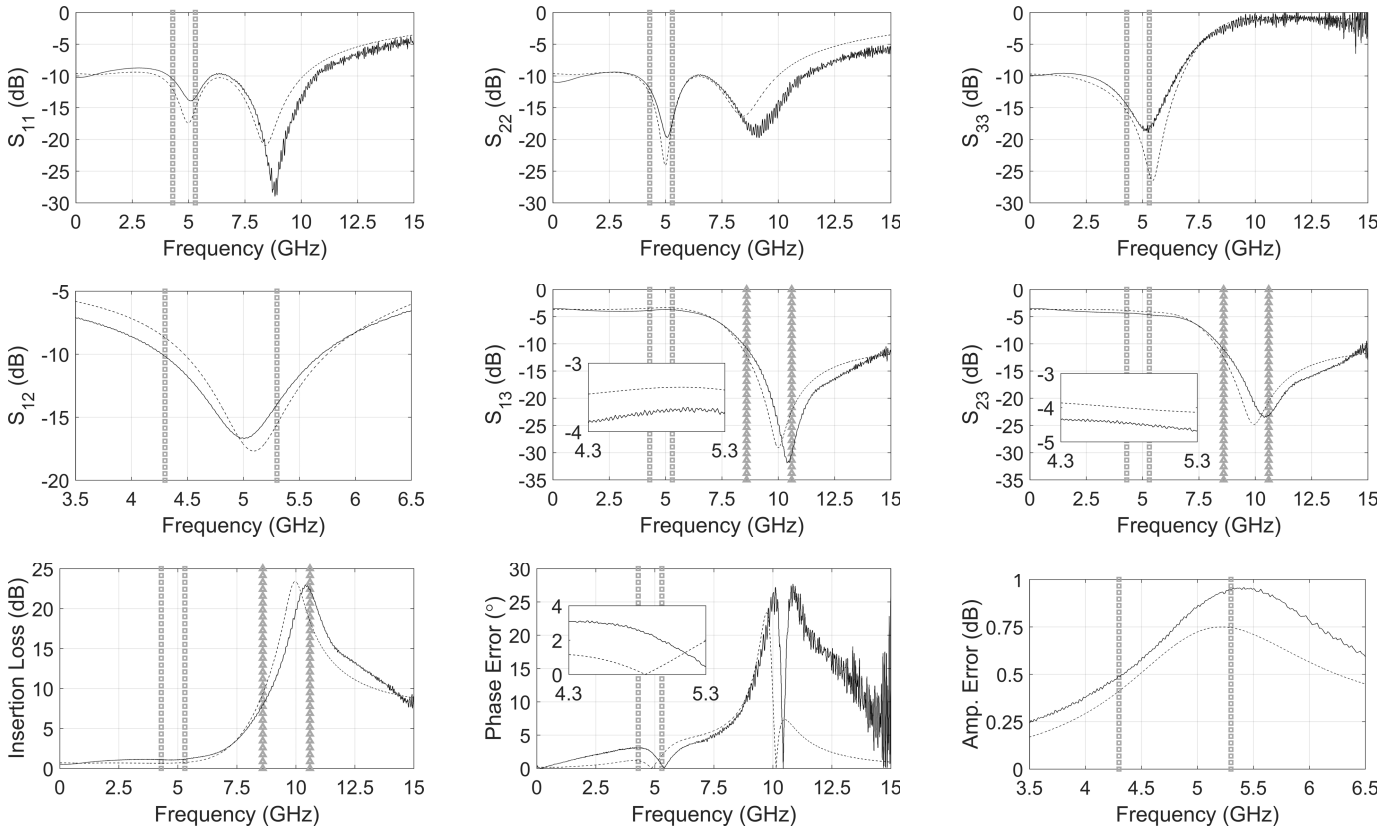

Fig. 12.   S-parameters results of Design *D*. Solid line: measurement. Dashed line: simulation. Squares: f_0 bandwidth. Triangles: $2f_0$ bandwidth.

the second idea, a Momentum simulation of Design *A* with the compensating coil moved 40 μm away from the SICC

was performed from 1 to 10 GHz and the peak amplitude error decreased from 0.32 to 0.15 dB and the peak phase

TABLE IV

SUMMARY OF MEASUREMENT RESULTS

Measurement	Design A		Design B		Design C		Design D	
	Min	Max	Min	Max	Min	Max	Min	Max
Input return loss $|S_{11}|$ (dB$_{GHz}$)	$17.5_{3.5}$	$29.1_{4.6}$	$19.6_{3.5}$	$32_{4.4}$	$11.5_{4.1}$	$17.8_{5.2}$	$10.5_{4.3}$	$14_{5.2}$
Input return loss $|S_{22}|$ (dB$_{GHz}$)	$21.5_{3.5}$	$36.6_{4.6}$	$18.2_{5.3}$	$24.1_{4.3}$	$10.9_{4.1}$	18.8_5	$12_{4.3}$	$19.7_{5.1}$
Output return loss $|S_{33}|$ (dB$_{GHz}$)	$11.8_{3.5}$	$16.8_{5.3}$	$11.6_{3.5}$	$17.1_{5.3}$	$15.3_{4.1}$	$22.7_{5.3}$	$14.6_{4.3}$	$18.9_{5.3}$
Isolation $|S_{12}|$ (dB$_{GHz}$)	$11.2_{3.5}$	$28.3_{5.2}$	$11_{3.5}$	$27.6_{5.2}$	$10_{4.1}$	18_5	$10.1_{4.3}$	16.7_5
Transmission coefficient $|S_{13}|$ (dB$_{GHz}$)	$4.5_{3.5}$	$4.6_{5.4}$	$4.5_{3.6}$	$4.6_{5.3}$	3.6_5	$4_{4.1}$	3.6_5	$3.9_{4.3}$
Transmission coefficient $|S_{23}|$ (dB$_{GHz}$)	$4.2_{4.7}$	$4.4_{5.4}$	$4.1_{4.9}$	$4.3_{3.5}$	$4.3_{4.1}$	$4.6_{5.4}$	$4.3_{4.3}$	$4.7_{5.3}$
Insertion loss (dB$_{GHz}$)	$1.3_{4.7}$	$1.5_{5.4}$	$1.3_{4.8}$	$1.4_{5.3}$	$1_{4.7}$	$1.2_{5.4}$	$1_{4.7}$	$1.2_{5.3}$
2nd harmonic rejection (dB$_{GHz}$)	1.6_7	$3.9_{10.6}$	2.0_7	$18_{10.2}$	$3.2_{8.2}$	$4.2_{10.8}$	$7.9_{8.6}$	$23_{10.4}$
Amplitude error (dB$_{GHz}$)	$0.15_{3.5}$	$0.26_{4.7}$	$0.18_{3.5}$	$0.42_{4.9}$	$0.33_{4.1}$	$0.89_{5.4}$	$0.49_{4.3}$	$0.95_{5.3}$
Phase error ($°_{GHz}$)	$1.3_{3.5}$	$4.2_{5.4}$	$< 0.01_{4.3}$	$1.6_{5.2}$	$< 0.01_{5.4}$	$2.8_{4.5}$	$0.46_{5.3}$	$3.1_{4.4}$

* Min/Max values are bounded by the circuit bandwidths in Table V

TABLE V

COMPARISON WITH THE STATE-OF-THE-ART WPCs

	[12]	[13]	[14] (4-way)	[9]	Design A	Design B	Design C	Design D
Technology	350 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm Bulk CMOS	130 nm Bulk CMOS	28 nm Bulk CMOS	28 nm Bulk CMOS	28 nm Bulk CMOS	28 nm Bulk CMOS
Frequency (GHz)	8-14	5.2-18.8	4.1-5.05	23.4-32	3.5-5.4	3.5-5.35	4.1-5.45	4.3-5.3
Bandwidth (%)	54	113	21	31	43	42	28	21
Input return loss (dB)	> 10	> 10	> 15	> 10	> 17.5	> 18.2	> 10.9	> 10.5
Output return loss (dB)	> 12	> 10	> 15	> 14	> 11.8	> 11.6	> 15.3	> 14.6
Isolation (dB)	> 10	> 10	> 17	> 12.5	> 11.2	> 11	> 10	> 10.1
Insertion loss (dB)	< 1.4	< 1.1	< 1.1	< 1.3	< 1.5	< 1.4	< 1.2	< 1.2
2nd harmonic rejection (dB$_{GHz}$)	3.5_{20}	1.1_{20}	$14_{9.2}$	N/A	3.8_{10}	$18_{10.2}$	3.7_{10}	$23_{10.4}$
Amplitude error (dB)	< 0.6	< 0.06	< 0.2	N/A	< 0.26	< 0.42	< 0.89	< 0.95
Phase error (°)	< 3	< 1	N/A	N/A	< 4.1	< 1.6	< 2.8	< 3.1
Dimensions (mm, mm)	0.6, 0.2	0.32, 0.34	0.56, 0.56	0.12, 0.29	0.26, 0.49	0.26, 0.51	0.3, 0.38	0.26, 0.35
Active area (mm^2)	0.12	0.11	0.31	0.035	0.13	0.13	0.11	0.09
Active area (λ_0^2)	162 µ	174 µ	73 µ	297 µ	28 µ	29 µ	29 µ	23 µ
Z_{in}, Z_{out} (Ω)	60, 100	50, 50	50, 50	50, 50	50, 50	50, 50	50, 50	50, 50

error decreased from 1.05° to 0.36°. These simulation results support the idea that the coupling between the SICC and the compensating coil has a nonnegligible influence on the amplitude and phase errors.

3) C and D: The single-coil design of C and D resulted in the smallest circuit areas and the simplest layouts with C requiring only three components. The reactive compensation resulted in a negligible size increase when compared with the uncompensated DNICC as the compensation capacitances were absorbed into C_X [Fig. 1(b)]. The benefit of the resonator $L_{D2}C_{D2}$ in D is apparent as D is 18% smaller than C.

C and D had good levels of bandwidth with the upper and lower bounds set by limiting the IL to <1.2 dB and isolation to >10 dB. The higher isolation of C enabled a 7% wider fractional bandwidth than D. The difference in isolation could be due to the differing shunt resistances of the DNICCs (Table III).

The IL was much lower than A and B due to the absence of the series compensating coil L_{A2}, L_{B2}, with C and D having a maximum IL 0.3 dB lower than A. The excellent isolation

centered at 5 GHz with a peak of 18 dB in C validates the technique of using coupling parasitics to provide the isolation resistance and thus removing the need for a discrete resistor.

The amplitude error has been attributed to the physical location of C_{C1} and C_{D1}, i.e., across ports 1 and 2 (Fig. 6), which causes an unbalanced resonance current to flow through the coil, altering the L_{C2} and L_{D2} inductances. The simulated inductances of the compensated DNICC in Design C are shown in Fig. 13. The simulation results show an inductance imbalance of ~250 pH between L_{13} and L_{23} at 5 GHz, with L_{23} ~16% greater than L_{13}, which results in $|S_{23}| < |S_{13}|$ as shown in Fig. 11. This inductance imbalance can be alleviated by using a more symmetric coupled coil than the Shibata coil shown in Fig. 7 and by placing the resonating capacitor C_2 (Fig. 2) in the center of the coil as shown in Fig. 14. The improved DNICC layout shown in Fig. 14 uses an octagonal version of the Frlan coil from [20] with the resonating capacitor placed below the center of the coil. A Frlan coil, including C_2 from Fig. 2, was EM simulated and the results are plotted in Fig. 13. At 5 GHz, the windings
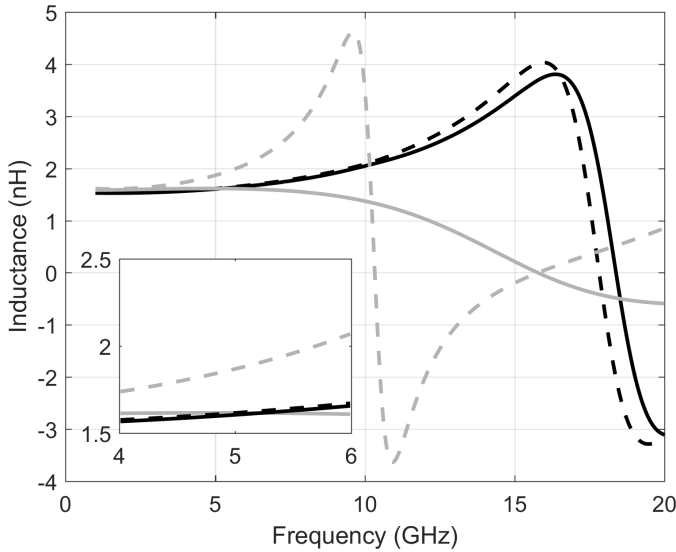
Fig. 13. Simulation results of Shibata (gray) and Frlan (black) compensated DNICCs where the solid lines are L_{13}, the dashed lines are L_{23}, and L_{ij} is the inductance between ports i and j.
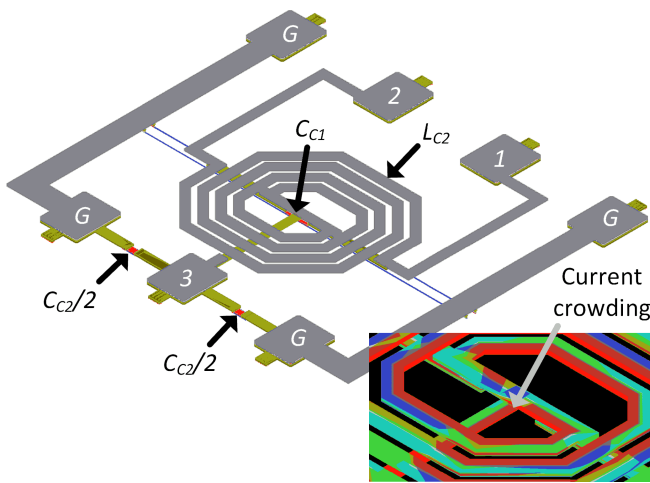

Fig. 14. Layout of an alternative Design C using a symmetric Frlan DNICC. Inset: current distribution in the EM simulated coil.
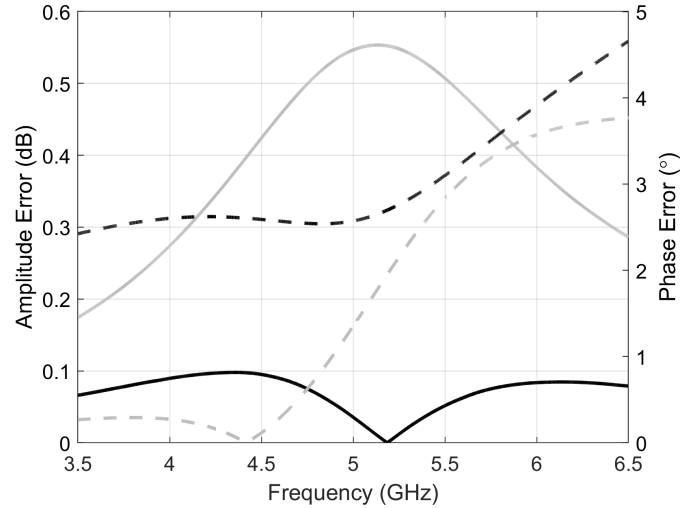

Fig. 15. Simulated amplitude (solid lines) and phase (dashed lines) errors of the Shibata (gray) and Frlan (black) DNICCs based on Design C.
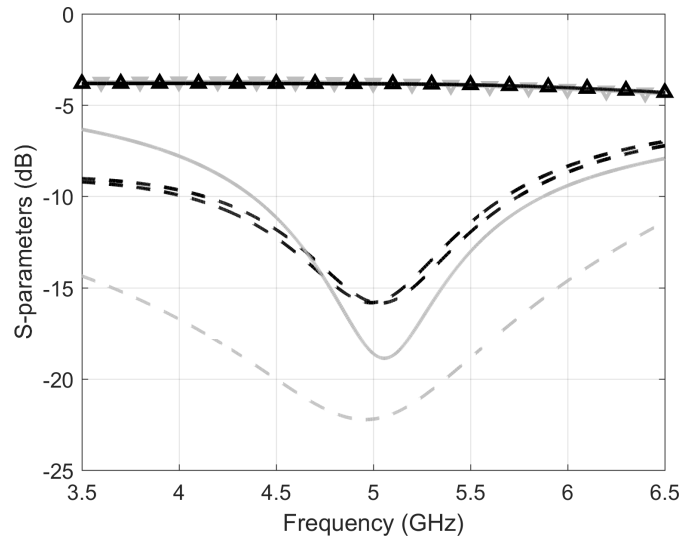

Fig. 16. S-parameters of the unoptimized Frlan-based Design C. (S_{11}/S_{22}: black dashes. S_{33}: gray dashes. S_{12}: gray line. S_{13}: gray line with downward-pointing triangles. S_{23}: black line with upward-pointing triangles).

net inductances are $L_{23} = 1.615$ nH and $L_{13} = 1.605$ nH, with L_{23} only 0.6% larger than L_{13}, and this could be further optimized. The Frlan coil shown in Fig. 14 is also shown in Fig. 13 to have a much higher self-resonant frequency (17.8 GHz) than the Shibata coil shown in Fig. 6 (10.3 GHz).

Simulation results of the unoptimized Frlan-based version of Design C in Fig. 14 are shown in Figs. 15 and 16 with $Z_0 = 50$ Ω. The design process used the methodology for Design C described in Section. IV. The layout, excluding the capacitors, shown in Fig. 14 was EM-simulated in Momentum with ports connected to the bond-pads and the ends of the capacitor routing lines. The EM-simulated S-parameters in conjunction with TSMC capacitor models were then simulated in SpectreRF. The simulated amplitude error now peaks at 0.1 dB across a 3.5 to 6.5-GHz frequency range, compared to 0.55 dB in the original simulated Design C, with the phase error increased slightly within an acceptable range. At close

to dc, both the amplitude and phase errors are close to zero, implying that internal coupling results in an increasing error as frequency increases. The error is thought to be due to unbalanced current crowding caused by the rotation of the currents through the coil as shown in the inset of Fig. 14.

4) B and D: Designs B and D exhibit good levels of second-harmonic rejection of 18 and 23 dB, respectively. The peak harmonic rejection of D is higher than B since the resonating inductance L_{D2} is greater than L_{B2} (see Appendix B for the explanation).

The second minima of S_{11} and S_{22} (which also occur in Designs A and C at around 15 GHz in simulations) are caused by parasitic capacitances in the design. To demonstrate this, three identical parasitic capacitances (C_{par}) are added to the WPC shown in Fig. 1(b), where they are connected between ports 1–3 and ground. As shown in Fig. 17, in the absence of
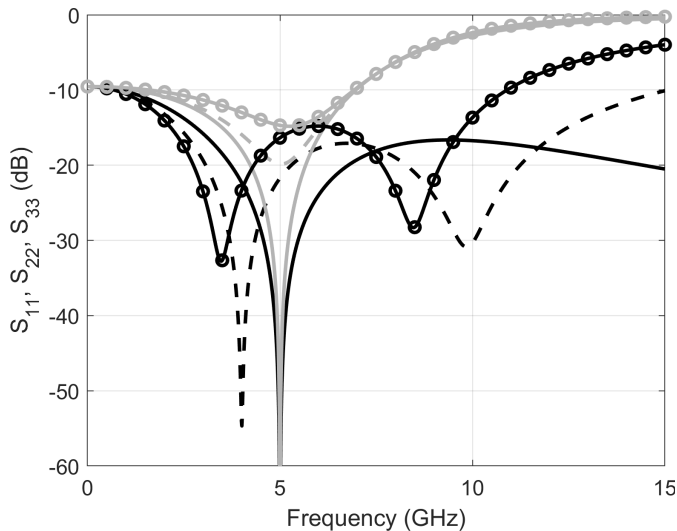
Fig. 17. S_{11} and S_{22} (black), and S_{33} (gray), simulations of the WPC in Fig. 1(b)with grounded parasitic capacitors attached to each port of 0 fF (solid line), 100 fF (dashed line), and 200 fF (line with circles).
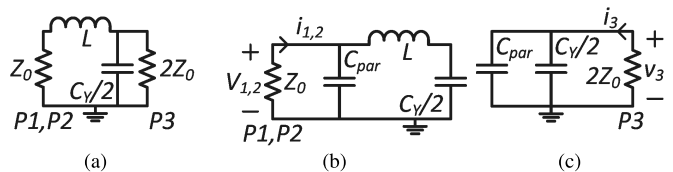

Fig. 18. (a) Even mode representation of the WPC in Fig. 1(b) and (b) resulting circuits when measuring Z_{11} and Z_{22}, and (c) Z_{33}, in the presence of capacitive parasitics.

C_{par} (i.e., $C_{par} = 0$), there is only one dip in the responses of S_{11}, S_{22}, and S_{33}, i.e., at 5 GHz. By introducing C_{par} (i.e., $C_{par} \neq 0$), a second dip appears in the S_{11} and S_{22} responses, but not in the S_{33} response. This can be explained through the WPC's even-mode equivalent circuit [Fig. 18(a)], where it has one capacitor connected to port 3 (i.e., $C_Y/2$) but no capacitor connected to port 1 or 2. As a result, the presence of C_{par} at ports 1 and 2 increases the number of poles of Z_{11} and Z_{22} (input impedances seen from ports 1 and 2) by one [Fig. 18(b)], hence producing a second dip in the S_{11} and S_{22} responses. On the other hand, the presence of C_{par} at port 3 increases the net capacitance at port 3 from $C_Y/2$ to $C_Y/2 + C_{par}$ [Fig. 18(c)], but does not increase the number of poles of Z_{33} (input impedance seen from port 3), hence no second minima produced. Furthermore, as shown in Fig. 17, the frequency and the magnitude of the second minima were strongly influenced by the value of C_{par}.

5) Comparison With the Literature: Designs $A-D$ are compared with [9] and [12]–[14] in Table V. While there are no publications of lumped-element WPCs that use a 28-nmbulk CMOS process, the designs in [9] and [14] use 130-nm bulk CMOS processes and the designs in [12] and [13] operate at frequencies close to those used by Designs $A-D$.

The electrical areas of Designs $A-D$ are considerably smaller than the other designs in Table V. While the larger size of [14] can be attributed to the four-way design, Designs $A-D$

are still very competitive with the largest design, B, being only 40% of the circuit in [14]. It should be noted that the output port of [14] is in the center of the transformer, which is impractical to connect to in a more complex system and the additional routing lines required to connect the combiner to other parts of the system would substantially increase the area and IL.

With regards to the IL, the four designs achieve good levels of performance when considering that [9] used a 4-μm aluminum metal layer, 43% thicker than that used in this paper, and that [12] and [13] benefited from a high-resistivity SiGe BiCMOS substrate which would experience much lower losses due to substrate coupling than CMOS circuits [25].

The most suitable design for comparison is [14], which also used a bulk CMOS process and a similar operating frequency. When compared to [14], it can be seen that the $A-D$ have good levels of performance while operating on a much more advanced CMOS process with much higher integration density that is attractive for SOC applications. The other CMOS design [9] operates at a much higher frequency and has the largest electrical area of the designs in Table V.

Designs B and D have a much greater second harmonic suppression than the designs in [12] and [13]. The design in [14] achieved 14 dB of second-harmonic suppression, which was 4 dB lower than B and 9 dB lower than D.

VI. CONCLUSION

The theory, design, and measurements of four lumped-element two-way WPCs employing star inverting and DNICC in a 28-nm bulk CMOS process, including a design methodology for effectively exploiting mutual coupling and nullifying the coupling parasitics have been presented. The DNICC-based designs exploit the coupling parasitics to provide the isolation resistance, removing the need for a discrete resistor. The fabricated circuits achieved good levels of performance and size when compared with other pertinent designs in the literature as summarized in Table V, with the measurement results having excellent agreement with the simulation results. The concept presented can be extended for n-way WPC design and applied directly to other circuits employing inductors as discussed in Appendix C.

When compared with the SICC-based circuits, the DNICC-based circuits have the best overall performance as they have lower IL, smaller areas, and better output RL with similar input RL and isolation. However, the SICC-based circuits have wider bandwidths since, unlike the DNICC-based circuits, their bandwidths are relatively unaffected by the coupling factor k.

The ability to integrate a second harmonic trap into the DNICC enables a large decrease in circuit area and this is a key advantage over the SICC as there is no access to the internal node of the SICC so the $L_x + M$ inductances cannot be resonated. The compensating inductance in the SICC WPC can be resonated but it results in lower harmonic suppression than the resonated DNICC WPC and has little effect on the circuit area.
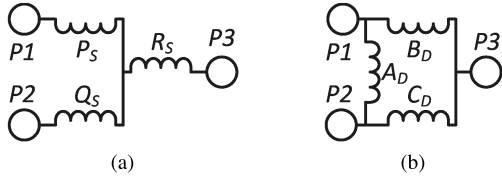
Fig. 19. (a) Star and (b) delta networks.

Fig. 20. Lossy parallel LC resonators.

APPENDIX A
LOSSY NONINVERTING STAR–DELTA COUPLED COIL CONVERSION

The conversion of a star model of a noninverting coupled coil to a delta model, shown in Fig. 19, will be presented. The three impedances of the star network, P_S, Q_S, and R_S, are converted to the delta network impedances A_D, B_D, and C_D using (2) and (3)

$$(A_D, B_D, C_D) = \left(\frac{\Sigma}{R_S}, \frac{\Sigma}{Q_S}, \frac{\Sigma}{P_S} \right) \tag{2}$$

$$\Sigma = P_S Q_S + P_S R_S + Q_S R_S. \tag{3}$$

The three star impedances are defined in (4) and (5) where L_x is the windings' self-inductance, M is the mutual inductance, R_x is the parasitic resistance, and quality factor is $Q_x = (\omega L_x)/R_x$

$$P_S = Q_S = R_x + j\omega(L_x - M) \tag{4}$$

$$R_S = j\omega M. \tag{5}$$

The three delta impedances are thus calculated in (6) and (7). It can be seen that the real part of A_D is a function of the coupling factor

$$
\begin{aligned}
B_D &= C_D \\
&= P_S + 2R_S \\
&= R_x + j\omega(L_x + M) \\
&= R_x + j\omega L_x(1 + k) \tag{6}
\end{aligned}
$$

$$
\begin{aligned}
A_D &= \frac{P_S^2}{R_S} + 2P_S \\
&= \frac{\omega L_x}{k} \left(\frac{2}{Q_x} + j \left[1 - \frac{1}{Q_x^2} - k^2 \right] \right). \tag{7}
\end{aligned}
$$

For a desired parallel resistance R_{PA}, (7) can be rearranged to find the required value of k. First, express A_D as the admittance Y_A

$$
\begin{aligned}
Y_A &= \frac{1}{A_D} \\
&= \frac{\frac{2}{Q_x} + j \left[1 - \frac{1}{Q_x^2} - k^2 \right]}{\frac{\omega L_x}{k} \left(\frac{2(1+k^2)}{Q_x^2} + 1 - 2k^2 + \frac{1}{Q_x^4} + k^4 \right)}. \tag{8}
\end{aligned}
$$

Equate the parallel resistance $1/\text{Real}(Y_A)$ to the desired parallel resistance R_{PA}

$$
\begin{aligned}
R_{PA} &= \frac{1}{\text{Real}(Y_A)} \\
&= \frac{Q_x \omega L_x}{2k} \left(\frac{2(1+k^2)}{Q_x^2} + 1 - 2k^2 + \frac{1}{Q_x^4} + k^4 \right). \tag{9}
\end{aligned}
$$
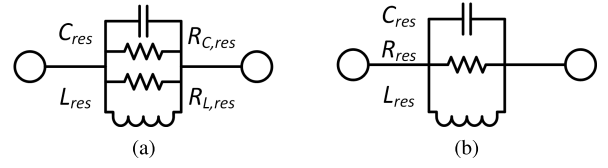
Defining the total inductance of B_D and C_D as $L_T = L_x(1 + k)$, rearrange (9) in terms of k to get (10) which can be solved with numerical tools such as MATLAB

$$
k^4 + 2k^2 \left[\frac{1}{Q_x^2} - 1 - \frac{R_{PA}}{Q_x \omega L_T} \right] - k \left[\frac{2R_{PA}}{Q_x \omega L_T} \right] + \left[1 + \frac{1}{Q_x^4} + \frac{2}{Q_x^2} \right] = 0. \tag{10}
$$

APPENDIX B
CMOS RESONATOR IMPEDANCE

This appendix will explain why the harmonic rejection of Design D is greater than B due to the larger resonating inductance L_{D2} compared to L_{B2}.

We begin with the lossy parallel LC resonator shown in Fig. 20(a) with capacitance C_{res} and its resistance $R_{C,\text{res}}$, and inductance L_{res} and its resistance $R_{L,\text{res}}$. The two resistances can be combined to form R_{res} as shown in Fig. 20(b). At resonance, C_{res} and L_{res} will cancel out leaving only R_{res}, and thus, to maximize the resonator's impedance during resonance, we must maximize $R_{C,\text{res}}$ and $R_{L,\text{res}}$.

The parallel resistance of a series RL or RC component is defined in terms of its series resistance R_{series} and its series reactance X_{series} as shown in (11). Substituting the quality factor $Q_{\text{series}} = X_{\text{series}}/R_{\text{series}}$ into (11) gives (12) which shows that R_{parallel} is a function of both X_{series} and Q_{series}

$$R_{\text{parallel}} = \frac{R_{\text{series}}^2 + X_{\text{series}}^2}{R_{\text{series}}} \tag{11}$$

$$= \frac{X_{\text{series}} + X_{\text{series}} Q_{\text{series}}^2}{Q_{\text{series}}}. \tag{12}$$

Thus, to increase the impedance of the resonator, Q_{series} and X_{series} must be increased. This can be done by using small capacitances and large inductances to maximize their reactances.

Using small inductances to maximize the inductor quality factor, and thus R_{parallel}, in CMOS circuits is not an effective strategy as it would require larger capacitances with lower reactances and quality factors, and the detrimental effect of the smaller inductor reactance on R_{parallel} would almost certainly be greater than the positive effect from the increase in quality factor. Thus, to design resonators with a high impedance on a standard CMOS process, large inductors and small capacitors must be used and this explains why Design D had better harmonic rejection than B as $L_{D2} > L_{B2}$

APPENDIX C
ADDITIONAL COUPLED COIL APPLICATIONS

The inductance compensation techniques presented here can be applied to many other circuits that utilize inductors. Two
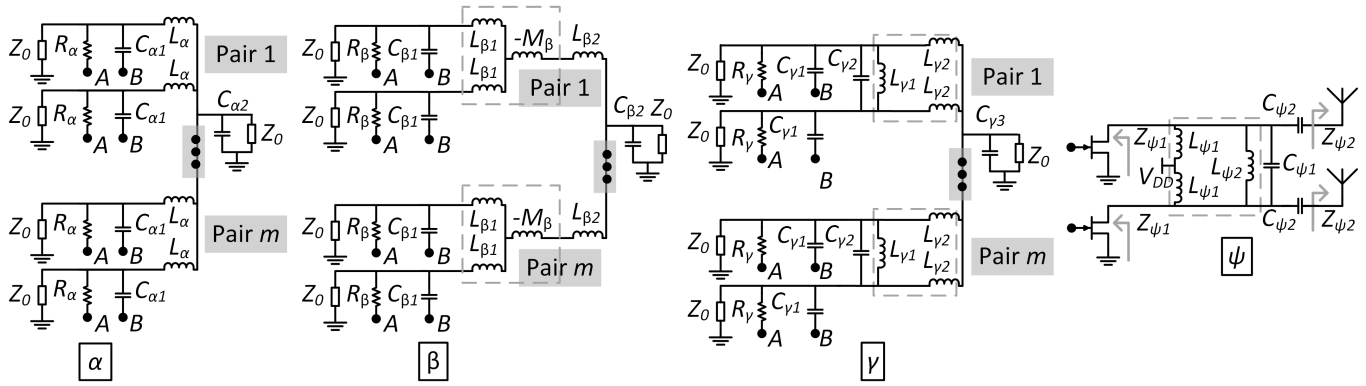
Fig. 21. Lumped-element n-way combiner (α) comprised of m pairs of inputs ($m = n/2$) with variants using SICCs and DNICCs (β and γ, respectively). A and B are the circuit nodes with the connecting lines between each component removed for clarity. Circuit ψ shows a pair of PAs in a phased array with a single DNICC replacing the two dc feed inductances. The PA drain impedances and the antenna resistances are defined as $Z_{\psi 1}$ and $Z_{\psi 2}$, respectively. The coupled coils are enclosed by dashed gray boxes.

TABLE VI
n-WAY WPC DESIGN EQUATIONS

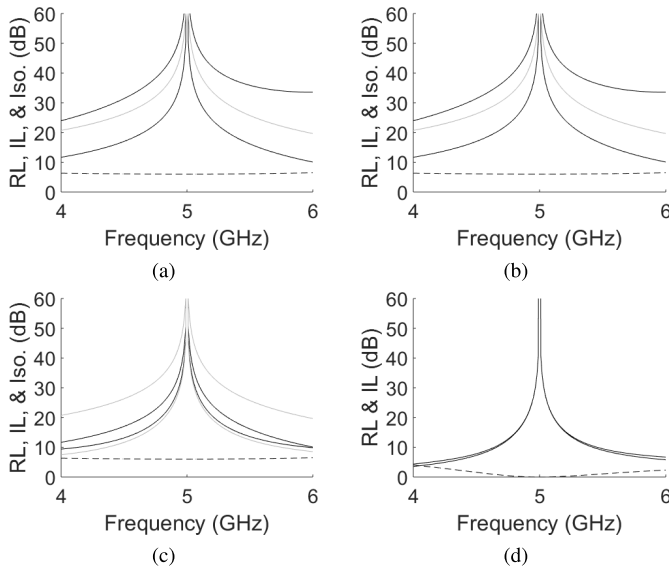| Design α	Design β	Design γ
$L_\alpha = \frac{Z_0\sqrt{n-1}}{\omega_0}$	$L_{\beta 1} = L_\alpha$	$L_{\gamma 2} = L_\alpha$
$C_{\alpha 1} = \frac{1}{\omega_0^2 L_\alpha}$	$L_{\beta 2} = M_\beta$	$C_{\gamma 1} = C_{\alpha 1}$
$C_{\alpha 2} = \frac{n L_\alpha}{Z_0^2 + \omega_0^2 L_\alpha^2}$	$C_{\beta 1} = C_{\alpha 1}$	$C_{\gamma 2} = \frac{1}{\omega_0^2 L_{\gamma 1}}$
$R_\alpha = Z_0$	$C_{\beta 2} = C_{\alpha 2}$	$C_{\gamma 3} = C_{\alpha 2}$
	$R_\beta = R_\alpha$	$R_\gamma = R_\alpha$

Fig. 22. S-parameters of (a) design α, (b) design β, (c) design γ, and (d) design ψ. Black line: RL. Dashed line: IL. Gray line: isolation.

situations will be presented: an n-way power divider and PAs in a phased-array.

An n-way version of the lumped-element combiner from Fig. 1(b), along with SICC and DNICC-based variants, is shown in Fig. 21 with design equations in Table VI. Each pair of input branches can utilize an SICC or

a DNICC to reduce the required circuit area in the same manner as Designs A and C. S-parameters simulations of the three combiners in a four-way configuration are plotted in Fig. 22, where $Z_0 = 50\ \Omega$ and $k = 0.8$.

Phased arrays, and other circuits that use arrays of identical PAs, expend a significant amount of circuit area on the dc feed inductances for each PA. The number of dc feed inductances can be halved by replacing each pair of dc feed inductances with a DNICC as in Design ψ in Fig. 21. Design equations are given in (13) and (14) with simulated S-parameters of an ideal circuit plotted in Fig. 22 where $Z_{\psi 1} = 10\ \Omega$, $Z_{\psi 2} = 50\ \Omega$, and $k = 0.6$

$$(C_{\psi 1}, C_{\psi 2}) = \left(\frac{1}{\omega_0^2 L_{\psi 2}}, \frac{1}{\omega_0\sqrt{Z_{\psi 1}Z_{\psi 2} - Z_{\psi 1}^2}} \right) \quad (13)$$

$$L_{\psi 1} = C_{\psi 2} Z_{\psi 1}^2 + \frac{1}{\omega_0^2 C_{\psi 2}} \quad (14)$$

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