An Ultra-Wideband Fast Frequency Ramp Synthesizer at 60 GHz With Low Noise Using a New Loop Gain Compensation Technique

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***Abstract*— Phase-locked loops (PLLs) for ultra-wideband, low noise, and linear frequency ramp synthesis exhibit a wide variation of the loop gain, if no compensation method is applied. This impairs the performance of the PLL and the corresponding microwave measurement systems. To overcome the disadvantages of existing compensation techniques, we present a new compensation method based on a phase-frequency detector gain modulation. This offers low hardware complexity and avoids additional noise. Furthermore, we present an ultra-wideband, low noise monolithic microwave-integrated circuit for 60-GHz PLLs. Based on this, a 60-GHz frequency synthesizer with a modulation bandwidth of 22 GHz and a jitter of less than 79 fs at the center frequency are realized. The new compensation technique reduces the variation of the loop gain from 14.2:1 to 1.67:1 and is compared with an existing compensation technique utilizing a voltage-dependent damping network, which reduces the variation of the loop gain to 1.78:1. Due to the reduction of the variation of the loop gain, the maximum ramp slope increases from 22 GHz/2.9 ms up to 22 GHz/0.35 ms. In addition, the time jitter of the output signal of the PLL decreases by up to 18%. Furthermore, the PLL performance is constant in the temperature range from 0 °C to 70 °C.**

***Index Terms*— Closed-loop systems, microwave circuits, millimeter-wave radar, phase-frequency detector (PFD), phase-locked loops (PLLs), voltage-controlled oscillators (VCOs).**

I. Introduction

MICROWAVE measurement systems based on linear frequency ramps offer a high resolution, precision, and accuracy. Well-known applications for the linear frequency-modulated continuous-wave (FMCW) measurement principle are distance and velocity measurements by means of FMCW radar systems [1] as well as fast vector network analysis [2]. Moreover, this measurement principle can also be applied for various applications, such as material characterization [3], biomedical sensing [4], or plasma diagnostics [5]. The bandwidth, phase noise, and ramp linearity of the microwave measurement signal are the limiting factors for the system performance in terms of resolution, precision, and accuracy [6], [7].

The phase-locked loop (PLL) is the most appropriate and widely used approach for microwave frequency synthesizers in such measurement systems. It offers the generation of ultra-wideband, low noise, and highly linear microwave frequency ramps. There are two possibilities to obtain a frequency ramp at the output of a PLL. On the one hand, a frequency ramp can be applied as a reference signal [8]. On the other hand, the division factor in the feedback loop of the PLL can be modulated [9], [10]. In any case, increasing the bandwidth is beneficial regarding a high system performance. However, this causes several challenges concerning the microwave circuit design. The realization of a wideband voltage-controlled oscillator (VCO) is one major issue. Since wideband VCOs exhibit a high variation of the VCO gain over the output frequency [10], [11], which is increasing with the tuning range, the loop gain of the PLL also varies in a wide range over the output frequency. Thus, the loop filter design can only be optimized for a small range of the output frequency, which is typically close to the center frequency. The loop bandwidth and phase margin of the PLL varies over the output frequency [10], which leads to a reduced phase noise performance outside of the small optimized frequency range [12]. Furthermore, this decreases the maximum ramp slope of the total PLL [13].

In research, three techniques to compensate the variation of the loop gain and thus reduce the mentioned drawbacks are already applied to PLL-based wideband frequency ramp synthesizers. Fig. 1 shows the first technique, which is described in detail in [10]. This so-called offset PLL utilizes an additional local oscillator and mixer in the feedback loop of the PLL. By this means, the output frequency of the VCO is downconverted in reverse frequency position before it is applied to the frequency divider. Therefore, an increasing

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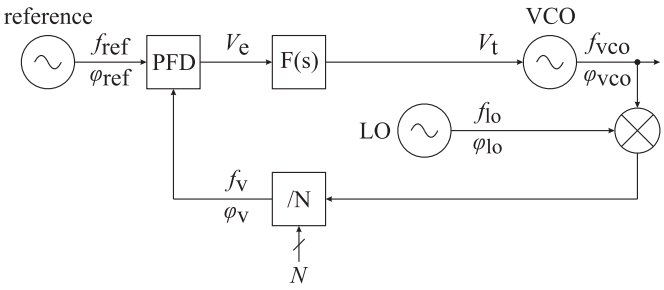

Fig. 1. Block diagram of the offset PLL with a downconversion of the PLL output signal in reverse frequency position to compensate the variation of the loop gain.

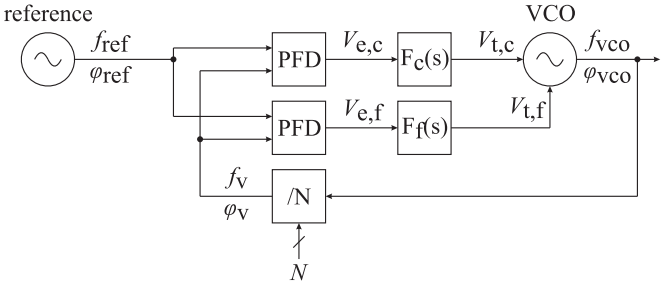

Fig. 2. Block diagram of the PLL with a dual-loop structure to compensate the variation of the loop gain.

division factor N causes a decreasing output frequency. If the division factor is modulated in order to generate a frequency ramp, the modulation is now contrary to the variation of the VCO gain and reduces the loop gain variation. Besides this, the division factor is reduced, which additionally increases the phase noise performance. However, the profile of this compensation is not adjustable to different profiles of VCO gain variations. Moreover, this technique can only be applied if the frequency ramp is generated by a division factor modulation. If the reference signal is a frequency ramp, this technique cannot be applied or has no effect, respectively. Furthermore, the additional local oscillator also requires a dedicated, second PLL. Thus, the hardware effort and complexity as well as the power consumption increase remarkably, especially in the case of systems with multiple synthesizers, such as an MIMO radar.

The second technique is shown in Fig. 2 and described in detail in [14] and [15]. It utilizes two feedback paths to the VCO and thus creates a dual-loop structure. While the wideband integral path with the loop filter $F_c(s)$ is used for coarse tuning, the narrowband proportional path with the loop filter $F_f(s)$ is used for fine tuning. This technique enables a good and adjustable compensation of the loop gain for different VCO designs. However, it requires an advanced VCO design with two tuning mechanisms and inputs. This is usually only available if a dedicated VCO is designed. Although one phase-frequency detector (PFD) with two charge pumps instead of two entire PFDs can be used, the additional hardware effort is still considerable.

Fig. 3 shows the third technique, as described in [12] and [16]. It introduces a voltage-dependent damping network (VDDN) between the output of the loop filter and the tuning input of the VCO. The VDDN consists of cascaded diodes, which are parallel to resistors. This results in a voltage-dependent voltage divider. However, the transfer function of

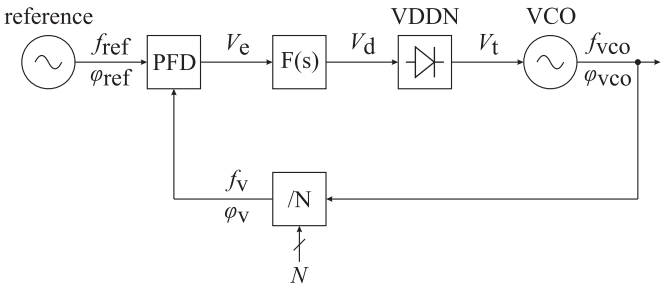

Fig. 3. Block diagram of the PLL with a VDDN to compensate the variation of the loop gain.

the VDDN is not stepped. Instead, it is smoothed by the exponential characteristic of the diodes. Thus, this technique enables a wide adjustability of the compensation to different profiles of VCO gain variations. In any case, an active loop filter with a reasonably higher supply voltage is required compared to the case without VDDN. Besides the need for an additional high supply voltage with low noise, only operational amplifiers exhibiting a higher noise contribution are applicable.

Furthermore, a technique to adjust the transfer function of the PLL components to different output frequencies in case of static frequencies is already known. For this purpose, a charge pump with a programmable output current is used as described in [17] and [18]. By programming the output current contrary to the VCO gain variation, a compensation of the loop gain over the output frequency can be achieved. However, the hardware effort and complexity would increase remarkable, as the charge pump current has to be controlled and programmed by an additional external logic. Especially for frequency ramps, this would require a very fast logic. Moreover, the modulation of the charge pump current is usually realized by switching different current sources. Thus, the output current can exhibit spurious during a frequency ramp, which could influence the linearity of the ramp. In general, a PLL with a combination of bipolar PFD and active loop filter but without charge pump can achieve a better noise performance than a PLL with a charge pump, which holds especially true for fractional-N PLLs [19].

In [20], we basically presented the concept of our new approach to compensate the loop gain variation overcoming the disadvantages of the existing concepts and simulated a 60-GHz PLL based on the measured characteristics of single components. In Section II, we expand the concept by detailed theoretical background. In Section III, we present the monolithic microwave-integrated circuit (MMIC)-based components for an ultra-wideband 60-GHz synthesizer, which is used to demonstrate the new compensation technique. Compared to [20], these components are improved, especially concerning the modulation bandwidth, and characterized by new and more detailed measurements. In our previous work, only final simulation results of the PLL with our new compensation technique are presented, whereas, in Section IV, we describe the simulation-aided design of the PLL and the compensation based on the new approach as well as on a VDDN in detail. This is supported by the measurements of the compensation network (CN) and VDDN. In Section V, we present and discuss the obtained results of the realized synthesizer and

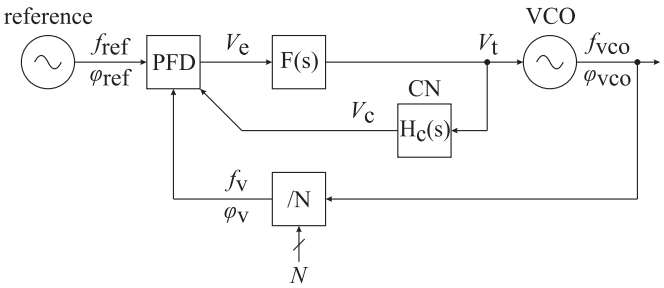

Fig. 4. Block diagram of the PLL with the new approach for the compensation of the loop gain variation.

the compensation. This includes loop gain, frequency ramp, and phase noise measurements.

II. Concept

Concerning a commonly known single-loop PLL, the loop gain $G_{\text{loop}}(s)$ and the transfer function $\varphi_{\text{VCO}}(s)/\varphi_{\text{ref}}(s)$ in the frequency domain are

$$G_{\text{loop}}(s) = \frac{K_{\text{VCO}} \cdot K_{\text{PFD}} \cdot \text{F}(s)}{N \cdot s} \tag{1}$$

$$\frac{\varphi_{\text{VCO}}(s)}{\varphi_{\text{ref}}(s)} = \frac{N \cdot G_{\text{loop}}(s)}{1 + G_{\text{loop}}(s)} \tag{2}$$

where N is the division factor of the frequency divider, F(s) is the transfer function of the loop filter, K_{VCO} is the VCO gain, and K_{PFD} is the PFD gain. This small-signal model assumes a linearized and constant VCO gain K_{VCO}. However, in wideband PLLs, the VCO gain K_{VCO} is not constant over the output frequency, as described in Section I. Moreover, also N may vary over the output frequency if a frequency ramp is generated by division factor modulation. Thus, (2) and (2) are depending on the output frequency f_{VCO}.

The essential idea of the proposed new compensation technique is the modulation of the PFD gain K_{PFD} contrary to the variation of the loop gain without compensation. This means the modulation of K_{PFD} is contrary to the variation of the factor K_{VCO}/N over the output frequency. Therefore, the PFD offers an additional input for the voltage V_c, which controls the PFD gain K_{PFD} in a linear way

$$K_{\text{PFD}} = K_{\text{PFD},0} + \Delta K_{\text{PFD}} \cdot V_c. \tag{3}$$

In order to modulate the PFD gain as desired, the VCO gain K_{VCO} and the division factor N have to be known precisely. The relation between K_{VCO}, N, and the output frequency f_{VCO} can be measured and is well known in advance. Moreover, the output frequency f_{VCO} is directly related to the tuning voltage V_t. Thus, we use the tuning voltage in combination with a CN with the transfer function $H_c(s)$ to generate the PFD gain control voltage V_c. This introduces a second feedback loop in the PLL, as shown in Fig. 4. Admitting CN to be nonlinear, we can compensate an almost arbitrary variation of the loop gain.

However, numerous wideband VCOs exhibit a VCO gain, which can be approximated by

$$K_{\text{VCO}} = K_{\text{VCO},0} + \frac{\Delta K_{\text{VCO}}}{V_t} \tag{4}$$

which is due to the typical characteristic of a varactor [21]. It can be observed, e.g., in [10] and [11] as well as in Section III.

This is beneficial, as (5) and (4) are multiplied in (2). Thus, the realization of CN as a simple linear network generating

$$V_c = V_{c,0} + \Delta V_c \cdot V_t \tag{5}$$

results in a factor

$$G_{\text{PV}} = K_{\text{PFD}} \cdot K_{\text{VCO}} = G_0 + G_1 \cdot V_t + G_2 \cdot {V_t}^{-1} \tag{6}$$

with

$$G_0 = K_{\text{VCO},0} \cdot (K_{\text{PFD},0} + \Delta K_{\text{PFD}} \cdot V_{c,0}) + \Delta K_{\text{VCO}} \cdot \Delta K_{\text{PFD}} \cdot \Delta V_c \tag{7}$$

$$G_1 = K_{\text{VCO},0} \cdot \Delta K_{\text{PFD}} \cdot \Delta V_c \tag{8}$$

$$G_2 = \Delta K_{\text{VCO}} \cdot (K_{\text{PFD},0} + \Delta K_{\text{PFD}} \cdot V_{c,0}). \tag{9}$$

In the case without the new compensation technique, G_{PV} would be equal to the multiplication of (4) with a constant factor $K_{\text{PFD},0}$. Thus, it would consist of a constant as well as an inversely proportional part and exhibit the same variation as the VCO gain. However, in the case of the new compensation technique according to (6), G_{PV} consists of a constant (G_0), an inversely proportional (G_2), and a proportional (G_1) part due to the modulation of the PFD gain. As a result, (6) exhibits the minimum

$$G_{\text{PV,min}} = G_0 + 2 \cdot (G_1 \cdot G_2)^{1/2} \tag{10}$$

and the maximum

$$G_{\text{PV,max}} = G_0 + G_1 \cdot V_{t,\text{max/min}} + G_2 \cdot {V_{t,\text{max/min}}}^{-1} \tag{11}$$

where it depends on the parameters G_1 and G_2 of the realized PLL, whether the minimum tuning voltage $V_{t,\text{min}}$ or the maximum tuning voltage $V_{t,\text{max}}$ has to applied to (11). The proportional part in (6) can be used to minimize the influence of the inversely proportional part by optimizing the parameters of the CN $V_{c,0}$ and ΔV_c. Therefore, the corresponding optimization problem is

$$\min \left\{ \frac{G_{\text{PV,max}}(V_{c,0}, \Delta V_c)}{G_{\text{PV,min}}(V_{c,0}, \Delta V_c)} \,|\, 0 \le \Delta V_c \le 1 \wedge (V_{c,\text{min}} - \Delta V_c \cdot V_{t,\text{min}}) \le V_{c,0} \le V_{t,\text{min}} \right\}. \tag{12}$$

Theoretically, the constant part of the CN is not required ($V_{c,0} = 0$) to minimize $G_{\text{PV,max}}/G_{\text{PV,min}}$. However, the input of the control voltage of a realized PFD will always require a certain minimum $V_{c,\text{min}}$. This is ensured with a constant offset voltage $V_{c,0} \ge (V_{c,\text{min}} - \Delta V_c \cdot V_{t,\text{min}})$. The conditions $V_{c,0} \le V_{t,\text{min}}$ and $0 \le \Delta V_c \le 1$ in (12) allow for a passive realization of CN. If a more complex, active realization of CN is affordable, the boundaries of these conditions could be chosen different according to the properties of the desired components of CN.

However, the stability investigations for the complete PLL are impeded by the second feedback loop. The tuning voltage

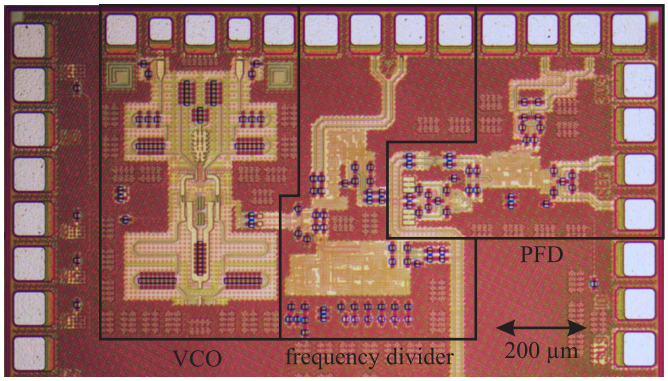

Fig. 5. Photograph of the realized MMIC, including a VCO, a PFD, as well as a frequency divider.

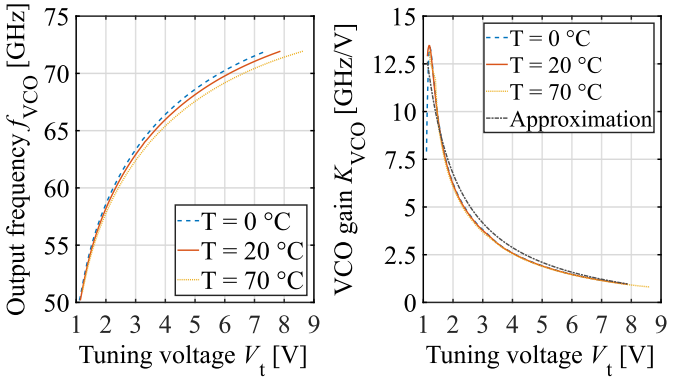

Fig. 6. Measured tuning curve of the VCO (left) and deviated VCO gain K_{VCO} (right) at different temperatures.

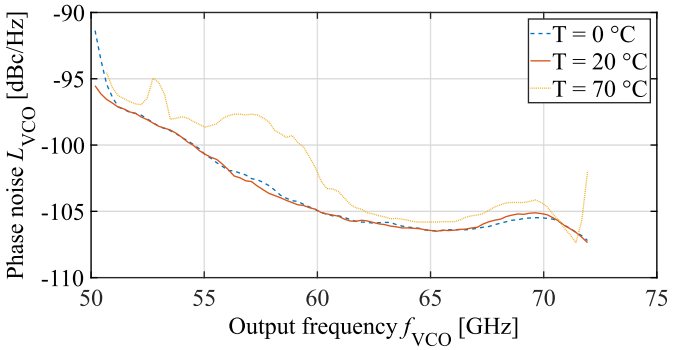

Fig. 7. Measured phase noise of the free running VCO at an offset frequency from the carrier of $\Delta f = 1$ MHz as a function of the output frequency f_{VCO} at different temperatures.

cannot be expressed in closed form

$$V_t(s) = \mathrm{F}(s) \cdot [K_{\mathrm{PFD},0} + \Delta K_{\mathrm{PFD}} \cdot H_c(s) \cdot V_t(s)] * \left[\varphi_{\mathrm{ref}}(s) - \frac{K_{\mathrm{VCO},0} \cdot V_t(s) + \Delta K_{\mathrm{VCO}}}{N \cdot s}\right] \quad (13)$$

as the input value is multiplied with the feedback value of the second loop. This nonlinear feedback loop prohibits a general closed-form solution [22]. Thus, we implemented a simulator to investigate the stability of the PLL numerically. The simulator is based on MATLAB and Simulink and simulates the PLL in the time domain. The simulation model uses the block diagrams and signals in Figs. 1, 3, and 4, depending on which compensation technique is applied. The VCO consists of a lookup table to model the nonlinear VCO gain and an integrator. A subtractor and a variable gain stage are the basic model elements of the PFD. The model of the frequency divider is a gain stage with a gain of $1/N$. The loop filter is modeled using its transfer function $\mathrm{F}(s)$. For the compensation techniques, CN and VDDN are implemented as lookup tables. However, these are only the basic model elements and more elements are included to model the entire behavior of the single components.

III. Components Realization

We designed an MMIC for an ultra-wideband 60-GHz PLL utilizing our new loop gain variation compensation technique. It is implemented in Infineon's SiGe:C BiCMOS technology B11HFC offering $f_t/f_{\max} = 250/370$ GHz [23]. Fig. 5 shows the photograph of the realized MMIC. It contains an improved VCO, a PFD, as well as a feedback loop frequency divider. Furthermore, all components are fully differential.

In order to obtain a high tuning range in combination with low phase noise, the VCO is based on a fully differential Colpitts architecture with a double varactor and a cascode stage, as shown in [10]. The output frequency f_{VCO} can be continuously tuned in the range from 50 to 72 GHz, as shown in Fig. 6. The obtained absolute tuning range of $B_{VCO} = 22$ GHz corresponds to a high relative tuning range of $B_{VCO,rel} = 36\%$. In addition, the VCO offers a low phase noise L_{VCO}, as shown in Fig. 7. At room temperature ($T = 20$ °C), it is below -95 dBc/Hz over the entire output frequency range and -105 dBc/Hz at the center frequency. Concerning a temperature range from 0 °C to 70 °C, the VCO's phase noise increases by a maximum of 5 dB over the entire output frequency range. However, the VCO exhibits a high variation of the VCO gain $K_{VCO,max}/K_{VCO,min}$ of 14.2:1. Fig. 6 shows that it can increase to a maximum of 16.3:1 in the temperature range from 0 °C to 70 °C. The parameters for the suggested approximation in (4) can be extracted with $K_{VCO,0} = -1$ GHz/V and $\Delta K_{VCO} = 15.5$ GHz. Applying these parameters to (4) results in an approximation, which is in good agreement with the measurements, as shown in Fig. 6.

The architecture of the PFD is comparable to [1] and implemented in emitter-coupled logic to handle high input frequencies [24]. This is beneficial concerning the phase noise performance due to a lower frequency division factor N and, in case of fractional operation, due to the very high PFD linearity. Moreover, we extended the PFD by a modified output stage. It is shown in Fig. 8 and allows for the modulation of the PFD gain. The control voltage V_c directly modulates the reference current of the output stage. Thus, the output voltage V_e and the PFD gain K_{PFD} are related very linearly to the control voltage V_c. This output characteristic is shown in Fig. 9, where the parameters for (5) can be extracted with $K_{PFD,0} = -0.6/(2\pi)$ V · rad^{-1} and $\Delta K_{PFD} = 0.66/(2\pi)$ rad^{-1}, concerning room temperature. In the temperature range from 0 °C to 70 °C, the PFD gain K_{PFD} varies only by a maximum of $0.066/(2\pi)$ V · rad^{-1}.

The utilized frequency divider is also implemented in emitter-coupled logic and described in detail in [25].

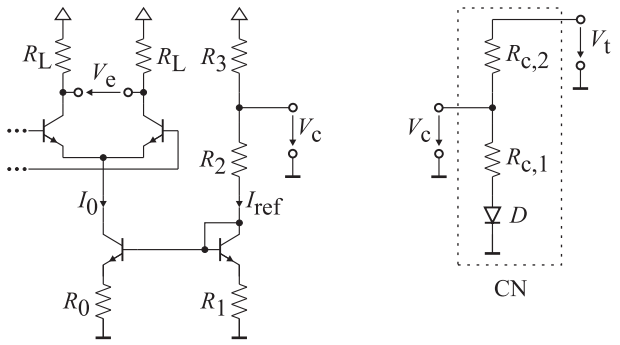

Fig. 8. PFD output stage for a modulation of the PFD gain (left) and CN realized as a resistive voltage divider with a diode in series to generate a constant offset voltage (right).

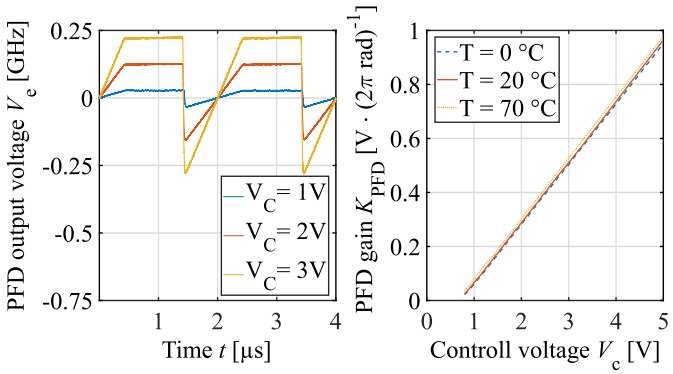

Fig. 9. Left: measured, low pass filtered output voltage of the PFD V_d with $f_{ref} = 425$ MHz and $f_v = f_{ref} - 1$ MHz at different, exemplary control voltages V_c. Right: deviated PFD gain K_{PFD} as a function of the control voltage V_c at different temperatures.

It operates at input frequencies up to 80 GHz and is fully programmable in the range of $12 \leq N \leq 259$. Moreover, it offers the capability for fractional modulation as well as synchronizing of multiple PLLs.

The architecture of the generator of the reference signal f_{ref} is based on [12]. It consists of the same frequency divider as in the feedback loop of the PLL, which is fed by an input signal with a fixed frequency of $f_0 = 20$ GHz, and a digital logic to control the division factor R. Since the reference frequency is

$$f_{ref} = \frac{f_0}{R}, \quad 12 \leq R \leq 259 \tag{14}$$

it offers a wide frequency range from 77 MHz to 1.6 GHz. In general, this concept enables a very high relative bandwidth of the reference signal

$$B_{ref,rel} = 2 \cdot \frac{R_{max} - R_{min}}{R_{max} + R_{min}} = 189\%. \tag{15}$$

We use this generator with a $\Sigma\Delta$-modulated division factor R in order to generate a frequency ramp reference signal. The further advantages are the $20\log_{10}(R)$ reduced phase noise and the binary output signal. Thus, the reference signal can be distributed to multiple PLLs with moderate effort.

IV. PLL and Compensation Design

In this PLL, we use an active differential third-order loop filter applying the operational amplifier LT6200, due to its excellent noise performance. As our own designed PFD enables high reference frequencies, the division factor of the feedback loop is chosen to be $N = 128$. This results in a reference frequency f_{ref} in the range of 390.6–562.5 MHz. Applying the measurement results of the microwave components presented in Section III, we designed and analyzed the PLL in detail utilizing our MATLAB-based simulator. The simulator is able to consider VCO gain variations as well as the three discussed loop gain compensation techniques in Figs. 1, 3, and 4. The PLL is optimized at the design frequency $f_{VCO,d} = 60$ GHz with respect to the best phase noise performance in terms of the minimal jitter. This results in a loop bandwidth of $B_{loop} = 1.5$ MHz. In order to ensure high ramp slopes, we choose a phase margin of $\Delta\phi_{loop} = 55°$. To ensure comparability, the PFD gain K_{PFD} of the PLL without and with compensation is equal at the design frequency. Thus, the loop filter design as well as the PLL performance at $f_{VCO,d} = 60$ GHz are equal for the PLL without and with the compensation. Figs. 10 and 11 show the resulting phase noise L and loop gain G_{loop} as a function of the offset frequency from the carrier Δf, respectively.

The shape of the loop gain magnitude $|G_{loop}(j2\pi\Delta f)|$ is independent of the PLL's output frequency. Thus, we will describe the loop gain variation over the output frequency f_{VCO} and the effect of the compensation at a fixed offset frequency from the carrier $\Delta f = 100$ kHz. Without any

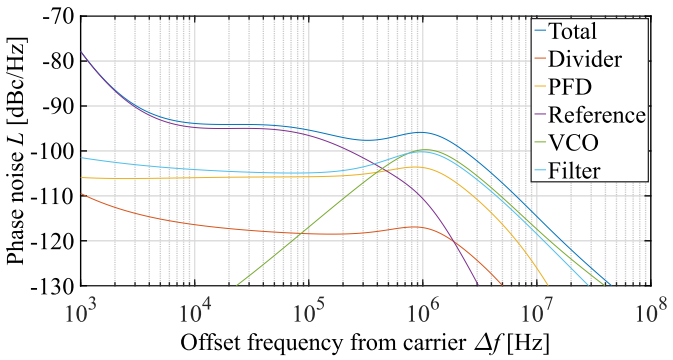

Fig. 10. Simulated contributions and total phase noise L of the PLL as a function of the offset frequency from the carrier Δf at the design output frequency $f_{VCO,d} = 60$ GHz.

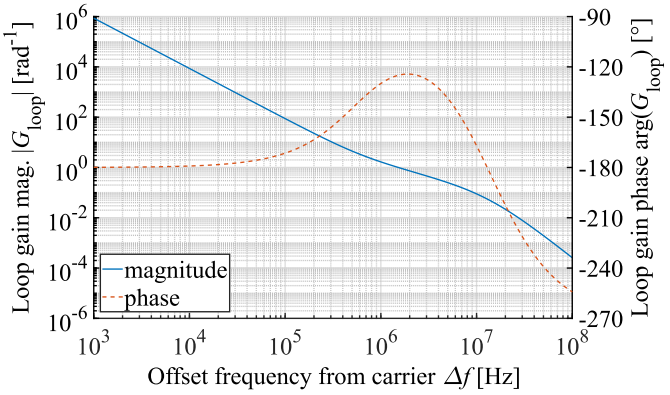

Fig. 11. Simulated magnitude and phase of the loop gain G_{loop} of the PLL as a function of the offset frequency from the carrier Δf at the design output frequency $f_{VCO,d} = 60$ GHz.

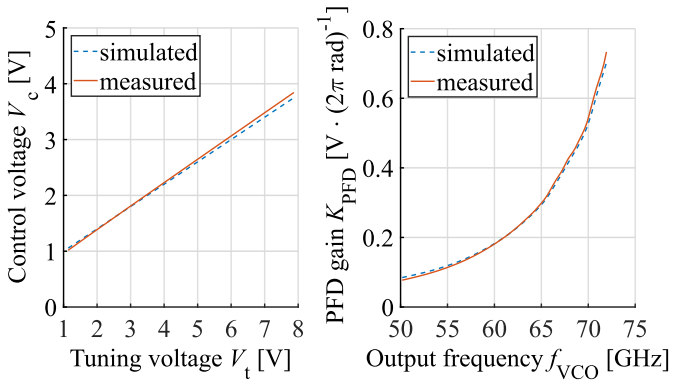

Fig. 12. Simulated and measured characteristic of the CN (left) as well as the resulting modulation of the PFD gain K_{PFD} as a function of the output frequency f_{VCO} (right).

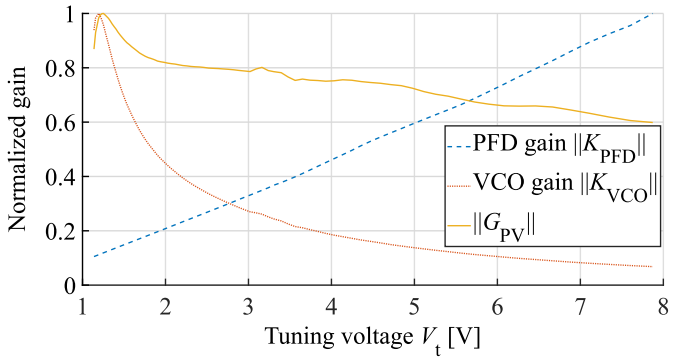

Fig. 13. Measured, normalized PFD gain $||K_{PFD}||$ and normalized VCO gain $||K_{VCO}||$ as well as the calculated factor $||G_{PV}|| = ||K_{PFD} \cdot K_{VCO}||$ of the PLL with the new compensation technique as a function of the tuning voltage V_t.

compensation, the variation of the loop gain equals the variation of the VCO gain of 14.2:1 at room temperature.

In order to compensate this high loop gain variation, we insert the linear feedback network CN for the PFD control voltage V_c as proposed in Section II. It consists of a single diode and two resistors, as shown in Fig. 8. The diode creates the constant offset voltage $V_{c,0}$ corresponding to its threshold voltage, whereas the resistors realize a resistive voltage divider to set the factor ΔV_c, with which the tuning voltage V_t is fed back to the PFD control voltage V_c. In order to compensate the loop gain appropriate, we designed CN according to (12) resulting in

$$V_c(t) = 0.7\text{V} + 0.43 \cdot V_t(t). \tag{16}$$

Fig. 12 shows the measured characteristic of this network, which is in good agreement with the simulation. However, the offset voltage and the voltage division ratio have to be optimized according to (12) for each VCO design with its characteristic tuning curve. Therefore, other diode types with different threshold voltages or a cascade of diodes can be used, and the ratio of the resistors $R_{c,1}$ and $R_{c,2}$ can be changed.

Fig. 13 shows the normalized PFD gain $||K_{PFD}||$ and the normalized VCO gain $||K_{VCO}||$ of the PLL with the new compensation technique as a function of the tuning voltage V_t. As a result of the PFD gain modulation and optimization of CN, the relative variation of the calculated factor $||G_{PV}|| = ||K_{PFD} \cdot K_{VCO}||$ for the PLL with the new compensation technique is reduced by a factor of 8.8 compared to the one without compensation technique. The latter would be equal to the normalized VCO gain.

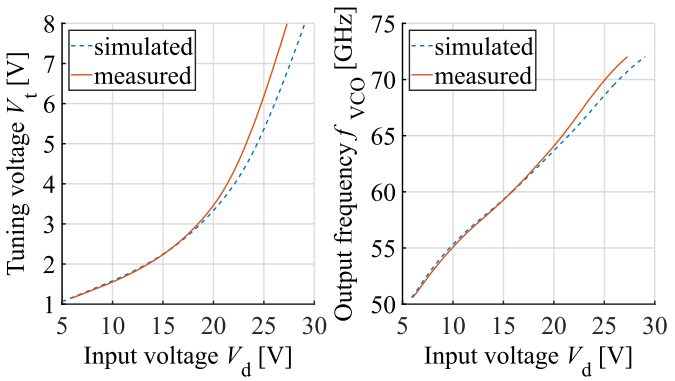

Fig. 14. Simulated and measured characteristic of the VDDN (left) as well as the resulting tuning curve of the VCO (right).

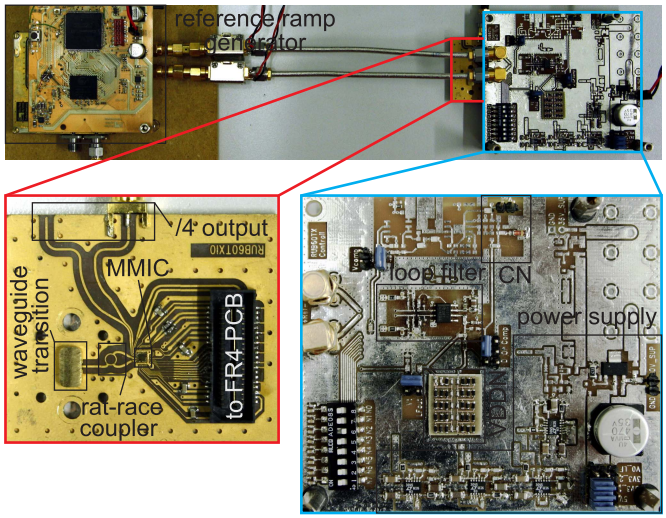

Fig. 15. Top: photograph of the synthesizer. Bottom left: detailed photograph of the RT5880 substrate. Bottom right: detailed photograph of the FR4 PCB.

Furthermore, we also designed a VDDN for comparison of the compensation of the loop gain. In this case, an appropriate compensation requires nine stages, each with three diodes parallel to one resistor. The resistor values are distributed logarithmically over the stages. This results in an exponential transfer function of the VDDN and approximates the inverse function of the tuning curve in Fig. 6. The measured and simulated characteristic of the VDDN is shown in Fig. 14. The deviation of measurement and simulation at high input voltages V_d are caused by an insufficient model of the single diodes, which was delivered by the manufacturer. However, the VDDN requires a maximum input voltage of $V_{d,\max} = 27.3$ V, which is 3.4 times higher than the maximum tuning voltage. Thus, the supply voltage of the loop filter must be increased by the same factor and we had to use the THS4031 instead of the LT6200. The THS4031 has a higher maximum supply voltage but exhibits a slightly decreased noise performance ($V_{\text{noise,LT6200}} = 0.9$ nVHz$^{-1/2}$ and $V_{\text{noise,THS4031}} = 1.6$ nVHz$^{-1/2}$).

Fig. 15 shows a photograph of the synthesizer consisting of the reference ramp generator, a Rogers RT/duiroid 5880

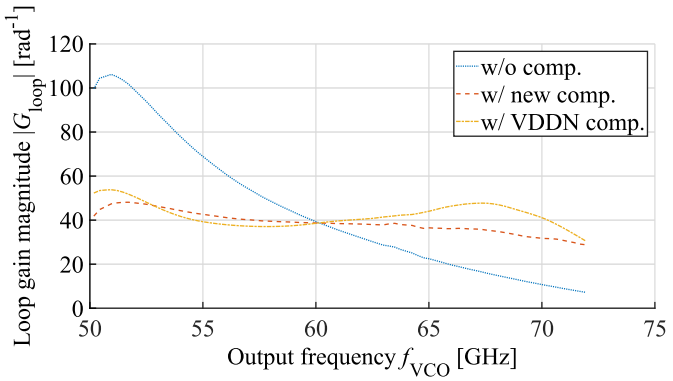

Fig. 16. Loop gain magnitude as a function of the output frequency f_{VCO} at an offset frequency from the carrier of $\Delta f = 100$ kHz for the PLL without a compensation, the PLL with the new compensation, and the PLL with VDDN compensation.

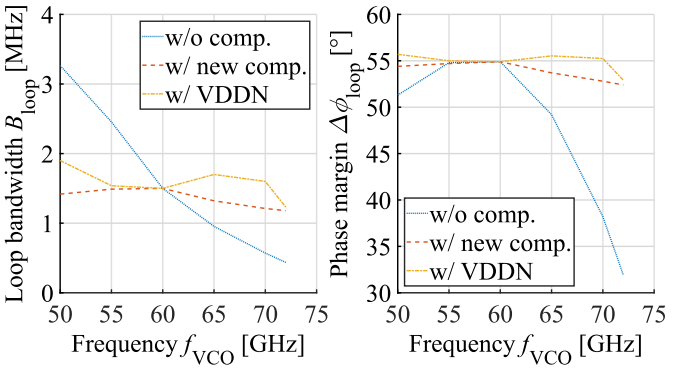

Fig. 17. Loop bandwidth B_{loop} (left) and phase margin $\Delta\phi_{loop}$ (right) as a function of the output frequency f_{VCO} for the PLL without a compensation technique, the PLL with the new compensation, and the PLL with VDDN compensation.

substrate, and an FR4 printed circuit board (PCB). The MMIC is embedded in the RT/duiroid 5880 substrate and connected via a rat-race coupler and microstrip-to-waveguide transition to a waveguide. Furthermore, it exhibits a dedicated divide-by-4 output to perform precise and accurate phase noise measurements. The FR4 PCB contains the power supply, the loop filter, the CN for the new compensation technique, as well as the VDDN.

V. Results

Fig. 16 shows the loop gain magnitude $|G_{loop}|$ as a function of the output frequency f_{VCO} in case of the PLL without any compensation, utilizing the new compensation technique and the VDDN, respectively. The new compensation technique reduces the loop gain variation from 14.2:1 to 1.67:1, whereas the VDDN reduces it to 1.79:1. This corresponds to a reduction by a factor of 8.5 and 8. The factor of the reduction of the loop gain variation with the new compensation technique is in good agreement with the reduction of the variation of the calculated factor $||G_{PV}||$ from Fig. 13.

As described in Section I, the loop gain variation directly affects the phase margin $\Delta\phi_{loop}$ and loop bandwidth B_{loop} of the PLL. Fig. 17 shows the actual loop bandwidth and phase margin as a function of the output frequency. This has an impact on the loop stability and the maximum ramp slope, as well as the phase noise performance.

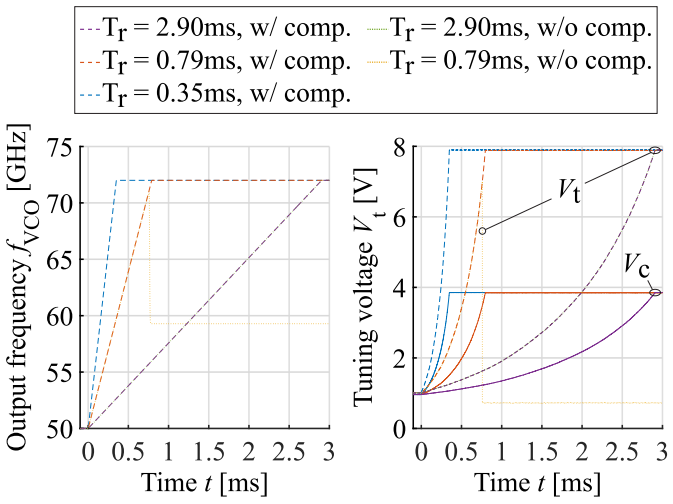

Fig. 18. Measured output frequency f_{VCO} (left) and tuning voltage V_t as well as PFD gain control voltage V_c (right) as a function of the time t for the PLL without a compensation and the PLL with the new compensation technique, while generating frequency ramps with a modulation bandwidth of $B_r = 22$ GHz and different sweep times T_r.

First, the loop bandwidth and the phase margin variation limit the maximum ramp slope B_r/T_r for a stable frequency ramp. In the case of the uncompensated PLL, the sweep time has to be at least $T_r \geq 2.9$ ms for the maximum modulation bandwidth of the output frequency $B_r = 22$ GHz. However, the phase margin of the PLL without any compensation cannot be chosen smaller than $\Delta\phi_{loop,d} = 55°$ at the design frequency $f_{VCO,d} = 60$ GHz, because, for stability reasons, it has to be at least $\Delta\phi_{loop} \geq 30°$ over the entire output frequency range 50 GHz $\leq f_{VCO} \leq$ 72 GHz [13]. If the loop gain variation compensation is applied, the minimum sweep time is reduced to $T_{r,min} = 0.79$ ms for the maximum modulation bandwidth. Moreover, in the case of the PLL with compensation, we could reduce the phase margin to $\Delta\phi_{loop,d} = 40°$ at the design frequency, which is not feasible without any compensation. This results in a minimum sweep time of $T_{r,min} = 0.35$ ms. This corresponds to a reduction by a factor of 3.6 and 8.3, respectively.

Generating linear frequency ramps with the maximum modulation bandwidth $B_r = 22$ GHz, but different sweep times T_r, results in the transient output frequency f_{VCO} (measured with R&S FSWP), tuning voltage V_t, and PFD gain control voltage V_c, as shown in Fig. 18. It can be observed that the PLL without any compensation unlocks at sweep times $T_r <$ 2.9 ms, as exemplary shown for $T_r = 0.79$ ms, whereas the PLL with the new compensation technique can appropriately operate down to sweep times $T_r = 0.35$ ms. Fig. 19 shows the frequency error f_e between an ideal frequency ramp and the frequency ramp measured with a video bandwidth of 100 kHz. Ignoring the first 5% of each frequency ramp, we calculated the corresponding rms frequency error $f_{e,rms}$. In the case of a sweep time of $T_r = 2.9$ ms, the PLL without compensation and the PLL with the new compensation technique offer a quite similar rms frequency error of $f_{e,rms} = 6.66$ kHz and $f_{e,rms} = 6.63$ kHz, respectively. For shorter sweep times, the frequency error increases, which results in rms frequency errors of $f_{e,rms} = 20.1$ kHz ($T_r = 0.79$ ms) and

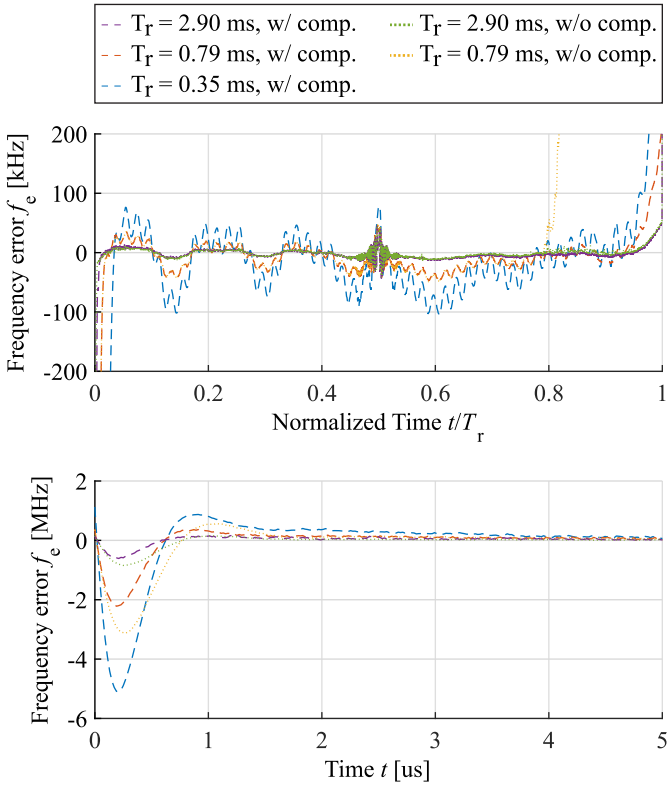

Fig. 19. Measured frequency error f_e of the entire frequency ramps as a function of the time normalized to the sweep time t/T_r (top) and measured frequency error f_e at the beginning of the ramps as a function of the time t (bottom) for the PLL without a compensation and the PLL with the new compensation technique, while generating frequency ramps with a modulation bandwidth of $B_r = 22$ GHz and different sweep times T_r.

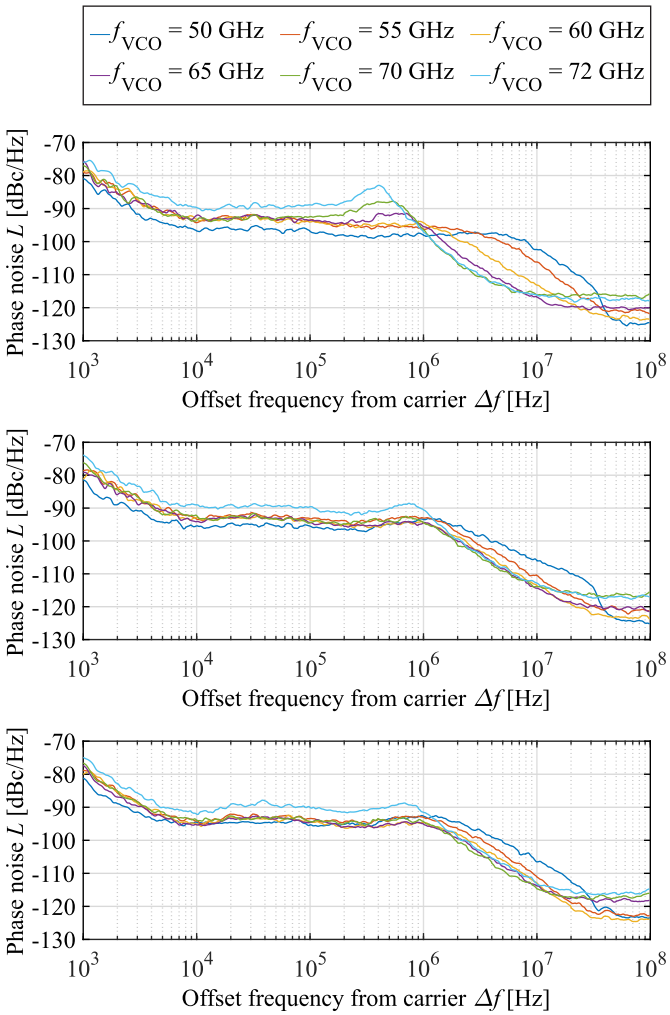

Fig. 20. Measured phase noise L of the PLL without compensation (top) as well as the PLL with new compensation by means of utilizing CN (middle) and by means of applying the control voltage V_c externally (bottom) as a function of the offset frequency from the carrier Δf at different output frequencies f_{VCO}.

$f_{e,\mathrm{rms}} = 43.8$ kHz ($T_r = 0.35$ ms) for the PLL with the new compensation technique. If the rms frequency error of the PLL without a compensation is calculated for $T_r = 0.79$ ms by ignoring the end, where it is unlocked, it reaches a value of $f_{e,\mathrm{rms}} = 22.4$ kHz. This is slightly higher, but comparable to the value of the PLL with the new compensation technique. The settling behavior of the PLL can be investigated by means of concerning the first microseconds of the frequency ramps, which were measured with a video bandwidth of 5 MHz and are shown in Fig. 19. The amplitude of the frequency error during settling increases with an increased ramp slope, corresponding to a shorter sweep time. However, the time constants of the settling are not affected by the ramp slope. Moreover, by comparing the PLL with the new compensation technique with the PLL without compensation, the settling time is slightly reduced. Neither the rms frequency error nor the settling time is increased with the new compensation technique, the dynamic behavior of the PLL is not degraded by the second nonlinear feedback loop.

However, these sweep times and ramp slopes are based on a phase noise-optimized PLL. The sweep times could be decreased if the loop bandwidth is increased by the cost of higher phase noise. In any case, a PLL with compensation allows for higher ramp slopes compared to the one without compensation. Depending on the application, a PLL with compensation allows for a design with increased phase noise performance if a certain sweep time is required.

Second, the loop bandwidth variation decreases the phase noise performance. Fig. 20 shows the phase noise of the PLL without and with compensation as a function of the offset frequency from the carrier Δf for different output frequencies f_{VCO}. In contrast to the PLL with compensation, the shape of the phase noise of the PLL without compensation strongly varies for different output frequencies. At low output frequencies, the region of constant in loop phase noise is extended to high offset frequencies due to the increased loop bandwidth. At high output frequencies, the phase noise peaks at frequencies slightly below the loop bandwidth.

To proof, that CN itself does not decrease the phase noise performance, we additionally measured the phase noise of the PLL without CN, but instead with applying V_c by an external ultra-low-noise voltage source. This voltage source generates the appropriate control voltage to modulate the PFD gain in the same way as CN according to Fig. 12. As shown in Fig. 20, the phase noise of the PLL with the new compensation technique is comparable in the case of utilizing CN and in the case of applying the control voltage V_c externally.

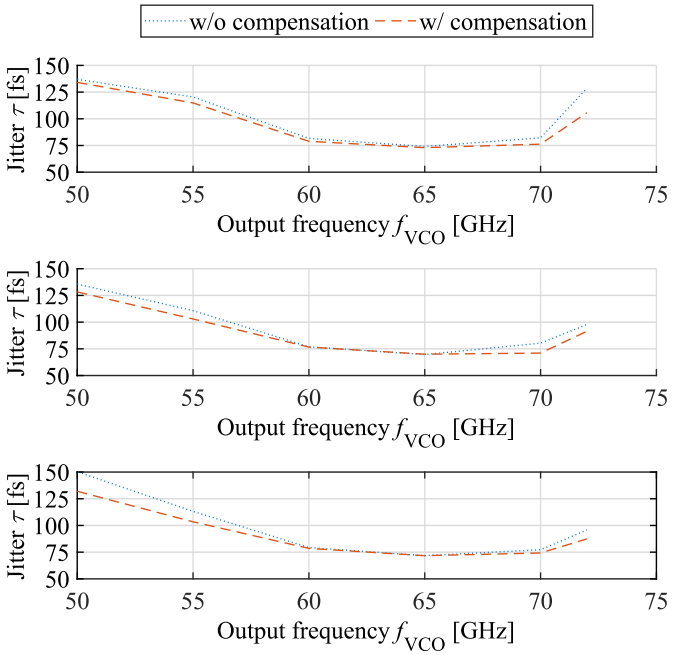

Fig. 21. Measured time jitter τ of the PLL without compensation and the PLL with new compensation technique as a function of the output frequency f_{VCO} at a temperature of $T = 0$ °C (top), $T = 20$ °C (middle), and $T = 70$ °C (bottom).

The suboptimal phase noise characteristic of the PLL without compensation results in an increased rms phase jitter $\Delta\phi_{rms}$ and time jitter τ. Fig. 21 shows the time jitter τ of the output signal as a function of the output frequency for the PLL without and with compensation. At room temperature, the jitter can be decreased by up to 12%. To demonstrate that the compensation is robust against environmental drifts, we measured the phase noise at different temperatures T. Fig. 21 shows the resulting time jitter. In the temperature range from 0 °C to 70 °C, the time jitter only deviates slightly and is smaller or equal in case of the applied compensation. Moreover, the decrease of the time jitter due to the compensation of the loop gain variation even improves to 18% near the minimum and maximum output frequency. In any case, for the design frequency $f_{VCO,d} = 60$ GHz, the time jitter is below 79 fs. The small time jitter and the high modulation bandwidth allow for highly precise and accurate microwave measurement systems.

Moreover, the phase noise performance at low output frequencies of the PLL with the new compensation technique could be increased in an improved version. As Fig. 12 shows, the PFD gain is relatively small at low output frequencies. Thus, at these frequencies, the contribution of the loop filter's noise to the total phase noise of the PLL increases as depicted in the simulated noise contributions of the PLL with the new compensation technique in Fig. 22. This is also visible in the phase noise measurement of the PLL with compensation at $f_{VCO} = 50$ GHz, as shown in Fig. 20. A possibility to solve this problem is to increase the current of the output stage of the PFD I_0, as shown in Fig. 8. This can be used to either increase the PFD gain in general or to decrease the resistor values R_L and those of the loop filter. In both the cases, the contribution of the loop filter's noise to the total phase noise of the PLL with compensation will be decreased. Thus, the advantage of the PLL with compensation compared to the one without compensation would be further increased.

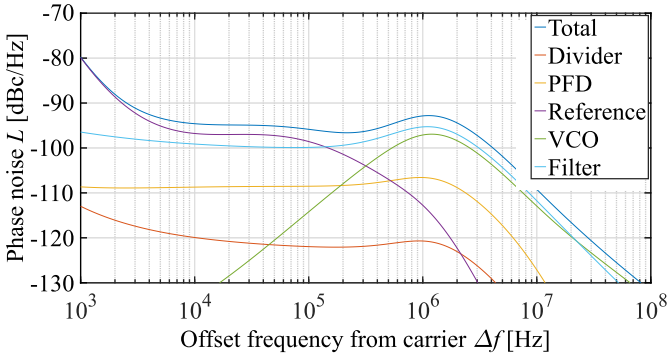

Fig. 22. Simulated contributions and total phase noise L of the PLL with the new compensation technique as a function of the offset frequency from the carrier Δf at the lower output frequency $f_{VCO} = 50$ GHz.

VI. Conclusion

We presented a new technique to compensate the variation of the loop gain in wideband PLLs. It is especially intended for frequency ramp synthesis and requires only low hardware complexity. Furthermore, we presented an MMIC for ultra-wideband, low noise 60-GHz PLLs as well as a corresponding reference ramp generator, allowing for driving and synchronizing multiple PLLs. The VCO offers a tuning range of $B_{VCO} = 22$ GHz and a phase noise of less than -95 dBc/Hz at offset frequencies of $\Delta f = 1$ MHz over the entire output frequency range. Based on this, a low noise 60-GHz frequency synthesizer has been realized for operation without compensation, with the new compensation technique, and with VDDN. We optimized the synthesizer for a design frequency of 60 GHz and achieved a time jitter of less than 79 fs. Applying our new proposed compensation technique, we reduced the variation of the loop gain from 14.2:1 to 1.67:1 and compared it to the compensation with VDDN, which is 1.79:1. The resulting loop bandwidth and phase margin of the PLLs with compensation is smooth over the entire output frequency range. This increases the maximum ramp slope from 22 GHz/2.9 ms to 22 GHz/0.79 ms for $\Delta\phi_{loop,d} = 55°$. For $\Delta\phi_{loop} = 40°$, which is not feasible without compensation, it increases further to 22 GHz/0.35 ms. Applying the new compensation technique, we demonstrated FMCW operation with these ramp slopes and measured rms frequency errors of 6.63 kHz ($T_r = 2.9$ ms), 20.1 kHz ($T_r = 0.79$ ms), and 43.8 kHz ($T_r = 0.79$ ms). The rms frequency error and the settling time are not increased compared to the uncompensated PLL. Moreover, the compensation technique reduces the time jitter of the output signal by up to 12% ($T = 20$ °C) and 18% (0 °C $\leq T \leq$ 70 °C). The time jitter at low output frequencies could be further reduced if the proposed modification is applied. Furthermore, we demonstrated that the compensation technique is robust against temperature drifts. Thus, the performance of microwave measurement systems based on the FMCW principle can be increased by the presented new compensation technique.

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