A CMOS RF-to-DC Power Converter With 86% Efficiency and −19.2-dBm Sensitivity

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***Abstract*— This paper proposes an RF-to-dc power converter for ambient wireless powering that is efficient, highly sensitive, and less dependent on the load resistance with an extended dynamic range. The proposed rectifier utilizes a variable biasing technique to control the conduction of the rectifying transistors selectively, hence minimizing the leakage current; unlike the prior work that has a fixed feedback resistors, which limits the efficient operation to a relatively high RF power and causes a drop in the peak power conversion efficiency (PCE). The proposed design is fabricated using a 0.18-μm standard CMOS technology and occupies an area of 8800 μm^2. The measurement results show an 86% PCE and −19.2-dBm (12 μW) sensitivity when operating at the medical band 433 MHz with a 100-kΩ load. Furthermore, the PCE is 66%, and the sensitivity is −18.2 dBm (15.1 μW) when operating at UHF 900 MHz with a 100-kΩ load.**

***Index Terms*— Energy harvesting, rectifier, RF–dc converter, self-bias, wireless powering.**

I. Introduction

WIRELESSLY powering electronic devices have been the goal for many researchers [1], almost since the discovery of electricity [2], [3]. The true freedom of wireless power transfer (WPT) enables compact, lightweight, and battery-less devices that can even operate while located in remote or inaccessible areas, without the fear of providing a costly wireline connection (can be physically impossible) or recharging the internal batteries (can be challenging or impossible) in the conventional approaches [3]. Recently, with the enhanced WPT techniques and the increased efficiency of the integrated circuits [4], the dream of having a simple low-power truly wireless electronic devices is becoming a reality [5].

WPT is divided into three different categories based on its powering capabilities: near-field WPT provides a few tens of watts for less than one meter of distance; microwave WPT offers milliwatts of power for a few meters of distances; ambient microwave WPT operates with microwatts range of power with unlimited range of distance (assuming within the range of an RF transmitter) [5].

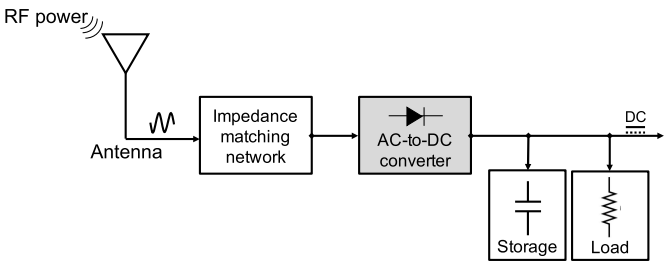

Fig. 1. Block diagram of a wireless power receiver.

Nowadays, ambient WPT is becoming a key enabler for a variety of applications, including biomedical and healthcare devices [6]–[12], RFIDs [13], and remote sensors [14]–[17]. Depending on the application, frequencies ranging from the low megahertz range [6], [7], [18] to the UHF bands [13] are used. A fundamental building block within the WPT receiver is the RF-to-dc converter as it is responsible for rectifying the limited available RF power into a dc voltage, as shown in Fig. 1. In fact, it is responsible for the sensitivity of the WPT receiver, defined as the minimum input power required to generate a usable output dc voltage; a significant portion of the overall power conversion efficiency (PCE); and the dynamic range (DR), defined as the range of the input power where the converter operates efficiently [19]. The operating conditions of the WPT receiver vary significantly depending on its application. Hence, an RF-to-dc converter must be capable of working at the maximum level of efficiency to undertake different operating frequencies as well as a wide range of loading conditions and input power levels.

Fig. 2 shows some recent RF-to-dc converters' architectures and their respective PCE versus input power. Diode-based designs, such as Dickson [20] [Fig. 2(a)] and full-bridge rectifiers, suffer from a high-dropout voltage (V_{th}) across the diodes, leading to a poor sensitivity and poor overall performance at low RF power. As a consequence, this technique is not practical for the ambient WPT where the RF power is low. Fully cross-coupled rectifier (FX) [13] overcome the sensitivity problem and can operate efficiently at a relatively low power by applying the RF power differentially across four rectifying transistors, as shown in Fig. 2(b). However, the FX design suffers from a poor performance at high RF power and

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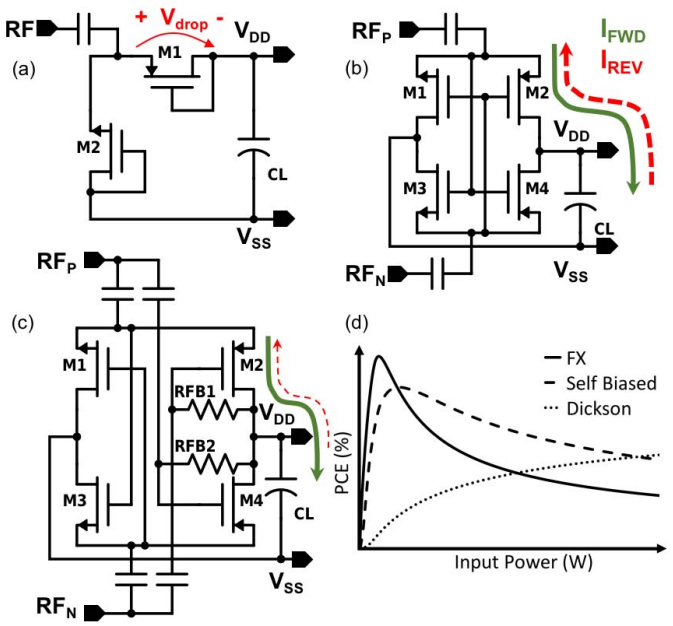


Fig. 2. Schematics of (a) Dickson [20], (b) FX [13] and (c) self-biased [19] rectifiers, and (d) their PCE for different input power levels.

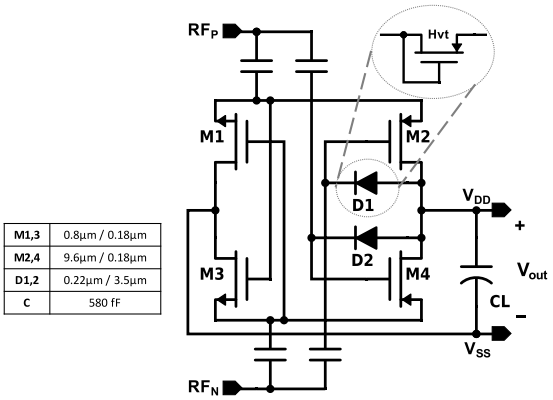
a poor DR due to the presence of a reverse current (I_{REV}) leaking some of the harvested energy back to the RF input. Self-biased design introduced by Ouda *et al.* [19] utilizes two feedback resistors to reduce I_{REV} by lowering the driving voltage of the rectifying transistors, as shown in Fig. 2(c). As a result, both the performance at high RF power and the DR are improved. However, the feedback resistors limit the forward current (I_{FWD}) as well, resulting in a drop in the peak PCE and a poor performance at low RF power [Fig. 1(d)]. Moreover, the performance of the rectifier becomes highly sensitive to the loading value. For example, the peak PCE drops by about 27% when the load varies from 50 to 200 kΩ. Besides, the loading effect introduced by the added resistors limit the efficient operation to a few hundreds of megahertz.

This paper presents enhanced single- and double-sided RF-to-dc power converters for ambient WPT, which are based on the self-biased technique. The proposed designs provide a high PCE, high sensitivity, wide DR, less sensitivity to the load (compared to the self-biased architecture), and are capable of operating efficiently by employing feedback diodes. This paper is organized as follows. Section II explains the proposed design and its basic working methodology, Section III shows and compares the measurement results for different architectures, and Section IV presents the conclusion.

II. Proposed Design

A. Proposed Single-Sided Architecture

Fig. 3 shows a schematic of the proposed single-sided design for the enhanced performance. The design is based on the cross-coupled configuration to maintain the high-sensitivity feature. Moreover, it realizes the self-biased concept by replacing the feedback resistors from the self-biased architecture [19] with two feedback diodes (D1, 2). These diodes are positioned



M1,3	0.8μm / 0.18μm
M2,4	9.6μm / 0.18μm
D1,2	0.22μm / 3.5μm
C	580 fF

Fig. 3. Schematic of the proposed single-sided rectifier.

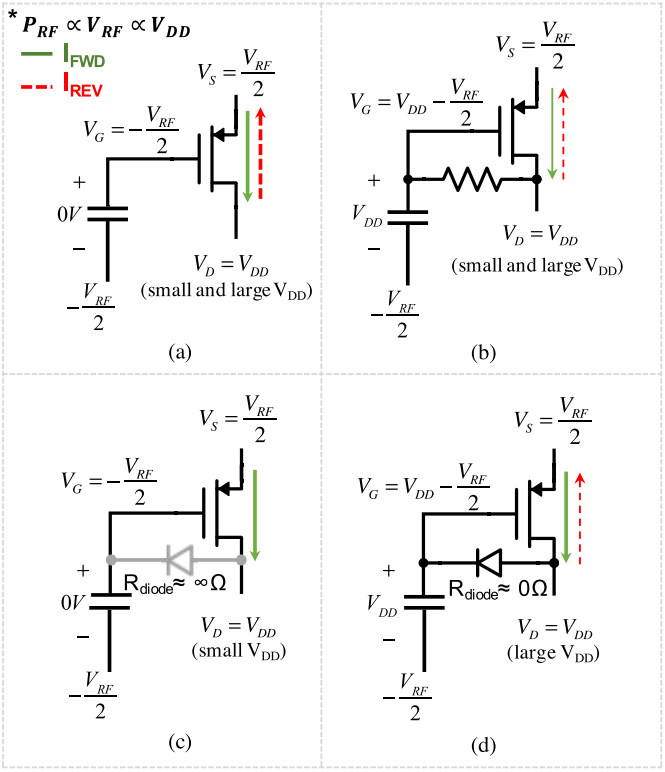


Fig. 4. Steady-state operating points for (a) FX rectifier, (b) self-biased rectifier, (c) proposed single-sided rectifier at low input power, and (d) proposed single-sided rectifier at high input power.

to be reverse biased for the RF signal and forward-biased for the dc voltage. The prime advantage of using diodes is to provide a variable resistance for the dc voltage depending on the RF power while minimizing the passage of the RF signal from the input to the output. For example, at low RF power the diodes remain OFF ($R_{\mathrm{diode}} \approx \infty\ \Omega$), and the proposed design acts as the FX architecture. At high RF power, in contrast, the diodes turn ON ($R_{\mathrm{diode}} \approx 0\ \Omega$) and the whole design acts as the self-biased architecture.

Fig. 4 shows the voltages across M2, 4 and their impact on I_{FWD} and I_{REV}. The driving voltage for I_{FWD} is the source–gate voltage (V_{SG}), and the driving voltage for I_{REV} is the

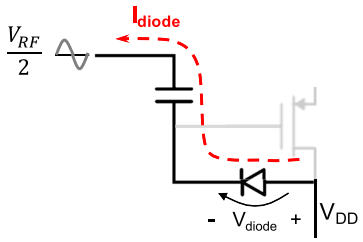


Fig. 5. Current (I_{diode}) through D1, 2.

drain–gate voltage (V_{DG}). To boost the PCE performance of a rectifier at low RF power, I_{FWD} becomes critical, and it is maximized by maximizing V_{SG}. On the other hand, to boost the performance of a rectifier at high RF power, I_{REV} becomes critical, and it is minimized by minimizing V_{DG}. Note that I_{REV} is negligible at low RF power due to the relatively small V_{DD} (i.e., $|V_{\text{DG}}| < |V_{\text{th}}|$). The FX architecture has high driving voltages for both I_{FWD} and I_{REV} limiting the superb PCE performance to the low RF power. Whereas the self-biased design [Fig. 4(b)] has low driving voltages for both I_{FWD} and I_{REV}, limiting the superb PCE performance to the high-RF power. In comparison, the proposed design combines the strengths of both the FX and the self-biased architectures by offering an adjustable driving voltage depending on the RF power.

B. Leakages and Performance Evaluation

The threshold voltage and the sizing of the diodes determine: 1) the voltage level where the behavior of the diode changes from open circuit to short circuit and 2) the switching current (I_{diode}) leaking some of the harvested energy through the diodes to the input. It is important to understand the impact of each point in order to optimize the performance of the circuit.

It is desired to use high-threshold voltage diodes to make the diodes act as a short-circuit for the dc signal, only when I_{REV} is significant (i.e., at high input power). Note that a diode with low-threshold voltage will reduce I_{FWD} at lower RF power levels (where I_{REV} is negligible), resulting in a degraded low power performance (i.e., similar to the self-biased architecture).

I_{diode} is represented in Fig. 5, and it is simply a nonzero mean switching current. I_{diode} occurs when the instantaneous voltage of the RF signal at the cathode is smaller than V_{DD}. For the case of $(V_{\text{RF}}/2) < (V_{\text{DD}} - V_{\text{diode}})$, I_{diode} is modeled as

$$I_{\text{diode}} = \frac{1}{2}K'\frac{W}{L}\left(\frac{V_{\text{RF}}}{2} - V_{\text{diode}}\right)^2 \tag{1}$$

and for the case of $(V_{\text{DD}} - V_{\text{diode}}) < \frac{V_{\text{RF}}}{2} < V_{\text{DD}}$, I_{diode} is modeled as

$$I_{\text{diode}} = I_{\text{ds0}} e^{\frac{V_{\text{DD}} + \frac{V_{\text{RF}}}{2} - V_{\text{diode}}}{n v_T}} \left(1 - e^{\frac{-V_{\text{ds}}}{v_T}}\right) \tag{2}$$

where K' is process dependent, W/L is the size of the transistor, V_{diode} is the threshold voltage of the diode, I_{ds0} is the current at the threshold, v_T is the thermal voltage, and n is a process-dependent term [21]. From (1) and (2), the damage arising from I_{diode} is reduced by using high-threshold transistors (high V_{diode}) with a weak current conduction. A weak current conduction is achieved using a diode-connected transistor with long channel length. In our case, D1, 2 have a width (W) of 220 nm and a length (L) of 3.5 μm.

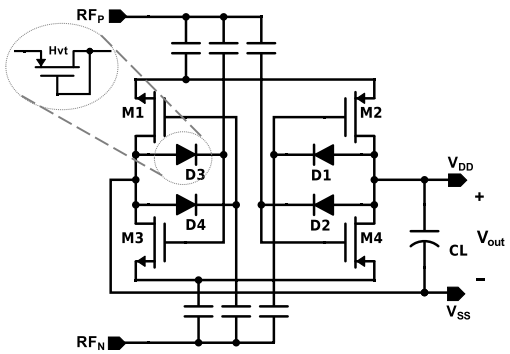


Fig. 6. Schematic of the proposed double-sided rectifier.

C. Proposed Double-Sided Architecture

Normally, the self-biased concept is applied only to one side of the rectifier [i.e., self-biased design in Fig. 2(c)]. This is because the conventional self-biased architecture suffers from a poor PCE performance at low RF power. Hence, it is not practical to add more feedback resistors connected to M1,3, as doing so causes the PCE performance to degrade significantly at both the low and medium RF power levels.

Fig. 6 proposes a double-sided architecture. Again, the added diodes (D3, 4) are reverse biased for the RF signal and forward-biased for the dc signal. This way, the proposed double-sided architecture can provide an even better performance with better sensitivity and higher PCE. When the instantaneous RF power at the cathode of D3, 4 is larger than V_{SS}, D3, 4 remains OFF, and the whole architecture acts as the single-sided design. In contrast, when the instantaneous RF power at the cathode of D3, 4 is smaller than V_{SS} by V_{diode}, D3, 4 turns ON and supports M1,3 by draining more current from the negative terminal of the load. In other words, while D1, 2 enhances the PCE and DR by reducing I_{REV}, D3, 4 enhances the PCE and sensitivity further by increasing I_{FWD}. Note that D3, 4 does not change the operating points of M1,3, unlike D1, 2. This is because the dc voltages at the cathodes of D3, 4 are always larger than V_{SS}, no dc current can flow through. Also, since the optimum dc voltages at the gates of M2, 4 are different compared to M1,3, two extra coupling capacitors are connected to the gates of M1,3.

Fig. 7 shows the transient current flowing in the rectifier [Fig. 7(a)] and the corresponding forward and reverse charge distributions [Fig. 7(b)] when different architectures operate at 10-μW RF power and 433 MHz with a 100-kΩ load. The FX design has a relatively large I_{FWD} and I_{REV}, resulting in a net charge equal to 34.1 fCol/Cycle. The self-biased design has a relatively small I_{FWD} and a negligible I_{REV}, and the net forward charge is 33.9 fCol/Cycle. In contrast, the proposed

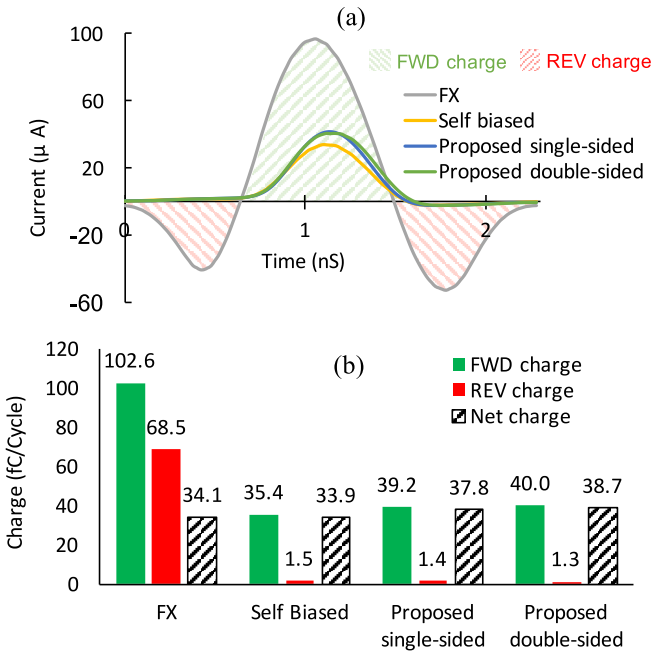


Fig. 7. (a) Simulated transient current. (b) Charge distribution for different architectures at RF power of 10 μW and operating frequency of 433 MHz. Load is 100 kΩ.

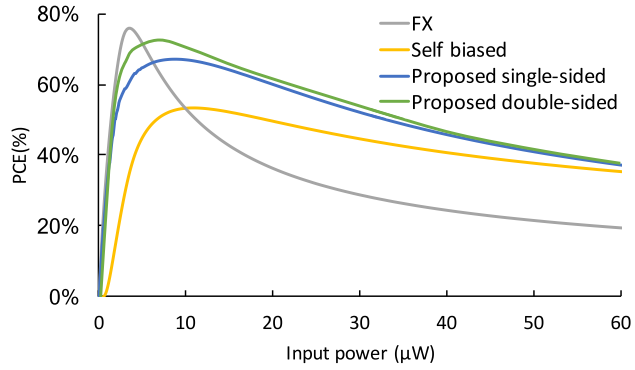


Fig. 8. Simulated PCE operating at 433 MHz. Load is 100 kΩ.

double-sided design maintains a higher I_{FWD} (compared to the self-biased) and a negligible I_{REV}; hence, it has the highest net charge, which is equal to 38.7 fCol/Cycle, translating to more than 13% charge conversion efficiency versus both FX and self-biased structures. This enhancement is reflected on the PCE performance, as shown in Fig. 8.

III. Measurement Results and Discussion

The proposed architectures are designed in a 0.18-μm standard CMOS technology, die microphotographs of the proposed designs are shown in Fig. 9. The FX and self-biased designs are also fabricated on the same die for a fair comparison. The active area of the proposed single-sided design is 8400 μm^2 and for the double-sided design 8800 μm^2, compared to 5000 μm^2 for the FX design and 16 900 μm^2 for the self-biased design.

The measurement setup consists of a vector network analyzer (VNA) (Agilent N5225A), a digital multimeter (Keysight 34420A), and a programmable variable load resistor.

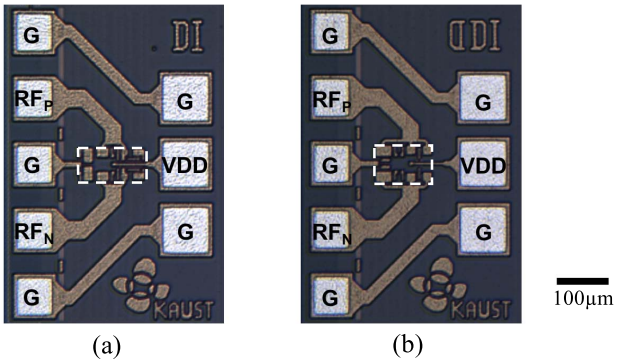


Fig. 9. Die microphotograph for (a) proposed single-sided and (b) double-sided architectures in 0.18-μm CMOS technology.

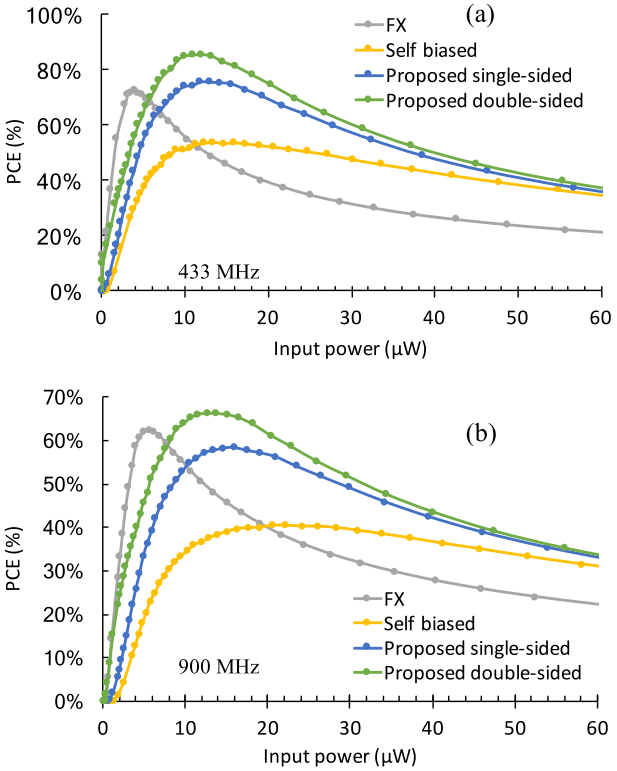


Fig. 10. Measured PCE at operating frequencies of (a) 433 and (b) 900 MHz. Load is 100 kΩ.

The test is accomplished by sweeping the input RF power, the load, and the operating frequency, and recording the corresponding output voltage and the S-parameters. The S-parameters are measured using on-chip probing via GSGSG differential probes with the reference plane set to be the on-chip pads of the rectifier input. After that, the instantaneous input power delivered to the rectifier's input is calculated by de-embedding the reflection and transmission losses [19], [22], [23], as shown by the following equation:

$$P_{in}(\text{dBm}) = P_{source}(\text{dBm}) - L_{cable}(\text{dB}) - 10\log|S_{11rec}|^2 \quad (3)$$

where P_{source} is the output RF-power of the VNA port, L_{cable} is the cable loss, and S_{11rec} is the measured S-parameters of the rectifier input. Last, the PCE is calculated using the

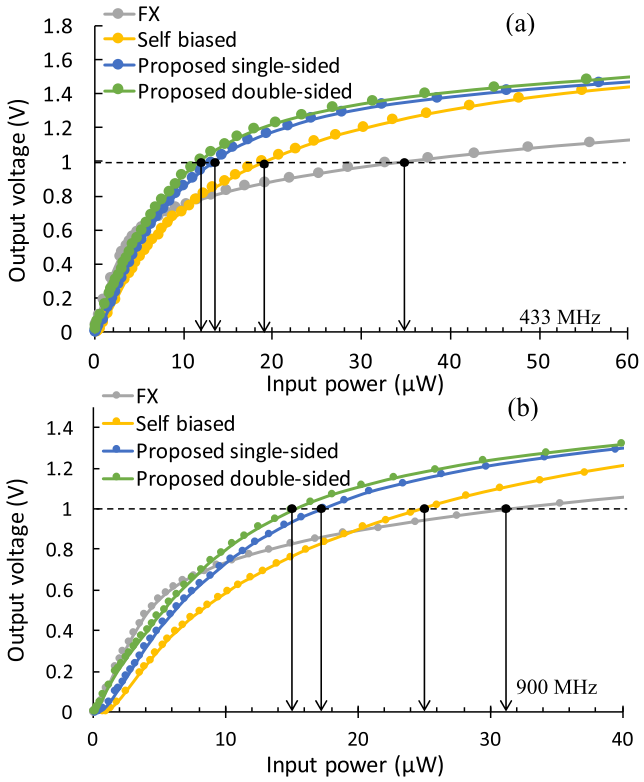


Fig. 11. Measured output voltage versus input power at operating frequency of (a) 433 and (b) 900 MHz. Load is 100 kΩ.

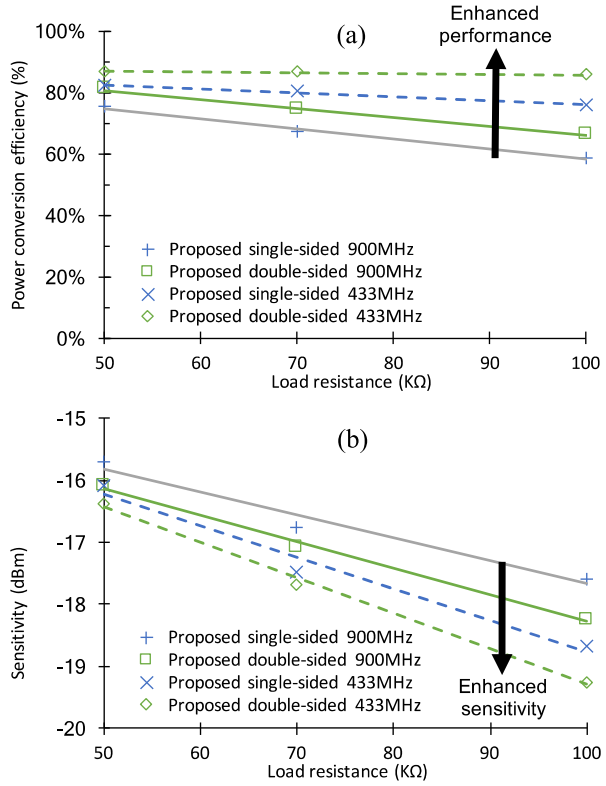


Fig. 12. (a) Measured peak PCE. (b) 1-V sensitivity at different loads.

following equation:

$$\text{PCE} = \frac{P_o}{P_{\text{in}}} = \frac{v_o^2/R_{\text{Load}}}{P_{\text{in}}} \tag{4}$$

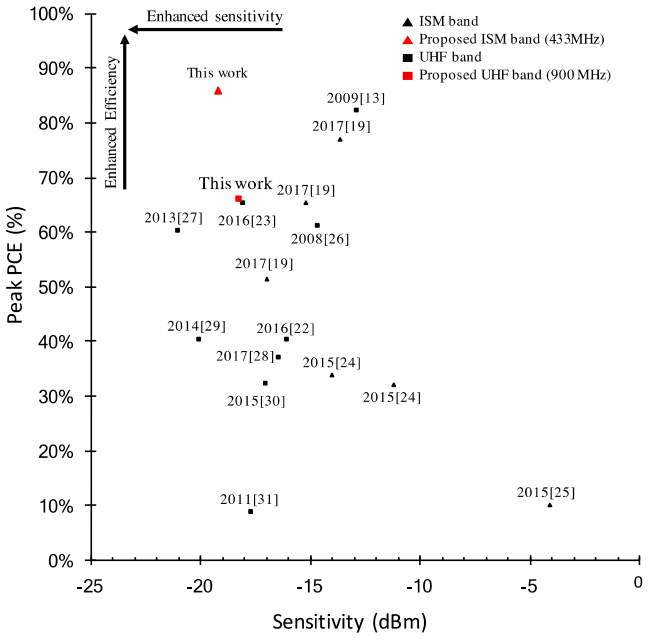


Fig. 13. Peak PCE verses 1-V sensitivity for different architectures operating at ISM and UHF bands.

where P_o is the output power delivered to the load, v_o is the output dc voltage, and R_{Load} is the load resistor.

In general, the proposed single-sided and double-sided designs offer a higher PCE for a wide range of input power. Fig. 10 shows the measurement results for the PCE versus the RF input power for different architectures, operating with a 100-kΩ load at the industrial, scientific, and medical (ISM) bands (433 MHz) [Fig. 10(a)] and the UHF 900-MHz band [Fig. 10(b)]. The proposed topologies combine the strengths of both the FX and the self-biased architectures by maintaining an efficient performance undertaking both low and high input powers. In addition, the proposed double-sided design offers the highest peak PCE of 82% and 66% when operating at the ISM and UHF bands, respectively.

Fig. 11 shows the measurement results for the output voltage at different RF power levels for the different architectures when the operating frequency is set to 433 MHz [Fig. 9(a)] and 900 MHz [Fig. 9(b)] and a 100-kΩ load. In general, both the single-sided and double-sided architectures are capable of producing the best sensitivity and higher output voltage for a broad range of RF power. Note that sensitivity, here is defined as the minimum RF power required to generate a voltage of 1 V at the load. In our case, the proposed double-sided topology enhances the sensitivity by more than 1.9 dB.

Fig. 12 demonstrates the dependence of the proposed architectures on the load. This is achieved by fixing the operating frequency, varying the load resistance, and measuring both the peak PCE [Fig. 12(a)] and the sensitivity [Fig. 12(b)]. At 433-MHz operating frequency, both the single-sided and double-sided architectures provide steady peak PCE with insignificant dependence on the loading value. At 900 MHz, the peak PCE varies by less than 15% for the double-sided architecture. The performance for the single-sided architecture is equally well with only 2% difference.

TABLE I
PERFORMANCE COMPARISON

Architecture [a]	Operating frequency	Technology	Area	Number of stages	Peak Power Conversion Efficiency (PCE)	Sensitivity [b]
	MHz	μm	$\times 10^3\ \mu m^2$	stage	%	dBm
Proposed single-sided	**433**	**0.18**	**8.4**	**1**	**76**	**-18.7**
Proposed double-sided	**433**	**0.18**	**8.8**	**1**	**86**	**-19.2**
Fully cross-coupled (FX)[c] [13]	433	0.18	5	1	73	-14.5
Self-biased [c] [19]	433	0.18	17	1	54	-17.3
Dickson rectifier with multiple- Vth offset cancellation [24]	433	0.18	15	4	34	-14
Fully cross-coupled with inter-stage RF injection [25]	433	0.18	88	3	10	-4.1
Proposed single-sided	**900**	**0.18**	**8.4**	**1**	**58**	**-17.6**
Proposed double-sided	**900**	**0.18**	**8.8**	**1**	**66**	**-18.2**
Fully cross-coupled (FX) [13]	953	0.18	13.4	1	82.6	-12.9
Self-biased [c] [22]	900	0.18	17	1	40	-16.0
Adaptive [23]	900	0.18	8.4	1	65	-18
Floating gate doubler [26]	910	0.25	400	36	60.7	-14.6
Reconfigurable [d] [27]	868	0.13	200	4	60	-21
Dual-path [e] [28]	900	0.65	48	5	36.5	-16.4

[a.] All architectures are operating with a 100 kΩ load, [b.] Input RF power at 1V output voltage, [c.] Measurement results are reproduced in this work, [d.] using tracking load, [e.] load is 147 kΩ

Table I shows a comparison of the proposed designs with different architectures operating at the ISM and the UHF bands. The proposed designs offer the best sensitivity while maintaining a high PCE and a relatively small area. Even though Kotani *et al.* [13] show a very high PCE when operating in the UHF range, it suffers from poor sensitivity and DR. Ouda *et al*. [23] show a decent sensitivity and peak PCE performance; however, the proposed double-sided architecture offers a better PCE performance at low RF power levels. Fig. 13 shows the performance of many recent architectures including the peak PCE and the 1-V sensitivity. In general, the proposed design offers a high PCE while maintaining a good sensitivity.

IV. CONCLUSION

This paper has demonstrated an enhanced RF-to-dc converter that selectively limits the conductions of the rectifying transistors depending on the RF power level. As a consequence, the proposed architecture limits the reverse current without degrading the forward current and can operate efficiently for a wider range of RF input power. When operating at the ISM band 433 MHz with a 100-kΩ load, the measurement results show a PCE of 86% and a sensitivity of −19.2 dBm, and a PCE of 66% and a sensitivity of −18.2 when operating at the UHF band. Furthermore, the measurement results show a minimum dependence on the loading for the PCE.

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