A 185–215-GHz Subharmonic Resistive Graphene FET Integrated Mixer on Silicon

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***Abstract*— A 200-GHz integrated resistive subharmonic mixer based on a single chemical vapor deposition graphene field-effect transistor (G-FET) is demonstrated experimentally. This device has a gate length of 0.5 μm and a gate width of 2 × 40 μm. The G-FET channel is patterned into an array of bow-tie-shaped nanoconstrictions, resulting in the device impedance levels of ∼50 Ω and the ON–OFF ratios of ≥4. The integrated mixer circuit is implemented in coplanar waveguide technology and realized on a 100-μm-thick highly resistive silicon substrate. The mixer conversion loss is measured to be 29 ± 2 dB across the 185–210-GHz band with 12.5–11.5 dBm of local oscillator (LO) pump power and >15-dB LO–RF isolation. The estimated 3-dB IF bandwidth is 15 GHz.**

***Index Terms*— Coplanar waveguide (CPW), field-effect transistors (FETs), graphene, harmonic balance, millimeter-wave integrated circuits, subharmonic resistive mixers.**

I. Introduction

GRAPHENE, a 2-D monolayer sheet of carbon atoms [1], has attracted considerable attention for high-frequency electronics [2]. The exquisite characteristics of graphene, particularly its high intrinsic carrier mobility and high carrier saturation velocity, make it a potential material for field-effect transistors (FETs) operating at millimeter-wave and terahertz-wave frequencies [3]. The potential applications at these frequencies are predicted to have a significant societal impact, including high-speed wireless communication links [4] and security imaging [5]. Practically, to implement such systems based on a graphene platform, the development of graphene FET (G-FET)-based integrated circuits is necessary [6].

However, the reported operating frequencies of G-FET integrated circuits are all below 30 GHz [7], [8]. Undeniably, the obstacle for active G-FET circuits is still the low extrinsic maximum frequency of oscillation ($f_{\max}$) for G-FETs, which is limited to less than 40 GHz [9], [10]. Consequently, the active G-FET-based circuits are currently restricted to the microwave range [10], [11]. Thus, extensive efforts have been focused on passive G-FET device applications and circuit demonstrators, which are decoupled from $f_{\max}$. At higher frequencies, millimeter-wave [12]–[14] and terahertz power detectors [15], [16] have been reported. Additionally, frequency translating mixers have been widely investigated in different configurations. The fundamental single-ended [17] and double-balanced [18] resistive G-FET mixers have achieved the conversion loss (CL) values of 14 dB at 2 GHz and 33 dB at 3.6 GHz, respectively. These mixers, however, do not utilize the inherent symmetry of the G-FET channel resistance. To this end, the subharmonic resistive G-FET mixer was proposed at Chalmers [19], and it has been reported to reach a CL of 19 dB at 24–31 GHz [8]. The G-FET subharmonic mixer implementation uses a single transistor and no balun is required, making the circuit topology more compact. Evidently, an enhanced operating frequency and an improved performance of the G-FET integrated circuits are the keys to satisfying the expectations for graphene electronics.

In this paper, we report an integrated subharmonic resistive G-FET mixer circuit on Si operating at 185–215 GHz, which is the highest reported for any graphene integrated circuit. The primary motivation for using a subharmonic mixer in this paper is to reduce the frequency of the necessarily high power local oscillator (LO) source. The circuit is designed in coplanar waveguide (CPW) technology, which is predominant when approaching submillimeter-wave frequencies [20] due to the relaxed requirement on substrate thickness compared with the microstrip technology [21]. Due to the lack of CPW models in current CAD packages, full-wave EM simulations are applied for the design of the circuit. Subsequently, the resulting S-parameter matrices are inserted into a harmonic balance simulator [22], which predicts frequency generation in the G-FET, to simulate the complete mixer performance.

The results in this paper represent an optimized design of the mixer circuit presented in [23]. Metalized airbridges are added to the updated mixer circuit to balance the potentials of the ground planes as well as to ensure single-mode wave propagation at the circuit T-junctions. Moreover, a more thorough characterization is presented: RF and IF frequency sweeps, LO power and gate bias dependences, port isolations, and return loss. The measurements yield a record CL for graphene-based mixers of 29 ± 2 dB in the 185–210-GHz band, which is 5 dB less than [23]. The performance of our G-FET mixer on silicon is inferior to both GaAs HEMT [24] and CMOS [25]. Nevertheless, if the process on Si is adapted to flexible substrates [26], then the results in this

Manuscript received July 1, 2016; revised September 16, 2016; accepted October 2, 2016. Date of publication December 2, 2016; date of current version January 26, 2017. This work was supported by the Swedish Foundation of Strategic Research under Grant SE13-0061. An earlier version of this paper was presented at the IEEE MTT-S International Microwave Symposium, San Francisco, CA, USA, May 22–27, 2016.

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Digital Object Identifier 10.1109/TMTT.2016.2615928

paper show promise for ubiquitous graphene millimeter-wave electronics.

II. Mixer G-FET Design and Fabrication

There are two main FET mixer operating principles, namely, transconductance (active) mixer and resistive (passive) mixer. Accordingly, either the transconductance (g_m) or the channel resistance ($R_{\rm ds}$) is swept in a time-varying periodic manner as $g_m(t)$ or $\mathrm{R_{ds}}(t)$, respectively. Because of the relatively low transconductance, the reported G-FET-based active mixers have exhibited poor performance [27]. Moreover, the unique symmetry of electron and hole conduction in the G-FET transfer characteristics makes it suitable for the subharmonic resistive mixing concept. This symmetry enables mixing at the first harmonic of the LO frequency using only one G-FET. In contrast, with traditional unipolar FETs, a balun is required to feed the LO signal 180° out-of-phase to the gates of two devices [28]. In addition, a passive mixer is the only option at millimeter waves due to the low $f_{\rm max}$ of G-FETs.

A. Mixer G-FET Design

In a G-FET-based subharmonic resistive mixer, the drain is unbiased and the gate is biased at the Dirac point. Under such conditions, applying the LO to the G-FET gate makes the periodically swept channel resistance primarily contain the first harmonic of the LO frequency. For a resistive mixer, the CL can be determined by [29]

$$CL = \frac{\pi^2}{(\Gamma_{\rm max} - \Gamma_{\rm min})^2}. \tag{1}$$

Here, $\Gamma_{\rm max}$ and $\Gamma_{\rm min}$ are the reflection coefficients that are observed when looking into the drain of the G-FET when the time-varying channel resistance is maximum and minimum, respectively. Mathematically, it is the maximum and minimum of the standard expression

$$\Gamma(t) = \frac{R_{\rm ds}(t) - Z_0}{R_{\rm ds}(t) + Z_0} \tag{2}$$

where Z_0 is the embedding impedance, typically 50 Ω. Ideally, a minimum CL of 3.9 dB is attainable for the given $R_{\rm max} \to \infty$ and $R_{\rm min} \to 0$. As a general rule, to minimize the CL, a high $\Gamma_{\rm max}$ and a low $\Gamma_{\rm min}$ are required, which correspond to $R_{\rm max} \gg Z_0$ and $R_{\rm min} \ll Z_0$, respectively. Thus, G-FETs with a high current ON–OFF ratio and an impedance level of $Z_0 = (R_{\rm max} \cdot R_{\rm min})^{1/2} \approx 50\ \Omega$ are required.

Special care must be taken when designing G-FETs for resistive mixers due to the lack of a bandgap in graphene, which results in a low current ON–OFF ratio in G-FETs. The drain–source resistance of G-FETs is given by $R_{\rm ds} = R_{\rm channel} + R_c$. Here, $R_{\rm channel}$ is the gate variable G-FET channel resistance, which is essentially proportional to $L_{\rm channel}/W_{\rm channel}$. Furthermore, R_c is the contact resistance at the graphene–metal interface and access resistance that scales with the gate width, $W_{\rm gate}$. To obtain a lower $R_{\rm min}$, a wide device is necessary. However, this requirement simultaneously reduces $R_{\rm max}$ because G-FETs have no OFF state. Moreover, the gate capacitance must be considered in millimeter-wave designs because it limits the mixer performance at high frequencies. The total gate capacitance is proportional to the channel area, $L_{\rm channel} \cdot W_{\rm channel}$, and it also increases in a wider device. In a standard G-FET design, $L_{\rm channel} = L_{\rm gate}$ and $W_{\rm channel} = W_{\rm gate}$, which limit the degrees of freedom in the device design.

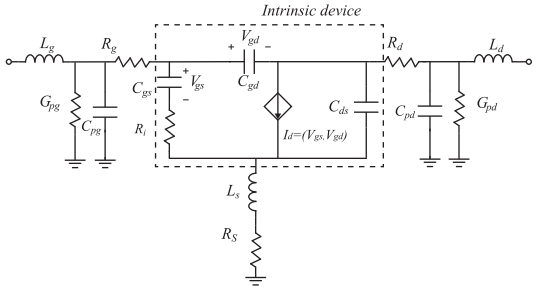
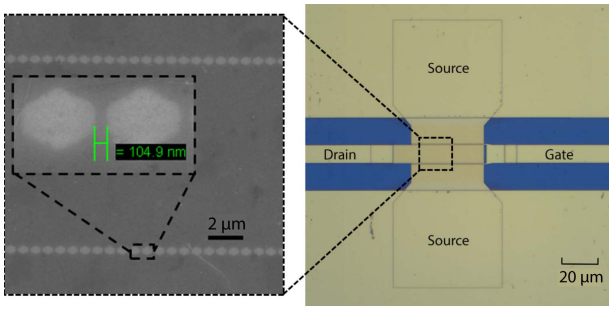


Fig. 1. Equivalent circuit of the G-FET used in the mixer simulations. The IV nonlinearity models the frequency conversion, and all capacitors are linear.



(a) (b)

Fig. 2. (a) SEM image of the fabricated graphene nanoconstriction channels. (b) Micrograph of the G-FET with $L_{\rm gate} = 0.5\ \mu$m, $W_{\rm gate} = 2 \times 40\ \mu$m, and $W_{\rm channel} = 2 \times 6\ \mu$m.

To relieve this tradeoff problem in the device dimensions, bow-tie-shaped nanoconstrictions in the G-FET channel can be used [30]. The impedance of an individual constriction channel is reported to be 1–2 kΩ, which is considerably higher than the typical 50-Ω embedding impedance. Therefore, an array of parallel bow-tie-shaped G-FET channels, yielding $W_{\rm gate} > W_{\rm channel}$, are used to achieve a higher current ON-OFF ratio and a proper impedance level. Moreover, using constrictions, the gate capacitance is reduced by a factor of ∼3, which results in a better performance of the G-FETs at high frequencies. This approach was utilized in the resistive mixer in [8], resulting in a G-FET with an ON–OFF ratio of ∼7 for exfoliated graphene.

In our approach, harmonic balance simulations with the large-signal G-FET model in Fig. 1 were used to optimize the device design to obtain the lowest CL at 200 GHz. The IV model was implemented following the approach in [31], while the capacitors were assumed to be linear and to contribute negligibly to the mixing performance. The G-FET dimensions were swept for the given area-normalized gate oxide capacitance $C \approx 100$ fF/cm^2 extracted from S-parameters [14] and under the assumption of $C_{\rm gs} \approx C_{\rm gd}$ for the unbiased G-FET. Furthermore, the contact resistance normalized to gate width was taken to be $R_s W_{\rm gate} = R_d W_{\rm gate} \approx 800\ \Omega\mu$m. Finally, the images in Fig. 2 illustrate the chosen optimum dimensions of

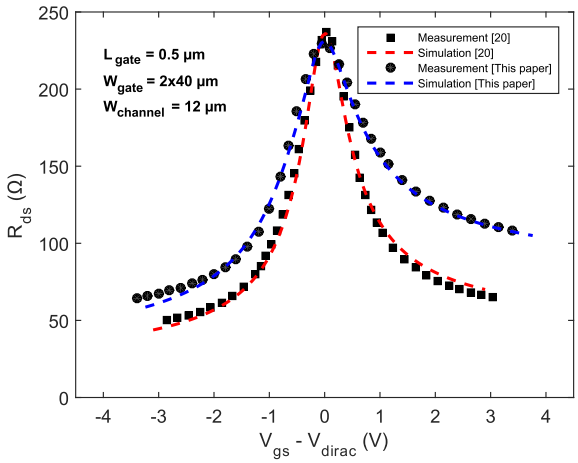


Fig. 3. Measured and modeled transfer characteristics at V_{ds} = 0.1 V.

the G-FET for obtaining the lowest CL at $f_{RF} = 200$ GHz. The component has a gate length of 0.5 μm, where the gate–drain and the gate–source gaps are 0.1 μm. The gate width is set to be 80 μm (2×40 μm) and the optimal channel width is 12 μm (2×6 μm), i.e., ~120 constrictions each with a width of ~100 nm. This channel width yields nominal intrinsic gate capacitors $C_{gs} = C_{gd} \approx 11$ fF for the unbiased G-FET.

B. G-FET Fabrication and DC Characterization

To fabricate the G-FET, a graphene sample was first produced using the chemical vapor deposition (CVD) process on the copper film and transferred to a highly resistive silicon substrate (10-kΩ·cm bulk resistivity) covered by 90-nm SiO_2. Subsequently, the G-FETs were fabricated using an electron beam lithography-based process. First, a directional 50-mtorr pressure O_2 plasma etching step was applied to define mesas and pattern the channel into nanoconstrictions. Then, ohmic contacts were aligned onto the mesas and formed by the evaporation of 1-nm Ti, 15-nm Pd, and 100-nm Au followed by lift-off. Subsequently, the gate dielectric of ~ 20-nm Al_2O_3 was formed by atomic layer deposition seeded by naturally oxidized Al. Finally, the gate fingers, which were metalized by 250-nm Al, 10-nm Ti, and 50-nm Au, were evaporated and lifted off. Importantly, the process is scalable to wafer size.

The measured and simulated dc transfer characteristics of the two fabricated mixer G-FETs included in this paper are shown in Fig. 3. As shown, the resulting current ON–OFF ratios achieved for the CVD G-FETs with $L_{gate} = 0.5$ μm are ~4–5. The model parameters extracted from the dc transfer characteristics are listed in Table I. The unintentional variability is due to the poor reproducibility of the fabrication process currently encountered for CVD graphene.

III. Mixer Circuit Design and Fabrication

A. Mixer Circuit Design

The subharmonic mixer was designed to downconvert the center frequency $f_{RF} = 200$ GHz to $f_{IF} = 1$ GHz. Thus, the LO frequency band is centered around 100.5 GHz. The circuit topology of the proposed mixer is shown in Fig. 4(a).

TABLE I
Extracted DC Model Parameters of the G-FETs [31]

	Ref. [20]	This paper
μ_e (cm^2/Vs)	1250	1100
μ_h (cm^2/Vs)	1500	1250
R_c (Ω)	11	18
R_{ext} (Ω)	20	50
n_0 (10^{11} cm^{-2})	9.3	14.5

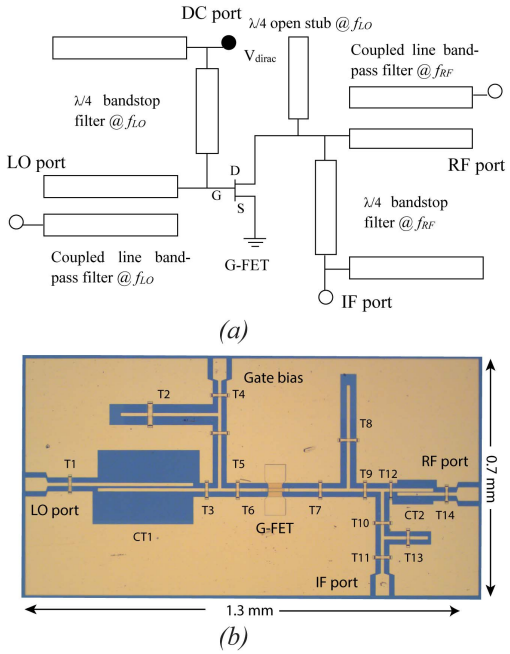


Fig. 4. (a) Equivalent circuit illustrating the selected mixer circuit topology. (b) Micrograph of the fabricated mixer circuit including the dimensions.

The IF signal readout is through a bandstop filter, which consists of a quarter wavelength open stub and a quarter wavelength transmission line at the RF frequency. Coupled line bandpass filters are utilized at both the LO port branch and the RF port branch to block the dc gate bias and the IF signal, respectively. The G-FET requires a bias of $V_{gs} = V_{dirac}$ for optimum subharmonic mixing performance. Rather than applying high-order coupled line filters, because $f_{LO} \approx f_{RF}/2$, first-order filters are preferred to simplify the circuit and to reduce its footprint. However, because of the narrowband characteristics of the IF port stub filter and the broadband property of the RF port coupled line filter, neither the IF nor RF filters are capable of completely attenuating the LO signal. Therefore, an additional quarter-wavelength bandstop filter at the LO frequency was added on the drain side to improve both the LO–RF and LO–IF rejection capabilities.

The circuit was implemented by CPW transmission lines, as depicted in Fig. 4(b). The physical circuit dimensions are listed in Table II. The 50-Ω CPW lines have center conductor widths designed to be 10 μm, with two 15-μm gaps at both sides, for a convenient connection to the G-FET. The lengths and characteristic impedances of the stubs were optimized for

TABLE II

PHYSICAL CPW DIMENSIONS. ALL CENTERLINES HAVE $W = 10\ \mu$m. THE COUPLED LINES HAVE $S_{CT1} = 5.5\ \mu$m AND $S_{CT2} = 1.5\ \mu$m SPACINGS. THE PORTS HAVE $L = 60\ \mu$m, $W = 40\ \mu$m, AND $G = 15\ \mu$m

	T1	T2	T3	T4	T5	T6	T7	T8
G (μm)	15	25	15	15	15	15	15	18
L (μm)	146	283	77	99	214	137	193	300
	T9	T10	T11	T12	T13	T14	CT1	CT2
G (μm)	15	15	15	15	14	15	95	25
L (μm)	99	134	103	43	128	68	278	105

most favorable filter operations. Because both conductors of the CPW lines are in the same plane, the parasitic inductance of the source–ground connections remains low [21]. Moreover, a relatively lower risk of parasitic mode propagation and a lower dispersion for a given substrate thickness make CPW competitive with microstrip in millimeter-wave circuits [32]. However, T-junctions are often inevitable in circuit design, particularly when using stub filters. A parasitic slotline mode can be excited at such discontinuities unless metal airbridges are inserted in the circuit to keep the electric potential the same between two sides of the CPW ground planes. In addition, a parasitic parallel plate waveguide mode may propagate if the substrate is too thick in terms of the circuit operating wavelength. In both cases, the energy is radiated rather than propagated, resulting in high loss.

To ensure suppression of parasitic effects and for layout dimensional optimization, full-wave EM simulations (CST Microwave Studio, finite-difference time-domain) were applied. Based on these simulations, the silicon substrate thickness was selected to be 100 μm. The transmission between the LO and RF ports and a 50 Ω port at the G-FET position was simulated. The improvement from adding the metal airbridges is clearly demonstrated: 0.6- and 2.3-dB reductions in loss are achieved at the 100-GHz LO passband center and the 200-GHz RF passband center, respectively. In addition, ∼30% larger RF bandwidth is achieved due to the wider stopband of the RF stub filter. This result directly demonstrates the improved mixer performance in this paper compared with that in [23].

B. Circuit Fabrication and S-Parameter Characterization

The circuit layer was overlaid on the G-FET using e-beam lithography and e-gun evaporation of 20-nm Ti and 500-nm Au after etching the Al_2O_3 dielectric layer to form a proper contact. Next, the silicon substrate was lapped down to the intended 100-μm thickness. Finally, the airbridges were added with an ∼1.5-μm separation to the center conductor using a conformal PMGI support layer. As illustrated in Fig. 4(b), the final circuit measured 0.7×1.3 mm^2.

To verify the functions of the filters, separate circuits were fabricated in parallel to the mixers, where the G-FET was replaced by a through CPW line. The ports were oriented to allow individual two-port S-parameter measurements in all possible combinations, leaving the other two ports

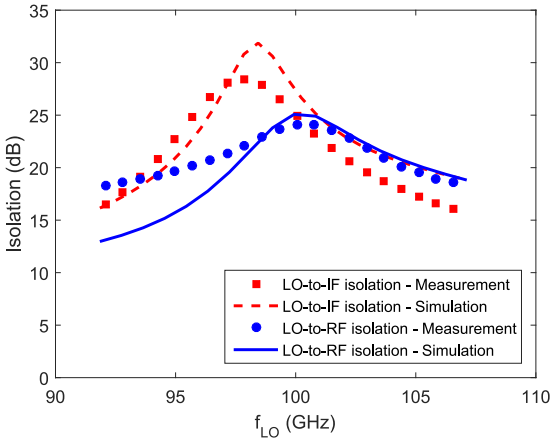


Fig. 5. Measured (symbols) and simulated (lines) LO-to-IF and LO-to-RF isolations of the mixer circuit from S-parameter measurement.

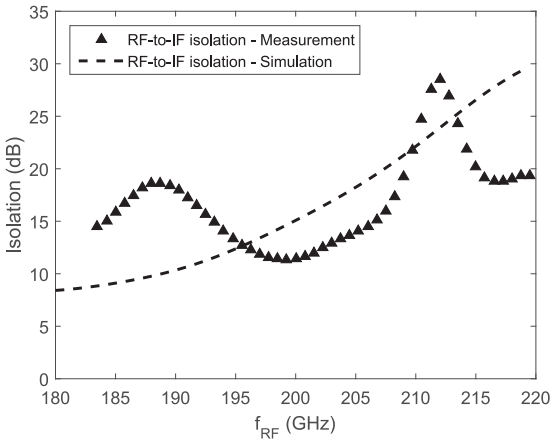


Fig. 6. Measured (triangles) and simulated (solid line) RF-to-IF isolation of the mixer circuit from S-parameter measurement.

open. The on-wafer S-parameters were measured wideband (≤145 GHz) using an Anritsu ME7838A VNA equipped with millimeter-wave extenders and in the WR-5.1 waveguide band (140–220 GHz) with Keysight N5247A PNA-X and VDI extenders. In both cases, LRRM calibrations on a Cascade 138-356 impedance standard substrate were used. Through an intermediate conversion to Z-parameters, the full S-parameter matrix of the four-port can be derived [33]. Based on the measured S-parameters, the LO–IF and LO–RF isolations are both >15 dB, as shown in Fig. 5, and the RF–IF isolation is >10 dB, as shown in Fig. 6, across the mixer band.

IV. MIXER CHARACTERIZATION

A. Mixer Measurement Setup

The fabricated G-FET subharmonic mixer was characterized on-wafer using waveguide-interfaced GSG microprobes. A photograph and a schematic illustration of the full setup are presented in Fig. 7. The LO chain consists of an OML ×6 multiplied source and a W-band power amplifier, followed by a mechanical attenuator to control the LO power level. The LO power was measured at the attenuator WR-10 output waveguide using an Agilent E4419B power meter together with a W8486A power sensor. Compensating for the LO probe

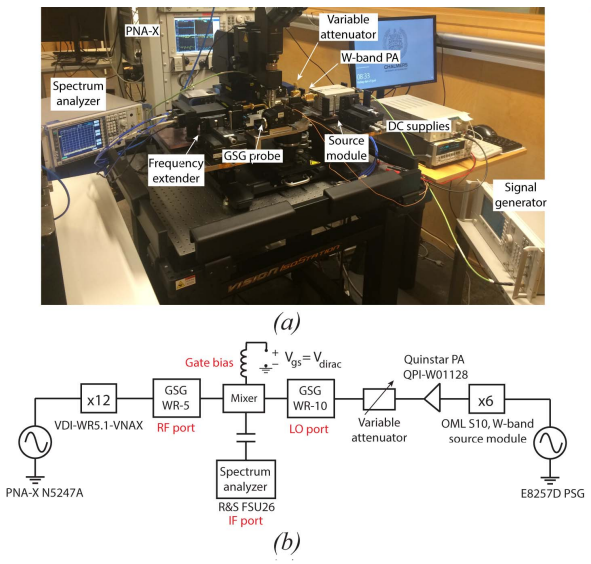


Fig. 7. (a) Photograph and (b) block diagram of the measurement setup.

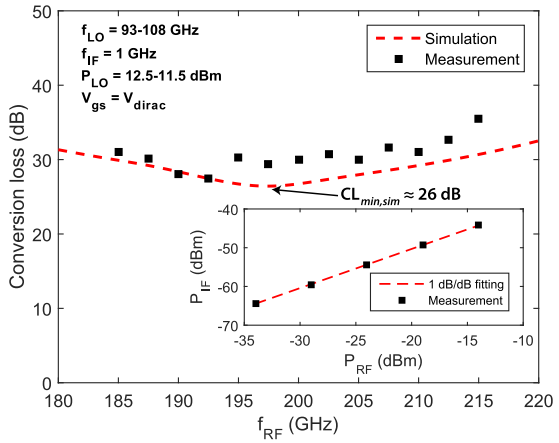


Fig. 8. CL versus RF frequency. The LO frequency is swept and the IF frequency fixed. Inset: P_{IF} versus P_{RF} at f_{RF} = 200 GHz.

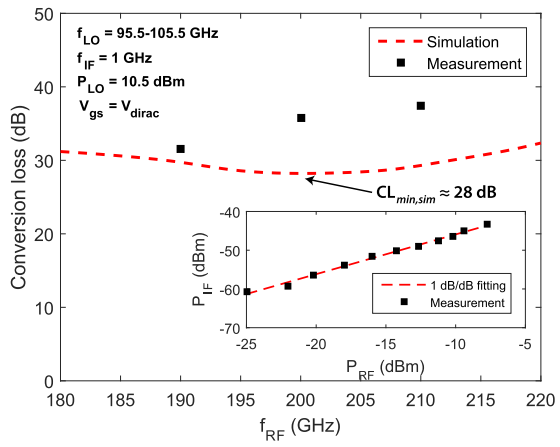


Fig. 9. CL versus RF frequency for the subharmonic G-FET integrated resistive mixer circuit in [23]. The LO frequency is swept and the IF frequency fixed. Inset: P_{IF} versus P_{RF} at $f_{RF} = 200$ GHz.

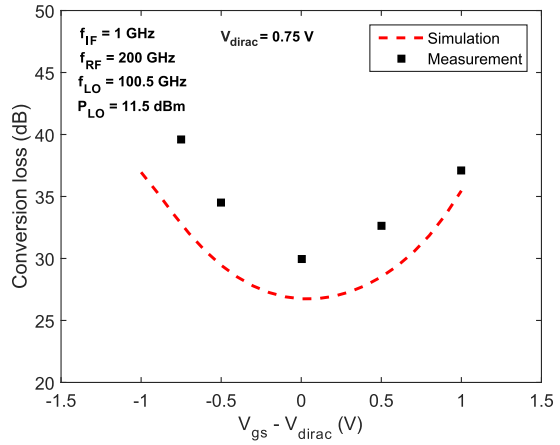


Fig. 10. Gate bias dependence of the CL at the center frequency.

loss, the power at the mixer LO port is 12.5–11.5 dBm for the LO frequency range 93–108 GHz. The RF power level was automatically leveled at the output waveguide flange of the VDI WR-5.1 extender using the PNA-X reference receiver. The RF probe loss was subsequently subtracted to calculate the actual power at the mixer RF port on-wafer. Finally, the IF signal power was monitored using an FSU26 spectrum analyzer.

B. Mixer Characterization Results

Initially, the subharmonic G-FET mixer was biased at the Dirac point ($V_{gs} = V_{dirac}$) for the best performance. Sweeping the LO frequency to maintain a fixed IF frequency of 1 GHz, the mixer CL was measured to be 29 ± 2 dB across the RF frequency range 185–210 GHz. The full plot in Fig. 8 shows an overall minimum CL of 27.5 dB at 192.5 GHz. The result for our previous mixer [23] is presented in Fig. 9 for comparison. Notably, a 5-dB lower CL is measured in this paper. The reasons for this improvement are the decreased loss of the CPW circuit, as discussed in Section III-A, and the somewhat higher LO power in the measurement setup. However, the enhancement is diminished by the less ideal transfer characteristics of the G-FET, as shown in Fig. 3. Simulating the G-FET from [23] together with the new filter designs, a further decrease in the mixer CL to $CL_{min,sim} \approx 22$ dB appears to be feasible. In conclusion, this represents an estimated 6-dB improvement from the new filters (see Fig. 9). Similarly, the improved bandwidth and the lower center frequency shift in the new mixer are due to the parasitic mode suppression from the metal airbridges. Nevertheless, the mixer RF bandwidth is limited by the narrowband characteristics of the LO and RF stopband stub filters. Moreover, the measured IF output power versus RF input power is depicted in the insets of Figs. 8 and 9 to confirm the linear operation regime for both mixers. There was not sufficient output power from the RF source to drive the mixer into saturation.

The high sensitivity of the CL to gate bias voltage is demonstrated in Fig. 10. This result is a consequence of the fact that the mixer utilizes the symmetrical transfer characteristics of the G-FET. Quantitatively, the CL increases by as much as 8 dB when deviating ±1 V from the Dirac point. A possible

TABLE III
COMPARISON OF THE G-FET SUBHARMONIC MIXER WITH RESISTIVE MIXER IMPLEMENTATIONS IN OTHER TECHNOLOGIES

	[25]	[25]	[34]	[24]	[35]	[36]	This work
Technology	Bulk CMOS	Bulk CMOS	SOI CMOS	GaAs mHEMT	GaAs mHEMT	Schottky diode	CVD G-FET
Gate length (nm)	65	65	45	100	100	N/A	500
Harmonic order	1	2	1	1	2	2	2
f_{RF} (GHz)	230	180-220	130-180	200-220	220	230	185-210
DSB CL (dB)	23	19-22	12-13	8-10	12	5.7	28-31
P_{LO} (dBm)	-5	-	3	1.5	2-3	5.6	12.5-11.5
3-dB IF-BW (GHz)	20	30	>26	25	-	10	∼15

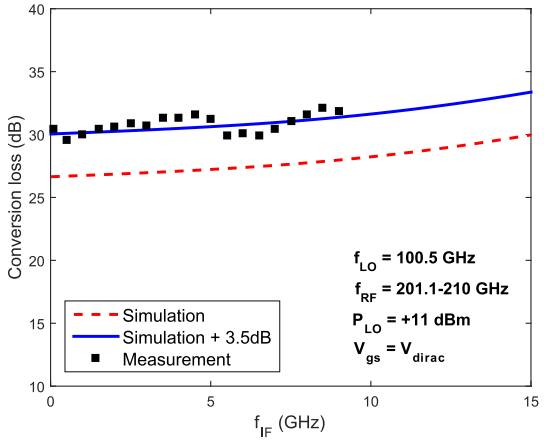


Fig. 11. Extraction of the 3-dB IF bandwidth of the mixer to be ∼15 GHz.

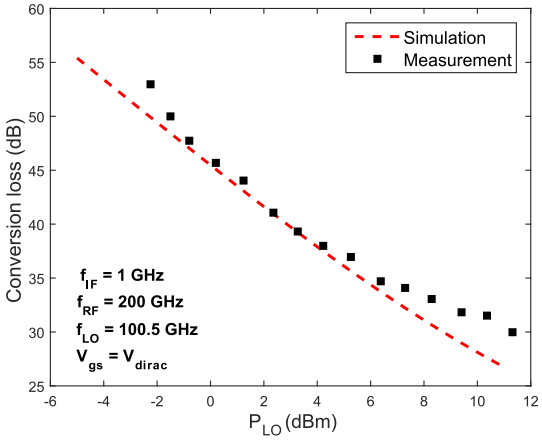


Fig. 12. Dependence of the CL over a wide range of LO powers.

reason for the discrepancy between the measurement and the simulation of the mixer in Fig. 9 could be the instability of the G-FET [23]. A Dirac point drift of ±0.4 V during the measurements could already provide a 2-dB deviation.

The measured and simulated CLs versus the IF frequency are shown in Fig. 11 as measured by sweeping the RF frequency at a fixed LO frequency. At the high RF operating frequency and with the intentionally broadband design of the RF coupled line filter, the mixer presents a relatively large IF bandwidth. To verify that the simulated trend overlaps the measurement, an offset is added to the simulation. In this way, the 3-dB IF bandwidth is extracted to be ∼15 GHz.

As illustrated in Fig. 12, a major drawback of the resistive mixer in this paper is the high LO power required to minimize the CL. This high power is necessary to properly pump the G-FET mixer device between the ON and OFF states. As shown in comparison with Table III, at LO power levels typically used in CMOS and HEMT millimeter-wave resistive mixers in the same frequency range, the G-FET resistive mixer CL increases by 5–10 dB compared with the best value. The higher graphene mobility and the scaling of the gate oxide thickness could both mitigate the LO power requirement.

Finally, the measured and simulated reflection coefficients on the RF port of the mixer are presented in Fig. 13. In this case, there is no LO pump, the G-FET is unbiased, and the IF port is left as an open circuit. Fig. 13 also shows the simulated return loss for the mixer under the real operating conditions

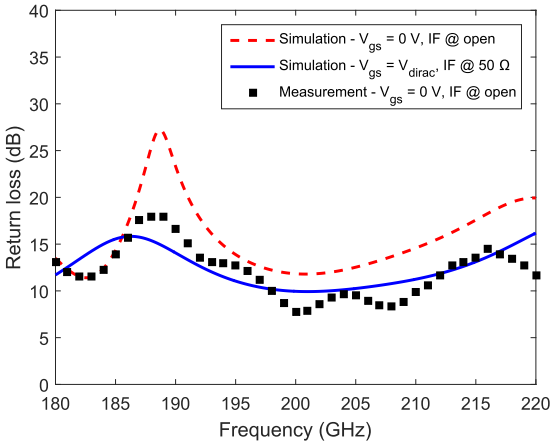


Fig. 13. Return loss on the RF port. The measurement is without an LO pump, the G-FET is unbiased and the IF port terminated in an open circuit.

with the G-FET biased at the Dirac point and the IF port terminated in 50 Ω. The estimated return loss under such realistic operating conditions is ≥10 dB across the RF band. Note that the probing pads are not de-embedded. These act as short low-impedance (35 Ω) transmission lines and effectively present shunt capacitances to the CPW lines. This reduces the return loss particularly at the high-frequency RF port.

The performance in this paper is compared with those of other resistive mixer technologies and other implementations of G-FET resistive mixers in Tables III and IV, respectively.

TABLE IV
PERFORMANCE COMPARISON OF GRAPHENE-BASED FREQUENCY MIXERS
† RESISTIVE G-FET MIXERS ‡ NONLINEAR GRAPHENE FILMS

	[17]	[18]	[37]	[8]	[38]	This work
Harmonic order	1†	1†	2†	2†	6‡	2†
f_{RF} (GHz)	2-20	3.6	5	24-31	220	185-210
CL (dB)	14-18	33	20	18-20	65	28-31
P_{LO} (dBm)	0-4	9	0	10	22	12.5-11.5

As shown, our results represent a sevenfold improvement in operating frequency compared with the results of the previously reported G-FET integrated mixer circuits. In the frequency range considered in this paper, only waveguide-mounted and high-order ($n \geq 6$) harmonic mixers based on nonlinear generation in graphene films have been previously reported [38]. Compared with such a frequency mixer implementation, the integrated G-FET mixer presented in this paper represents a significant performance improvement (∼35 dB), albeit at a lower harmonic order. However, our G-FET mixer is still worse than CMOS and particularly III-V HEMT resistive mixers both in terms of CL and the required LO power. This is of particular concern in applications that demand high receiver sensitivity because the G-FET resistive mixer noise figure at room temperature is at best equal to the CL [37].

V. CONCLUSION

In this paper, a 200-GHz integrated subharmonic resistive mixer based on a single G-FET was reported. An array of nanoconstrictions was applied in the G-FET channel to simultaneously obtain an impedance level of ∼50 Ω and a current ON–OFF ratio of ≥4. The mixer was realized in the airbridged CPW technology on a 100-μm highly resistive silicon substrate to avoid parasitic mode propagation. The circuit S-parameters were measured broadband up to 220 GHz to verify its operation.

The mixer CL over the RF frequency band through 185–210 GHz was measured to be 29 $\pm$ 2 dB with 12.5–11.5 dBm of LO power. The mixer shows ∼15 GHz of 3-dB IF bandwidth. These results represent the state-of-the-art performance among reported G-FET based mixers both in terms of operating frequency and performance. Our integrated mixer circuit demonstrator on silicon is a step toward the potential future utilization of CVD graphene in ubiquitous millimeter-wave and even terahertz-wave receivers. Nevertheless, material growth and transfer and G-FET process optimization are necessary to improve the mobility, contact resistance, and ON–OFF ratio. In this way, the problem of poor CL in the G-FET mixer can be amended at relaxed LO power.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. Stenarson for the assistance with the millimeter-wave measurement setup.

REFERENCES

[1] K. S. Novoselov *et al.*, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.
[2] S. O. Koswatta, A. Valdes-Garcia, M. B. Steiner, Y.-M. Lin, and P. Avouris, "Ultimate RF performance potential of carbon electronics," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2739–2750, Oct. 2011.
[3] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proc. IEEE*, vol. 101, no. 7, pp. 1567–1584, Jul. 2013.
[4] J. Wells, "Faster than fiber: The future of multi-G/s wireless," *IEEE Microw. Mag.*, vol. 10, no. 3, pp. 104–112, May 2009.
[5] R. Appleby and H. B. Wallace, "Standoff detection of weapons and contraband in the 100 GHz to 1 THz region," *IEEE Trans. Antennas Propag.*, vol. 55, no. 11, pp. 2944–2956, Nov. 2007.
[6] Y.-M. Lin *et al.*, "Wafer-scale graphene integrated circuit," *Science*, vol. 332, no. 6035, pp. 1294–1297, Jun. 2011.
[7] S.-J. Han, A. Valdes-Garcia, S. Oida, K. A. Jenkins, and W. Haensch, "Graphene radio frequency receiver integrated circuit," *Nature Commun.*, vol. 5, pp. 3086-1–3086-6, Jan. 2014.
[8] O. Habibpour, J. Vukusic, and J. Stake, "A 30-GHz integrated subharmonic mixer based on a multichannel graphene FET," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 841–847, Feb. 2013.
[9] Z. Guo *et al.*, "Record maximum oscillation frequency in C-face epitaxial graphene transistors," *Nano Lett.*, vol. 13, no. 3, pp. 942–947, 2013.
[10] C. Yu *et al.*, "Graphene amplifier MMIC on SiC substrate," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 684–687, May 2016.
[11] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier," *Electron Lett.*, vol. 48, no. 14, pp. 861–863, Jul. 2012.
[12] J. S. Moon *et al.*, "Graphene FET-based zero-bias RF to millimeter-wave detection," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1357–1359, Oct. 2012.
[13] O. Habibpour *et al.*, "Graphene FET gigabit ON–OFF keying demodulator at 96 GHz," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 333–336, Mar. 2016.
[14] M. A. Andersson and J. Stake, "An accurate empirical model based on Volterra series for FET power detectors," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1431–1441, May 2016.
[15] L. Vicarelli *et al.*, "Graphene field-effect transistors as room-temperature terahertz detectors," *Nature Mater.*, vol. 11, pp. 865–871, Sep. 2012.
[16] A. Zak *et al.*, "Antenna-integrated 0.6 THz FET direct detectors based on CVD graphene," *Nano Lett.*, vol. 14, no. 10, pp. 5834–5838, 2014.
[17] J. S. Moon *et al.*, "Graphene FETs for zero-bias linear resistive FET mixers," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 465–467, Mar. 2013.
[18] H. Lyu *et al.*, "Double-balanced graphene integrated mixer with outstanding linearity," *Nano Lett.*, vol. 15, no. 10, pp. 6677–6682, Sep. 2015.
[19] O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland, and J. Stake, "A subharmonic graphene FET mixer," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 71–73, Jan. 2012.
[20] L. A. Samoska, "An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 9–24, Sep. 2011.
[21] W. R. Deal, "Coplanar waveguide basics for MMIC and PCB design," *IEEE Microw. Mag.*, vol. 9, no. 4, pp. 120–133, Aug. 2008.
[22] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Norwood, MA, USA: Artech House, 2003.
[23] Y. Zhang, M. A. Andersson, and J. Stake, "A 200 GHz CVD graphene FET based resistive subharmonic mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.
[24] S. E. Gunnarsson, N. Wadefalk, I. Angelov, H. Zirath, I. Kallfass, and A. Leuther, "A 220 GHz (G-band) microstrip MMIC single-ended resistive mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 3, pp. 215–217, Mar. 2008.
[25] B. Khamaisi and E. Socher, "130-320-GHz CMOS harmonic down-converters around and above the cutoff frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2275–2288, Jul. 2015.
[26] N. Petrone, I. Meric, T. Chari, K. L. Shepard, and J. Hone, "Graphene field-effect transistors for radio-frequency flexible electronics," *IEEE J. Electron Devices Soc.*, vol. 3, no. 1, pp. 44–48, Jan. 2015.
[27] H. Madan *et al.*, "Record high conversion gain ambipolar graphene mixer at 10GHz using scaled gate oxide," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2012, pp. 4.3.1–4.3.4.
[28] H. Zirath, "A subharmonically pumped resistive dual-HEMT-mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jul. 1991, pp. 875–878.
[29] K. Yhland, "Simplified analysis of resistive mixers," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 604–606, Aug. 2007.

[30] Y. Lu, B. Goldsmith, D. R. Strachan, J. H. Lim, Z. Luo, and A. T. C. Johnson, "High-on/off-ratio graphene nanoconstriction field-effect transistor," *Small*, vol. 6, no. 23, pp. 2748–2754, Dec. 2010.
[31] O. Habibpour, J. Vukusic, and J. Stake, "A large-signal graphene FET model," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 968–975, Apr. 2012.
[32] F. Schnieder, T. Tischler, and W. Heinrich, "Modeling dispersion and radiation characteristics of conductor-backed CPW with finite ground width," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 1, pp. 137–143, Jan. 2003.
[33] K. Reimann, R. Kiewitt, M. Matters-Kammerer, and R. Pietig, "Multiport S-parameter measurements of linear circuits with open ports," *IEEE Trans. Instrum. Meas.*, vol. 55, no. 5, pp. 1767–1771, Oct. 2006.
[34] O. Inac, A. Fung, and G. M. Rebeiz, "Double-balanced 130–180 GHz passive and balanced 145–165 GHz active mixers in 45 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2011, pp. 1–4.
[35] S. E. Gunnarsson *et al.*, "A 220 GHz single-chip receiver MMIC with integrated antenna," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 4, pp. 284–286, Apr. 2008.
[36] I. Mehdi *et al.*, "Improved 240-GHz subharmonically pumped planar Schottky diode mixers for space-borne applications," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 12, pp. 2036–2042, Dec. 1998.
[37] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Resistive graphene FET subharmonic mixers: Noise and linearity assessment," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4035–4042, Dec. 2012.
[38] C. Vazquez-Antuña *et al.*, "High-order subharmonic millimeter-wave mixer based on few-layer graphene," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1361–1369, Apr. 2015.

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