

Output Impedance Mismatch Effects on the Linearity Performance of Digitally Predistorted Power Amplifiers

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Abstract—This paper analyzes the effects of load impedance mismatch in power amplifiers which linearity has been enhanced using various digital predistortion (DPD) algorithms. Two different power amplifier architectures are considered: a class AB and a Doherty amplifier and three model structures for the DPD model are compared: memoryless polynomial (MLP), general memory polynomial (GMP) and Kautz-Volterra functions (KV). This paper provides a sensitivity analysis of the linearized amplifiers under load mismatch conditions and reports the performance when dynamic parameter identification for the DPD is used to compensate for the changes in the load impedance. In general, power amplifiers linearity is sensitive to load impedance mismatch. Linearity may degrade as much as 10 dB (in normalized mean square error) according to the magnitude and the phase of the reflection coefficient provided by the load impedance. However, depending on the amplifier design, the sensitivity to load impedance mismatch varies. While the Doherty amplifier studied show significant linearity degradations in the in-band and out-of-band distortions, the out-of-band distortions of the studied class AB were less sensitive to the load impedance mismatch. In adaptive DPD schemes, the performance obtained in the MLP model does not benefit from the updating scheme and the performance achieved is similar to a static case, where no updates are made. This stresses the memory requirements in the predistorter. When employing the GMP and the KV models in an adaptive DPD scheme, they tackle to a larger extent the linearity degradations due to load impedance mismatch.

Index Terms—Digital predistortion, impedance mismatch, load impedance, power amplifiers.

I. INTRODUCTION

POWER amplifiers are one of the main building blocks in wireless networks, because they spend a significant portion of the total energy in the network. In addition, power amplifiers are one of the main contributors to nonlinear distortions in the system. These nonlinear distortions decrease the overall

throughput and capacity of the network. Therefore, the enhancement of amplifier performance has been a subject of intense research for the last several decades.

One of the most attractive and extended techniques to improve amplifier performance is digital predistortion (DPD). DPD is implemented entirely in digital platforms and is flexible, inexpensive, and easy to implement. DPD enhances amplifier linearity and enables its operation at higher power levels, which improves its energy efficiency [1]. Several forms of DPD have been proposed in the literature (see [2] and [3] and references therein). Predistorters compensate nonlinear effects presented in the transmitter, such that, the tandem connection of the predistorter and amplifier is a linear function. Predistorters are constructed in various ways e.g., as Volterra models [4] and pruned forms of Volterra series, as generalized memory polynomials (GMP) [5], and dynamic deviation reduction models [1], [6]. In addition, artificial neural networks [7], [8] and separable basis functions [9] are examples of different forms of predistorter models.

Despite large research efforts aimed at studying DPD techniques, the vast majority of these techniques have been tested under match impedance conditions. In match conditions, the impedance of the load (antenna) that is connected to the amplifier is the conjugate of the output impedance of the amplifier. Hence, the maximum power transfer is achieved [10]. In this case, the antenna absorbs all the incoming power, and zero reflections are returned to the amplifier. An impedance mismatch is defined as a deviation from the ideal impedance value. A load impedance mismatch creates reflections, which travel back to the amplifier and affect its behavior. A load impedance mismatch may appear because of faulty cables and transmission lines or because of objects located near the antenna creating coupling effects and altering antenna properties. The latter is a well-known problem in the cellphone manufacturing industry [11].

Load impedance mismatch can be avoided by using an isolator at the amplifier output; as the reflected waves will be absorbed by the termination load in the isolator [10]. However, isolators are not desired at the output of amplifiers because they are expensive and because they can be associated with nonlinear distortions [12]. Furthermore, the forthcoming multiband communication scenarios may require the isolator to operate in several frequency bands, causing design challenges and increased cost [13]. For these reasons, this paper studies an isolator-free scenario.

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In general, the load impedance mismatch at the amplifier degrades the performance of a wireless network. First, by shrinking the coverage as total radiated power reduces. Secondly, by decreasing the throughput because the amplifier changes its operating point and may produce significant amount of nonlinear distortions [14]. Moreover, an amplifier in load impedance mismatch may reduce its efficiency [15]. In summary, the effects of the load impedance mismatch may oppose the benefits obtained by using a DPD technique. Thus, when a load impedance mismatch occurs, a DPD-enhanced amplifier may present severe degradations such that the DPD has a negative effect over the linearity of the transmitter [14].

A study of the effects of load impedance mismatch in different amplifier architectures was presented in [16], but the study did not include linearization techniques as DPD for the amplifiers. A sensitivity study of a DPD-linearized amplifier under mismatch conditions [14] showed large variations for different load impedances. However, the DPD model studied was a memoryless polynomial (MLP), which is not currently a state-of-the-art linearization model. Several DPD models are more powerful for amplifier linearization (see [17] and references therein). The authors in [18] analyzed the effect of load mismatch in a DPD-enhanced Doherty amplifier. The results were obtained using a black-box simulation of the amplifier under load mismatch conditions. The drawback of this approach is that a black-box model of the amplifier may not be valid for different load impedances used in the simulation, as shown in [19]. Although the control or “knowledge” of the load impedance may yield improved linearization techniques [14], [20], this paper studies the performance of different DPD algorithms when no information of the load impedance is available for the DPD algorithm.

Advanced solid state and integrated switching techniques may mitigate the output impedance mismatch in an amplifier by permitting the design of switchable matching networks that compensate for the mismatch. However, inexpensive sensing solutions and mitigation schemes must be developed to this end. While this area is actively researched [14], [15], [21], [22], few measurement results of the interaction between DPD and load impedance mismatch are available. This paper attempts to fill in the gap of knowledge for the interaction between DPD linearization techniques and load impedance mismatch at the amplifier output. In particular, relating the DPD model structure, which could include memory effects of different orders of magnitude. This paper reports the effects of various DPD techniques under load impedance mismatch when applied to different power amplifier architectures. The present paper builds on [19] and contrasts three different types of DPD models: an MLP, a GMP [5], and a Kautz-Volterra (KV) model [23] for two different power amplifier architectures: a class AB amplifier and a Doherty amplifier [24].

Two aspects are addressed in the present paper. First, the sensitivity of a DPD-linearized amplifier to variations of its load impedance is addressed. In this scenario, the DPD remains unchanged while the load impedance varies. Thus, we can compare the behavior of the different DPD models and its robustness to load impedance mismatch. Secondly, the paper studies the performance convergence of an adaptive DPD scheme for

an amplifier subjected to variations of the load impedance. In this second scenario, the DPD parameters are updated for each load impedance. Thus, from a linearity perspective, the steady state performance indicates how well the DPD models cope with a load impedance mismatch in the amplifier. Furthermore, we compare two different hardware amplifiers architectures that are widely used.

This paper outlines as follow: Section II reviews the relevant background, and discusses the effects of load impedance mismatch at the amplifier, particularly, for the class AB and Doherty. Further, Section II lists amplifier evaluation metrics and covers the different DPD techniques studied. Section III describes the measurement test setup and the methodology used in the experiments. The results and analysis are presented in Section IV. Finally, discussions and conclusions are provided in Section V and VI.

II. THEORY

This papers studies two types of power amplifiers architectures: A class AB and a Doherty. Despite the design differences from 1 transistor design of the class AB to a 2 transistors parallel design of the Doherty, the main difference is that Doherty have higher efficiency than class AB.

A. Power Amplifier Design

In general, power amplifier design involves the tradeoff between different metrics, i.e., gain, noise, output power, nonlinear distortion and efficiency. Unfortunately, these metrics are optimal at different transistor load impedance values, which has been empirically observed using load pull techniques in both AB [25]–[27] and Doherty design [28], [29]. Hence, the power amplifier designer must choose the load impedance at transistor levels compromising between these metrics. Since a load impedance mismatch at the amplifier varies the designed transistor load impedance, it affects the designed amplifier behavior.

B. Class AB Operation

In the following, the relationship of the load impedance to a class AB Field Effect Transistor (FET) amplifier operation is discussed. The analysis is not meant to be precise, this task is by far complex and out of the scope of this paper. However, the model seeks to be descriptive for the effects of load impedance mismatch. A simple model amenable for analysis, has been derived in [30] for a general AB amplifier under the following assumptions: linear input and output matching networks, unilateral FET transistor working in its active region with low output conductance. This model has an equivalent Thevenin impedance Z_{Tran} at the transistor load. This model is depicted in Fig. 1(a). The input signal $RF_{\text{in}} = \text{Re}\{u(t)|e^{j(\omega_c t + \angle(u(t)))}\}$, is a modulated wave by the base-band signal $u(t)$ at a carrier frequency ω_c .

Under these assumptions, the drain source voltage V_{DS} is approximated by

$$V_{\text{DS}}(t) = V_{\text{D}} - C_{\text{v}} \int_0^{\tau} Z_{\text{Tran}}(\tau) |u(t - \tau)| d\tau \quad (1)$$

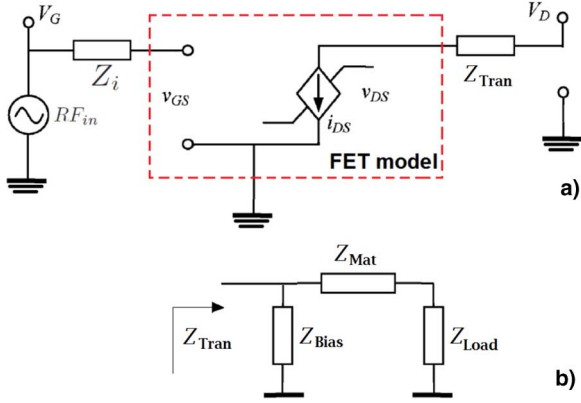


Fig. 1. (a) Circuitual model of a class AB amplifier using a FET transistor. (b) Thevenin load impedance model at the transistor level Z_{Tran} .

with C_v a positive constant accounting for the voltage to current amplification of the FET (from the gate voltage to the drain current) and V_D the drain voltage. Z_{Tran} denotes the Thevenin load impedance seen by the FET transistor and it is composed by the impedance of the bias network Z_{Bias} , the output matching network Z_{Mat} and the load impedance at the amplifier Z_{Load} as depicted in Fig. 1(b)

$$Z_{Tran} = Z_{Bias} \parallel (Z_{Mat} + Z_{Load}) \quad (2)$$

with \parallel denoting a parallel connection. Consider the fundamental current at the FET drain $I_F(t)$ as a polynomial expansion of the form

$$I_F(t) = \sum_{p=1}^P C_{i,p} [1 + \gamma_p V_{DS}(t)] u^p(t) \quad (3)$$

with $C_{i,p}$ being a positive constant that models the output current gain and γ_p describe the effect of the FET output conductance at the p -th harmonic of the input signal. P is the non-linear order considered in the polynomial. Substituting (1) into (3) yields a expression of the fundamental current

$$I_F(t) = C_{S,1} u(t) + \sum_{p=2}^P C_{S,p} u^p(t) + \dots + \sum_{p=1}^P C_{N,p} u^p(t) \int_0^\tau Z_{Tran}(\tau) |u(t - \tau)| d\tau \quad (4)$$

with $C_{S,p} = C_{i,p}(1 + \gamma_p V_D)$ and $C_{N,p} = C_{i,p} \gamma_p C_v$. The linear behavior is described by the first term in (4), while the nonlinear behavior is captured by the second and third terms. Some static nonlinear behavior does not interact with the load impedance as indicated in the second term in (4). On the other hand, nonlinear dynamic behavior interacts with load impedance, as indicated in the last term in (4). The dynamic nonlinear behavior is scaled by transistor physical constants here described by $C_{N,p}$. From (4), it follows that a frequency flat load impedance $Z_{Tran}(\tau)$ produces only static nonlinear behavior, while a dynamic impedance $Z_{Tran}(\tau)$ contributes to the nonlinear dynamics, such as, memory effects or asymmetric spectral components [31].

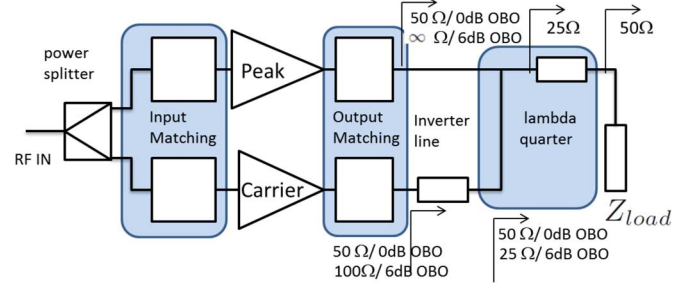


Fig. 2. Schematic of a Doherty amplifier.

The effects caused by the amplifier load impedance Z_{Load} can be studied by analyzing the variations of Z_{Tran} . This requires knowledge of the output matching network and of the bias circuitry as indicated by (2). Typically in a class AB design, the bias network impedance Z_{Bias} (at the fundamental) is an order of magnitude larger than the cascade impedance of the output matching network Z_{Mat} and load impedance Z_{Load} [32]. Thus, variations of the amplifier load impedance Z_{Load} at the fundamental frequency interact significantly with the output matching network, but less with the bias network. Thus, the transistor load impedance Z_{Tran} can be approximated by the cascade connection of the output matching network and the amplifier load impedance, that is, $Z_{Tran} \approx Z_{Mat} + Z_{Load}$. Thus, the S-parameters of the output matching network can be used to de-embedded the effect of the amplifier load impedance [10], this procedure will be exploited to analyze measured results.

Summarizing, the effects of load impedance mismatch in an AB FET amplifier depend on: i) its physical constants, described by $C_{N,p}$ in (4), ii) bias network impedance, and iii) output matching network impedance. However, at the fundamental frequency, the impact of output matching network impedance is significantly larger than the one of the bias network.

C. Doherty Operation

The Doherty amplifier is based on two power transistors working in parallel, as depicted in Fig. 2. Typically, the first one, referred to as ‘‘carrier amplifier’’ is biased for a linear operation such as class-AB mode, while the second one, called ‘‘peaking amplifier’’ is operated as a Class-C.

The operation of the Doherty amplifier divides the input voltage in two regions. The low input voltage, from $-\infty$ to 6 dB output power back off (OBO) and the high input voltage region from 6 dB to 0 dB of OBO. In the low input voltage region, the carrier amplifier operates normally with double output impedance, while the peak amplifier does not operate and its load impedance is large. In the higher input voltage region, the peak amplifier starts operating, thereby, loading the carrier amplifier [32]. The peak amplifier output impedance reduces in this region towards the nominal value at highest output power, while the carrier amplifier output impedance goes from double towards the nominal value at highest output power [33]. This is depicted in Fig. 2 for a nominal impedance of 50 Ohm. In the load modulation process previously described, the amplifiers output impedance change along real values only.

Load impedance mismatches at the Doherty amplifier will severely affect the load modulation principle. Thereby, reducing the amplifier efficiency. Furthermore, output matching networks in Doherty amplifiers are optimized for linearity [34]. In consequence, the load mismatch alters the design impedance of these matching networks and affects linearity. When the carrier Doherty amplifier is a class AB, the previous analysis of impedance mismatch is applicable for low input voltage region. However, as the input voltage increases, the load modulating the carrier amplifier deviates from the desired value, particularly, reaching impedance values with significant reactive part which creates dynamic effects from the unbalanced loading [32].

D. Thermal Effects

An amplifier load impedance mismatch causes a variation of the output power. Thereby, altering its thermal equilibrium. Since thermal behavior and amplifier memory effects are intrinsically related [31], [35], the load impedance mismatch changes the amplifier memory effects. Thus, under load impedance mismatch, the DPD models require adaptivity to cope with the variations of the memory effects. While, thermal memory effects in the amplifier are difficult to quantify and isolate (from the electrical memory effects), this paper reports the linearity degradations observed under static and adaptive DPD.

E. DPD Models

Amplifiers are weakly nonlinear systems with fading memory. Hence, amplifiers are well represented using Volterra series [4]. Volterra series deals with real-valued bandpass input and output signals. However, standard amplifier instrumentation provides measurements in the complex-valued baseband domain. An equivalent representation of the Volterra series using complex-valued baseband signals has been developed [36] and shows that the equivalent baseband Volterra representations are possible using only odd nonlinear orders. Thus, the DPD models studied contain only odd nonlinear orders. A description of those models is provided in the following.

Let $u(n)$ and $y(n)$ denote the input and output complex-valued baseband measured sequences from the amplifier, with n as the normalized sampled instant $n = 0, 1, \dots, N - 1$.

1) *Memoryless Polynomial (MLP)*: A memoryless polynomial MLP model is described as

$$y(n) = \sum_{p=1}^{\lfloor \frac{P+1}{2} \rfloor} h_{2p-1} u(n) |u(n)|^{2(p-1)} \quad (5)$$

where h_{2p-1} are the model parameters, and P is the nonlinear model order.

2) *General Memory Polynomial (GMP)*: A GMP model is described by the input output relationship [5]

$$y(n) = \sum_{p=1}^{\lfloor \frac{P+1}{2} \rfloor} \sum_{m_1, m_2}^{M_1, M_2} h_{2p-1}^{(m_1, m_2)} u(n - m_1) |u(n - m_1 - m_2)|^{2(p-1)} \quad (6)$$

where $\sum_{m_1, m_2}^{M_1, M_2}$ is a short notation for the double sum over m_1 and m_2 , respectively. M_1 and M_2 denote the memory depths,

$h_{2p-1}^{(m_1, m_2)}$ are the model parameters, and P is the nonlinear model order.

3) *Kautz-Volterra (KV)*: A Kautz-Volterra (KV) model is represented as [37]

$$\begin{aligned} y[n] = & \sum_{l=1}^{N_1} h_1^l x_{1,l}(n) \\ & + \dots \sum_{l_1, l_2, l_3=1}^{N_3} h_3^{(l_1, l_2, l_3)} x_{3,l_1}(n) x_{3,l_2}(n) x_{3,l_3}^*(n) \\ & + \dots \sum_{l_1, l_2, \dots, l_p=1}^{N_p} h_p^{(l_1, l_2, \dots, l_p)} x_{p,l_1}(n) \\ & \dots x_{p, l_{(p+1)/2}}(n) x_{p, l_{\frac{(p+3)}{2}}}^*(n) \dots x_{p, l_p}^*(n) \end{aligned} \quad (7)$$

where p denotes the nonlinear model order, N_p represents the number of basis functions of the p -th nonlinear model order. \sum_{l_1, \dots, l_p} is a short notation for the multiple sum over l_1, l_2 up to l_p . Further, $x_{i,l}(n)$ is the output of the filter with transfer function $\mathbf{G}_{i,l}(z)$

$$\mathbf{G}_{i,l}(z) = \sqrt{1 - |\xi_l|^2} \frac{z}{z - \xi_l} \prod_{q=1}^{l-1} \frac{(1 - \xi_q^* z)}{z - \xi_q} \quad (8)$$

and excited with input $u(n)$, $l = 1, 2, \dots, N_p$.

The GMP model subsumes the MLP model, since the GMP becomes MLP when no memory is considered. Additionally, the KV model subsumes the GMP model, because the KV model transforms to a Volterra series when the poles of the KV functions are located at the origin ($\xi_l = 0$). Hence, the KV model subsumes both the MLP and GMP models. However, the parameter identification technique of the KV model is different from the technique used for MLP and GMP models. In the following section, the parameter identification techniques for these three model structures are revised.

Note that, the GMP model has been physically motivated in the class AB power amplifier [30], where memory effects were assumed to appear due to the thermal effects, bias and output matching networks.

F. System Identification

The predistorter parameters of the models described above are computed interchanging the input with the output, in the framework of the indirect learning architecture [3], by which the postdistorter is used as a predistorter, as previously noted [4], [9].

Note that the MLP and GMP models are linear in the parameters. Thus, the parameters in MLP and GMP models can be computed using least square (LS) approaches [38]

$$\hat{\boldsymbol{\theta}} = (\boldsymbol{\Psi}^H \boldsymbol{\Psi})^{-1} \boldsymbol{\Psi}^H \mathbf{u} \quad (9)$$

where $\boldsymbol{\theta}$ is the vector containing the parameters we wish to estimate. The regression matrix $\boldsymbol{\Psi}$ is a function of the output sampled sequence $\boldsymbol{\Psi} = f(\mathbf{y})$, where \mathbf{u} and \mathbf{y} denote $N \times 1$ complex vectors containing the input and output sampled sequences, respectively.

For the KV model, estimating the poles ξ_q is nonlinear, while estimating $h_i^{(l_1, l_2, \dots, l_i)}$ is a linear problem. The pole estimation is tackled using a grid search in the bounded and stable pole space (complex numbers in the unit circle). The performance is recorded for every pole tested using LS techniques to compute $h_i^{(l_1, l_2, \dots, l_i)}$. Finally, the pole with the lowest model error is selected. This process is repeated in ascending order for all nonlinear orders in the model. Once the poles are fixed, linear identification techniques such as LS can be used for the estimation of the parameters $h_i^{(l_1, l_2, \dots, l_i)}$.

G. Figures of Merit

The DPD performance results are presented in terms of the normalized mean-square error (NMSE) and the adjacent channel power ratio (ACPR). The NMSE is computed as [17]

$$\text{NMSE} = \frac{\int \Phi_e(f) df}{\int \Phi_y(f) df} \quad (10)$$

where $\Phi_e(f)$ and $\Phi_y(f)$ are the power spectrum of the error signal $e(n)$ and the output signal $y(n)$, respectively. The error signal is defined as the difference between the output and the ideally amplified input. The integrations are performed across the complete available bandwidth.

The ACPR is computed as [17]

$$\text{ACPR} = \frac{\int_{\text{adj. ch.}} \Phi_y(f) df}{\int_{\text{ch.}} \Phi_y(f) df} \quad (11)$$

where the numerator integral is performed across the adjacent channel with the largest amount of power and the denominator integrates over the channel band.

The power added efficiency (PAE) of the amplifier is defined by [32]

$$\text{PAE} = \left(\frac{P_{RFout} - P_{RFin}}{P_{DC}} \right) 100\% \quad (12)$$

where P_{RFout} and P_{RFin} are the average output and input power of the amplifier, respectively, and P_{DC} is the power delivered by the power supply.

III. EXPERIMENTAL

A. Measurement Setup

A block diagram of the measurement setup is depicted in Fig. 3. While the actual measurement system is shown in Fig. 4. This setup is composed by a R&S SMU 200A vector signal generator (VSG) and a power amplifier connected in tandem. The output of the power amplifier is followed by a 3 dB attenuator and of an in-house designed triplexer, which separates the fundamental signal from the harmonics signals. The harmonic signals are then terminated by 50 Ohm loads. The signal around the fundamental frequency is fed to a mechanical tuner MT982E30 from Maury microwave that controls the load impedance. This signal is measured using a 20 dB directive coupler and a R&S FSQ 26 vector signal analyzer (VSA). This setup mimics the standard operating conditions of a feedback loop of DPD-linearized power amplifiers.

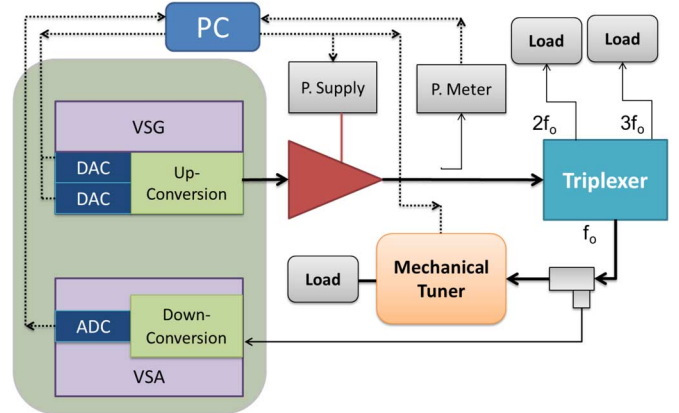


Fig. 3. Block diagram of the measurement setup used in the experiments.

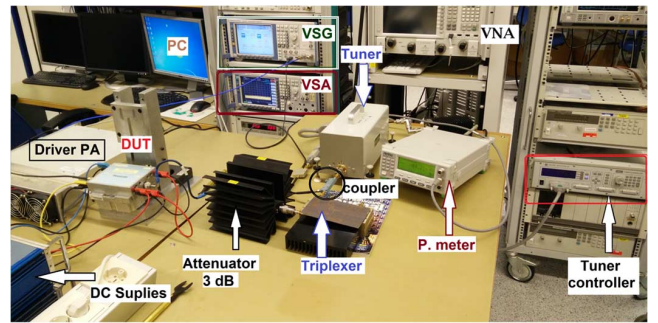


Fig. 4. Measurement setup used in the experiments.

By terminating the harmonics through the triplexer, the present study considers only the in-band mismatch impedance. Although techniques exist for amplifier enhancement using harmonics' impedances [39], [40], they are out of the scope of this paper.

A total of 106 load impedance values covering uniformly the Smith-chart region with $RL \leq 9$ dB ($VSWR \leq 2.1$) were randomly selected to perform the experiments. The impedances in Fig. 5 were characterized using a calibrated vector network analyzer (VNA) N5242-A from Agilent. This characterization takes into account the effects of the triplexer, attenuator, coupler, cables and terminations, and represents the impedance encountered at the output of the amplifier.

The excitation signal was a 225-tone with random phases with peak-to-average power ratio of 7.8 dB using a 4.8 MHz bandwidth. This signal was created digitally using 16000 complex-valued samples that were uploaded to the generator and upconverted to 2.1 GHz to excite the power amplifier. The same signal was used during all experiments. The amplifiers tested were: a class AB base station LDMOS power amplifier intended for 3G operation from Ericsson AB with a total of 52 dB linear gain, rated at 52 dBm output power in compression, and a MRF8S21120HS Doherty amplifier from Freescale with 14 dB linear gain and rated at 46 dBm output power in compression. Both amplifiers are shown in Fig. 6. The Doherty amplifier requires the use of a linear driver amplifier that is not included in Fig. 3 for clarity.

During the measurement process, the time delay of the signal between the generator and analyzer was compensated digitally.

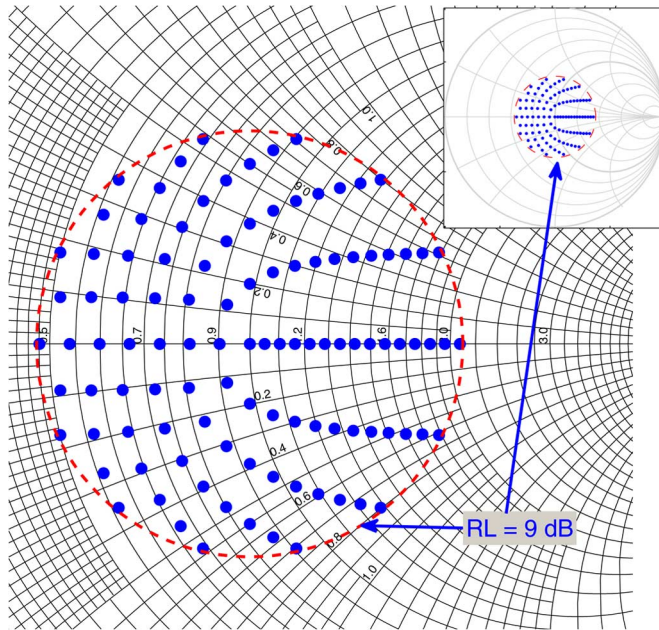


Fig. 5. Grid of load impedance points to test DPD enhanced amplifiers.

TABLE I
SETTINGS OF THE DPD MODELS

DPD Model	Memory	Order	Number of parameters	Estimation
Memoryless polynomial (MLP)	0	7	7	LS
General Memory polynomial (GMP)	$M_1 = 2,$ $M_2 = 2$	7	21	LS
Kautz-Volterra (KV)	$N_i = 1,$ $i = 1, \dots, 7$	7	40 (lin.) 4 (nonlin.)	LS pole search

TABLE II
PERFORMANCE OF THE LINEARIZED AMPLIFIERS IN
50 Ω MATCHED CONDITIONS

Amplifier		No DPD	DPD		
			MLP	GMP	KV
AB	NMSE (dB)	-32	-40	-49	-49
	ACPR (dB)	-41	-55	-62	-61
Doherty	NMSE (dB)	-27	-35	-43	-44
	ACPR (dB)	-35	-41	-54	-52

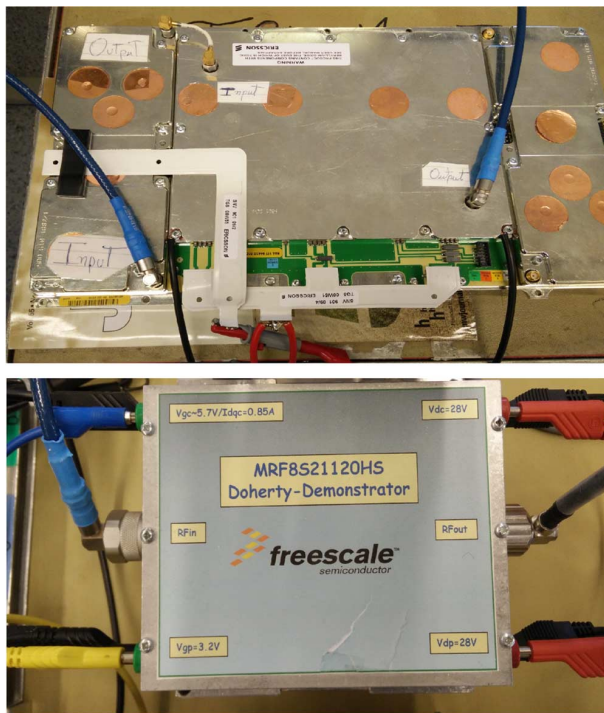


Fig. 6. Power amplifiers used in the experiments. (a) Two-stage class AB amplifier. (b) Doherty amplifier.

The evaluation was made on validation data; from the measured 16000 complex-valued samples, the DPD parameter estimation used a 65% of the sequence while the remaining 35% was used to compute the NMSE and ACPR. An iterative DPD is implemented, to produce reliable linearization results [41]. Further, the variations of the controlled load impedance in 12 MHz frequency band around 2.1 GHz were below 15% of the value of

the reflection coefficient. For simplicity, we refer only the load impedance value at 2.1 GHz.

B. Methodology

Different DPD models can be compared in different forms e.g., performance [17], or complexity [42]. In this paper, a different approach is preferred. We selected the DPD models that are extensively used with different modeling properties and computationally different, to illustrate the differences that can be encountered in practice due to this choice.

For the linearity comparisons presented in this paper, we set a fixed input power level for all the tested mismatch conditions. The input power was different for the two power amplifiers and corresponds to a 6.5 dB input back off.

Table I indicates the settings of the three different DPD models tested in this study. All models use nonlinear order 7. However, these models differ in memory, number of parameters and parameter estimation techniques. Table II shows the performance of these three DPD models, in NMSE and ACPR when applied to the power amplifiers. The DPD parameters were obtained in a matched scenario where nearly zero reflections were at the output of the amplifier (c.f. Fig. 3).

As seen in Table II, the amplifiers without linearization (no DPD) present significant amount of nonlinear distortions. The use of DPD improves linearity in both amplifiers. However, DPD scheme using an MLP model, performs poorly for both types of amplifiers when compared to the other DPD models such as the GMP or the KV models. Thus, a significant amount of memory is required to produce enhanced linearization results. Finally, quantitatively, the Doherty amplifier is more difficult to linearize than the class AB as its linearity performance is lower, which may be tied to its internal hardware structure.

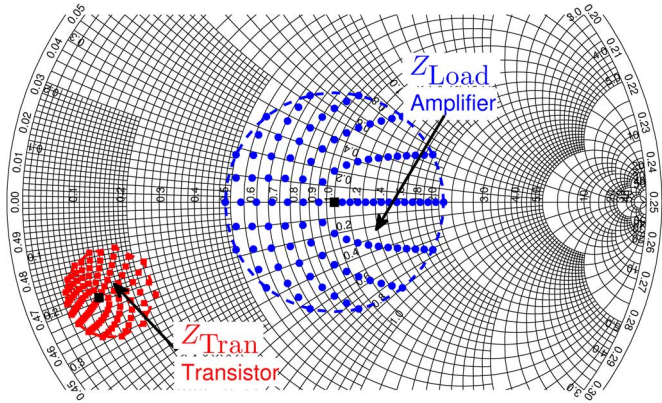


Fig. 7. Load impedance at the transistor level Z_{Tran} produced by output load at the amplifier Z_{Load} cascaded with the output matching network in the class AB amplifier.

IV. RESULTS

The output matching network of the studied class AB amplifier can be described by the following S parameters (at 2.1 GHz and 50 Ohm of characteristic impedance)

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.81\angle -148^\circ & 0.62\angle -60^\circ \\ 0.62\angle -60^\circ & 0.81\angle -148^\circ \end{bmatrix} \quad (13)$$

which were drawn from the design procedure. Cascading the amplifier load impedance Z_{Load} with this matching network produces the load impedance at the transistor depicted in Fig. 7. The impedance transformation is given by [10]

$$\Gamma_{\text{Tran}} = S_{11} + \frac{S_{12}S_{21}\Gamma_{\text{Load}}}{1 - S_{22}\Gamma_{\text{Load}}} \quad (14)$$

with Γ_{Tran} and Γ_{Load} as the reflection coefficients at transistor and amplifier loads, respectively. Notice that, the impedance scatters in a smaller region of the Smith-chart of low impedance. A decreased variation of Z_{Tran} reduces the effects of the load impedance mismatch as depicted by (4). Further, as later shown by measurements, it is plausible that the design of the amplifier was made to optimize the out-of-band error produced by the amplifier.

A. Power Added Efficiency

The PAE of the two tested power amplifiers without DPD is shown as a function of the load impedance in Fig. 8. The PAE in the class AB amplifier is not maximized at the center of the Smith-chart, as it is shown later, this amplifier was designed to minimize the level of nonlinear distortion, particularly the ACPR, in consequence compromising the efficiency c.f. Fig. 8. The PAE of the Doherty amplifier achieves maximum values at the center of the Smith-chart and decreases for increasing values of return loss. Doherty amplifiers work under the principle of load modulation; this condition is violated in load mismatches, and hence, a decrease of the efficiency is expected. However, efficiency decreases at different rates depending on the angle of the impedance tested. Similar results for Doherty amplifiers under impedance load mismatch were reported in [43].

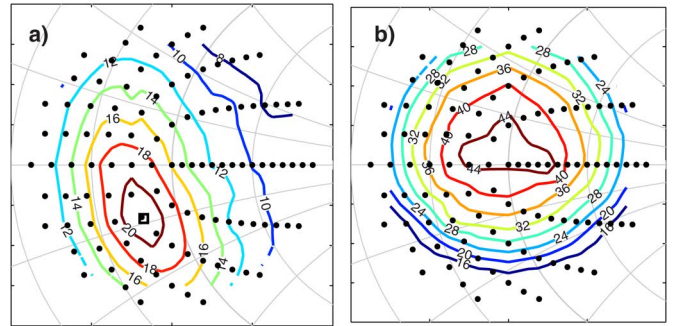


Fig. 8. Power added efficiency with respect to the load impedance variations in the two amplifiers tested. (a) class AB, contours show variations of 2% in the PAE. (b) Doherty amplifier, contours show variations of 4% in the PAE.

B. Sensitivity

The sensitivity of a DPD-linearized amplifier to load impedance mismatch is reported. We computed the DPD model parameters of the predistorter in a zero reflection scenario (match condition). Once the DPD is in operation, the load impedance is changed in a load-pull scheme. For every impedance point tested, both the NMSE and the ACPR are recorded and indicate the performance of DPD-linearized amplifier and its robustness to load impedance mismatch.

Evaluating the PAE with a DPD scheme in operation result with efficiency values similar to those presented in Fig. 8. This is of little surprise as the DPD scheme optimizes solely for linearity. Variations of the PAE are due to the nature of the power amplifier that changes its output power depending on the load impedance.

Fig. 9 shows the NMSE (in dB scale) of two different DPD models tested in the class AB power amplifier. Fig. 9 (a) and (b) plots the NMSE of the MLP model and the GMP mode, respectively. The NMSE varies considerably for different load impedance values. The NMSE is strongly dependent on both the magnitude and phase of the reflection coefficient as indicated by its variations on the Smith chart. The minimum (best) NMSE does not occur at the same load impedance for both models and does not occur at the center of the Smith chart for the MLP model. These can be attributed to the effect of the load impedance in the memory effects of the amplifier as discussed in Section II-B. Note that the load impedance will have some frequency variations, and in consequence, there may be regions in which the MLP model is more suitable. In particular, when the frequency variations are flattened by the load impedance of the amplifier reducing the memory effects. Despite of the complexity and more expressive power of the GMP model, the GMP model exhibits degradations of the same order of magnitude as the MLP model, which is a computationally simpler model and does not include memory in the DPD. However, the GMP model achieves better NMSE compared to the MLP.

Fig. 10 shows the NMSE sensitivity of the DPD-linearized Doherty amplifier. The MLP model fails to compensate for the nonlinear effects as observed in Fig. 10(a) with a relatively high NMSE. On the other hand, the GMP model has improved performance indicated with lower levels of NMSE in Fig. 10(b). However, a clear dependence exist for the NMSE and the load

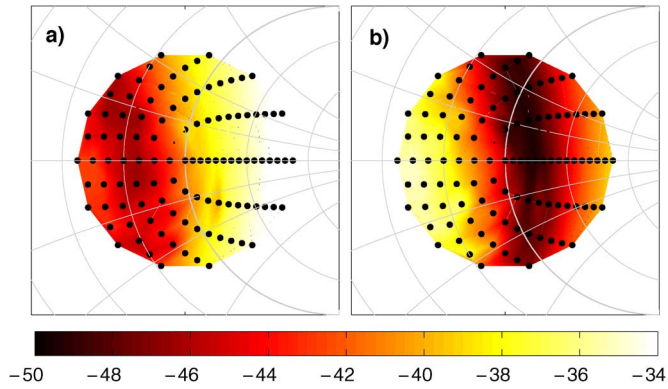


Fig. 9. NMSE for a DPD enhanced class AB power amplifier, sensitivity to changes in the load impedance. The DPD model is obtained in zero reflection. (a) MLP. (b) GMP.

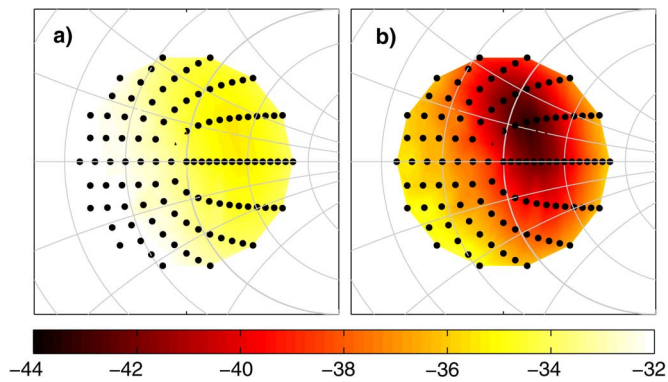


Fig. 10. NMSE for a DPD enhanced Doherty power amplifier, sensitivity to load impedance. The DPD model is obtained in zero reflection. (a) MLP. (b) GMP.

impedance. A region of the Smith chart with an angle of the reflection coefficient of approximately 45 degrees achieves lower values of NMSE. c.f. Fig. 10(b). From this result it can be understood that the Doherty amplifier has been designed to provide the best efficiency, as PAE is maximized at the center of the Smith-chart (c.f. Fig. 8), while the linearity has been trade-off.

Fig. 11 shows the ACPR sensitivity to load impedance mismatch in a class AB DPD-linearized power amplifier. Each point in Fig. 11 represents a distinct load impedance. Despite that the ACPR levels of the two DPD models are significantly different, minor variations of the ACPR for different load impedances exist in the same DPD model. The AB amplifier without DPD exhibits an ACPR of -41 dB (noted in Table II). As noted in Fig. 11, the improvement in the out-of-band emissions obtained by the DPD is maintained regardless of the load impedance mismatch. Hence, the DPD-linearized class AB amplifier is robust when considering the out-of-band error (c.f. Fig. 11). Thus, class AB amplifier design which is robust to impedance variations is feasible.

This is an important difference with the linearized Doherty amplifier, as the ACPR varies with the load impedance as shown in Fig. 12. The memoryless polynomial MLP model in the linearized Doherty amplifier does not correctly suppress the nonlinear effects appearing at the out-of-band, as shown in Fig. 12(a). The ACPR of the GMP linearized Doherty amplifier

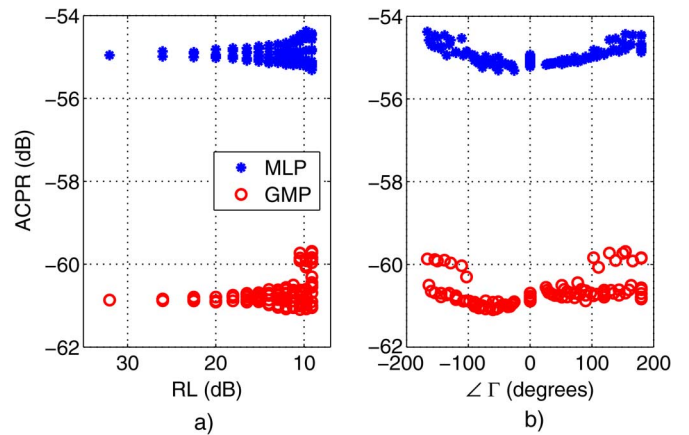


Fig. 11. ACPR of an DPD enhanced AB amplifier, two DPD models tested: an MLP and a GMP model. The DPD model obtained in zero reflection. (a) ACPR versus Return Loss. (b) ACPR versus phase of the reflection coefficient.

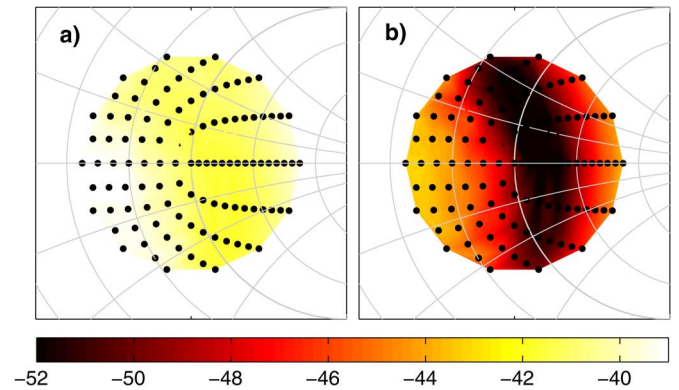


Fig. 12. ACPR of a DPD Doherty power amplifier, sensitivity to load impedance. The DPD model obtained in zero reflection. (a) MLP. (b) GMP.

is depicted in Fig. 12(b). Compared to the class AB amplifier, the Doherty type exhibits an ACPR that is impedance dependent. Several load impedances degrade the ACPR by as much as 10 dB compared to the level obtained at zero reflections (in the center of the Smith Chart).

In summary, under load impedance mismatch conditions, the linearized AB amplifier exhibits large variations of the in-band error (NMSE). However, due to its design, the same amplifier is robust to impedance mismatch conditions for the out-of-band error (ACPR). Therefore, AB amplifier architecture may be considered when out-of-band emissions and load impedance mismatches may occur. The minimization of the out-of-band error or any other metric can be done using load pull techniques [27]. These techniques can also provide, in the form of contours, the sensitivity to load impedance variations. For the DPD-linearized Doherty amplifier, both the NMSE and ACPR are vastly affected by load impedance mismatches, which is expected from the dynamic load modulation principle under which Doherty operates.

The performance of a DPD-linearized amplifier depends not only on the magnitude of the reflection coefficient Γ but also on its phase. This observation can be further exploited to design linearity mitigation techniques to handle load impedance mismatch. For instance, a phase shifting device at the output of the

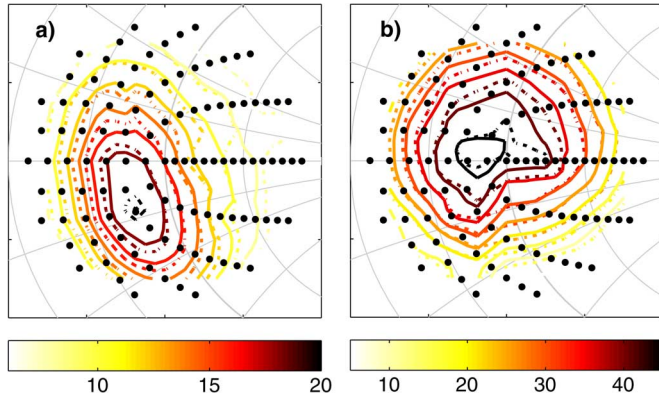


Fig. 13. PAE of the linearized amplifiers using 2 DPD models: MLP (dashed) and GMP (solid). (a) class AB power amplifier, 2% PAE variations. (b) Doherty amplifier, 4% PAE variations.

amplifier may aim to change the load impedance towards values that simultaneously minimize the NMSE and the ACPR [28].

We test a DPD using a Kautz-Volterra (KV) model for both types of amplifiers. The sensitivity results obtained for the KV model are similar to those presented for the GMP model in this section.

C. Adaptivity

The performance convergence of an adaptive DPD scheme under load impedance variations is reported in this section. In this scenario, it is assumed that the DPD parameters are continuously updated to maximize linearity in the amplifier. The updates are achieved by repeating the identification stage described in Section II during amplifier operation. We update the DPD model parameters as the load impedance changes using an iterative scheme [41]. The performance obtained after the DPD scheme has reached its steady state behavior is then recorded.

When using the adaptive scheme in the DPD, the efficiency (PAE) of the two tested amplifiers for the MLP and the GMP models is shown in Fig. 13. In both amplifiers tested, the PAE is strongly dependent on the load impedance but appear to be less dependent on the DPD model used c.f. Fig. 8. On the other hand, PAE variations between different DPD models are related to the change in the input signal statistics produced by a specific model. From Fig. 13, it can be seen that the MLP model shows slightly higher efficiency, around 2% or 3%, than the GMP model. However, the MLP shows poor linearity results.

Fig. 14 plots the converged NMSE of the DPD-linearized AB power amplifier. Two DPD models are compared: the MLP model in Fig. 14(a) and the GMP model in Fig. 14(b).

Comparing Fig. 9(a) with Fig. 14(a), updating of the DPD parameters in the MLP model provides only a minor performance improvement of the NMSE. Furthermore, the performance of the MLP class AB amplifier remains nearly the same even if the parameters of the DPD are updated to cope with the linearity degradations that appear due to load impedance mismatch. From the model of the AB amplifier (4), the dynamic nonlinear behavior in the amplifier is represented by the convolution of the Thevenin impedance and the envelope of the input signal. Thus, dynamic behavior of the bias or output matching network will be uncompensated in the model regardless of its adaptivity. This

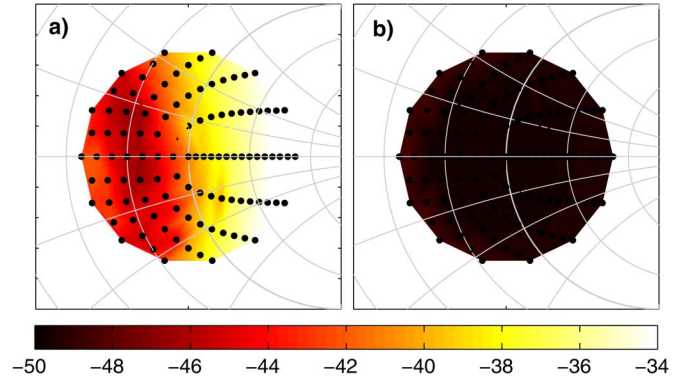


Fig. 14. Converged NMSE of an adaptive DPD when used in a class AB amplifier. (a) MLP. (b) GMP.

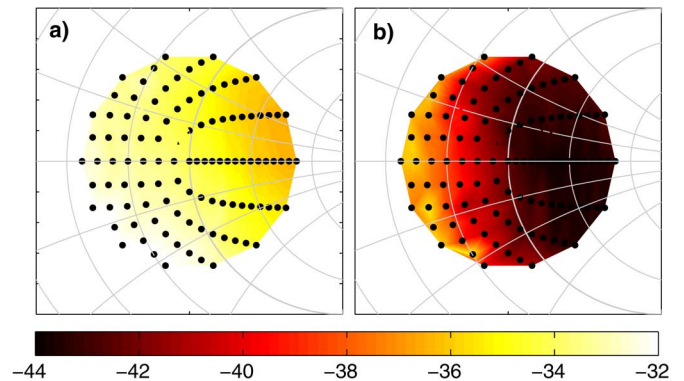


Fig. 15. Converged NMSE of an adaptive DPD applied to a Doherty amplifier under load impedance changes. (a) MLP. (b) GMP.

agrees with measured results in Fig. 9(a) and Fig. 14(a). Hence, from the linearity perspective, the MLP model is not a good candidate when load impedance mismatches are likely to occur.

Fig. 14(b) shows the converged NMSE of the DPD with a GMP model in the AB amplifier. The NMSE was lower compared to Fig. 9(b) where no update were performed for the DPD parameters. Updating the GMP parameters provides enhanced NMSE regardless of the load impedance tested, as observed in the Smith chart in Fig. 14(b) and suggest that the GMP model structure is expressive enough to describe the behavior of amplifier when the load impedance varies. this is in accordance with the physical motivation of the GMP model in class AB amplifiers [30]. Hence, the GMP model is a good candidate for coping with the linearity degradations due to load impedance changes in the class AB power amplifier.

Applying the same DPD adaptive scheme to the Doherty amplifier yields the result presented in Fig. 15. The NMSE of the MLP and GMP models is shown in Fig. 15(a) and (b), respectively. The NMSE achieved by updating GMP model is improved compared to the NMSE obtained by updating the MLP model, as observed in Fig. 15.

The effect of updating the GMP model parameters for the Doherty amplifier can be observed comparing Figs. 10(b) and 15(b). This updating scheme has a positive effect over the linearity of the Doherty amplifier. For a certain level of the NMSE, the coverage region in the Smith Chart containing the “allowed” load impedances is larger when an updating scheme is used, as

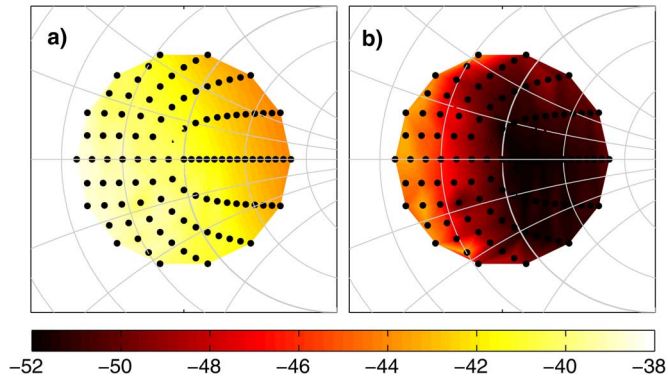


Fig. 16. Converged ACPR of an adaptive DPD applied to a Doherty amplifier under load impedance changes. (a) MLP. (b) GMP.

TABLE III
PERCENTAGE OF LOAD IMPEDANCE POINTS WITH NMSE ≤ -40 dB

Amplifier	Model	Fixed DPD	Adaptive DPD
AB	MLP	52%	53%
	GMP	72%	100%
	KV	71%	100%
Doherty	MLP	0%	0%
	GMP	24%	77%
	KV	26%	72%

depicted in Fig. 15(b). Even when updating DPD parameters, the GMP model presents performance that is notably degraded for some impedance points as noted in Fig. 15(b), at the left side of the Smith Chart where the $\angle \Gamma \approx 180^\circ$.

Fig. 16 shows the ACPR of the Doherty amplifier when the updating scheme for the DPD parameters was used. Fig. 16(a) and (b) presents the MLP and the GMP model results, respectively. A positive correlation of the performance with the load impedance is exhibited when comparing Fig. 15 with Fig. 16, which indicates that linearity can be improved for both NMSE and ACPR at some load impedances.

The Kautz-Volterra (KV) model was used in both amplifiers using the DPD updating parameter scheme. The results obtained for the KV model are similar for those presented for the GMP model in this section. We will further compare the GMP model with the KV model in the next Section.

Table III presents the percentage of the load impedance values with a performance lower (better) than -40 dB for the NMSE. For the AB amplifier, the DPD updating scheme using the MLP model did not significantly change the performance as previously noted. However, the GMP and the KV models achieve the improved performances in NMSE and ACPR. For the Doherty amplifier, the DPD using an MLP model is clearly unsuitable because any impedance point achieves a NMSE lower than -40 dB, while both the GMP and the KV models present improved NMSE as indicated in Table III.

Similarly, Table IV indicates the percentage of the impedance values which had a performance lower than -50 dB for the ACPR. While in the class AB amplifier the effect of the load

TABLE IV
PERCENTAGE OF LOAD IMPEDANCE POINTS WITH ACPR ≤ -50 dB

Amplifier	Model	Fixed DPD	Adaptive DPD
AB	MLP	100%	100%
	GMP	100%	100%
	KV	100%	100%
Doherty	MLP	0%	0%
	GMP	32%	74%
	KV	24%	62%

impedance on the ACPR is minor, the Doherty amplifier suffers severe degradations as indicated in Table IV. These degradations can be partially reduced by introducing adaptive DPD schemes.

D. GMP and KV Models

As indicated in previous sections, the performance of the KV and the GMP models is similar in both scenarios: in fixed and in adaptive DPD schemes. Fig. 17 shows the results for the GMP and the KV models in a Doherty power amplifier when using the adaptive DPD scheme. Fig. 17 presents both the NMSE in the upper plots a) and b) and ACPR in the lower plots (c) and (d), respectively. Each point in Fig. 17 is a different load impedance. The GMP and the KV models exhibit a similar performance when compared to each other. It may appear strange that the GMP model slightly outperforms the KV model since the KV model subsumes GMP model. However, this can be explained by the added variability to the parameter identification process when larger amount of parameters are used in a model [44]. Further, the nonlinear parameter identification technique used in the KV model is less mature than the LS techniques and leads to non-optimal solutions and to non-robust numerical implementations.

V. DISCUSSIONS

Load impedance mismatch in the Doherty power amplifier decreased the efficiency and affect the linearity performance. In particular, NMSE and ACPR degrade vastly with variations of the load impedance, as load modulation principle is altered. However, due to its design, in the studied class AB amplifier the out-of-band error (ACPR) is less sensitive to load impedance mismatch conditions.

The results presented in this paper suggests that the effects of the load impedance mismatch in power amplifiers can be tackled to some extent in the design process, similarly to those designs using modulated-stimuli and load-pull measurement data. However, the enlarge bandwidth usage in wireless systems poses a problem for controlling the impedance values over larger bandwidths. Future research is needed devising control impedance methods and measurement techniques over large bandwidths.

For DPD models which have enhanced linearity performance and do not employ adaptivity, the transmitter (DPD and amplifier) linearity is significantly affected by the hardware effects produced on the amplifier under load impedance mismatch and not by the DPD model used. Such a models like GMP or KV have similar linearity performances when evaluated. Further,

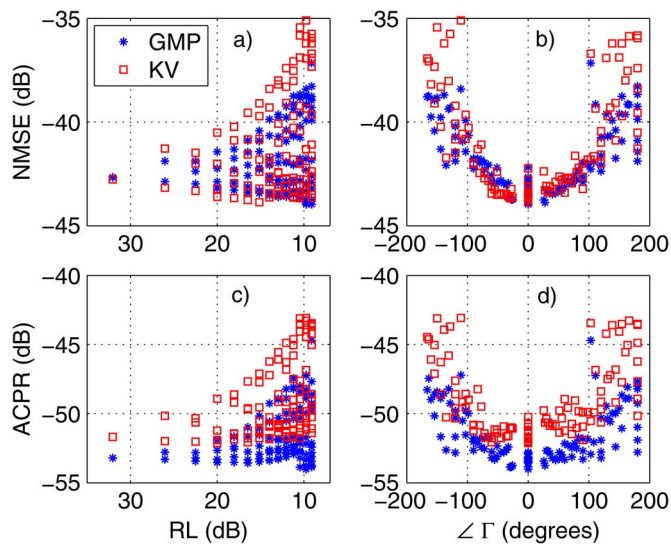


Fig. 17. Performance of an adaptive DPD technique in a Doherty power amplifier for different load impedance values.

updating DPD schemes using the GMP and KV models exhibit improved levels of linearization.

VI. CONCLUSION

The linearity in DPD-enhanced power amplifiers degrades under load impedance mismatch conditions. Severe degradations, as large as 10 dB, of the NMSE and the ACPR in linearized amplifiers can be encountered compared to the performance under matched operating conditions. Further, linearity degradations are impedance dependent as they vary with the magnitude and phase of the reflection coefficient provided by the load impedance. The analysis of the effects under load impedance mismatch require physical knowledge of the transistors and of the amplifier design process, which may not be available in most cases. Thereby, highlighting the need of embedded measurement and compensation techniques for load impedance mismatch in power amplifiers.

Due to the change in electrical and thermal memory effects produced by a load impedance mismatch, enhanced level of linearization can be achieved for DPD models considering memory effects, such as the GMP or the KV. For the same reason, updating DPD schemes of memoryless models, such as, the MLP do not achieve good levels of linearity in the presence of a load impedance mismatch.

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