A Current-Shared Cascade Structure With an Auxiliary Power Regulator for Switching Mode RF Power Amplifiers

Hoyong Hwang, *Student Member, IEEE*, Changhyun Lee, *Student Member, IEEE*, Jonghoon Park, *Student Member, IEEE*, and Changkun Park, *Member, IEEE*

***Abstract*—In this study, we propose an auxiliary power regulator (APR) for the current-shared cascade (CSC) structure of the driver stages of RF CMOS power. Although the CSC structure provides a method to reduce the power consumption at the driver stages of a differential power amplifier (PA), it is difficult to obtain optimum levels of effective supply voltage for the first and second driver stages. Additionally, the transistor sizes of the first and second driver stages of the CSC structure must be identical to ensure the proper operation of the PA. Thus, in this work, we propose an APR structure that ensures the proper operation of a PA with different transistor sizes in its first and second driver stages. To prove the feasibility of the proposed technique, we designed the PA with a CSC structure using an APR. From the measured results, we successfully verify the feasibility of the proposed structure. Additionally, we provide experimental results for a typical CMOS PA to determine the optimum supply voltage for the second driver stage.**

***Index Terms*—Amplifier, cascade, efficiency, regulator, supply voltage.**

I. Introduction

CURRENTLY, the performance levels of CMOS power amplifiers (PAs) are improving with the introduction of various techniques to improve the efficiency and linearity of these amplifiers. In particular, the distributed active transformer (DAT) proposed by Aoki *et al.* has become the most popular component for watt-level CMOS PAs, as this component minimizes the loss induced by the output matching network of the CMOS PA [1]. The DAT solves the gain reduction problems induced by the parasitic inductance, the silicon substrate loss, and the sensitivity problems of the output matching network. Based on this DAT, much research has sought to maximize the efficiency of CMOS PAs [2]–[5]. Some earlier works have proposed successful power stage structures that are optimized for the DAT structure [6]–[8]. Other valuable attempts to minimize current consumption in the power stage have adapted an envelope tracking (ET) technique to CMOS PAs [8]–[12].

Manuscript received January 08, 2014; revised June 30, 2014; accepted September 01, 2014. Date of publication September 23, 2014; date of current version November 03, 2014. This work was supported by the Ministry of Education, Science and Technology under the Basic Science Research Program through the National Research Foundation of Korea (NRF) (2012-044627).

The authors are with the School of Electronic Engineering, College of Information Technology, Soongsil University, Seoul 156-743, Korea (e-mail: pck77@ssu.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2014.2356974

As described above, efficiency enhancement techniques related to the power stage have progressed remarkably, as evidenced by several earlier works. However, few studies have focused on the other parts of CMOS PAs to enhance amplifier efficiency. For example, the driver stage has thus far been regarded as useful for driving the power stage to obtain high efficiency in the power stage. The power consumption of the driver stage compared to that of the power stage is negligible in the high output power region. However, the power consumption of the driver stage affects the overall efficiency of the PA if the output power decreases from the maximum output power of the PA [13]–[17]. If we consider the average efficiency to extend the lifetime of the battery of a wireless mobile system, the efficiency in the low output power region needs to be improved. Accordingly, the power consumption of the driver stage also needs to be minimized to enhance the average efficiency of the PA.

Recently, a current-shared cascade (CSC) structure has been proposed to reduce the power consumption of the driver stages [18]. However, whereas the CSC structure itself reduces the power consumption of the driver stages, the voltage waveform of the output of the driver stages may be restricted by the transistor size of the driver stages. Thus, if the transistor size of the driver stage is designed with an improper ratio, the power stage may operate inappropriately, thus decreasing the overall efficiency. In this paper, for polar transmitter applications, we propose a CSC structure with an auxiliary power regulator (APR) that can assure a proper voltage waveform of the driver stages while reducing the power consumption. In Section II, we describe the problems inherent to typical structures of CMOS PAs. The typical CSC structure to resolve issues related to typical amplifiers is shown in Section III. In Section IV, in an effort to enhance the feasibility of the CSC structure, we propose a new APR structure. Sections V and VI describe a schematic and provide the measurement data of the proposed CMOS PA. Additionally, in the Appendix, we provide the experimental results from a test implemented to extract the optimum transistor size of the APR.

II. Typical Structure of a CMOS PA

In general, RF CMOS PAs use an identical supply voltage, V_{DD}, in the driver and power stages to avoid increasing the complexity of the PA. In general, the V_{DD} of a PA is optimized in the power stage to obtain a high maximum output power. Ideally, the driver stage can be optimized by properly adjusting either the supply voltage or the bias current. However, adjusting

0018-9480 © 2014 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

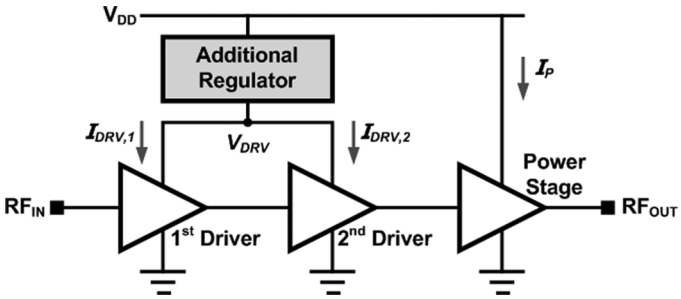


Fig. 1. Conceptual block diagram of a typical PA with a regulator.

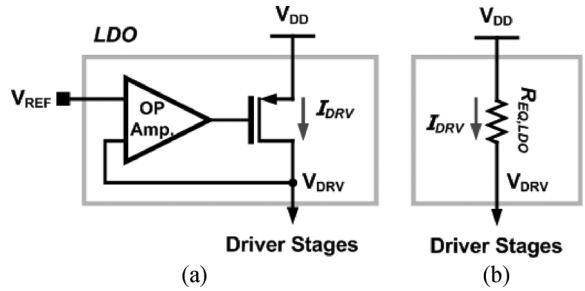


Fig. 2. Typical LDO. (a) Schematic. (b) Equivalent circuit.

the current to an optimal value is not always possible or practical due to unreasonable impedance transformation between the driver and the power stages. Additionally, impedance transformation requires a bulky inductor to complete the matching network. Optimizing or lowering the supply voltage of the driver stage may therefore be more attractive. Some previous works have shown that if the driver stage is composed of class D, and the dc blocking capacitor between the driver and power stages is removed to elevate the driveability of the driver stage, with $V_{DD} = 3.3$ V, the optimum value of the supply voltage for the driver stage will be lower than V_{DD} [15], [16]. In this case, if V_{DD} is used for the supply voltage of the driver stage, an unnecessary amount of dc power will be dissipated in the driver stages [15], [16]. The power-added efficiency (PAE) of a typical amplifier with an identical supply voltage, V_{DD}, can be expressed as follows:

$$\mathrm{PAE}_{VDD} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{(I_{\mathrm{DRV}} + I_P)\, V_{DD}}. \tag{1}$$

Here, PAE_{VDD} and P_{OUT} are the PAE, with $V_{\mathrm{DRV}} = V_{DD}$, and the output power of the PA, respectively. I_{DRV} and I_P denote the current of the driver stage and the power stage, respectively. To avoid unnecessary power consumption in the driver stage, V_{DRV}, which is the supply voltage of the driver stage, must differ from V_{DD}, as shown in Fig. 1. From the results of earlier work, it is known that the optimized value of V_{DRV} is lower than that of V_{DD} [15], [16]. If the loss due to the additional regulator shown in Fig. 1 is ignored, the efficiency of the PA itself, with an optimized value of V_{DRV}, can be enhanced, as follows:

$$\mathrm{PAE}_{\mathrm{OPT}} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{I_{\mathrm{DRV}} V_{\mathrm{DRV}} + I_P V_{DD}}. \tag{2}$$

Here, $\mathrm{PAE}_{\mathrm{OPT}}$ is the PAE with optimized V_{DRV}. If we define $I_{\mathrm{DRV,FIR}}$ and $I_{\mathrm{DRV,SEC}}$ as the currents of first and second driver stages, respectively, I_{DRV} can be calculated from $I_{\mathrm{DRV,FIR}} + I_{\mathrm{DRV,SEC}}$. However, in reality, an additional regulator is required to separate V_{DRV} from V_{DD} [18]. The additional regulator can be designed using a low-drop-out (LDO) converter or a dc–dc converter. Although the dc–dc converter has high efficiency, a bulky off-chip inductor, which cannot easily be integrated with the PA, is essential. This increases the overall system size and cost. On the other hand, although the LDO can be integrated with the CMOS PA, the LDO consumes dc power to generate the desired V_{DRV}. Fig. 2(a) shows the typical LDO. For the sake of simplicity, the equivalent circuit of the LDO can be expressed as a simple resistor, $R_{\mathrm{EQ,LDO}}$, as shown in Fig. 2(b). During the operation of the PA, the dc power is consumed at $R_{\mathrm{EQ,LDO}}$. Accordingly, if we include the power consumption in the LDO, the efficiency improvement owing to the optimized V_{DRV} is degraded as follows:

$$\begin{aligned}
&\mathrm{PAE}_{\mathrm{OPT}}\ (\text{including losses in the LDO}) \\
&\quad = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{I_{\mathrm{DRV}} V_{\mathrm{DRV}} + I_P V_{DD} + P_{\mathrm{LDO}}} \\
&\quad = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{I_{\mathrm{DRV}} V_{\mathrm{DRV}} + I_P V_{DD} + I_{\mathrm{DRV}} (V_{DD} - V_{\mathrm{DRV}})} \\
&\quad = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{I_{\mathrm{DRV}} V_{DD} + I_P V_{DD}} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{(I_{\mathrm{DRV}} + I_P)\, V_{DD}}.
\end{aligned} \tag{3}$$

Here, P_{LDO} is the power losses in the LDO and equals $I_{\mathrm{DRV}}(V_{DD} - V_{\mathrm{DRV}})$. For the sake of simplicity of analysis, the power consumption induced by the operational amplifier is ignored because the power consumption is much lower than overall power consumption of the general PA with watt-level output power. Although the result of (3) is identical to that of (1), the I_{DRV} of (3) becomes different from that of (1) according to the values of V_{DRV} in (3); this discrepancy will be investigated in Section V. As a consequence, although the I_{DRV} level in (3) may differ from that in (1), it is clear that PAE, calculated using (3), is lower than that calculated using (1).

III. CSC Structure

A. Principle of the CSC Structure

To solve the problems associated with the use of the typical structure of a PA, as described above, a CSC structure was proposed in an earlier work. This structure is shown in Fig. 3. The overall CSC structure is shown in Fig. 3(a). The first driver stage, shown in Fig. 3(b), is stacked on top of the second driver stage, shown in Fig. 3(c). For Fig. 3, we have assumed that all of the depicted circuits are designed with differential structures to generate a virtual ground at the node of V_X.

In the earlier work, MP_{FIR} and MN_{FIR} are identical to MP_{SEC} and MN_{SEC}, respectively, to ensure that V_X is half of V_{DD}. The peak-to-peak voltage of $\mathrm{RF}_{\mathrm{OUT,SEC}}$, which is the input of the power stage, then becomes $V_{DD}/2$. According to the earlier work, we can consider half of V_{DD} as the effective supply voltage of each of the driver stages in spite of the absence of an additional regulator; this situation is different from that of the typical PA shown in Fig. 1. Thus, by removing the loss induced by the additional regulator, the overall efficiency of the PA can be increased compared to that of a typical PA.

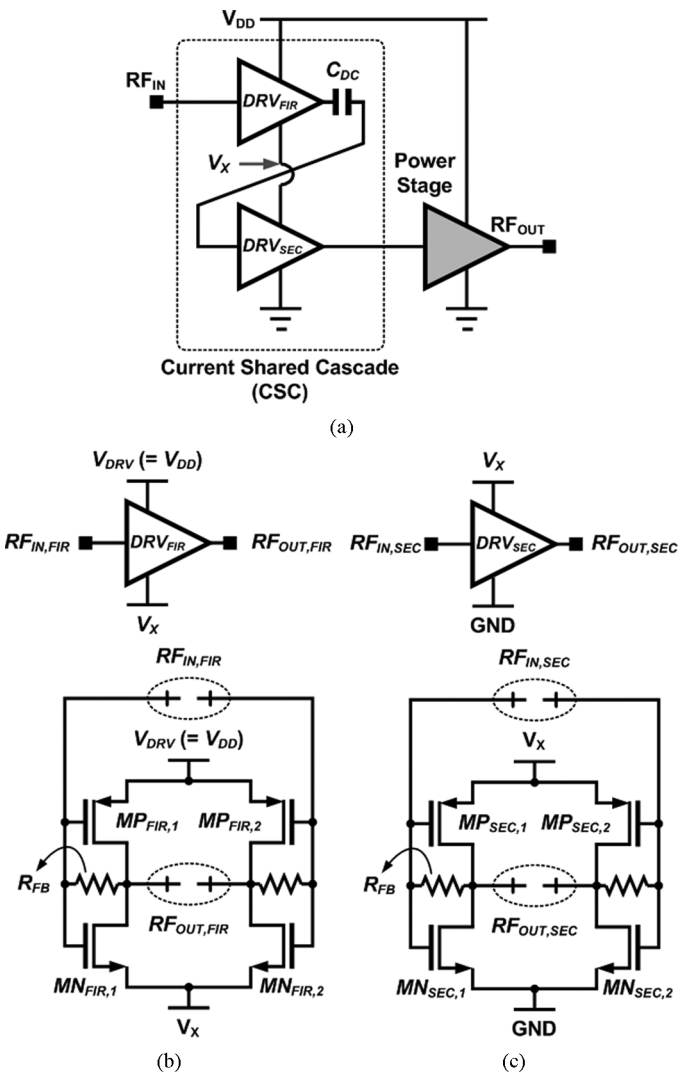


Fig. 3. CSC structure. (a) Overall structure. (b) Schematic of the first driver stage. (c) Schematic of the second driver stage.

B. Transistor Size Issues Associated With the CSC Structure

Although the sizes of the transistors for the first and second driver stages needed to be identical in the CSC structure in the previous work, the transistor size of the second driver stage is designed to be larger than that of the first driver stage in a general PA. However, if we assume that the transistor size of the second driver stage is N times larger than that of the first driver stage in the CSC structure in the previous work, V_X deviates from half of V_{DD}. In Fig. 4, $R_{\rm FIR}$ and $R_{\rm SEC}$ are the equivalent resistance levels of the first and second driver stages, respectively. The values of V_X according to the ratio N can then be calculated as follows:

$$\begin{aligned} I_{\rm DRV,SEC} &= I_{\rm DRV,FIR} \\ R_{\rm SEC} &= \frac{R_{\rm FIR}}{N} \\ V_X &= \frac{R_{\rm SEC}}{R_{\rm FIR}+R_{\rm SEC}}V_{DD} = \frac{1}{N+1}V_{DD}. \end{aligned} \tag{4}$$

Given that N is generally greater than 1, V_X becomes lower than half of V_{DD}, and hence the effective supply voltage of the second driver stage becomes lower than half of V_{DD}. In spite of the increased transistor size of the second driver stage, the peak-to-peak voltage of the output of the second driver stage then decreases considerably. As a consequence, the driver stages cannot drive the power stage properly. Thus, the restriction related to the transistor size of the first and second driver stages may be regarded as a drawback of the CSC structure.

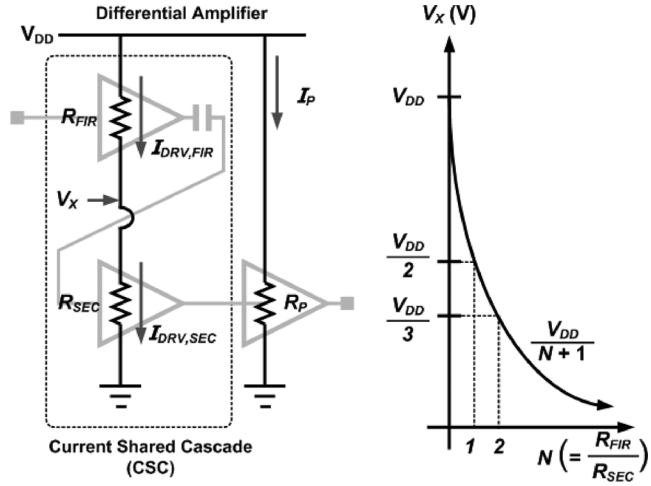


Fig. 4. Typical CSC structure. (a) Overall structure. (b) V_X according to N.

IV. Proposed CSC Structure With an APR

Although the CSC structure solves the problems introduced by the additional regulator in the typical PA, the sizes of the transistors in the first and second driver stages in the typical CSC structure need to be identical to assure the proper operation of the PA. In this work, we propose a CSC structure with an APR; this regulator makes it possible for the CSC structure to obtain proper V_X voltage with N higher than 1.

Fig. 5 provides a conceptual diagram and the operation of the proposed structure. To make the V_X node in Fig. 5 a virtual ground for the fundamental frequency component, all of the driver and power stages are designed using the differential structure. The APR uses $V_{C,P}$ as the input to control the desired output voltage, V_X, as shown in Fig. 5(a). The APR is composed of an operational (OP) amplifier and an $MP_{\rm APR}$, as shown in Fig. 5(b). If the value of N is higher than 1, V_X of the CSC structure without the APR tends to be lower than half of V_{DD}. If V_X becomes lower than $V_{C,P}$, $MP_{\rm APR}$ turns on to increase V_X. By setting $V_{C,P}$ equal to the desired V_X, we can then obtain V_X as the desired voltage level regardless of the value of N, as shown in Fig. 5(c). As a consequence, the APR can assure that V_X is the desired voltage level in spite of the transistor size of the second driver stage, which is larger than that of the first driver stage.

Fig. 6 shows the V_X level according to $V_{C,P}$. In Fig. 6, the transistor of $MP_{\rm APR}$ is assumed to be an ideal switch. To determine the desired value of V_X, and hence the size of $MP_{\rm APR}$, we use the measured results shown in the Appendix. From the results of the typical PA shown in the Appendix, the optimum V_X of the proposed amplifier can be seen to range from 1.9 to 2.4 V. However, as shown in Fig. 6, an excessive value of V_X reduces the effective supply voltage of the first driver stage. In

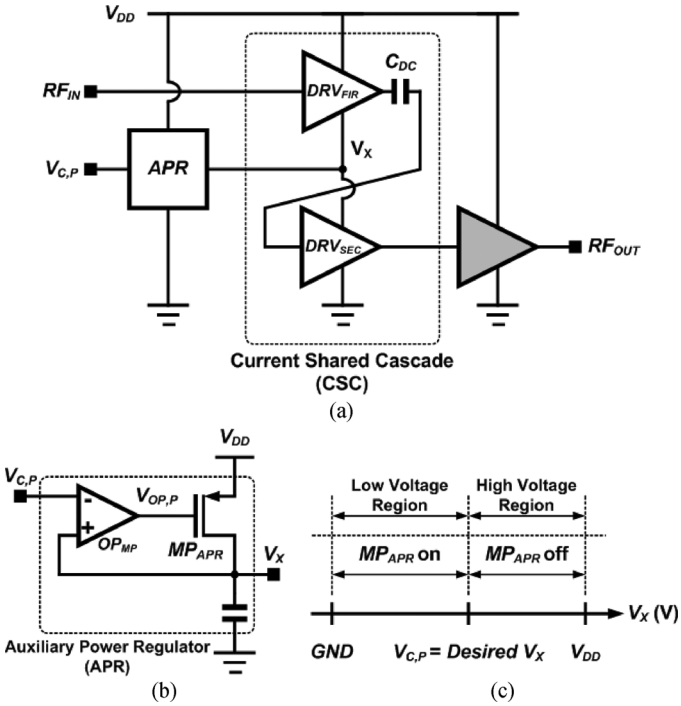


Fig. 5. Proposed CSC structure with an APR. (a) Conceptual block diagram. (b) Structure of the APR. (c) Operation and output voltage of the APR according to the control voltages.

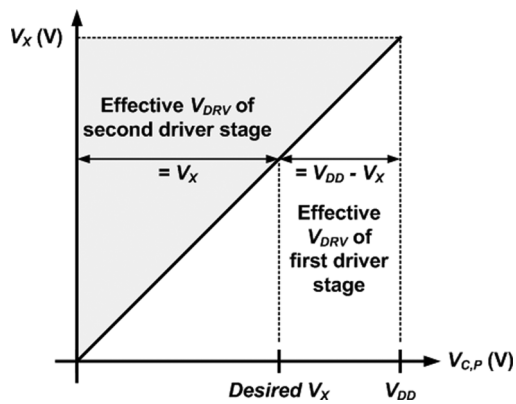


Fig. 6. Effective supply voltages of first and second driver stages according to the value of $V_{C,P}$ with the assumption of MP_{APR} as an ideal switch.

this work, to ensure the proper operation of the first and second driver stages, the designed V_X ($V_{C,P}$) is 1.9 V.

If we consider MP_{APR} as the actual transistor, MP_{APR} has finite on-resistance. The operation of MP_{APR}, and the V_X level, can then be expressed as shown in Fig. 7. In the $V_{C,P}$ ranges from 0 V to V_X without the APR, MP_{APR} is turned off because $V_{C,P}$ is lower than V_X. Thus, the V_X level of the CSC structure with an APR is identical to the level of V_X without an APR. If $V_{C,P}$ exceeds V_X without an APR, MP_{APR} is switched on to allow V_X to reach $V_{C,P}$. However, given that, in reality, MP_{APR} has a finite on-resistance, there exists a saturation point according to the on-resistance of the MP_{APR}. In this work, we design the size of MP_{APR} so that it is saturated at a $V_{C,P}$ of 1.9 V, which is the desired level of V_X. Thus, if $V_{C,P}$ increases beyond the level of the desired V_X, V_X remains at its desired level regardless of the value of $V_{C,P}$, as shown in Fig. 7.

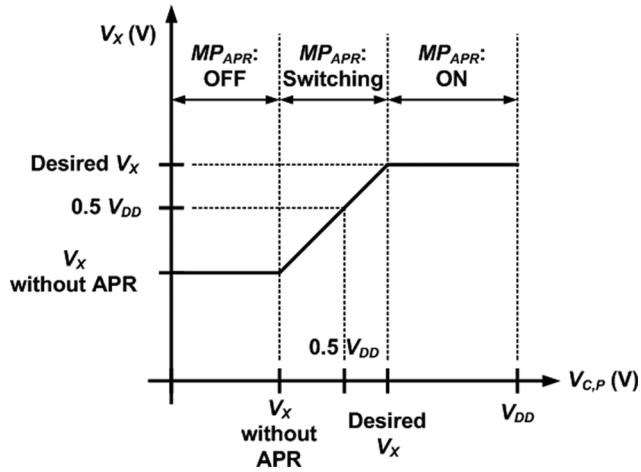


Fig. 7. Operation of MP_{APR} and V_X according to the value of $V_{C,P}$ with a finite transistor size of MP_{APR}.

V. Power Dissipation in the Driver Stages and APR

To verify that the power consumption of the proposed structure is lower than those of the various typical structures described in the previous sections, we calculate the power dissipation in the driver stage and the APR of the proposed and typical structures. For the sake of simplicity, we assume that the size of the second driver stage and the power dissipations in the power stages of the proposed and typical structures are identical. Accordingly, we calculate and compare the power dissipations in the driver stages and the APR of the proposed and typical structures.

If I_{APR} is the current dissipated in the APR, I_{APR} can be calculated as follows:

$$\begin{aligned} I_{\mathrm{APR}} &= I_{\mathrm{DRV,SEC}} - I_{\mathrm{DRV,FIR}} = \frac{V_X}{R_{\mathrm{SEC}}} - \frac{V_{DD}-V_X}{R_{\mathrm{FIR}}} \\ &= \frac{(N+1)V_X - V_{DD}}{NR_{\mathrm{SEC}}} = \left(\frac{N+1}{NM} - \frac{1}{N}\right)\frac{V_{DD}}{R_{\mathrm{SEC}}} \\ &\left(\because\ R_{\mathrm{SEC}} = \frac{1}{N}R_{\mathrm{FIR}} \quad V_X = \frac{1}{M}V_{DD}\right). \end{aligned} \tag{5}$$

Here, $1/M$ is the ratio of V_X to V_{DD}. In general, M ranges from 1 to 2 and N is higher than 1. $I_{\mathrm{DRV,FIR}}$ and $I_{\mathrm{DRV,SEC}}$ are the currents of the first and second driver stages. The power dissipation in the APR, P_{ARP}, can then be calculated as follows:

$$\begin{aligned} P_{\mathrm{APR}} &= (V_{DD}-V_X)\,I_{\mathrm{APR}} \\ &= \left(1-\frac{1}{M}\right)V_{DD}I_{\mathrm{APR}} \\ &= \left(\frac{N+2}{NM} - \frac{N+1}{NM^2} - \frac{1}{N}\right)\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}}. \end{aligned} \tag{6}$$

The power dissipation in the driver stages, P_{DRV}, can be calculated as follows:

$$\begin{aligned} P_{\mathrm{DRV}} &= P_{\mathrm{DRV,FIR}} + P_{\mathrm{DRV,SEC}} \\ &= I_{\mathrm{DRV,FIR}}(V_{DD}-V_X) + I_{\mathrm{DRV,SEC}}V_X \\ &= \frac{(V_{DD}-V_X)^2}{R_{\mathrm{FIR}}} + \frac{{V_X}^2}{R_{\mathrm{SEC}}} \\ &= \left(\frac{1}{N} - \frac{2}{NM} + \frac{1+N}{NM^2}\right)\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}}. \end{aligned} \tag{7}$$

Here, $P_{\mathrm{DRV,FIR}}$ and $P_{\mathrm{DRV,SE}}$ are the power dissipations in the first and second driver stages. If we define $P_{\mathrm{DRV,APR}}$ as the overall power dissipation in the driver stage and APR, $P_{\mathrm{DRV,APR}}$ can be calculated as follows:

$$P_{\mathrm{DRV,APR}} = P_{\mathrm{DRV}} + P_{\mathrm{APR}} = \frac{1}{M}\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}}. \tag{8}$$

As can be seen from (8), the power dissipations in the driver stages and APR of the proposed structure are not functions of N, but functions of M.

A. Comparison of PA With $V_{\mathrm{DRV}} = V_{DD}$

To compare the power dissipation in the proposed structure to that in the typical structure, in which the supply voltage of the driver stage, V_{DRV}, is identical to that of the power stage, V_{DD}, we calculated the power dissipation in the driver stage of the typical driver stage, with $V_{\mathrm{DRV}} = V_{DD}$,

$$\begin{aligned} P_{\mathrm{DRV},VDD} &= P_{\mathrm{DRV,FIR}} + P_{\mathrm{DRV,SEC}} \\ &= I_{\mathrm{DRV,FIR}}V_{DD} + I_{\mathrm{DRV,SEC}}V_{DD} \\ &= \frac{{V_{DD}}^2}{R_{\mathrm{FIR}}} + \frac{{V_{DD}}^2}{R_{\mathrm{SEC}}} \\ &= \left(\frac{1}{N}+1\right)\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}}. \end{aligned} \tag{9}$$

Here, $P_{\mathrm{DRV},VDD}$ is the overall power dissipation in the driver stages. $P_{\mathrm{DRV},VDD}$ varies according to N, as shown in (9).

B. Comparison With PA With Optimized V_{DRV}

If we define $P_{\mathrm{DRV,OPT}}$ as the power dissipation in the driver stages with optimized V_{DRV}, $P_{\mathrm{DRV,OPT}}$ can be calculated as follows:

$$P_{\mathrm{DRV,OPT}} = I_{\mathrm{DRV}}V_{DD} = \frac{V_{\mathrm{DRV}}V_{DD}}{\frac{R_{\mathrm{FIR}}R_{\mathrm{SEC}}}{R_{\mathrm{FIR}}+R_{\mathrm{SEC}}}} = \frac{N+1}{NM}\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}}$$
$$\left(\because\ R_{\mathrm{SEC}} = \frac{1}{N}R_{\mathrm{FIR}} \quad V_{\mathrm{DRV}} = \frac{1}{M}V_{DD}\right). \tag{10}$$

Here, $P_{\mathrm{DRV,OPT}}$ includes the power consumption at the additional regulator as well as at the driver stages. $P_{\mathrm{DRV,OPT}}$ varies according to M and N, as shown in (10).

C. Comparison With Typical CSC Structure

If we define $P_{\mathrm{DRV,CSC}}$ as the power dissipation in the driver stages of the typical CSC structure, $P_{\mathrm{DRV,CSC}}$ can be calculated as follows:

$$\begin{aligned} &P_{\mathrm{DRV,CSC}} \\ &= P_{\mathrm{DRV,FIR}} + P_{\mathrm{DRV,SEC}} \\ &= I_{\mathrm{DRV,FIR}}\left(V_{DD}-V_X\right) + I_{\mathrm{DRV,SEC}}V_X \\ &= \frac{\left(V_{DD}-V_X\right)^2}{R_{\mathrm{FIR}}} + \frac{{V_X}^2}{R_{\mathrm{SEC}}} \\ &= \frac{1}{N+1}\frac{{V_{DD}}^2}{R_{\mathrm{SEC}}} \end{aligned}$$
$$\left(\because\ R_{\mathrm{SEC}} = \frac{1}{N}R_{\mathrm{FIR}} \quad V_X = \frac{1}{M}V_{DD} = \frac{1}{1+N}V_{DD}\right). \tag{11}$$

Here, $P_{\mathrm{DRV,CSC}}$ is the overall power dissipation in the driver stages. $P_{\mathrm{DRV,CSC}}$ varies according to N, as shown in (11).

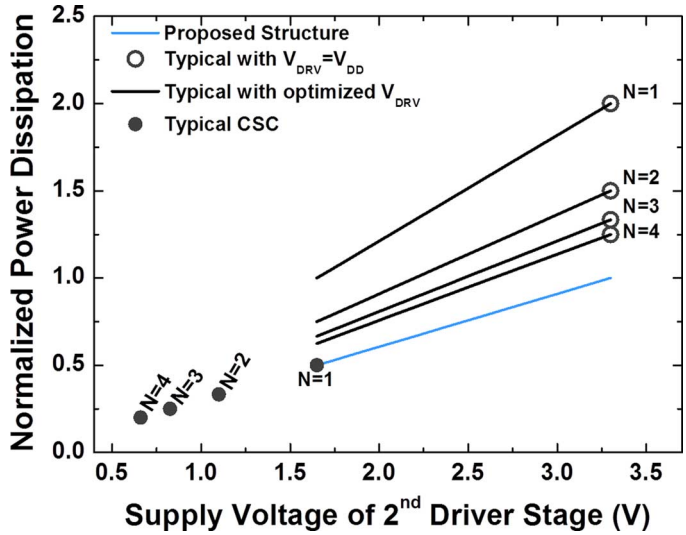


Fig. 8. Normalized power dissipations and supply voltages of the second driver stages according to N and M.

Fig. 8 provides the calculated power coefficients from (8)–(11). The normalized power dissipation of the Y axis is defined as follows:

$$\text{Normalized Power Dissipation} = \left(P_{\mathrm{DRV,APR}}, P_{\mathrm{DRV},VDD}, P_{\mathrm{DRV,OPT}}, P_{\mathrm{DRV,CSC}}\right) \times \frac{R_{\mathrm{SEC}}}{V_{DD}^2}. \tag{12}$$

The x axis in Fig. 8 is the supply voltage of the second driver stages of the proposed and typical structures according to the N and M. Although the power dissipation induced by the additional LDO is included in the calculation of $P_{\mathrm{DRV,OPT}}$, we can find that $P_{\mathrm{DRV,OPT}}$ is lower than $P_{\mathrm{DRV},VDD}$. As can be seen, the supply voltage of the second driver stage of the typical CSC structure is determined by the index N. On the contrary, the supply voltage of the second driver stage of the proposed structure is determined by the index M, regardless of index N. Except for that of the typical CSC structure, we can find that the power dissipation of the proposed structure is always lower than those of other structures. Although the power dissipation in the driver stage of the typical CSC structure is lower than that in the driver stage of the proposed CSC structure, the supply voltage of the second driver stage of the typical CSC structure is lower than half of V_{DD}.

If the N of the typical CSC structure becomes lower than 1, and hence if the first driver stage becomes larger than the second driver stage, the V_X of the typical CSC structure can be set to the desired value. However, in such cases, the required input power increases in proportion to the size of the first driver stage, and hence the PAE is degraded compared to that of the proposed structure.

VI. Design of a CMOS PA Using the CSC Structure With an APR

To verify the feasibility of the proposed CSC structure with an APR, we designed a fully integrated PA using 0.13-μm RF

CMOS technology with eight metal layers. The top layer is implemented using aluminum with a thickness of 4.06 μm.

The supply voltage, V_{DD}, is set at 3.3 V for mobile handset applications. To avoid gain reduction problems induced by various levels of parasitic inductance, the power and the driver stages are designed using a differential structure. The matching networks, the power combiner, and the test pads are fully integrated. An overall schematic of the proposed PA is shown in Fig. 9.

To ensure watt-level output power, two differential pairs are designed for the power stage. The transistor size for MN_{CS} is determined using an optimization technique proposed in an earlier work [17]. If the supply voltage directly enters through the drain node of the MN_{CG} transistors that use additional pads and an RF choke, including external components or bonder-wires, the efficiency can be enhanced. However, in this work, the supply voltage enters through the virtual grounds of the primary part of the DAT, to avoid the effects of inductance variation of the bonder-wires and the additional cost requirements of the off-chip components; this process allows the fabrication of a fully integrated CMOS PA. Additionally, to moderate the electrical overstress at the power transistor of the power stage, a cascode structure is adopted.

In the CSC structure, the designed value of N is 2, as shown in the schematic of first and second driver stages shown in Fig. 9. The comparator is designed using a general OP amplifier. Although we chose one of the simplest types of OP amplifier to verify the feasibility of the proposed structure, the structure of the OP amplifier can be modified to elevate its performance. Additionally, if topology related to the bandgap reference is applied to the APR, the voltage level of V_X can be more precisely adjusted. A metal–insulator–metal (MIM) capacitor with 1 pF is used in the V_X node. The feedback resistor, $R_{\rm FB}$, of the driver stages is 2 kΩ. A dc blocking capacitor, $C_{\rm DC}$, is used between the first and second driver stages to eliminate undesired effects that arise from the different voltage levels between the first stage output and the second stage input. To remove the dc blocking capacitor between the output of the second driver stage and the input of the power stage, the first driver stage is stacked on top of the second driver stage. On the other hand, if the second driver stage is stacked on top the first driver stage, a dc blocking capacitor between the second driver stage and the power stage is required to identify the dc references of the second driver stage output and the power stage input. However, the dc blocking capacitor between the second driver stage designed using class-D and the power stage degrades the efficiency of the PA [15]. Accordingly, in this work, the first driver stage is stacked on top of the second driver stage.

VII. Experimental Results

Fig. 10 provides a chip photograph of the proposed 1.9-GHz CMOS PA using the CSC structure with an APR. The chip size is 1.2×1.7 mm^2. To check the node voltage of V_X, several test pads were integrated, as shown in Fig. 10. Given that the designed PA is operated in switch mode, and hence designed for polar transmitter applications, we measured the performances of the PA according to the values of the supply voltage of the PA. The input power and the operating frequency of the proposed structure are fixed at 7.5 dBm and 1.9 GHz, respectively.

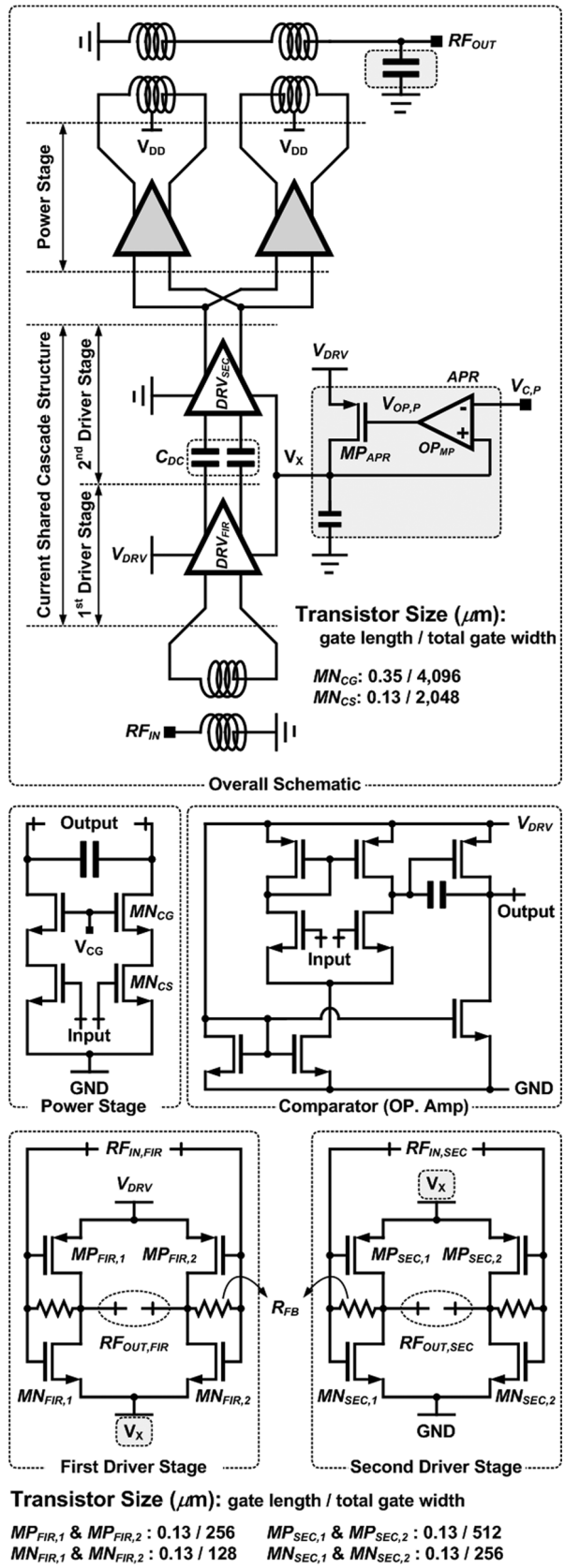


Fig. 9. Overall schematic of the proposed CMOS PA.

Fig. 11 shows the measured V_X, the output power, and the PAE according to $V_{C,P}$. All of the power consumption levels,

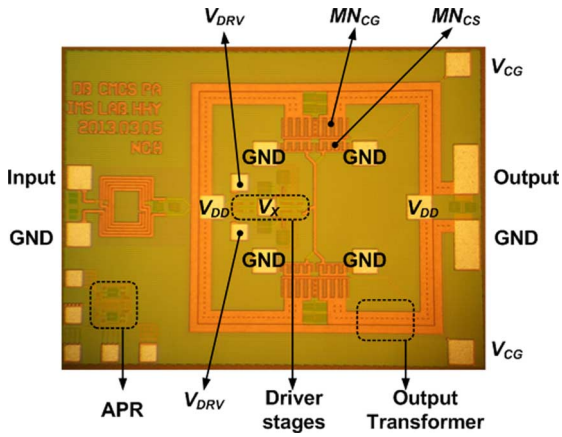
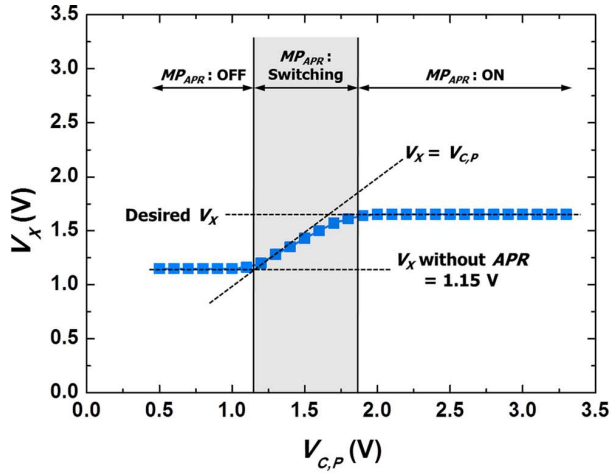
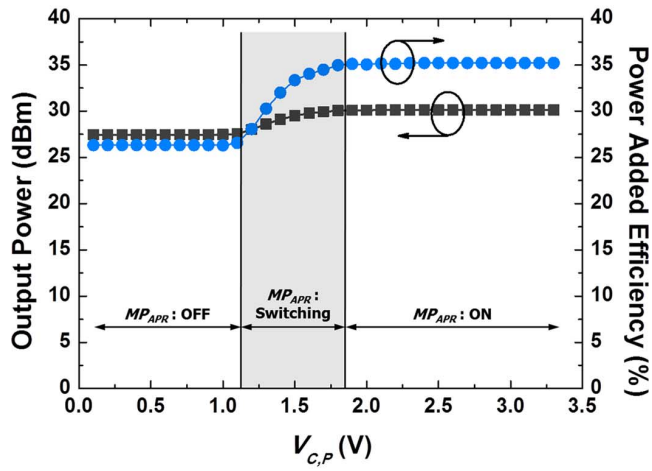


Fig. 10. Chip photograph of the proposed CMOS PA using the CSC structure with an APR.



(a)



(b)

Fig. 11. Measured results (operating frequency = 1.9 GHz, $V_{DD} = V_{\mathrm{DRV}} = 3.3$ V): (a) V_X, (b) output power, and PAE according to $V_{C,P}$.

including the consumption values of the driver stage, power stage, and APR, are considered in the measured PAE. As can be seen in Fig. 11(a), the measured operation regions are similar to those shown in Fig. 7. The measured V_X without an APR is 1.15 V, which is nearly 0.33 of V_{DD}, as predicted previously. However, although we designed the desired V_X to be 1.9 V, the measured V_X is saturated at 1.65 V. One possible reason for this is that the real current consumption of the second driver stage may be higher than the designed current consumption, and therefore, there is a greater voltage drop in the first diver stage, while MP_{APR} has already reached the saturation region. Another possible reason is that the real current consumption of the first driver stage may be lower than the designed current consumption, and therefore, there is less of a voltage drop in the second driver stage, while MPAPR has already reached the saturation region. Additionally, differences between the desired and measured values of the saturation point of V_X may arise due to the parasitic resistance induced by the interconnection metal lines and the via-holes. In particular, the parasitic resistance of the interconnection line between the output of the APR and the V_X node of the CSC structure may distort the desired saturation voltage. Fig. 11(b) shows the measured output power and PAE according to $V_{C,P}$ at an operating frequency of 1.9 GHz and with a V_{DD} value of 3.3 V. As predicted by the data shown in Fig. 7, the output power and PAE are saturated beyond the saturation point of V_X.

Fig. 12(a) shows the measured output power of the proposed PA according to the supply voltage of the power stage with a fixed operating frequency and a fixed $V_{C,P}$. To verify the feasibility of the proposed APR, we also measured the output power of the PA without an APR. As can be seen in the measured results, the output power of the proposed PA is improved under the same conditions as those of the PA without the APR. Additionally, we show the measured output powers of the typical PA that is described in the Appendix. From the results for the typical PA shown in the Appendix, the optimum V_{DRV} can be seen to range from 1.9 to 2.4 V. Although the designed V_X in this work is 1.9 V, V_{DRV} is set at 2.3 V because the typical PA has its maximum performance at this voltage. We also checked the PAEs of these two PAs, with results as shown in Fig. 12(b). As can be seen in Fig. 12(b), the efficiency in the high-power region is improved compared to that of the PA without the APR. If the APR is turned off, the dc component of the input signal of the power stage decreases. Accordingly, the power consumption in the low-power region with the APR turned off decreases.

Fig. 13 shows the measured current and power dissipations of the driver and power stage of the proposed structure according to the supply voltage of the power stages. Additionally, we show the dissipated current in the driver stages of the typical PA that is described in the Appendix. As can be seen in Fig. 13(a), the current consumption of the driver stage that includes the APR is almost 10% of the current consumption of the power stage at maximum output power.

Fig. 14 shows the measured frequency response of the proposed PA. As can be seen in this figure, the maximum performance is obtained at an operating frequency of 1.95 GHz. Fig. 15(a) shows the measured output power and PAE according to the input power at 1.9 GHz with $V_{DD} = V_{\mathrm{DRV}} = 3.3$ V. As can be seen in Fig. 15(a), with an input power of 7.5 dBm, the efficiency is maximized and the output power is already saturated. Accordingly, in this work, the input power is fixed at 7.5 dBm. Fig. 15(b) shows the measured $S11$. Table I provides comparisons of CMOS PAs.

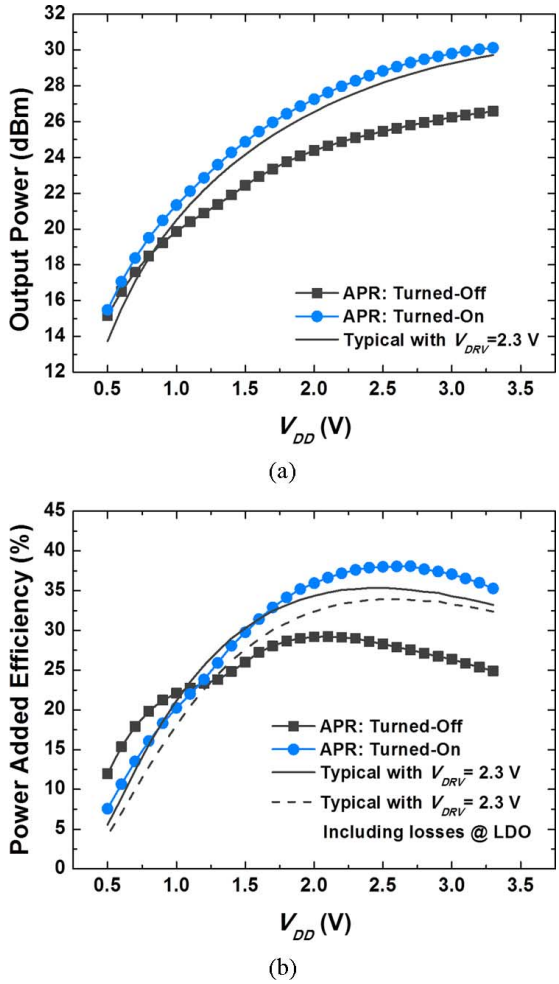


Fig. 12. Measured results (operating frequency = 1.9 GHz). (a) Output powers and (b) PAEs according to supply voltage of the power stage.

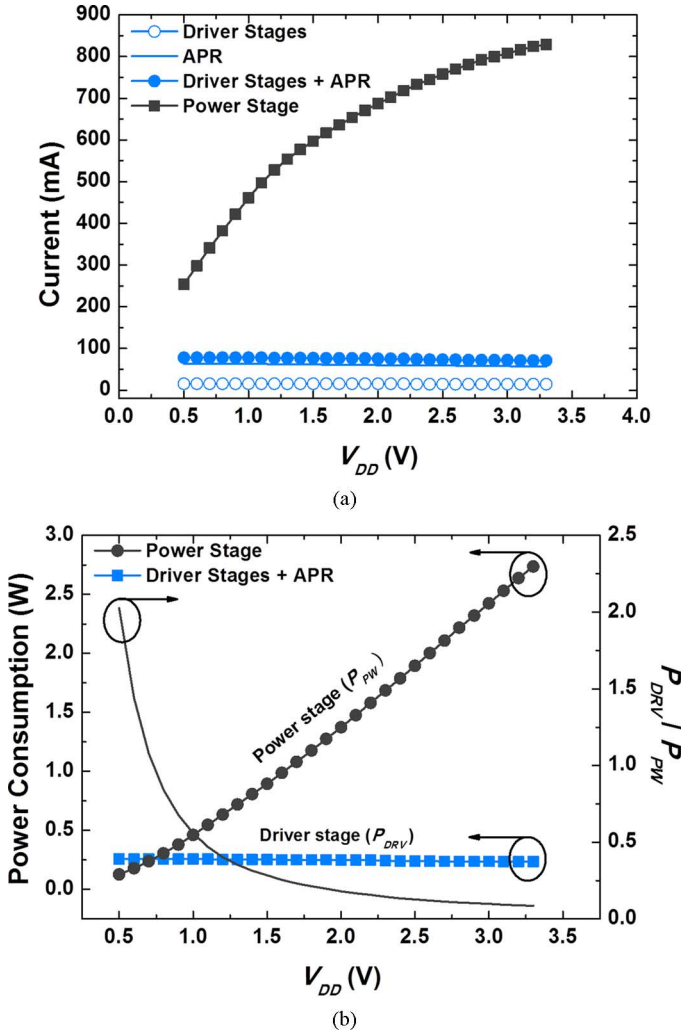


Fig. 13. Measured results (operating frequency = 1.9 GHz, $V_{\mathrm{DRV}} = 3.3$ V). (a) Current consumption. (b) Power consumption in the driver and power stages according to the supply voltage of power stages.

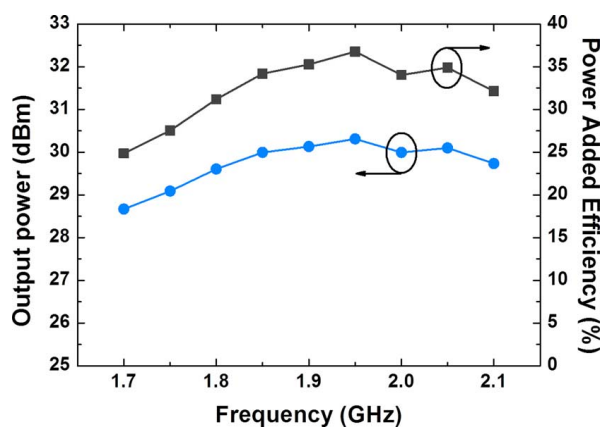


Fig. 14. Measured frequency response ($V_{DD} = V_{\mathrm{DRV}} = 3.3$ V).

VIII. Discussion

In this study, to solve the size issues of the driver stages of the typical CSC structure, we proposed a CSC structure with an APR. Although the idea of a stacking structure to reduce power consumption has been explored in many previous works, the stacking structures designed in those previous works were realized in the power stages [24], [25]. In most previous works related to stacking structures, the output power levels of the stacked power stages were combined using current- or voltage-combining methods; the input signal of the power stages were identical. On the contrary, the stacking structure in this study is applied to the driver stages. The output signal of the first driver stage, which is stacked on the top of the second driver stage, enters the input of the second driver stage. The current used for the first driver stage is reused for the second driver stage, while the APR is used to obtain the desired voltage drop in the second driver stage.

A. Stabilization of V_X

In this study, the effective supply voltages of the first and second driver stages are $(V_{DD} - V_X)$ and V_X, respectively. Although the APR is thought to guarantee a stabilized V_X, an additional bypass capacitor in the node V_X is required. In this study, a 1-pF MIM capacitor is used as a bypass capacitor. However, if we consider the power supply rejection ratio (PSRR) issues or the fact that the supply voltage must be modulated for polar or envelope elimination and restoration (EER) transmitters, the value of the bypass capacitor needs to be investigated to stabilize V_X.

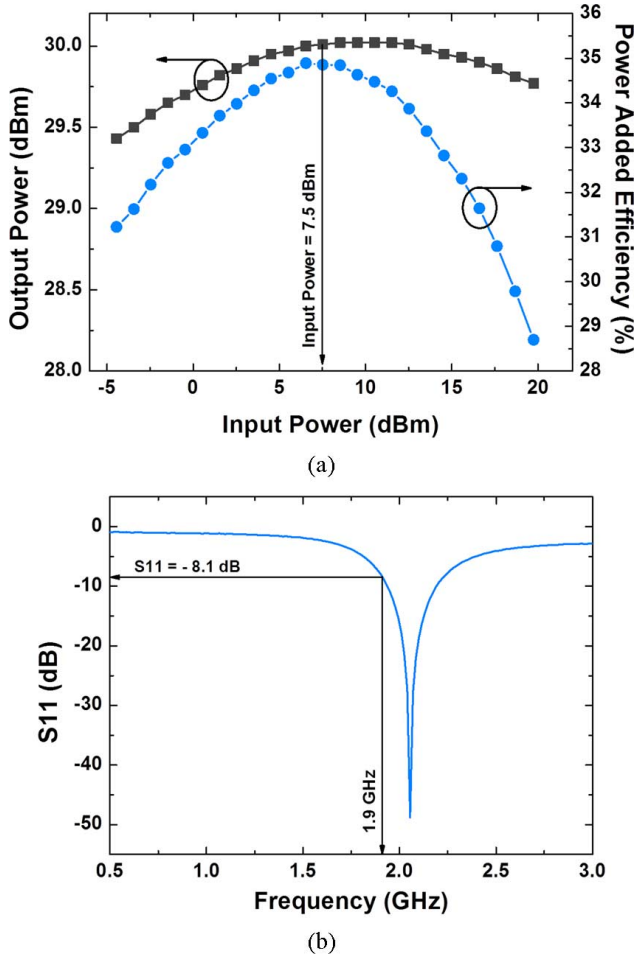


Fig. 15. Measured results. (a) Output power and PAE according to input power ($V_{DD} = V_{\mathrm{DRV}} = 3.3$ V) and (b) $S11$.

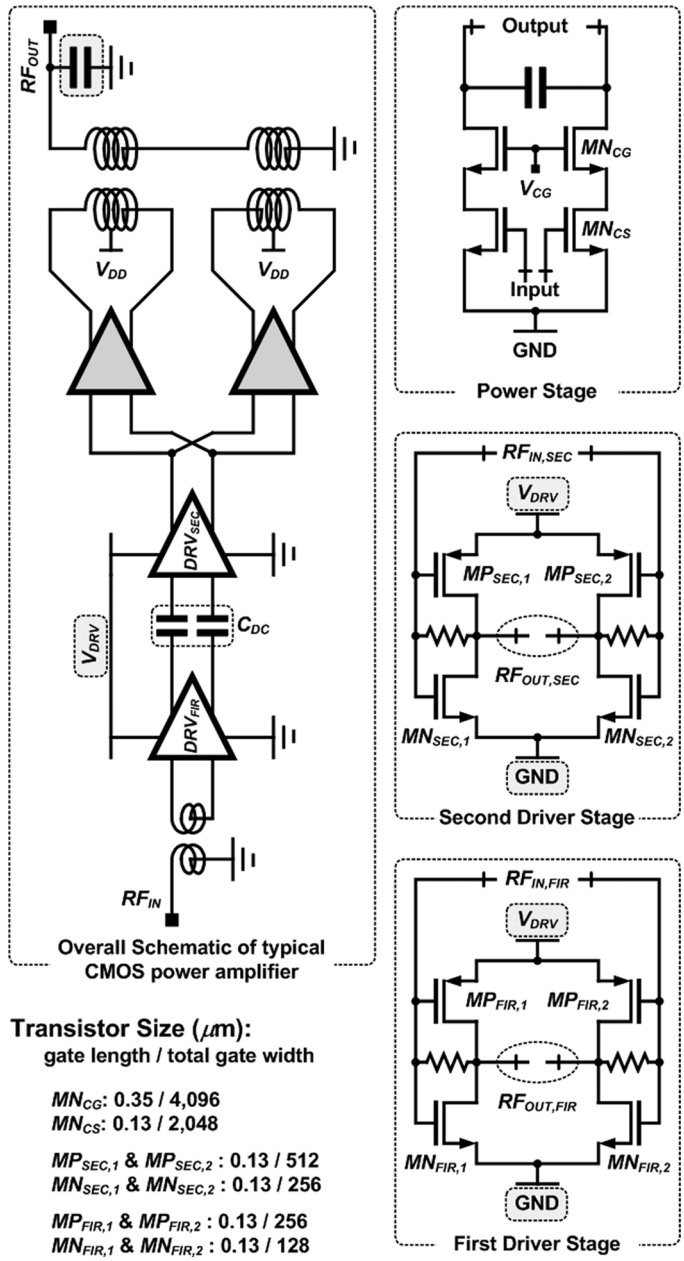
TABLE I
COMPARISONS OF CMOS PAs

Ref.	Freq. (GHz)	P_{OUT} (dBm)	PAE (%)	Process (nm)	Size (mm^2)
[13]	2.4	21	33	180	0.9 × 0.6
[18]	1.9	28.6	30	130	1.7×1.0
[19]	2.4	31	33	180	2
[20]	2.5	30.8	30.6	180	2.0 × 1.2
[21]	1.8	33	31	180	1.8×1.65
[22] [1)]	2.4	25 [2)]	60 [3)]	130	1.0×1.0
[23]	2.4	23 [2)]	18 [3)]	180	0.81×0.57
This work (Typical [4)])	1.9	29.7	32.9 [4)]	180	1.7×1.2
This work (Proposed)	1.9	30.1	35.2	180	1.7×1.2

1) Off chip components are used
2) Maximum output power
3) PAE @ P1dB
4) $V_{DRV} = 2.3$ V,
5) loss of additionally required regulator is ignored.

B. Transistor Size of MP_{APR}

Although in this study we set the value of V_X by sizing MP_{APR}, the size of MP_{APR} need to be sufficiently large so as not to enter the triode region during the normal operation of the PA. Once MP_{APR} enters the triode region, V_X cannot be set to the desired voltage and the regulator feedback loop will no longer have sufficient gain.



Transistor Size (μm):
gate length / total gate width

MN_{CG}: 0.35 / 4,096
MN_{CS}: 0.13 / 2,048

$MP_{SEC,1}$ & $MP_{SEC,2}$: 0.13 / 512
$MN_{SEC,1}$ & $MN_{SEC,2}$: 0.13 / 256

$MP_{FIR,1}$ & $MP_{FIR,2}$: 0.13 / 256
$MN_{FIR,1}$ & $MN_{FIR,2}$: 0.13 / 128

Fig. 16. Overall schematic of the typical CMOS PA.

C. Limitation of Applications

The proposed PA is designed for 1.9-GHz applications with 3.3-V battery voltage using 1.8-μm RF CMOS technology. However, if the process technology and the value of the battery voltage are modified, the optimized value of V_X could also vary.

In this work, the proposed PA is designed for polar transmitter applications in which a switching mode PA is required. However, if the PA is designed as a linear PA, additional analysis and

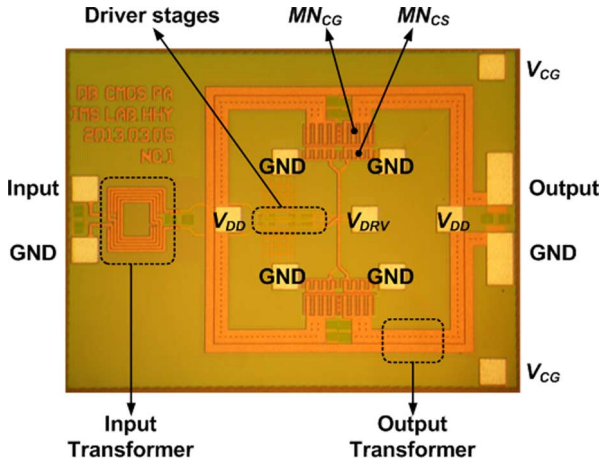


Fig. 17. Chip photograph of the designed typical CMOS PA.

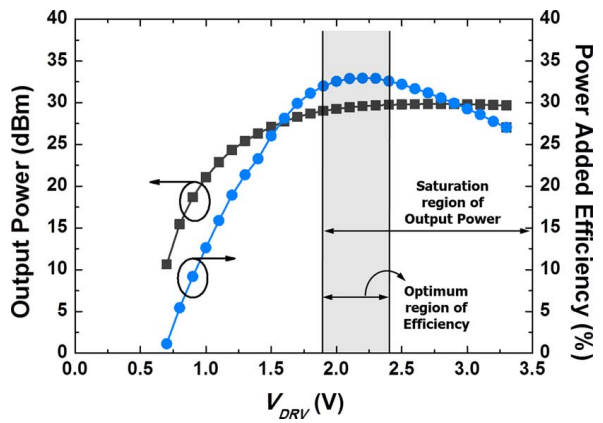
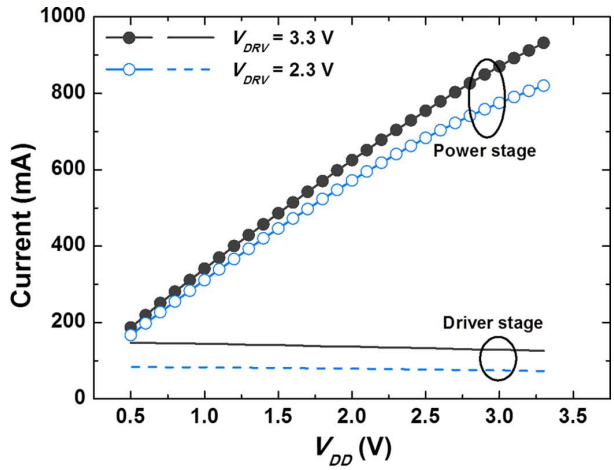
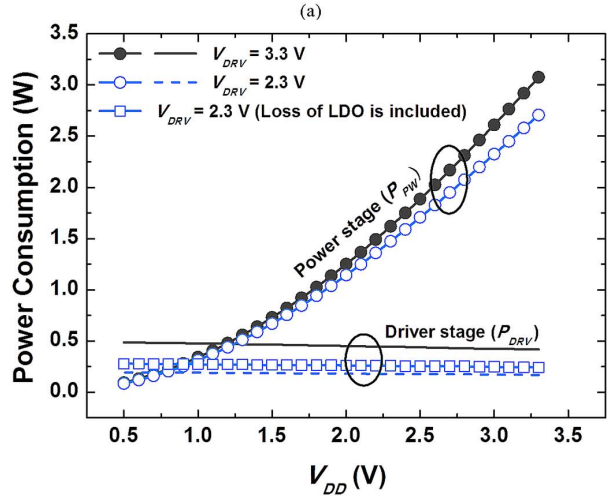


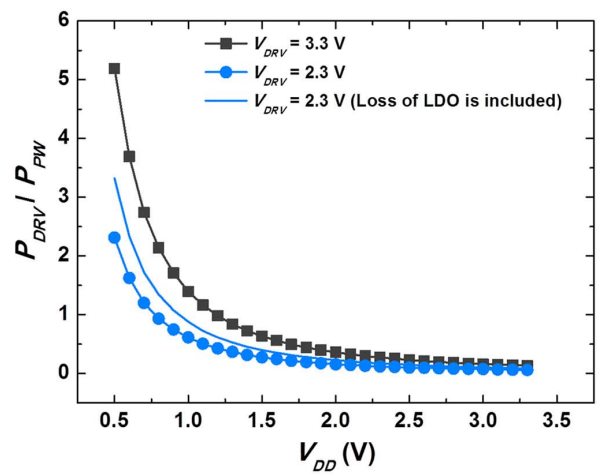
Fig. 18. Measured output power and PAE according to V_{DRV} (operating frequency $=$ 1.9 GHz, V_{DD} $=$ 3.3 V).



(a)



(b)



(c)

Fig. 19. Measured results (operating frequency $=$ 1.9 GHz). (a) Current consumption, (b) power consumption, and (c) ratio of P_{DRV} to P_{PW}.

modifications related to the modulated input signals, effects induced by harmonics, and PSRR of the driver stages are required.

IX. Conclusion

In this study, we propose an APR to support the proper operation of a CSC structure for the driver stages of an RF CMOS PA. Using the APR, we can provide optimum voltage for the second driver stage. In particular, the transistor sizes of the first and second driver stages can be optimized with the proposed APR, whereas the transistor sizes of the first and second driver stages need to be identical in any PA using a CSC structure alone. To extract the optimum transistor size of the APR, we analyzed the output power and the efficiency of a typical PA. Additionally, to verify the feasibility of the proposed APR, a PA using the CSC structure with an APR was designed. From the measured results, we successfully verify the feasibility of the proposed structure.

Appendix
Design of Typical CMOS PA to Determine the Transistor Size of the APR

In this section, we describe the designed typical CMOS PA that was used to determine the transistor size of the MP_{APR} of the proposed CMOS PA. The size of MP_{APR} is a key parameter to maximize the performance of the PA with CSC structure using an APR.

Fig. 16 shows an overall schematic of a typical CMOS PA. The typical amplifier is designed using the structure shown in Fig. 1. All of the design parameters, for example, the sizes of the transistors and transformers, are identical to those of the

proposed amplifier shown in Fig. 9. Additionally, the typical amplifier is fabricated using 0.13-μm RF CMOS technology, which is identical to that used for the proposed PA. Fig. 17 provides a chip photograph of the designed typical amplifier, which has an operating frequency of 1.9 GHz and a chip size of 1.2×1.7 mm^2.

However, the typical amplifier is designed without a CSC structure and with separate supply voltages between the power and driver stages. As highlighted in Fig. 16, the supply voltage of the driver stages, $V_{\rm DRV}$, differs from that of the power stage, V_{DD}. The transistor size of the second driver stage is twice as large as that of the first driver stage, as in the case of the proposed amplifier.

Fig. 18 shows the measured output power and efficiency according to $V_{\rm DRV}$ with a fixed supply voltage of the power stage, V_{DD}, to extract the optimum values of $V_{\rm DRV}$. As can be seen in Fig. 18, the output power is saturated when $V_{\rm DRV}$ exceeds 1.9 V. The measured efficiency is calculated using (2), which ignores the loss of the required additional regulator. In a $V_{\rm DRV}$ range from 1.9 to 2.4 V, the efficiency of the PA is maximized. Beyond a $V_{\rm DRV}$ value of 2.4 V, the excessive current through the driver stages degrades the overall efficiency. Numerical analysis of the optimum $V_{\rm DRV}$ necessary to improve the efficiency was provided in earlier works [16], [17]. In those earlier works, $V_{\rm DRV}$ was optimized by considering the charging loss and the on-resistance loss induced by the transistors. In consequence, the optimum values of $V_{\rm DRV}$ can be regarded as ranging from 1.9 to 2.4 V. This optimum range of $V_{\rm DRV}$ is used to determine the optimum size of $MP_{\rm APR}$.

Fig. 19 shows the current and power consumptions of the driver and power stages of the designed typical PA. Fig. 19(a) provides the current consumption for $V_{\rm DRV} = 2.3$ V and 3.3 V. As can be seen in Fig. 19(b), the power consumption of the driver stage, considering the effect of the LDO with $V_{\rm DRV} = 2.3$ V, is lower than that of the driver stage with $V_{\rm DRV} = 3.3$ V. In this work, we assume that LDO is ideal; we also ignore the power consumption induced by the control circuits, for example, that of the operational amplifier of the LDO. Accordingly, the loss of the LDO is calculated using the voltage drop of V_{DD}–$V_{\rm DRV}$ and the current of the drive stages. Compared to the case of the proposed structure, shown in Fig. 13, the current consumption of the driver stage of the typical structure is higher than that of the proposed structure. Additionally, as can be seen in Fig. 19(c), the ratio of $P_{\rm DRV}$ to P_{PW} of the proposed structure is lower than that of the typical structure, regardless of the values of $V_{\rm DRV}$ of the typical structure.

REFERENCES

[1] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer—A new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.

[2] B. Francois and P. Reynaert, "A Fully integrated watt-level linear 900-MHz CMOS RF power amplifier for LTE-applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1878–1885, Jun. 2012.

[3] E. Kaymaksut and P. Reynaert, "Transformer-based uneven Doherty power amplifier in 90 nm CMOS for WLAN applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659–1671, Jul. 2012.

[4] B. J. C. Zhao and B. Kim, "A compact broadband transformer-based linear CMOS power amplifier design," *Microw. Opt. Technol. Lett.*, vol. 53, no. 2, pp. 422–425, Feb. 2011.

[5] A. M. Niknejad, D. Chowdhury, and J. Chen, "Design of CMOS power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1784–1796, Jun. 2012.

[6] K. H. An, D. H. Lee, O. Lee, H. Kim, J. Han, W. Kim, C.-H. Lee, H. Kim, and J. Laskar, "A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 7, pp. 479–481, Jul. 2009.

[7] O. Lee, K. H. An, C.-H. Lee, and J. Laskar, "A parallel-segmented monolithic step-up transformer," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 9, pp. 468–470, Sep. 2011.

[8] H. Lee, C. Park, and S. Hong, "A quasi-four-pair class-E CMOS RF power amplifier with an integrated passive device transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 4, pt. 1, pp. 752–759, Apr. 2009.

[9] T. Joo, H. Lee, S. Shim, and S. Hong, "CMOS RF power amplifier for UHF stationary RFID reader," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 106–108, Feb. 2010.

[10] J. Kim, J. Son, S. Jee, S. Kim, and B. Kim, "Optimization of envelope tracking power amplifier for base-station applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1620–1627, Apr. 2013.

[11] Y. Cho, D. Kang, J. Kim, D. Kim, B. Park, and B. Kim, "A dual power-mode multi-band power amplifier with envelope tracking for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1608–1619, Apr. 2013.

[12] D. Kim, D. Kang, J. Kim, Y. Cho, and B. Kim, "Highly efficient dual-switch hybrid switching supply modulator for envelope tracking power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 6, pp. 285–287, Jun. 2012.

[13] Y.-J. E. Chen, C.-Y. Liu, T.-N. Luo, and D. Heo, "A high-efficient CMOS RF power amplifier with automatic adaptive bias control," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 11, pp. 615–617, Nov. 2006.

[14] C. Park, J. Han, H. Kim, and S. Hong, "A 1.8-GHz CMOS power amplifier using a dual-primary transformer with improved efficiency in the low power region," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 4, pp. 782–792, Apr. 2008.

[15] H. Hwang, D. Seo, J. Park, and C. Park, "Study of the inter-stage capacitor effects of a RF CMOS power amplifier to enhance its efficiency," *Prog. Electromagn. Res. C*, vol. 37, pp. 29–40, Feb. 2013.

[16] H. Hwang, D. Seo, C. Lee, and C. Park, "Numerical analysis of the supply voltage of a switching mode RF CMOS power amplifier to enhance its efficiency," *Microw. Opt. Technol. Lett.*, vol. 55, no. 10, pp. 2479–2484, Oct. 2013.

[17] H. Hwang, D. Seo, J. Park, and C. Park, "Investigation of the power transistor size related to the efficiency of switching-mode RF CMOS power amplifier," *Microw. Opt. Technol. Lett.*, vol. 56, no. 1, pp. 110–117, Jan. 2014.

[18] H. Hwang and C. Park, "Current shared cascade structure for the driver stages of switching mode RF power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 605–607, Nov. 2013.

[19] K. H. An, D. H. Lee, O. Lee, H. Kim, J. Han, W. Kim, C.-H. Lee, H. Kim, and J. Laskar, "A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 7, pp. 479–481, Jul. 2009.

[20] B. Jin, J. Moon, C. Zhao, and B. Kim, "A 30.8-dBm wideband CMOS power amplifier with minimized supply fluctuation," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1658–1666, Jun. 2012.

[21] O. Lee, K. H. An, H. Kim, D. H. Lee, J. Han, K. S. Yang, C.-H. Lee, H. Kim, and J. Laskar, "Analysis and design of fully integrated high-power parallel-circuit class-E CMOS power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 3, pp. 725–734, Mar. 2010.

[22] J. Kang, D. Yu, K. Min, and B. Kim, "A ultrahigh PAE Doherty amplifier based on 0.13-μm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 9, pp. 505–507, Sep. 2006.

[23] T. Sowlati and D. M. W. Leenaerts, "A 2.4 GHz 0.18-μm self-biased cascode power amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1318–1324, Dec. 2002.

[24] M. Fathi, D. K. Su, and B. A. Wooley, "A 30.3 dBm 1.9 GHz-bandwidth 2×4-array stacked 5.3 GHz CMOS power amplifier," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2013, pp. 88–89.

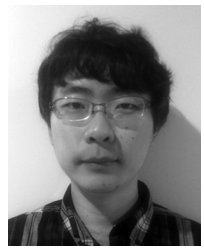
[25] Y. Luque, E. Kerherve, N. Deltimple, and D. Belot, "CMOS SFFDS PA with coupled transformer for high power RF applications," in *Proc. IEEE Int. Circuits Syst. Symp.*, 2009, pp. 1313–1316.

Hoyong Hwang (S'12) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, Korea, in 2012 and 2014, respectively.

His current research interests include CMOS RF PAs and transmitter systems.

Changhyun Lee (S'11) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, Korea, in 2011 and 2013, respectively, and is currently working toward the Ph.D. degree at Soongsil University.

His current research interests include CMOS RF PAs and transceivers for wireless chip-to-chip communication.



Jonghoon Park (S'11) received the B.S. and M.S. degrees in electronic engineering from Soongsil University, Seoul, Korea, in 2011 and 2013, respectively, and is currently working toward the Ph.D. degree at Soongsil University.

His current research interests include CMOS RF PAs and energy harvesting.

Changkun Park (S'03–M'08) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2001, 2003, and 2007, respectively.

From 2007 to 2009, he was with the Advanced Design Team of the DRAM Development Division, Hynix Semiconductor Inc., Icheon, Korea, where he was involved in the development of high-speed I/O interfaces of DRAM. In September 2009, he joined the faculty of the School of Electronic Engineering, Soongsil University, Seoul, Korea. His research interests include RF and millimeter-wave circuits, RF CMOS PAs, and wireless chip-to-chip communication and power transfers.