Model-Based Nonlinear Embedding for Power-Amplifier Design

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***Abstract*—A fully model-based nonlinear embedding device model including low- and high-frequency dispersion effects is implemented for the Angelov device model and successfully demonstrated for load modulation power-amplifier (PA) applications. Using this nonlinear embedding device model, any desired PA mode of operation at the current source plane can be projected to the external reference planes to synthesize the required multi-harmonic source and load terminations. A 2-D identification of the intrinsic PA operation modes is performed first at the current source reference planes. For intrinsic modes defined without lossy parasitics, most of the required source impedance terminations will exhibit a substantial negative resistance after projection to the external reference planes. These terminations can then be implemented by active harmonic injection at the input. It is verified experimentally for a 15-W GaN HEMT class-AB mode that, using the second harmonic injection synthesized by the embedding device model at the input, yields an improved drain efficiency of up to 5% in agreement with the simulation. A figure-of-merit is also introduced to evaluate the efficacy of the nonlinear embedding PA design methodology in achieving the targeted intrinsic mode operation given the model accuracy.**

***Index Terms*—De-embedding, embedding, harmonic load–pull, large-signal model, load modulation, load synthesis, nonlinear, power amplifier (PA).**

I. Introduction

WAVEFORM engineering has been introduced for improving the efficiency of RF power amplifiers (PAs) by minimizing the heat dissipation in active devices [1]. Also, continuous class J/F modes have been recently proposed for wideband operation [2], [3]. However, the waveforms at the measurement reference planes (MRPs) are significantly distorted by linear/nonlinear parasitic components and packages, making it difficult to directly apply these theories [4], [5]. Conventionally, harmonic source/load–pull measurements were performed to locate the optimal external loads in terms of performance figures of merit such as output power or efficiency. However, load–pull measurement data do not provide the intrinsic waveforms or the PA mode of operation without de-embedding the measured data [6]. Furthermore, the intrinsic gate and drain voltages, which can cause unwanted forward gate to source conduction or reverse breakdown in high electron-mobility field-effect devices, are unknown to designers solely relying on load–pull measurements [7].

Over the past decades, vector large-signal network analyzers (LSNAs) have made available to the designers, calibrated time-domain voltage and current waveforms in the RF frequency range at the external device planes [8]. Using this technology, significant advances in large-signal modeling, model validation, and de-embedding methodologies have also been reported [9]–[14]. Thanks to those modeling efforts, the behavior of the devices at the intrinsic reference planes are becoming more accessible to designers. Nevertheless, conventional PA design techniques rely on external driving sources and loads to iteratively optimize the internal waveforms. On the contrary, Raffo *et al.* started the PA design process from the intrinsic reference plane and embedded the nonlinear or linear parasitic components on top of the intrinsic load lines, to predict the input impedance and necessary harmonic loads at the extrinsic reference planes (ERPs) [7], [15]. This technique has been successfully applied to the design of class-E [16] and class-F [17], [18] amplifiers. Detail embedding/de-embedding methods circumventing low-frequency dispersions were reported in [19]–[22]. In these methods, the intrinsic operation mode is established by means of low-frequency measurements.

In this paper, a fully model-based embedding approach will be pursued for the non-quasi-static Angelov (Chalmers) model [23], [24]. Beside its non-quasi-static topology and drain delay accounting for high-frequency dispersion, the Angelov model includes an electrothermal memory sub-circuit accounting for low-frequency dispersion, as shown in Fig. 1(b). Memory effects associated with traps could also be included in the circuit topology [25], [26]. In the strictly model-based nonlinear-embedding approach pursued in this paper, the memory-effects affecting the device characteristics (I–V and Q–V) are indeed intended to be directly calculated by the device model itself. This contrasts with the low-frequency measurement approach where the IV characteristic are acquired experimentally at a specific operating point and device temperature. On the other hand, provided the model accounts for all low-frequency memory effects in the device, the model-based nonlinear-embedding approach is applicable to all operating points, device temperatures, and dynamic load lines possible for the intrinsic device.

To facilitate the projection of the transistor intrinsic mode of operation to the external reference planes we shall introduce in this paper an embedding transfer network (ETN), as shown in Fig. 1(b). An ETN is a nonlinear multi-port network used for the

Manuscript received October 25, 2013; revised January 26, 2014, April 21, 2014, and May 30, 2014; accepted June 13, 2014. Date of publication July 10, 2014; date of current version September 02, 2014. This work was supported in part by the National Science Foundation under Grant ECS 1129013.

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Digital Object Identifier 10.1109/TMTT.2014.2333498

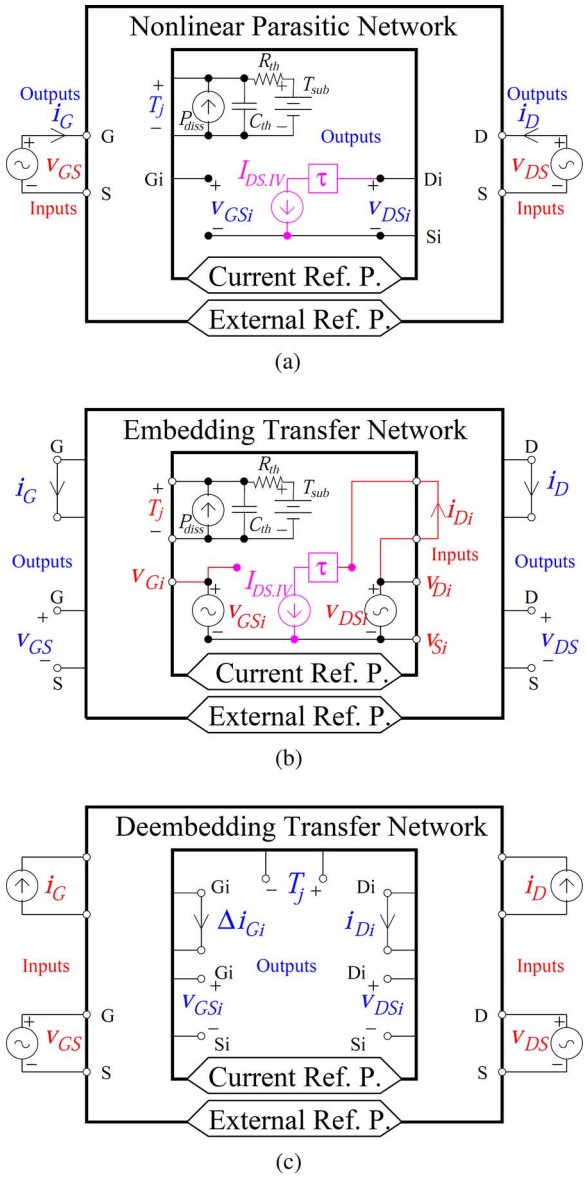

Fig. 1. (a) Circuits for the device model. (b) Embedding device model. (c) De-embedding device model. The input and output variables are grouped together and marked as Inputs (in red in online version) and Outputs (in blue in online version), respectively.

synthesis of the required multi-harmonic source and load terminations at the external reference planes. This embedding device model once developed will be verified in simulation to yield exact results (up to numerical precision) at all reference planes when driving the normal device model shown in Fig. 1(a). Note that the embedding device model for the Angelov model will be posted at publication online.[1]

The first issue encountered for nonlinear embedding PA design is that of the selection of the PA mode of operation at the intrinsic transistor level. Classes are usually defined for ideal piece-wise linear [5] dc–*IV* characteristics and some adaptation is needed for realistic nonlinear device *IV* characteristics. In this work, both the fundamental impedance yielding maximum power added efficiency (PAE) and output power will be determined using a load–pull at the fundamental while using all possible combinations of lossless second and third harmonic impedance terminations. A correlation with the traditional PA mode classification will also be attempted.

The second issue encountered for nonlinear embedding PA design not discussed in the literature is that most of the input and output harmonic impedances generated by the external load synthesis, will exhibit negative resistances making them unrealizable using passive circuits. To address this issue, an impedance re-normalization method will be introduced to find practical passive lossless terminations for which the intrinsic load line is not significantly affected. In both: 1) the external source/load synthesis and 2) the impedance re-normalization steps, the degradation in the PAE or output power can be monitored. For the device designer, steps 1) and 2) yield important technology information on the impact that the linear and nonlinear parasitics have upon the device performance. For the PA designer, step 1) will provide ways to improve the PA performance, as is discussed next.

Initially the impedance re-normalization step will be used such that only passive lossless terminations will be considered for the harmonics at the input and output reference planes. However, active harmonic impedances at the input could be implemented with the use of a proper PA driver. In the literature, the optimization of the input harmonic termination [27] or the injection of second harmonic for efficiency improvement were reported by sweeping the injected harmonic amplitude and phase [28], [29], and optimizing the internal waveforms [30], [31]. The embedding device model introduced in this work provides us with the means to actually synthesize the harmonic injections (amplitude and phase) required to implement the desired internal mode.

To experimentally study the nonlinear embedding PA design methodology, we will focus on the synthesis of constant drain-efficiency class-B modes of operation intended for the design of a load-modulation PA. A commercial packaged GaN device with 15-W peak power will be used for these studies. The internal PA design will be next projected to the external reference planes using the embedding device model of Fig. 1(b). The transistor will then be experimentally tested for actual impedance terminations approximating the synthesized and re-normalized output impedances. Finally, a figure-of-merit will be introduced to estimate the efficacy of the nonlinear embedding PA design methodology in controlling the intrinsic device operation in a real device given the model accuracy.

Furthermore, to demonstrate another application of the nonlinear embedding PA design methodology, we will inject at the transistor external input, a second-harmonic excitation with the phase and amplitude determined by the ETN in order to implement the targeted internal mode of operation. The nonlinear embedding PA design methodology will then be experimentally validated by comparing the predicted and measured variation of the output power and PAE versus incident power under load modulation in the presence of constructive and destructive second harmonic injection.

In accordance with our discussion and the literature review, this paper is organized as follows. The harmonic load–pull at the intrinsic reference planes for mapping and identifying the

[1][Online]. Available: http://www2.ece.ohio-state.edu/~roblin/NSFweb.html

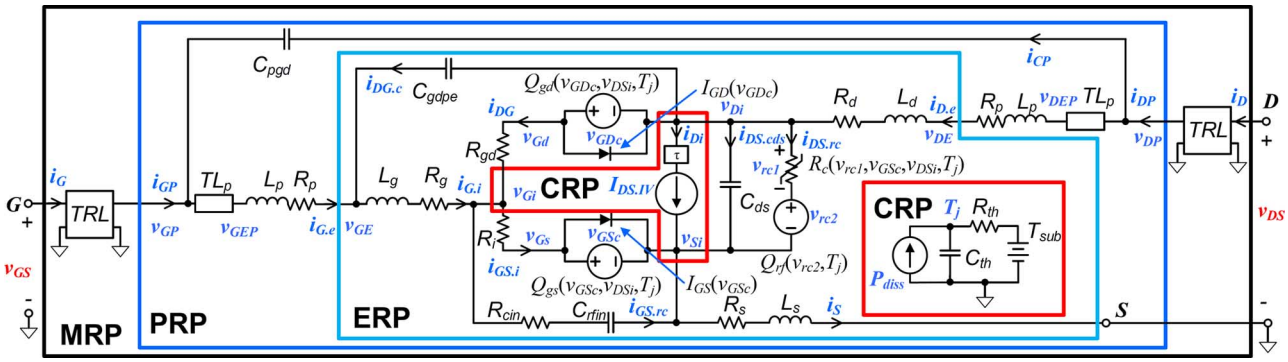

Fig. 2. Packaged large-signal equivalent circuit using Angelov model equations is used for loads synthesis process. The red (in online version), light blue (in online version), dark blue (in online version), and black boxes defines the CRP, ERP, PRP, and MRP, respectively.

intrinsic transistor operation modes and the mode projection to the external reference planes will be presented in Section II. An overview of the model extraction performed will be presented in Section III. The performance of the PA under load modulation and input harmonic injection will be first studied in simulation in Section IV, and compared to the measurements in Section V. Conclusions will then be drawn in Section VI.

II. Internal Design and Embedding Process

A. Embedding Nonlinear Parasitics

The circuit topology used for this work including the intrinsic device model, the linear and nonlinear parasitic networks, the package circuit model, and the device access circuit is shown in Fig. 2. The packaged device is mounted on a circuit board and connected to the RF connectors via access lines. The RF measurements are performed at the connector levels, which define the MRP. The reference plane outside the package is referred to as the package reference plane (PRP), while the reference plane inside the package is referred to as the ERP. The intrinsic nonlinear drain current at the current source reference plane (CRP) is a function of the intrinsic node voltages $v_{\mathrm{DS}i}$ and $v_{\mathrm{GS}i}$ and the junction temperature, T_j

$$i_{Di}(t) = I_{\mathrm{DS}.IV}(v_{\mathrm{GS}i}(t), v_{\mathrm{DS}i}(t), T_j(t)). \tag{1}$$

Note that high-frequency dispersion effect associated with the drain propagation delay τ is included as part of the intrinsic device model. The thermal network, which is shown in a separate CRP box on Fig. 2, is actually part of the intrinsic device model. The instantaneous dissipated power P_{diss} is a function of the intrinsic voltages and currents. Other low-frequency dispersion effects like trapping could also be included. Thus, the intrinsic device model is not necessarily memoryless like the intrinsic *IV* characteristics, but may include low-frequency dispersion and high-frequency dispersion effects. It is further noted that the charges Q_{gd} and Q_{gs}, which shunt the diodes I_{GD} and I_{GS}, are connected in series with the resistance R_{gd} and R_i, respectively. Thus, the Angelov device model cannot be separated in a pure resistive and capacitive core and the embedding device model will rely instead on the defined current reference plane.

Note also that use is made of the notation i_{Di} and $I_{\mathrm{DS}.1}$ to indicate the time- and frequency-domain voltages, respectively,

$$i_{Di}(t) = \mathcal{R}e\left[\sum_{n=0}^{N} I_{\mathrm{DS}.1}(n\omega)e^{jn\omega t}\right].$$

The intrinsic device operation can be fully controlled by the designer by applying any type of excitation between the intrinsic gate and source and between the drain and source. This includes, for example, the self-consistent case of a dc supply voltage and arbitrary harmonic impedance terminations applied between the drain and source terminals. The resulting outputs from the intrinsic device operation simulation include the intrinsic drain currents i_{Di}, the drain voltage $v_{\mathrm{DS}i}$, and the gate voltage $v_{\mathrm{GS}i}$, as shown in Fig. 1. Note that only the drain dc–*IV* $I_{\mathrm{DS}.IV}(v_{\mathrm{GS}i}, v_{\mathrm{DS}i}, T_j)$ is included among the device dc current sources. Thus, the dc gate current leakage is assumed to be part of the parasitic network and the intrinsic gate current at the CRP is zero and not needed.

Given the desired intrinsic voltages $v_{\mathrm{DS}i}$ and $v_{\mathrm{GS}i}$ and current $I_{\mathrm{DS}.IV}$, the required branch currents through the nonlinear and linear parasitic elements and the required node voltages to maintain the intrinsic operation can be readily calculated. In this work, this embedding process is done with the help of a multiport circuit, the so-called ETN of Fig. 1(b), which is composed itself of multiple linear/nonlinear parasitic sub-circuits of the device model, as shown in Fig. 3. It shows the complete ETN for the intrinsic mode projection from the CRP to the ERP.

Note that this embedding process, which thus works in the reverse direction of de-embedding, encompasses nonlinear elements accounting with non-quasi-static effects, as shown in Fig. 3(a) and (b). General equations for a quasi-static model are given in [7]. For the non-quasi-static Angelov model, the following self-consistent equations needs to be solved:

$$\begin{aligned} i_{DG} &= \frac{v_{Gi} - v_{Gd}}{R_{\mathrm{gd}}} \\ &= I_{\mathrm{GD}}(v_{\mathrm{GD}c}) + \frac{dQ_{\mathrm{gd}}(v_{\mathrm{GD}c}, v_{\mathrm{DS}i}, T_j)}{dt} \end{aligned} \tag{2a}$$

$$\begin{aligned} i_{\mathrm{GS}.i} &= \frac{v_{Gi} - v_{Gs}}{R_i} \\ &= I_{\mathrm{GS}}(v_{\mathrm{GS}c}) + \frac{dQ_{\mathrm{gs}}(v_{\mathrm{GS}c}, v_{\mathrm{DS}i}, T_j)}{dt} \end{aligned} \tag{2b}$$

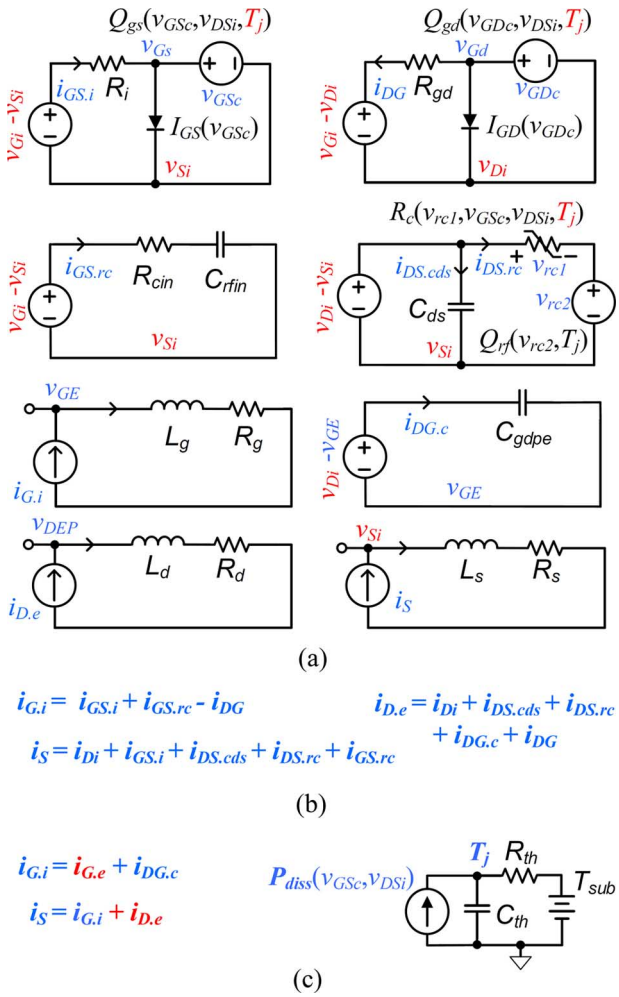

Fig. 3. ETN and de-embedding transfer network (DTN) for the intrinsic mode projection from the intrinsic to the ERPs. The sub-circuits common to the ETN and DTNs are shown in (a). The current equations and the thermal sub-circuits, which are specific to the ETN and DTN, are shown in (b) and (c), respectively (a) Common circuits. (b) Embedding only. (c) De-embedding only.

where $R_{\rm gd}$ and R_i are the channel resistances in series with the charges $Q_{\rm gd}$ and $Q_{\rm gs}$ establishing the non-quasi-static RC channel charging times. As mentioned in [7], these equations can be iteratively solved using, for example, the harmonic-balance method [32]. The additional dispersive sub-circuits shown in Fig. 3(a)–(c) are similarly analyzed.

The sum of all the drain branch currents, i.e., i_{De}, is then used to drive the drain parasitic sub-circuit L_d and R_d in Fig. 3(a). Similarly the sum of all the source branch currents, i.e., i_S, is used to drive the source parasitic sub-circuit L_s and R_s in Fig. 3(a).

This nonlinear embedding is performed by a circuit simulator, typically a harmonic-balance simulator. The simulation of the embedding device model yields both the external voltages, $v_{\rm GS}$ and v_{DS}, and the external currents, i_D and i_G, required for achieving the desired internal operation at the intrinsic reference plane. Since like the device model, the embedding device model is packaged as a standalone circuit, its operation is transparent to the designer who does not need to have access to its internal node and components, which may remain proprietary if needed.

Once the external voltage and currents (flowing into the device) are obtained, the complete set of external sources and loads can be calculated in the frequency domain for each harmonic (for $n > 1$ on the source side) using the usual formula

$$Z_S(n\omega) = -\frac{V_{\rm GS}(n\omega)}{I_G(n\omega)} \quad Z_L(n\omega) = -\frac{V_{DS}(n\omega)}{I_D(n\omega)}. \tag{3}$$

The exact same internal mode of operation can then be verified to be obtained from the original device model in Fig. 2 when the multi-harmonic gate and drain voltages and dc biases synthesized by the embedding device model of Fig. 1(b) are externally applied to the device model of Fig. 1(a). In this regard, the embedding device model and its associated ETN generate exact synthesis results as far as the model is concerned.

Alternatively the impedance terminations $Z_S(n\omega)$ and $Z_L(n\omega)$ can be used for the harmonic $n\omega$ when the real part of the impedances are positive. Otherwise for impedances with a negative real part, active sources are required. The presence of such negative resistances then becomes a source of concern as conventional amplifiers are usually driven by the dc supply, the fundamental input excitation, and passive harmonic load terminations. This issue will be addressed in more detail in Section II-B.

B. Intrinsic Operation Mode Identification and Projection

This section presents an example of PA mode mapping and identification at the CRP and projection to the PRPs using the embedding device model. The device model and embedding device model for the Angelov model were implemented in Agilent ADS using equation-based symbolically defined devices (SDDs). The package, parasitics, and model coefficients themselves used in this section are from [24]. Harmonic load–pull simulations at the fundamental frequency were performed in Agilent Technologies' Advanced Design System (ADS) at the intrinsic reference plane for all passive load $Z_L(\omega)$ while using lossless load termination for the harmonics, to find the fundamental load providing either maximum PAE or maximum output power. To map all possible lossless load terminations for the harmonics, the second and third harmonic phases of the load reflections $\Gamma_L(n\omega)$ were swept while keeping their amplitude unity: $|\Gamma_L(n\omega)| = 1$ (lossless). The drain was biased at 28 V, the gate at -4.5 V, and 40-mA drain current. The input was excited by an RF voltage source with an amplitude of 3.5 V at 2 GHz. The analysis reported here is limited to the second and third harmonic. The higher harmonics were assumed to be shorted, although other options were considered (not reported here).

The maximum PAE is plotted in Fig. 4(a) in the harmonic phase space (θ_2, θ_3) for the fundamental load $Z_L(\omega)$ maximizing the PAE: $\mathrm{PAE}(\theta_2,\theta_3)|_{\Gamma_{L.\mathrm{PAE}_{\max}}}$. The maximum output power is also plotted in Fig. 4(b) in the harmonic phase space (θ_2, θ_3) for the fundamental load $Z_L(\omega)$ maximizing the output power: $P_{\rm out}(\theta_2,\theta_3)|_{\Gamma_{L.P_{\rm out.max}}}$. θ_2 and θ_3 are the phases of the second and third harmonic load reflection coefficients $\Gamma_L(2\omega)$ and $\Gamma_L(3\omega)$, respectively.

The phase location of the conventional modes of class B/J, quasi-class F, and the recently proposed continuous J modes (◯, black) are indicated in Fig. 4. Also located are the $\mathrm{B}^{-1}/\mathrm{F}^{-1}$,

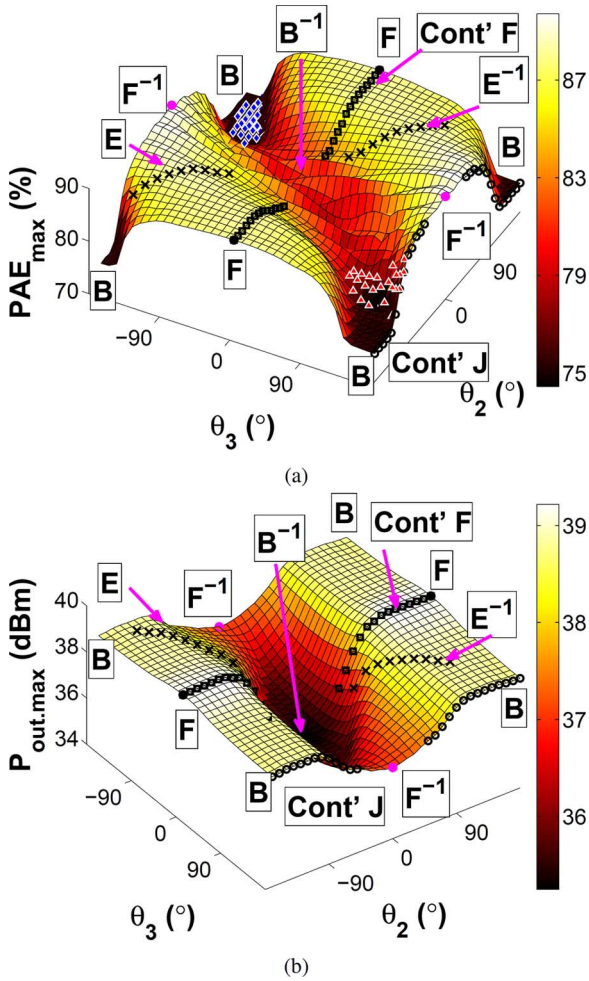

Fig. 4. Results of harmonic load–pull simulations at the intrinsic reference plane to maximize: (a) the PAE and (b) the output power using only the intrinsic *IV* model at 2 GHz.

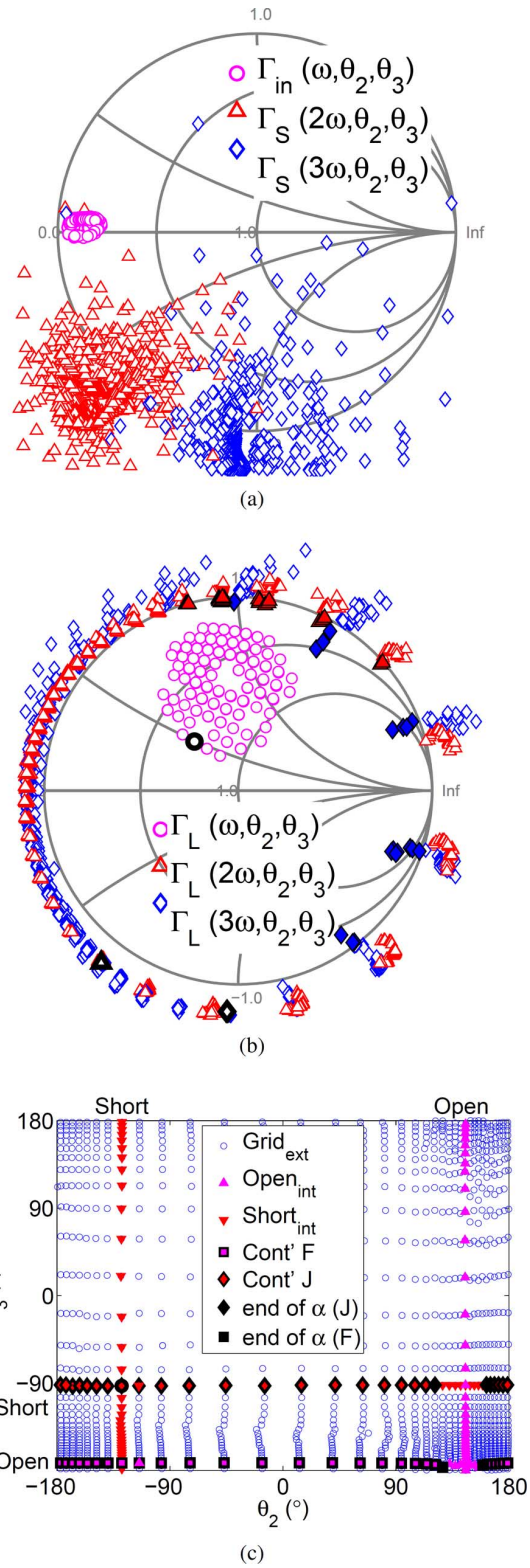

Fig. 5. Optimal source $\Gamma_S(n\omega), n = 1, 2, 3$ and load $\Gamma_L(n\omega), n = 1, 2, 3$ terminations maximizing the PAE once embedded to the PRP by the ETN are shown in Smith charts (a) and (b), respectively, at 2 GHz. The intrinsic harmonic phases θ_2 and θ_3 at the CRP (and its various PA modes) are remapped as indicated in (c) into the extrinsic θ_2 and θ_3 phase space at the PRP.

the inverse class B/F, as well as the quasi-continuous class F (□, black). Wide flattop (light color) areas of high PAE are observed for this device. However, noticeably different results may result if the designer elects to use different lossless terminations for the fourth and higher harmonics.

The black line $(\times)$ marked E and E^{-1} indicates the conditions when capacitive or inductive loads are used for the second and third harmonics as is the case for class E and inverse class E, respectively. In Fig. 4(a), the line connecting the two points associated with class F and inverse class F and intersecting with the class-E-like mode in the middle provides a robust high-efficiency operation with wide design choices. This mode was noticed in the literature [33], [35], and a similar area was called the "EF plateau" in [33]. Note that an absolute classification of the transistor modes is not possible since those are defined for ideal devices and the device used here features a realistic *IV* characteristic exhibiting a finite knee voltage, nonzero drain conductance, and gate–voltage-dependent transconductance.

The harmonic load–pull results were projected to the PRP using the nonlinear ETN including the fundamental, second, and third harmonics, as shown in Fig. 5(a) and (b) for the source and load, respectively. The optimal fundamental load and source termination required for maximum PAE for all second and third harmonic lossless terminations are indicated by the circles (magenta in online version) in Fig. 5(a) and (b). Note that the θ_2 and θ_3 phases were swept in a uniform harmonic grid at the CRP

with steps of 10°. This mapping reveals a strong asymmetry in the distribution of the terminations around the Smith chart at the PRP resulting in uneven harmonic loading sensitivity. The fundamental loads (◯, magenta in online version) in Fig. 5(a) are rotated by nearly 100° due to the parasitics. The class B is singled out by a thick black circle, triangle, and diamond for the fundamental, second, and third harmonics, respectively.

Fig. 5(c) focuses on the phase remapping of the intrinsic harmonic phase θ_2 and θ_3 at the CRP into the extrinsic θ_2 and θ_3 phase space at the PRP. As can be seen, the external grid has a nonuniform density compared to the uniform grid used for the internal harmonics. Highlighted are the location of the intrinsic open (△, magenta in online version), short (▽, red in online version) terminations, and other identified modes (□, black and ⋄, black) at the PRP. The extrema of the variable α from the continuous mode class J/F [2], [3], which has a finite second harmonic sweep range, are marked with solid black diamonds and squares, respectively.

Most of the synthesized external harmonic loads exhibit a negative resistance needed to compensate for the loss in the resistive parasitics. The synthesized external supply dc voltage is also higher than the internally applied dc voltage. However, a few of the harmonic terminations marked by solid triangles (red in online version) for the second harmonic and solid diamonds (blue in online version) for the third harmonic in Fig. 5(b) fall inside the Smith chart and thus exhibit a positive resistance. It can be verified that they are associated with low PAEs, as indicated by the filled white triangles and diamonds in Fig. 4(a).

In summary, in this section we have presented the nonlinear embedding PA design methodology for the design of the PA arbitrary mode of operation (class) after having developed an embedding device model for the non-quasi-static Angelov model. In the first step of the nonlinear embedding PA design, a load–pull at the fundamental frequency is performed at the CRP for a specific choice of lossless harmonic termination so as to select the targeted intrinsic mode of operation providing either maximum output power or maximum efficiency. Repeating this process for all second and third harmonics (2-D) lossless termination possible, all the optimal 2-D intrinsic mode can be mapped. In addition to the well-known PA modes (B, F, J, E), a continuum of unreported high-performance intrinsic modes available to the designer is identified. In the second step of the nonlinear embedding PA design, the projection of these intrinsic mode from the CRPs to the ERP is performed with the embedding device model to synthesize the exact required source and load terminations to achieve the desired intrinsic mode of operation. Performing this projection for all second and third harmonics (2-D) lossless termination possible, it is observed that most of the required multi-harmonic source and load terminations exhibit a negative resistance. This result, which was observed in all other devices tested, is to be expected since the mode projection synthesizes the multi-harmonic source and load terminations, which compensate among other things for the loss of the parasitics network. The techniques of: 1) active harmonic injection and 2) harmonic load re-normalization will be investigated in the remainder of this paper to address the negative resistance issue and present practical applications of the nonlinear embedding PA design methodology.

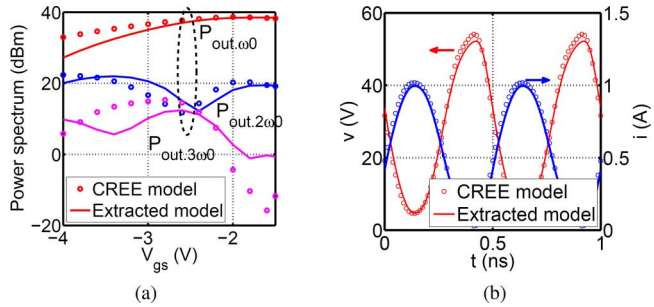

Fig. 6. Extracted Angelov model is compared to the original CREE model in terms of power spectrum: (a) up to third harmonics and waveforms (b) at the bias condition marked with dotted ellipse in (a).

III. Device Model Extraction

In the remainder of this paper, we will apply the nonlinear embedding PA design methodology to a 15-W peak power packaged GaN power device (CGH27015F, CREE Inc.). The Angelov device model and embedding device model presented in Figs. 1 and 2, respectively, are used for this purpose. The needed Angelov model parameters for this transistor were extracted using the Agilent commercial device modeling software Integrated Circuit Characterization and Analysis Program (ICCAP). The required dc characteristics and small-signal S-parameter data were generated in ADS from the device model provided by CREE for the CGH27015F transistor.

The following steps were used for this model extraction. First, the package was de-embedded in ADS using the package model (440166) provided for this device. Gate and drain voltage sweeps ranging from -8 to 0 V and -2 to 56 V, respectively, were used for the intrinsic device modeling. For the gate–voltage-dependent nonlinear capacitances, the gate was swept from -5 to -1 V with 0-V drain voltage from 100 MHz to 10.1 GHz. The drain voltage was swept from 0 to 56 V with 0-V gate voltage in the same frequency range for the extraction of the nonlinear drain voltage-dependent capacitance. So-called cold field-effect transistor (cold-FET) [36] data were also acquired for series parasitics extraction from simulations in the frequency range of 100 MHz to 2.1 GHz. The data was acquired at the temperature of 25 °C and the same temperature was maintained throughout the measurement in Section V. The thermal resistance of 8.0 °C/W from the data sheet was used and was not separately extracted.

The integrated charge Angelov model was used in the simulation considering the importance of charge conservation in the harmonic-balance solvers. The extracted model was implemented in the Agilent ADS using SDDs and compared with the original CREE model, as shown in Fig. 6. For comparison, the drain voltage was fixed at 28 V and the gate voltage was swept from -4.0 to -1.5 V around the threshold voltage of -2.9 V. Power spectra to the third harmonic were compared to each other. The extracted model (solid lines) agree reasonably well with the CREE model (dotted lines) above the threshold voltage, but does exhibit some deviation below it in the subthreshold region. Voltage and current waveforms generated at the bias condition marked with dotted ellipse in Fig. 6(a) exhibit good agreement, as depicted in Fig. 6(b). Therefore, the device model is

expected to give reasonable predictions for class-B, class-AB, and class-A bias conditions. Furthermore, we shall see that a high fidelity model is not critically required to obtain good results with the nonlinear embedding PA design technique.

IV. Design of a Load-Modulated Class-B PA

A. Constant Efficiency Load Modulation Design

To validate the nonlinear embedding PA design technique, a class-B PA intended for load modulation (R_L varying with $P_{\rm inc}$) will now be designed at the CRP. For improved linearity, we assume that the operation is limited to the linear (saturation) *IV* region with the load lines touching the knee of the *IV*. When using a piecewise-linear *IV* model with a constant knee voltage V_k, the drain efficiency η is given by

$$\eta = \frac{P_{\rm RF}}{P_{\rm DC}} = \frac{\pi R_L(P_{\rm inc})|I_D(\omega, P_{\rm inc})|}{4V_{DD}} = \frac{\pi}{4}\frac{(V_{DD}-V_k)}{V_{DD}} \quad (4)$$

where $P_{\rm RF}$ is the RF output power, $P_{\rm DC}$ is the supplied dc power, $I_D(\omega, P_{\rm inc})$ is the amplitude of the drain current at the fundamental frequency, and $R_L(P_{\rm inc})$ is the output load at the fundamental frequency and V_{DD} the drain bias. From (4), we deduce that the efficiency will remain constant if the product of the fundamental load and the fundamental output current, $R_L(P_{\rm inc})|I_D(\omega, P_{\rm inc})|$, is kept constant for all incident powers. Therefore, a constant drain-efficiency η can theoretically be realized by selecting the loads to be inversely proportionally to the drain current

$$R_L(P_{\rm inc}) = \frac{4\eta V_{DD}}{\pi|I_D(\omega, P_{\rm inc})|} = \frac{V_{DD}-V_k}{|I_D(\omega, P_{\rm inc})|}. \quad (5)$$

This design was applied to the extracted Angelov device model at the intrinsic reference plane to achieve in simulation a peak power of 10 W. The intrinsic *IV* model was biased with a drain voltage of 27.5 V and a gate voltage of -2.9 V resulting in 104 mA of drain current (with no RF applied) for class-AB operation. Fig. 7(a) shows the simulated internal loads and current relationship when the products of the normalized currents and loads are kept equal to "1." In Fig. 7(b), the actual intrinsic output power $P_{\rm out}$ and the intrinsic drain efficiency $\eta_{\rm int}$ are plotted versus incident power. The peak power is 40 dBm as designed and reduces quasi-linearly with reduced excitations. As intended, the drain efficiency remains nearly constant over the 26–29-dBm incident power range and slightly decreases at lower incident power. The drain efficiency decreases noticeably by 7% for lower incident powers when using the Angelov intrinsic *IV* model. This is due in part to the gradual transconductance reduction at gate voltages approaching the threshold voltage.

Fig. 8(a) and (e) shows the designed intrinsic load lines and waveforms, respectively, obtained in simulation. The intrinsic dc–*IV* curves obtained from the transistor model at the same reference planes as the load lines are provided as references. The six different load lines correspond to the six power levels in Fig. 7. The load lines are reaching the *IV* knee at low drain voltages for each load as intended. The intrinsic voltage waveform clearly exhibits a sinusoidal waveform due to the harmonics

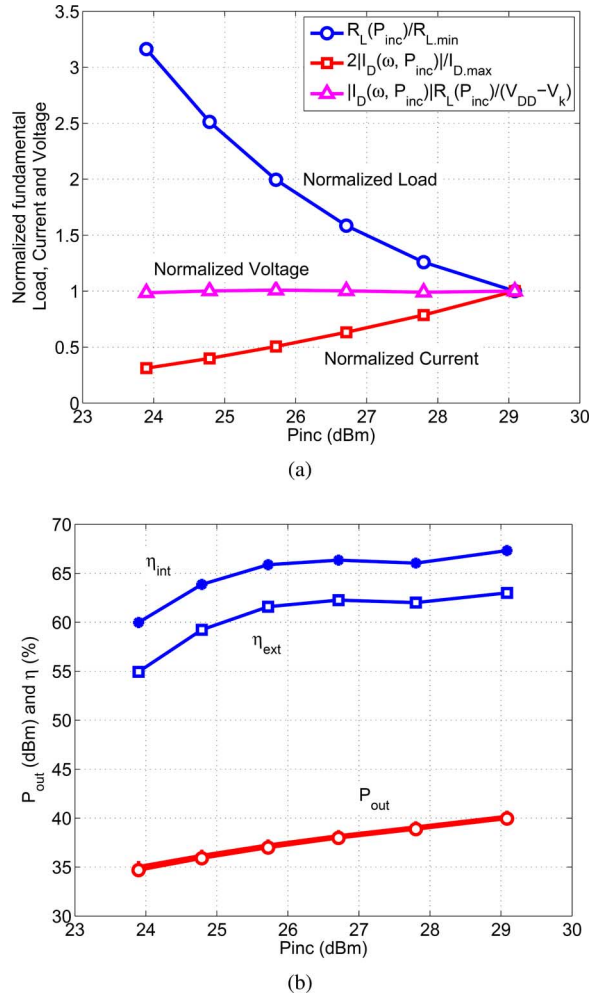

Fig. 7. Simulated fundamental load, output current, and output voltage at 2 GHz satisfying the constant drain efficiency criteria, are plotted in (a) versus incident power for the extracted Angelov device model. The currents and loads were normalized by their values at maximum output power. The simulated output power and drain efficiencies are plotted in (b) versus incident power for the extracted Angelov device model at both the current source and PRPs.

being shorted and the current waveforms approach half-rectified sinusoidal waves. Being able to shape the intrinsic load lines and waveforms during the design process is one of the targets of the nonlinear embedding PA design method for more effective waveform engineering. Fig. 7(b) compares the internal and external drain efficiencies. The internal efficiency was calculated at the CRP and the external efficiency was calculated at the PRP after the mode projection process with the ETN. Due to the lossy parasitic components, the external efficiency is lower than the internal efficiency by about 4%.

B. External Projection of Internal Operation

The current source PA design is embedded to the various reference planes (ERP, PRP, and MRP) using the ETN so as to predict the input excitations and loads at each harmonic, which are required to synthesize the desired internal PA operation at the CRP. The drain voltage (solid lines ←, red in online version) and drain current (solid lines →, blue in online version) waveforms, source $\Gamma_S(n\omega)$, and load $\Gamma_L(n\omega)$ reflection coefficients,

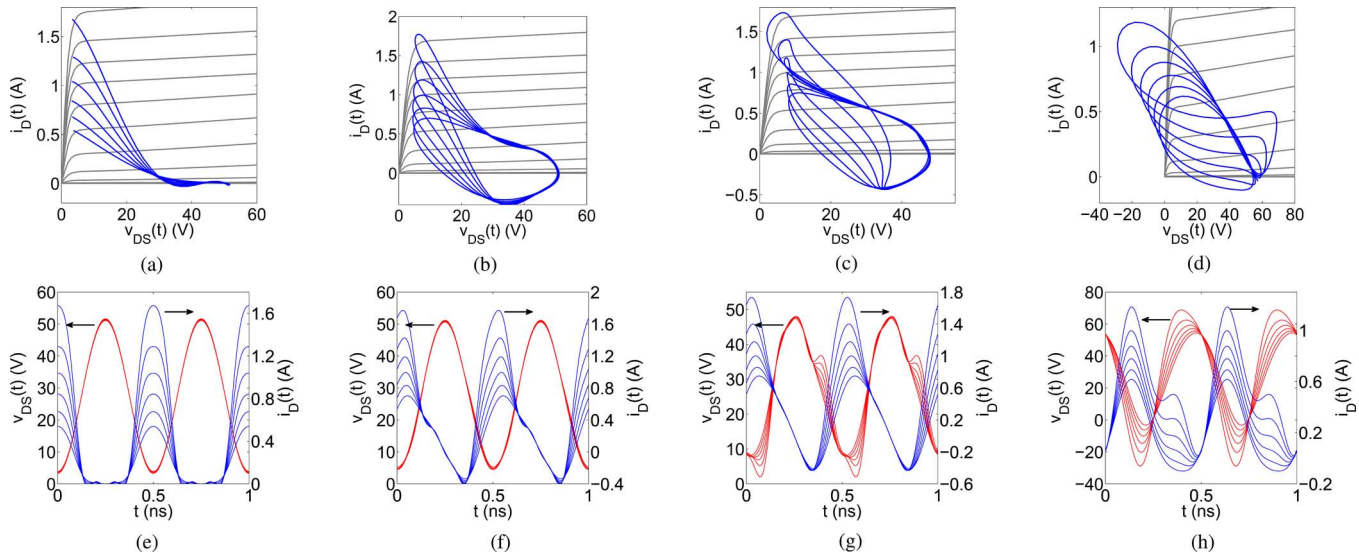

Fig. 8. Simulated 2-GHz load lines and waveforms at the CRPs (a) and (e), respectively, are embedded to the ERPs in (b) and (f), the PRPs in (c) and (g), and the MRPs at the connectors (d) and (h). (a) and (e) Current source. (b) and (f) Extrinsic. (c) and (g) At package. (d) and (h) At connector.

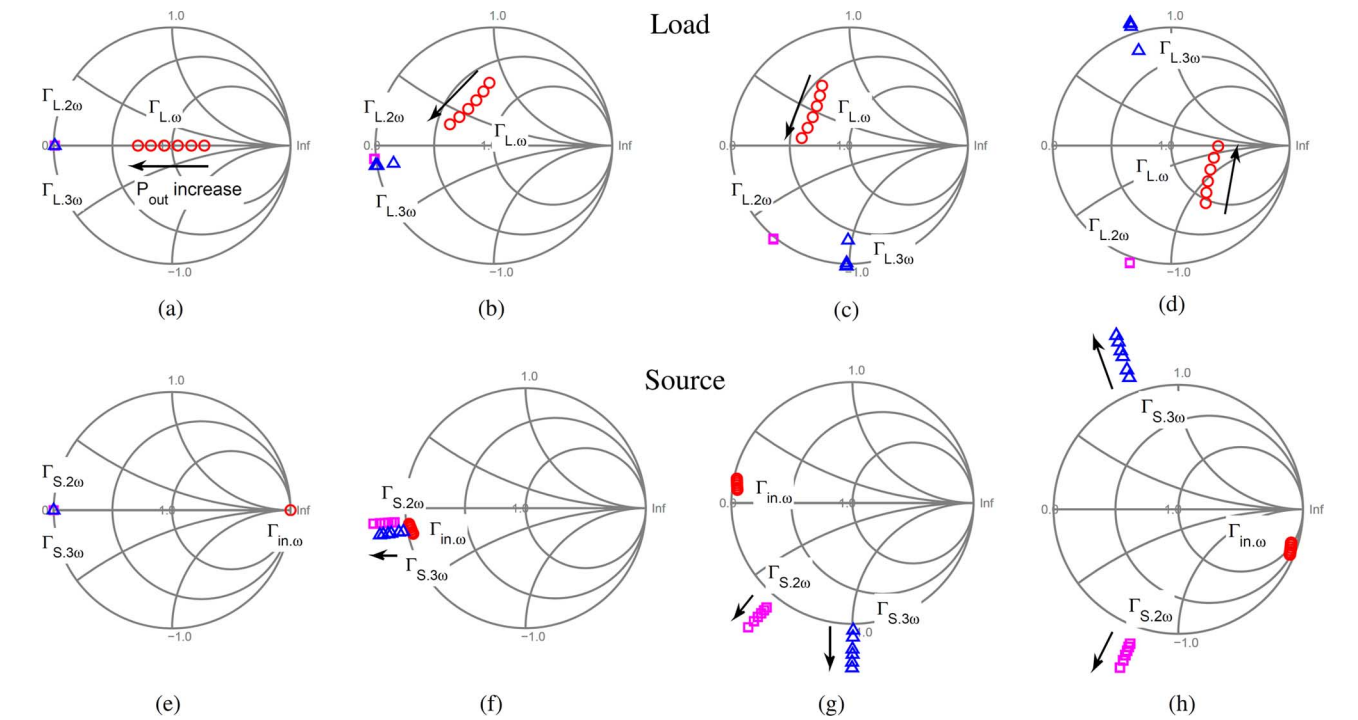

Fig. 9. Simulated 2-GHz intrinsic load and source reflection coefficients shown in (a) and (e), respectively, at the CRP, are successively mapped using the ETN to each of the external reference planes: in (b) and (f) for the ERP in (c) and (g) for the PRP, and in (d) and (h) for the MRP. (a) and (e) Current source. (b) and (f) Extrinsic. (c) and (g) At package. (d) and (h) At connector.

generated during the embedding process, are shown at each of the reference planes of interest in Figs. 8 and 9, respectively.

As can be seen in Fig. 9(a) and (e), the second and third harmonic source and load reflection coefficients are "−1" (short) at the intrinsic reference plane, as expected for an ideal class-B operation. The fundamental loads, $\Gamma_L(\omega)$, have only real components at the intrinsic reference plane, as shown in Fig. 9(a). The six circles (red in online version) correspond to the loads at the six considered power levels. The arrow in the figure is showing the required variation of the loads as the input and output power are increased.

The source reflection coefficients are calculated in the frequency domain using

$$\Gamma_S(n\omega) = \frac{V_G(n\omega) + I_G(n\omega)Z_0}{V_G(n\omega) - I_G(n\omega)Z_0} \tag{6}$$

where V_G and I_G are gate voltage and current phasors and Z_0 is the reference impedance. Since $I_G(n\omega)$ are "0" given the transistor IV model used at the CRP has infinite input impedance at all harmonics, and since a generator is only connected at the fundamental frequency, we have $\Gamma_S(n\omega) = 1/\Gamma_{\text{in}}(n\omega) = -1$ for $n > 1$ and $\Gamma_{\text{in}}(\omega) = 1$, as shown in Fig. 9(e).

When the contribution of the nonlinear and linear parasitic components are accounted for by the ETN, the load lines and the reflection coefficients at the ERP are, respectively, distorted and rotated, as shown in the second column of the Figs. 8 and 9. The third columns of Figs. 8 and 9 show the effect of the package parasitics at the PRP). The third harmonic reflection coefficients can be seen to be rotating faster in terms of phase than the second harmonic, as expected. The last columns show the results at the MRP after adding the access lines and connectors. A transmission-reflection-line (TRL) calibration kit was built and characterized using S-parameter measurements. It was found that the proper estimation of the indeterminate sign of the test bed S_{12} in the TRL deembedding [34] was critical to obtain the correct phases for the odd harmonics relative to the even harmonics. The measured error box of the access line and the connectors was imported in ADS for simulation. The TRL data were acquired in the range of 0.6–8.5 GHz covering up to the fourth harmonic to obtain reasonable accuracy in measurements [35].

It should be noted that $\Gamma_{\rm in}(\omega)$ in Fig. 9(h) remains inside of the Smith chart. However, the second and third harmonic reflection coefficients $\Gamma_S(n\omega)$ in Fig. 9(h) become larger than "1." This issue is discussed in more detail in Section IV-C.

C. Input Second Harmonic Injection

The ideal class-B condition, defined at the intrinsic reference plane, requires an internal harmonic short. Therefore, the harmonic power dissipated internally needs to be effectively regenerated at the ERP. Harmonic injection from the source side is thus required even though the class-B operation at the CRP does not by itself require any harmonic excitation. Also, since some of the parasitic components are lossy, higher harmonic injection power than can be obtained from passive harmonic terminations may be required, resulting in the harmonic reflection coefficients being outside of the Smith chart. The embedding device model provides in Fig. 9(h) the exact amount of harmonic excitations $(a_1(n\omega) = \Gamma_S(n\omega)b_1(n\omega))$ or reflection coefficients $\Gamma_S(n\omega)$ from the source to keep the desired internal class-B operation.

Simulations were conducted in addition to the previous load modulation conditions for three different cases: (a) with no harmonic injection and with second harmonic injection, (b) with the ETN predicted phase, and (c) with the opposite ETN phase (180° shift). The input harmonic excitations and loads predicted by the Angelov embedding device model were applied to two models, the extracted Angelov model and the original CREE device model. The simulation results show a significant impact of the harmonic injection on the PAE and negligible effect on the output power, as shown in Fig. 10. As can be seen in Fig. 10, the output powers overlap with each other for the three cases. On the other hand, the PAE exhibits a distinct improvement in a constructive way (solid and dashed lines with triangles, magenta in online version) compared to the fundamental only excitation (lines with circles, red in online version) without any harmonic injection. On the contrary, when the phase was opposite (180°) to the predicted ETN phase, the PAE was decreased, the harmonic injection working in a destructive way (lines with nabla, blue in online version). Even though the excitation and loads applied to the CREE model were predicted from the Angelov extracted device model using the ETN, the effect of the harmonic injection on the PAE is also similarly noticeable for the CREE model.

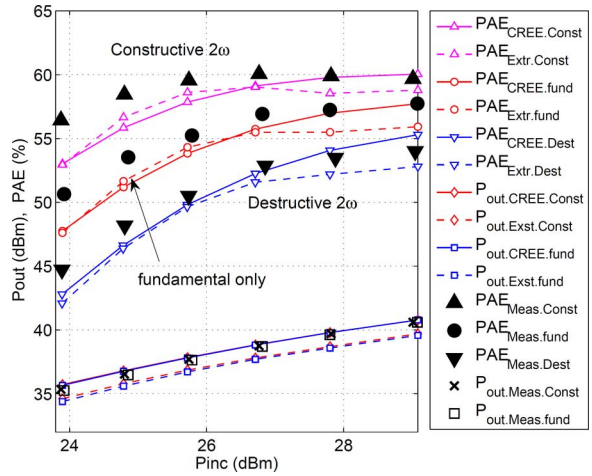

Fig. 10. Measured PAE and output power versus the fundamental incident power $|a_1(\omega)|^2$ are compared to the simulation results for the extracted Angelov model (dashed lines) and the original CREE model (solid lines) for three different injections of the second harmonic at 2 GHz: without injection (◯), injection with constructive phase (△,"constructive") and injection with destructive phase (▽,"destructive").

In this work, it has been assumed so far that by optimizing the power efficiency of the intrinsic device, the power efficiency of the extrinsic device will be optimal. This assumption is well justified in the case where the power dissipated in the parasitic network is a small fraction of the power dissipated by the intrinsic device. This is partly verified in the device studied here where the average intrinsic efficiency is about 65% and the average drain extrinsic efficiency is about 61%. To verify that the ETN indeed predicts the optimal phase for the second harmonic injection, a sweep of the phase is desirable. For this experiment, the input power at the fundamental was selected to correspond to one of the six power levels considered (fourth one with $|a_1(\omega)| = 26.7$ dBm). The second harmonic amplitude was kept to the value $(|a_1(2\omega)|/|a_1(\omega)| = -18.6$ dBc) predicted by the embedding device model and the phase was swept from $-180°$ to $180°$ [39].

Fig. 11 shows the simulated sinusoidal variation of the PAE with the second harmonic phase obtained using a solid line (blue in online version) for the Angelov model. The prediction of the embedding device model for the optimal phase and its opposite (180° shifted) are indeed verified to correspond to the maximum and minimum, respectively, of the phase sweep. Note that nearly the same results are predicted by the CREE device (dashed line, magenta in online version in Fig. 11) using the prediction of the Angelov embedding device model.

These various simulation predictions we have obtained from the Angelov and CREE models will now be compared to measured experimental data in Section IV-D.

D. Intrinsic Versus Extrinsic Harmonic Terminations

As mentioned in Section IV-C, the predicted harmonic sources and loads are usually active with some of them falling inside the Smith chart.

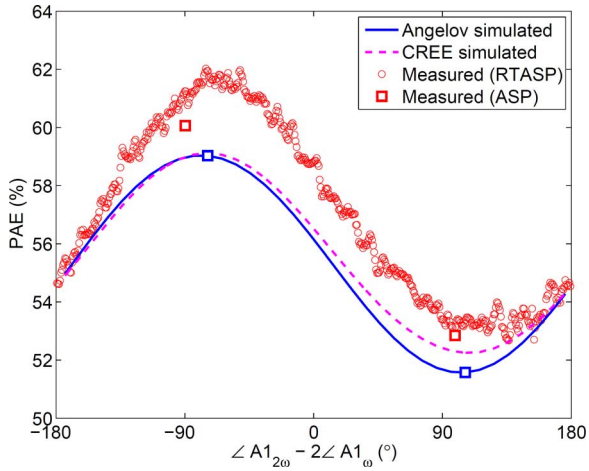

Fig. 11. Phase of the injected second harmonic at 4 GHz was swept in simulation and measurement. The extracted model (solid line, blue, in online version) and the CREE model (dashed-line, magenta, in online version) were used in the simulations.

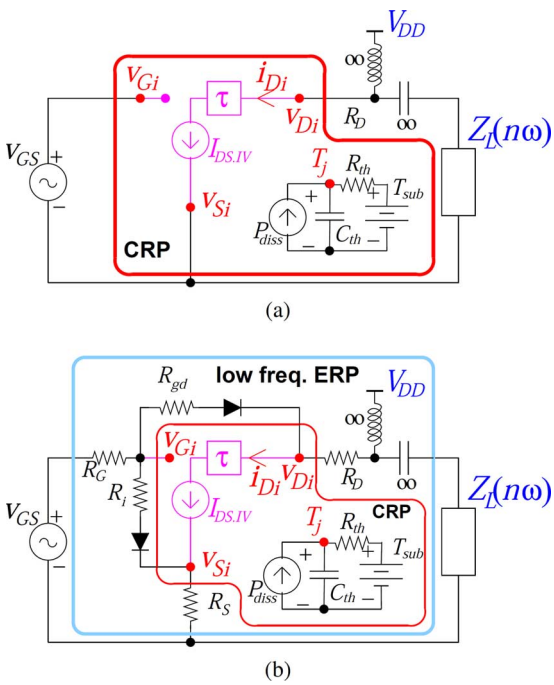

Fig. 12. Lossless harmonic terminations can be applied at: (a) the current reference plane (CRP) with no parasitics or at (b) the low-frequency ERPs (low-frequency ERP) using only resistive parasitics.

The results presented in Section IV-C focused on using active harmonic injection to synthesize the desired intrinsic mode of operation while improving the device efficiency. In such a case, to obtain the most optimal intrinsic mode of operation, the harmonic terminations were directly applied at the CRP of the intrinsic device, as shown in Fig. 12(a).

However, the designer is free to select any circuit for the mode mapping and thus can include the resistive parasitics of the device, as shown in Fig. 12(b). When passive harmonic loads are to be used, harmonic termination placed at the low-frequency ERP will provide a way to reduce the negative resistances in the source harmonic termination when doing the

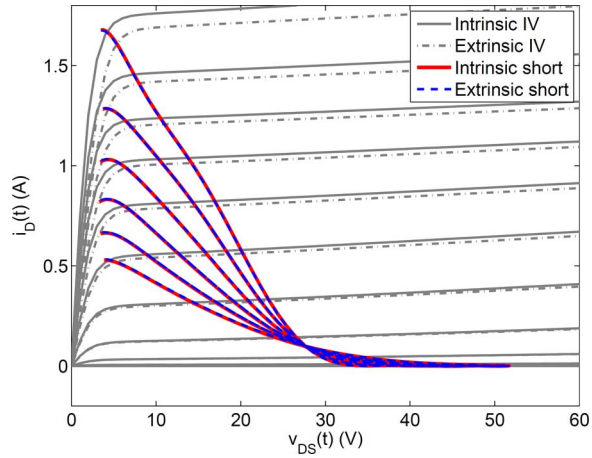

Fig. 13. Intrinsic load lines are compared for the two cases of shorted harmonics at intrinsic reference planes and ERPs.

mode projection at high frequencies. Indeed harmonic termination placed at the low-frequency ERP will permit the mode mapping to partially offset the series feedback introduced by the source resistance R_S.

To illustrate it, consider in simulation the case of a transistor operating in class B where the harmonic shorts are applied intrinsically (CRP) or extrinsically (low-frequency ERP). The extrinsic series resistances ($R_D = 0.69\ \Omega, R_S = 0.04\ \Omega$) were used in Fig. 12(b). The very small gate leakage current can be ignored. The fundamental RF gate drive and the device biasing were adjusted for the device to have approximately the same intrinsic mode of operation in both cases. Indeed, as shown in Fig. 13, due to the small parasitic resistances, the intrinsic load lines constructed with the extrinsic harmonic shorts closely overlap with those obtained with the intrinsic harmonic shorts even though the intrinsic harmonic voltages are not perfectly suppressed when using low-frequency extrinsic harmonic shorts.

The obtained intrinsic voltages v_{Di}, v_{Gi} and v_{Si} and current i_{Di} were then used in both cases by the nonlinear ETN to predict the extrinsic harmonic terminations (reflection coefficients) required at 2 GHz to maintain their respective intrinsic mode of operation. Note that the exact same Angelov ETN of Fig. 3 was used for both cases. The results are summarized in Table I. From this table, it is verified that harmonic load reflection coefficients of similar amplitudes slightly above one (negative resistance) are observed in both the intrinsic and extrinsic harmonic short cases. However, as expected, harmonic source reflection coefficients with substantially smaller amplitude are observed in the extrinsic harmonic short case compared to the intrinsic short case while still being larger than one.

E. Harmonic Reflection Coefficient Re-Normalization

As mentioned in the previous sections, the projected harmonic sources and loads are usually active even when using extrinsic harmonic terminations for the mode mapping. Three different re-normalization approaches for the harmonic reflection coefficients were investigated to implement the closest lossless harmonic terminations. First, the magnitude was reduced while the phase was kept the same as shown in (7). For the other two

TABLE I
SIMULATED SECOND AND THIRD HARMONIC REFLECTION COEFFICIENTS PROJECTED TO THE ERPS AT 2 GHZ BY THE EMBEDDING DEVICE MODEL FOR BOTH OF THE INTRINSIC AND EXTRINSIC HARMONIC SHORT CASES

No.	Source						Load			
	Intrinsic short			Extrinsic short			Intrinsic short		Extrinsic short	
	$V_g(V)$	$\Gamma_{S.2\omega}$	$\Gamma_{S.3\omega}$	$V_g(V)$	$\Gamma_{S.2\omega}$	$\Gamma_{S.3\omega}$	$\Gamma_{L.2\omega}$	$\Gamma_{L.3\omega}$	$\Gamma_{L.2\omega}$	$\Gamma_{L.3\omega}$
1	0.72	1.10∠-174°	1.04∠-169°	0.73	1.03∠-173°	1.03∠-169°	1.02∠-174°	0.89∠-173°	1.02∠-175°	1.17∠-179°
2	0.90	1.12∠-174°	1.09∠-169°	0.92	1.03∠-173°	1.03∠-169°	1.02∠-174°	1.01∠-170°	1.02∠-175°	1.01∠-172°
3	1.14	1.15∠-174°	1.18∠-169°	1.16	1.03∠-173°	1.03∠-169°	1.03∠-174°	1.02∠-170°	1.03∠-175°	1.02∠-172°
4	1.43	1.19∠-174°	1.26∠-169°	1.46	1.03∠-173°	1.03∠-169°	1.03∠-174°	1.02∠-170°	1.03∠-175°	1.02∠-172°
5	1.80	1.23∠-174°	1.27∠-169°	1.84	1.03∠-173°	1.03∠-169°	1.03∠-174°	1.02∠-170°	1.03∠-175°	1.02∠-172°
6	2.27	1.28∠-174°	1.17∠-169°	2.32	1.03∠-173°	1.03∠-169°	1.03∠-174°	1.02∠-170°	1.03∠-175°	1.02∠-172°

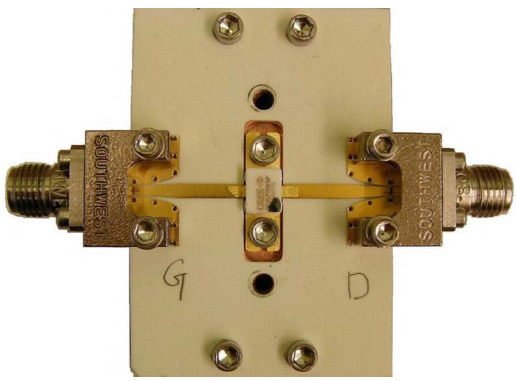

Fig. 14. Photograph of the test bed used for measuring the 15-W peak power GaN device (CGH27015F, CREE Inc.) [39]. A pressure bar (removed in the photograph) was used to electrically connect the device leads to the microstrip lines of the test-bed.

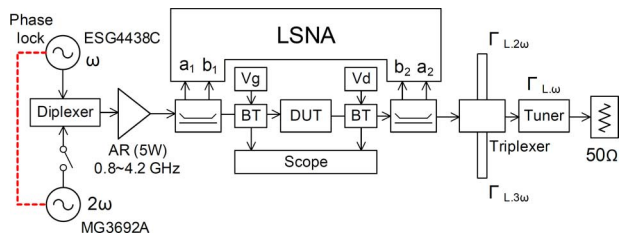

Fig. 15. Passive harmonic load–pull measurement setup with an LSNA was used for the linear load-modulation. It was combined with an ASP for the second harmonic injection at the input.

cases, the magnitude was reduced following either a constant reactance circle or a constant susceptance circle on the Smith chart, as expressed by (8) and (9), respectively. In these two cases, the phase of the reflection coefficients will vary,

$$\Gamma'_{L.\text{case1}}(n\omega) = \frac{\Gamma_L(n\omega)}{|\Gamma_L(n\omega)|} \tag{7}$$

$$\Gamma'_{L.\text{case2}}(n\omega) = \frac{jX_L(n\omega) - Z_0}{jX_L(n\omega) + Z_0} \tag{8}$$

$$\Gamma'_{L.\text{case3}}(n\omega) = \frac{Y_0 - jB_L(n\omega)}{Y_0 + jB_L(n\omega)}. \tag{9}$$

The three methodologies were found in practice to exhibit a similar performance in terms of PAE for the DUT considered. Experimental results will be presented in Section V.

V. MEASUREMENTS AND DISCUSSION

A. Measurement Setup

The 15-W peak power commercial GaN device (CGH27015F, CREE Inc.) shown in Fig. 14 in its test bed was used for both the (a) linear load-modulation class-B design with constant efficiency and (b) the second harmonic injection for PAE improvement. The packaged (440166) device provides 2-W average power with 28-V drain voltage. It provides 3.5-A saturated drain current. The device-under-test (DUT) was mounted on a copper heat sink, which sat on a thermal chuck with controlled temperature. All the measurements were performed at a chuck temperature of 25 ° C.

Fig. 15 shows the passive harmonic load–pull setup used with an LSNA (MT4463A) to verify the linear load modulation design. The harmonic injection measurements were conducted using the Agilent ESG4438C and Anritsu MG3692A signal sources combined with a diplexer. A triplexer (Maury Microwave, 9677G, 7 mm) working at 2 GHz was connected with two sliding shorts for the second and third harmonic loads and an automatic mechanical tuner for the fundamental load.

B. Experiment Conditions

The excitation powers and loads predicted by the embedding device model were applied to the DUT. Six fundamental loads and associated harmonic conditions for the linear load modulation operation were implemented using the passive tuners to be as close as possible to the ones predicted by the embedding device model given the loss in the test bed. This yielded the load terminations shown in Fig. 16, which were applied to the output of the DUT.

As mentioned in Section IV-B, the predicted harmonic sources and loads are usually active although some of them do fall inside the Smith chart, but close to the edge. Furthermore, in practical passive load–pull systems, the amplitude of the harmonic load reflections, which can be attained at the MRP, is limited to a maximum value $|\Gamma_{L.\text{tuner.max}}(n\omega)|$ by the loss in the various cables, 7-mm junctions, triplexer, and sliding short tuners. The re-normalization approach of (7) modified to

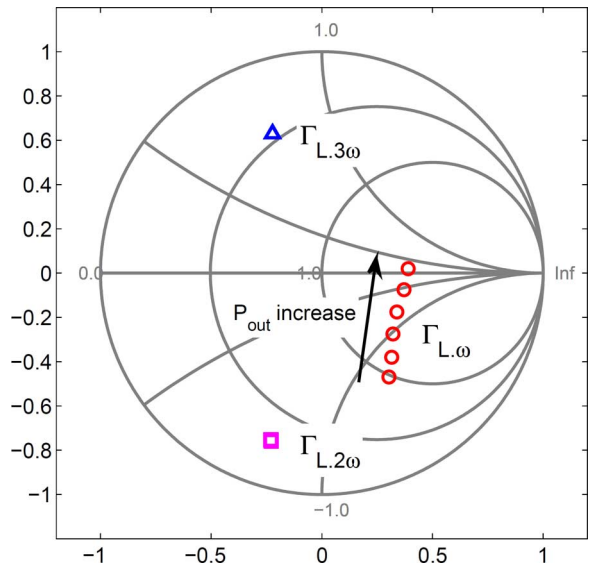

Fig. 16. Experimental harmonic loads provided by the passive tuners at the MRP and applied to the DUT. $\Gamma_L(2\omega) = 0.78\angle -108°$, $\Gamma_L(3\omega) = 0.69\angle 109°$. The fundamental loads provided from low to high power were $48.7 - j66.5$, $61.7 - j62.0$, $76.6 - j51.3$, $91.3 - j37.5$, $106.7 - j18.8$, and $113.8 + j5.3$ at 2 GHz.

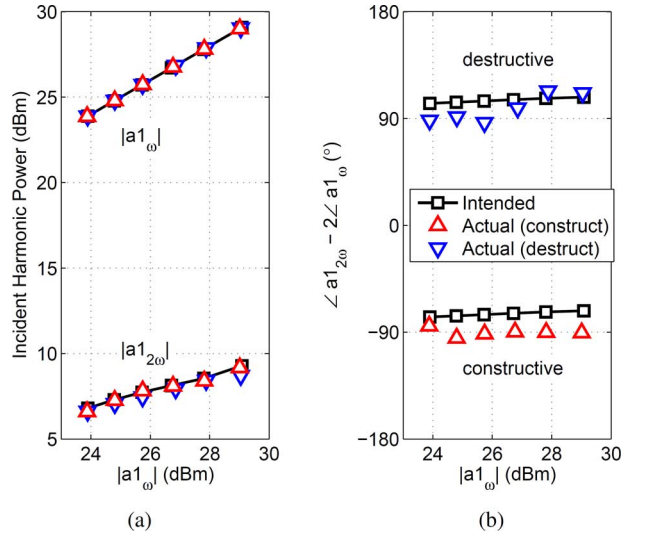

Fig. 17. Fundamental and second: (a) harmonic amplitude and (b) phase at 2 GHz versus the fundamental incident power as predicted by the class-B projection with the embedding device model and actual values used in the measurement. The predicted phase (△) are labeled as "constructive" and the opposite phase (▽) as "destructive." The amplitude of the fundamental is also shown for reference.

account for the maximum magnitude reflection available from the test bed was used:

$$\Gamma'_{L.\mathrm{case1}}(n\omega) = \frac{\Gamma_L(n\omega)}{|\Gamma_L(n\omega)|}|\Gamma_{L.\mathrm{tuner.\,max}}(n\omega)|. \tag{10}$$

Using the sliding shorts, the phases $\angle\Gamma_L(n\omega)$ of the second and third harmonic load reflection coefficients were set to the values predicted by the ETN while letting the amplitudes $|\Gamma_L(n\omega)|$ be the maximum attainable value at the MRP given the loss in the test bed. The resulting actual loads used are shown in Fig. 16. It should be noted that the same reduced amplitude for the harmonic passive harmonic loads have been applied as well to the simulations for a more meaningful comparison with measurements.

For the second harmonic injection, the synthesized input fundamental and second harmonic excitations obtained from the embedding device model are shown in Fig. 17 using □ symbols. Fig. 17(a) gives the intended values for the load modulation amplitude of the fundamental and second harmonic injected versus incident fundamental power, and Fig. 17(b) gives the predicted second harmonic phases versus incident fundamental power for a second harmonic injection yielding an improved PAE (bottom "constructive") and for a second harmonic injection with the opposite phase (top □,"destructive") yielding a degraded PAE.

For the second harmonic input injection experiment, an active source–pull (ASP) was used for the source side. As shown in Fig. 15, the second harmonic RF source was integrated with the fundamental input source using a diplexer. The two RF sources shared a 10-MHz reference signal for phase locking. The targeted phase differences, $\angle a_1(2\omega) - 2\angle a_1(\omega)$, at the MRP were obtained by tuning the phase of the second source. This phase tuning combined with amplitude tuning enable to implement for each fundamental incident power levels, the required amplitudes, and phases of the second harmonic synthesized by the embedding device model when targeting an intrinsic class-B operation. The actual amplitude and constructive phase used in the experiment for the expected PAE enhancement are shown using triangles (red in online version) in Fig. 17. Also shown for comparison are the amplitude and phase of the second harmonic (nabla symbols, blue in online version) versus incident power used in the experiment for the expected PAE degradation.

C. Measured Results and Discussion

The measured PAE results are plotted for comparison on top of the simulated results in Fig. 10. The incident power ($|a_1(\omega)|^2$) was varied with the load as intended in the internal design. The measured PAE clearly exhibits the targeted quasi-constant efficiency from 26- to 29-dBm incident power and gradually degraded below 26 dBm, as in the original simulations. As previously mentioned, the same actual load/source terminations were used in simulation as in the experiment. As in the simulation, the effect of the second harmonic injection on the PAE is evident for the three cases. When the injected second harmonic is canceling the nonlinear parasitic network phase shift, a PAE improvement varying from 2% at high power to 5% at low power is observed. On the other hand, when the injected phase adds to the nonlinear parasitic network phase shift, a PAE degradation is observed, which varies from 4% at high power to 6% at low power. Thus, Fig. 10 indicates that up to 12% in efficiency loss is possible relative to the maximum efficiency case if a destructive second harmonic is accidentally injected by the PA driver.

Among the three injection cases, the PAE reduction from high to low power is the smallest when the second harmonic is injected with a "constructive" phase; yielding less than 4% efficiency variation with incident power. On the contrary, the PA

features as much as 9% PAE variation with incident power when the second harmonic is injected with a destructive phase. Therefore, the measured and simulated results show that the intrinsic constant efficiency design can be better realized by applying the external loads and excitation conditions predicted by the proposed intrinsic to extrinsic mode projection method (nonlinear embedding PA design) using the embedding device model. Furthermore, the harmonic cancellation at the input not only improves the efficiency, but also is effective for maintaining a constant efficiency over a wider range on incident power.

In Section IV-C, it was verified in Fig. 11 using simulation, that the optimal phase and its opposite phase (180° shift) predicted by the embedding device model, did indeed correspond to the maximum and minimum PAE observed, respectively, when performing a continuous second harmonic phase sweep. In order to verify that these simulation results also hold experimentally, the fundamental amplitude was selected to be one (the fourth one) of the six load-modulation power levels studied. Thus, the fundamental amplitude with $|a_1(\omega)| = 26.7$ dBm was used together with the second harmonic amplitude set to $|a_1(2\omega)|/|a_1(\omega)| = -18.6$ dBc as predicted by the embedding device model. An automatic phase sweeping measurement using a frequency offset for the second harmonic [38], [39], also known as real-time active source–pull (RTASP), was used for this independent measurement. Fig. 11 compares the measured PAE (circles, red in online version) versus the relative swept second harmonic phases $\angle a_1(2\omega) - 2\angle a_1(\omega)$ to the simulated ones using the Angelov (solid line, blue in online version) and CREE (dashed line, magenta in online version) models. As can be seen, this RTASP experiment reports a maximum PAE at around a $-70°$ range and a minimum PA at around 100°. These RTASP results approximately agree with the experimental and simulation results in Fig. 11 obtained, respectively, using: 1) continuous wave (CW) active load–pull measurements or 2) simulation predictions using the embedding device model. For comparison, the CW ASP results of Fig. 10 are also shown using a square (red in online version) in Fig. 11, which gives a closer agreement to the simulation. The discrepancy between the CW ASP measurements and the modulated RTASP measurements is mostly due to errors in power calibration and time synchronization between the RF and baseband signals in RTASP.

The measured output power in Fig. 10 (bottom line) also agrees very well with the simulated results of the CREE model for all three cases. Only the fundamental (□) and constructive(+) cases are shown. The extracted model (dashed lines) predicted a slightly lower output power than the CREE model and the measured data. The accuracy of the prediction of the harmonic loads and second harmonic injection could be improved by using a better extraction for the Angelov model. It is to be noted that the Angelov model plays a key role in this work since the required load harmonic termination and second harmonic injection at the input were synthesized using the Angelov embedding device model reported in this paper.

Note that the small decrease, about 3% of the maximum measured efficiency in Fig. 10 relative to the maximum simulated efficiency achievable shown in Fig. 7, is due to the use of lossy harmonic terminations on the drain side (output) in the measurement whereas the exact harmonic terminations predicted by the embedding device model were applied in simulation at both the source (input) and drain (output) sides.

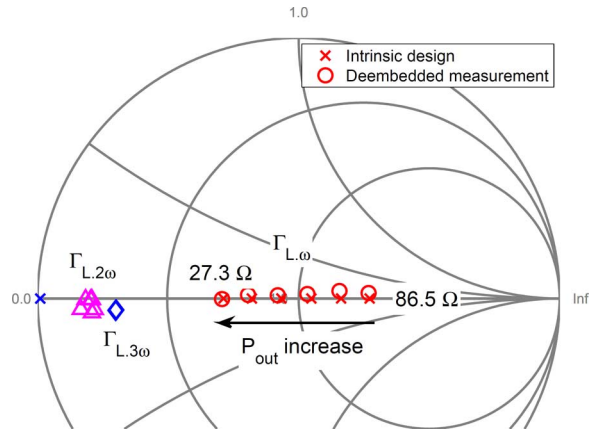

Fig. 18. Loads were deembedded from the measured data. The fundamental loads (◯) are compared to the intrinsic designed loads (×) selected for load modulation at 2 GHz.

The measured loads were de-embedded using the extracted Angelov model parameters in Fig. 18. The fundamental loads agree well with the intended intrinsic loads for the load modulation design. The second and third harmonic loads are all located in proximity to the short position given the limited magnitude achievable by the passive load–pull test bed used.

The Angelov embedding device model synthesizes the exact loads required for defining the desired intrinsic mode of operation of the Angelov device model. However, since the Angelov model does not perfectly represent the device, the desired intrinsic load lines targeted might not be well realized within the measured device. Furthermore, the external sources and terminations, which are required to drive the device, are not also perfectly implemented either. To evaluate the accuracy of the nonlinear embedding PA design methodology, a figure-of-merit is needed and is implemented as described in Section V-D.

D. Figure-of-Merit for Nonlinear Embedding PA Design

To develop a figure-of-merit at the intrinsic load line level, it is first necessary to deembed the measured data [10]–[12]. To perform the required nonlinear deembedding of the measured data, the DTN shown in Fig. 1(c) will be used. This DTN performs the reverse operation of the ETN to calculate the current voltages and currents at the CRPs given the voltages and currents measured at the MRPs. Note that the device temperature is also calculated by the DTN as it is used by the charges in the nonlinear parasitic networks. The ETN must then make use of the device thermal network model to calculate the device temperature from the power dissipated by the device.

The de-embedded intrinsic gate current i_{Gi} should be *zero* after de-embedding, considering the infinite input impedance of the intrinsic current source at the gate terminal. Therefore, the residual intrinsic gate currents (Δi_{Gi}) after de-embedding can be used as an indicator of the modeling and deembedding accuracy.

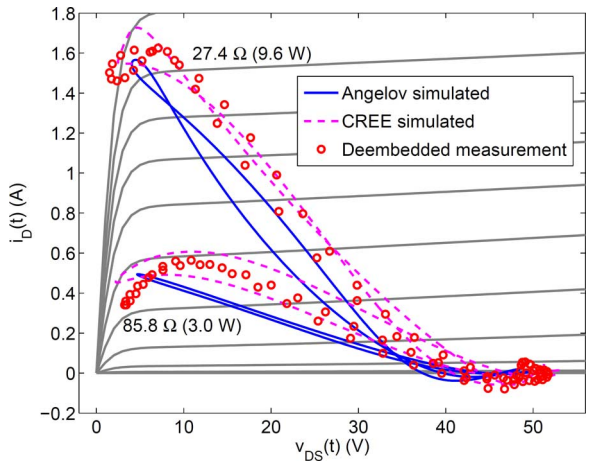

Fig. 19. Intrinsic load lines deembedded from the measured output voltages and currents at 2 GHz are compared to the simulated intrinsic load lines using the extracted Angelov (blue line in online version) and CREE (magenta line in online version) models.

Once the nonlinear DTN is available, it can be used to estimate the actual intrinsic load lines implemented for the load modulation operation by the nonlinear embedding PA design technique. Fig. 19 compares the intrinsic load lines de-embedded ($\circ$, red in online version) from the measured voltages and currents to the ones obtained using circuit simulations with the Angelov (solid line, blue in online version) and CREE (dashed line, magenta in online version) models. Two intrinsic load lines among the previous six loads considered are singled out: one for the highest power (*top*) and the other one for the lowest power (*bottom*).

The intrinsic load lines are directly accessible in the extracted Angelov model implemented in the circuit simulator. For the CREE model, the device manufacturer (CREE Inc.) provided a new six-port model with ports giving access to the internal voltages and currents at the current source planes [40]. In the harmonic-balance simulations, the Angelov and CREE models were both terminated at the output by the practical measured loads $\Gamma_L(n\omega)$ shown in Fig. 16. The measured fundamental excitation $a_1(\omega)$ was applied at the input while the higher input harmonics were terminated by the test-bed reflection coefficients $\Gamma_S(n\omega)$ as in the no-harmonic injection case in Fig. 10. The simulations and the de-embedding of the measured data were performed using four harmonics to match the number of harmonics measured.

The intrinsic de-embedded load lines from the measured data reveal that the intended load modulation for the various input excitation power levels are indeed achieved and agree reasonably well with the simulated load lines (Angelov and CREE) within the modeling accuracy range. The difference between the Angelov (solid line, blue in online version) and CREE (dashed line, magenta in online version) models is a direct measure of the Angelov model extraction accuracy since that model was extracted from the CREE model. The measured voltages and currents that were de-embedded using the Angelov based DTN are also affected by the Angelov model extraction accuracy.

TABLE II
RMS VALUES FOR THE CURRENT, VOLTAGE, AND GEOMETRICAL DEVIATIONS OF THE SIMULATED INTRINSIC LOAD LINES FROM THE MEASURED AND DEEMBEDDED INTRINSIC LOAD LINES

P_{inc}	CREE RMS_X (%)			Angelov RMS_X (%)		
(dBm)	I	V	G	I	V	G
23.9	13.44	1.58	4.62	18.24	3.83	8.36
24.8	10.41	1.29	3.66	16.98	3.92	8.15
25.7	7.98	1.17	3.06	15.71	4.09	8.02
26.7	6.29	1.19	2.74	14.42	4.40	7.97
27.8	5.06	1.33	2.60	13.82	5.02	8.33
29.1	4.35	1.67	2.69	13.98	5.31	8.62

In order to quantify the intrinsic load line deviations between the various techniques, a normalized root mean square (rms) will be used as a figure-of-merit for each incident power level,

$$\mathrm{RMS}_X(\%) = \sqrt{\frac{1}{K}\sum_k (x_{m.k} - x_{s.k})^2} \times 100 \tag{11}$$

where X can either be the drain current or drain voltage, m and s represent the measured and simulated data, respectively, and K is the number of samples per one cycle. The time-domain voltage and current waveforms X were normalized in magnitude by their time-domain peak values $X_{m,\mathrm{pk}}$. The various measurements were also synchronized using time alignment such that the phase of the fundamental voltage excitation at port 1 be set to zero in all techniques

$$x_m(t) = \mathcal{R}e\left[\sum_{n=0}^{\mathrm{NH}} \frac{X_m(n\omega)e^{jn\omega t}}{X_{m.\mathrm{pk}}e^{jn\vartheta_{v.1}}}\right] \tag{12}$$

where $X_{m.\mathrm{pk}}$ is the time-domain peak value, $\vartheta_{v.1}$ is the phase of the fundamental voltage, and NH is the number of harmonics used. The geometric mean (G) of the voltage and current rms values was also calculated to provide a single comprehensive figure-of-merit for the deviation between the measured and simulated load lines

$$\mathrm{RMS}_G(\%) = \sqrt{\mathrm{RMS}_I \times \mathrm{RMS}_V} \times 100. \tag{13}$$

The calculated results are summarized in Table II. The smaller numbers obtained for the geometric mean of the CREE model compared to that of the extracted Angelov model are indicative of the better fit provided by this model in agreement with Fig. 19. Further improvement in modeling accuracy will help reduce these rms errors. Parts of the limitation of the present model is that the Angelov model used in this paper does not account for the nonlinear influence of the trapping effects [41]. In [7], this was fully addressed for the case where the memory effects are located in the intrinsic FET by using the measured low-frequency RF load line. Alternately the effective intrinsic IV characteristics including memory effects used by the device can be extracted from nonlinear RF measurements [9]–[14], [42].

VI. Conclusion

In this paper, the nonlinear embedding PA design technique in [7], which starts from the intrinsic reference plane, was applied to the non-quasi-static Angelov model. A nonlinear ETN was developed for the Angelov model for this purpose. Using this ETN, an embedding device model was realized, which permits to project the desired load lines at the CRP to the ERPs (ERP, PRP, MRP). This projection synthesizes the external terminations, which exactly maintain the desired intrinsic PA mode of operation. However, it was found that the active injection of harmonics is usually required to offset the harmonic power losses due to the nonlinear parasitics. Various impedance termination re-normalization techniques were then tested and demonstrated in simulations and measurements to yield acceptable results. Alternatively, the embedding device model provides the designer with the precise higher harmonic (amplitude and phase) required to be injected at the input and output to achieve perfect intrinsic PA operation. This technique was verified experimentally with the injection of a second harmonic at the input for a class-B PA relying on load modulation.

The measured load modulation characteristics and harmonic input injection results validate the use of the proposed nonlinear embedding process for the Angelov model including harmonics. The harmonic cancellation at the input not only improves the efficiency, but also is effective for maintaining a more constant efficiency. The constructive phase also exhibited a 5% smaller efficiency variation upon the incident power compared to the destructive case. The analysis shows also that the inadvertent injection of a destructive second harmonic from the PA driver can even lead to a 10% lower efficiency relatively to the optimal case.

Unlike load–pull at the external reference planes, which is a mode-blind optimization, the large-signal model-based harmonic source or load synthesis with the proposed embedding device model and associated ETN, provides the PA designers with full control as to the operation of the device at the intrinsic reference plane. The resulting increased controls and insights into the PA operation should provide for faster design and wider design choices leading to a more efficient and robust design. Indeed the benefit of starting with a harmonic load–pull simulation at the intrinsic reference plane is to directly select the *desired* internal mode of operation of the transistor for the external application at hand.

The nonlinear embedding PA design technique also has the potential to greatly simplify and accelerate the design process for multi-harmonic PA design. Indeed for the design of a PA for a given power excitation with a specific class of operation (e.g., class F or class J) at the internal CRP with N harmonic impedances specified, the nonlinear embedding PA design technique replaces the N source–pulls and $N+1$ load–pulls ($4N+2$ dimension parameter sweep) performed at the external reference planes by a single simulation with no parameter sweep. The efficacy of the nonlinear embedding PA design technique is thus clearly evident. This efficient design process is particularly useful for the design of Doherty PAs where the mode projection is performed versus the input power level over the entire power backoff range [43].

However, to be successful with real devices, the nonlinear embedding PA design methodology requires that a sufficiently accurate device model be available. Since no nonlinear device model can be expected to perfectly represent a real device, given both the process fluctuations and the model's limitation, a figure-of-merit was introduced for quantifying the efficacy of the nonlinear embedding PA design methodology. This figure-of-merit relies on the nonlinear RF measurements for estimating the impact of the model accuracy on the intrinsic load lines actually synthesized. In this work, an accuracy figure-of-merit, varying from 4.6% to 2.7% from low to high incident powers, was obtained for the intrinsic loadlines despite using an embedding device model based on the rather coarse Angelov model extraction. This indicates that a high-fidelity model is not critically required to obtain useful results with the embedding nonlinear PA design technique. Provided the required confidence level is attained, waveform and load-line engineering at the intrinsic level using the nonlinear embedding PA design approach then becomes more readily achievable when using an nonlinear embedding device model implemented in a circuit simulator. As an example, the embedding device model reported in this paper was applied to the design of a Doherty PA for the synthesis of the multi-harmonic terminations for the auxiliary and main amplifiers [43].

It should be noted that, once developed, the internal working and circuit parameters of the embedding device model do not need to be disclosed and the intellectual property associated with the device technology can thus remain protected. In view of the significant timesaving advantages of the nonlinear embedding PA design technique, it is suggested that it would be a great benefit to the PA designer community if device manufacturers were to make embedding device model available.

Acknowledgment

The authors would like to thank CREE Inc., Durham, NC, USA, for providing the GaN HEMT transistors and the six-port model used in this study, and E. Schmidt, Agilent Technologies, Santa Clara, CA, USA, for support provided for ICCAP. Thanks also go to Y. Ko, The Ohio State University, Columbus, OH, USA, and A. Zárate-de Landa, CICESE, Ensenada Baja California, México, for supporting measurements and thru-reflect line (TRL) calibration kits. The authors are also grateful to the anonymous reviewers for in depth feedback and invaluable suggestions for improving this paper's manuscript.

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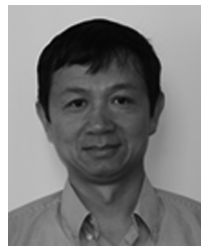

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