Analytical Extraction of a Schottky Diode Model From Broadband S-Parameters

Aik Yean Tang, *Student Member, IEEE*, Vladimir Drakinskiy, Klas Yhland, *Member, IEEE*, Jörgen Stenarson, *Member, IEEE*, Tomas Bryllert, and Jan Stake, *Senior Member, IEEE*

***Abstract*—We present an analytic method to extract Schottky diode parasitic model parameters. All the ten unknown model parameters are extracted via a straightforward step-by-step procedure. The challenges for a proper finger inductance and series resistance extraction are discussed and solutions are recommended. The proposed method is evaluated using three sets of S-parameter data for GaAs-based planar Schottky diodes, i.e., data from measurement up to 110 GHz and 3-D electromagnetic full-wave simulations up to 600 GHz. The extracted models agree well with the measured and simulated data.**

***Index Terms*—Analytical model, equivalent circuits, millimeter-wave devices, modeling, multibias, parameter extraction, scattering parameters, Schottky diodes, terahertz.**

I. Introduction

TODAY, GaAs-based planar Schottky diodes [1] are used in terahertz heterodyne receivers [2]–[4] for terahertz imaging and sensing application. However, the diode experimental performance is still far below expectations due to the lack of accurate high-frequency models.

In circuit design, empirical equivalent-circuit models [5]–[12] are usually favored in comparison to physical models solving basic transport equations [13]–[16]. This is due to their computational efficiency and the physical device parameters not being needed. In order to extract the equivalent-circuit model, a systematic and straightforward extraction method is needed. The availability of such a method is also important for automated parameter extraction in wafer mapping and fabrication process tracking.

The nonlinear parameters in the equivalent circuit are extracted from dc current–voltage (*I–V*) and low-frequency capacitance–voltage (*C–V*) data, whereas the linear parasitic model parameters are extracted from two-port S-parameter data. While the extraction of the parasitic capacitances is accurate, the extraction of inductances and resistances is challenging. Today, these elements are mostly estimated by fitting the model parameters to the S-parameter data [5]–[11]. In comparison to parameter-extraction methods for transistor models [17]–[21], a systematic and robust parameter extraction method for high-frequency diodes is still lacking.

In this study, we present a systematic and straightforward analytical method to extract the high-frequency diode model parameters. A new algorithm for the extraction of diode inductances is proposed. Compared to [5]–[11], the proposed algorithm provides a more consistent outcome, without influence of the definition of global error function, the starting parameter values, and the allowable parameter range [22]. Three sets of S-parameters are used to evaluate the method, i.e., measurement up to 110 GHz for diode in a coplanar waveguide (CPW) configuration, and 3-D electromagnetic (EM) full-wave simulation up to 110 GHz for a diode in a CPW configuration and up to 600 GHz for a diode in a suspended stripline configuration.

II. Schottky Diode Equivalent-Circuit Model

Fig. 1 illustrates a cross-sectional view of a high-frequency planar Schottky diode and its equivalent-circuit model. The Schottky junction, depicted as a diode symbol in Fig. 1(a), is modeled as voltage-dependent junction capacitance (C_j) and resistance (R_j) [23]. The diode parasitic resistance due to the un-depleted active junction epi-layer is a voltage-dependent epi-resistance. However, in combination with other extrinsic parasitic resistances [see Fig. 1(a)], the bias dependency of a total of the epi- and extrinsic parasitic resistances is weak. For simplicity, these resistances are modeled as one series resistance (R_s), as shown in Fig. 1(b).

The fringing field between both pads is modeled as a pad-to-pad capacitance $(C_{\rm pp})$, which is comprised of $C_{\rm pp}^{\rm air}$ and $C_{\rm pp}^{\rm subs}$. The finger-to-pad coupling is modeled as $C_{\rm fp}$ and the self-inductance of the air-bridge finger is modeled as L_f [1]. Each connecting pad is approximated as a π-network [17], comprising pad capacitance $(C_{\rm pad})$ and pad inductance $(L_{\rm pad})$. The π-network representation for the pad is sufficient and accurate when the pad length is less than 10% of the effective wavelength $(\lambda_{\rm eff})$ at the highest frequency and its characteristic impedance is free from dispersion.

With this, ten unknown parameters are sufficient for effective extraction and accurate modeling over a wide frequency range.

Manuscript received November 29, 2012; revised February 20, 2013; accepted February 22, 2013. Date of publication March 22, 2013; date of current version May 02, 2013. This work was supported in part by the European Community's Seventh Framework Program (FP7/2007-2013) under Grant 242424. This work was carried out at the GigaHertz Centre, Chalmers University of Technology, under a joint research project supported by the Swedish Governmental Agency of Innovation Systems (VINNOVA), the Chalmers University of Technology, Omnisys Instruments AB, Wasa Millimeter Wave AB, the Low Noise Factory, and the SP Technical Research Institute of Sweden.

A. Y. Tang, V. Drakinskiy, T. Bryllert, and J. Stake are with the GigaHertz Centre, Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, SE-41296 Göteborg, Sweden (e-mail: aik-yean.tang@chalmers.se).

K. Yhland and J. Stenarson are with the GigaHertz Centre, Chalmers University of Technology, SE-41296 Göteborg, Sweden, and also the SP Technical Research Institute of Sweden, 501 15 Borås, Sweden.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2013.2251655

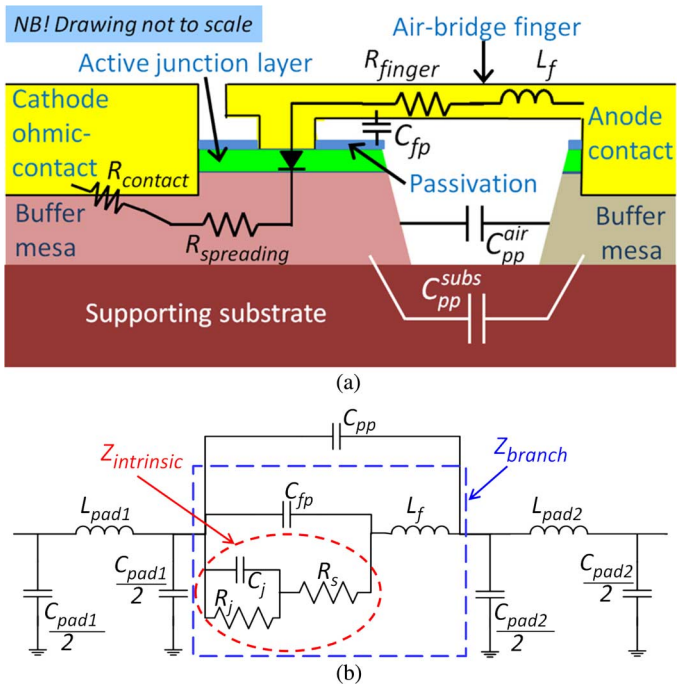


Fig. 1. Planar Schottky diode structure. (a) Cross-sectional view. (b) Small-signal equivalent-circuit model.

For frequencies where the diode geometry is in the order of 1/10 or larger of the effective wavelength, the models of air-bridge finger and connecting pads have to be extended, e.g., as distributed components.

III. Parameter-Extraction Method

The extraction method is based on an analytical calculation of the model parameters. A set of multi-bias broadband S-parameters is used to calculate all the model parameters. For the capacitance extraction, at least three reverse bias points are required, whereas for the series resistance and inductance extraction, at least one forward bias point beyond flat band is required. Moreover, S-parameters from one additional de-embedding structure are used to estimate the pad-to-pad capacitance $(C_{\rm pp}^{\rm de\text{-}embed})$. This de-embedding structure is identical to the diode structure, but with the absence of the air-bridge finger and Schottky anode contact.

A. Step 1—Capacitance Extraction

For a high-frequency planar diode, the capacitances are in the range of a tenth to tens of a femtofarad, whereas inductances are in the range of several to tens of pico-Henrys. Thus, at a relatively low frequency range, e.g., the lower gigahertz frequency range, the diode capacitances are dominant compared to the inductances. With this, the inductances in the equivalent circuit in Fig. 1(b) can be neglected, resulting in a π-network topology (see Fig. 2).

With this, the diode capacitances are extracted at a low-frequency reverse-biased case, i.e., $V \ll \psi_{\rm bi}$, where $\psi_{\rm bi}$ is the built-in potential. In comparison to the reverse-biased junction resistance, the series resistance is negligible small and the

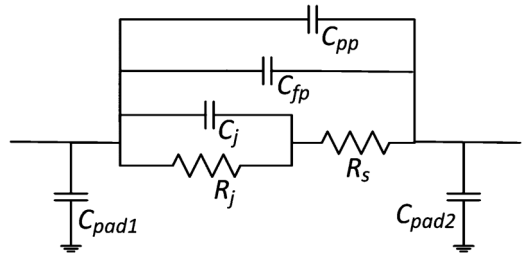


Fig. 2. Low-frequency diode equivalent circuit.

equivalent Y-parameters are written as

$$Y = \frac{1}{R_j(V)}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} + j\omega \begin{bmatrix} C_{\rm pad1}+C_j(V)+C_{\rm par} & -(C_j(V)+C_{\rm par}) \\ -(C_j(V)+C_{\rm par}) & C_{\rm pad2}+C_j(V)+C_{\rm par} \end{bmatrix} \tag{1}$$

$$C_{\rm par} = C_{\rm pp} + C_{\rm fp} \tag{2}$$

where ω is the angular frequency.

With this, the pad capacitances are extracted using

$$C_{{\rm pad}i} = \frac{{\rm Im}(Y_{ii}+Y_{ij})}{\omega} \tag{3}$$

where i and j denote pad 1 or 2 $(i \neq j)$.

Since the equivalent circuit is reciprocal, it is sufficient to use only the Y_{12}-parameter to calculate the total capacitance, as in (4). By using a set of multi-bias Y-parameters, the junction capacitance (C_j) [23] and the parasitic capacitance $(C_{\rm par})$ is extracted by fitting (4) to (5),

$$C_{\rm tot\_12}(V) = \frac{{\rm Im}\left(-Y_{12}(V)\right)}{\omega} \tag{4}$$

$$C_{\rm tot\_12}(V) = C_{j0}\left(1-\frac{V}{\psi_{\rm bi}}\right)^{-M} + C_{\rm par} \tag{5}$$

where C_{j0} is a zero-biased junction capacitance, and M is a parameter representing the doping profile of the active junction layer ($M = 0.5$ for a uniformly doped junction layer).

The diode $C_{\rm pp}$ is estimated from the de-embedding structure, using (4), i.e., $C_{\rm tot_{12}}^{\rm de\text{-}embed} = C_{\rm pp}^{\rm de\text{-}embed}$. The diode finger-to-pad capacitance is then deduced by

$$C_{\rm fp} = C_{\rm par} - C_{\rm pp}^{\rm de\text{-}embed}. \tag{6}$$

B. Step 2—Total Resistance Extraction

Similar to the capacitance extraction, the diode resistance is calculated at a low-frequency range. Referring to Fig. 2, the total resistance $(R_{\rm tot})$ is calculated using (7), with the following assumptions.

- R_j is dominating R_s at the reverse-biased case.
- C_j is negligible at the forward-biased case

$$R_{\rm tot}(V) \approx \frac{1}{Re\left(-Y_{12}(V)\right)} = R_s + R_j(V). \tag{7}$$

The series resistance is estimated when the diode is forward biased, where the junction resistance is assumed to be zero.

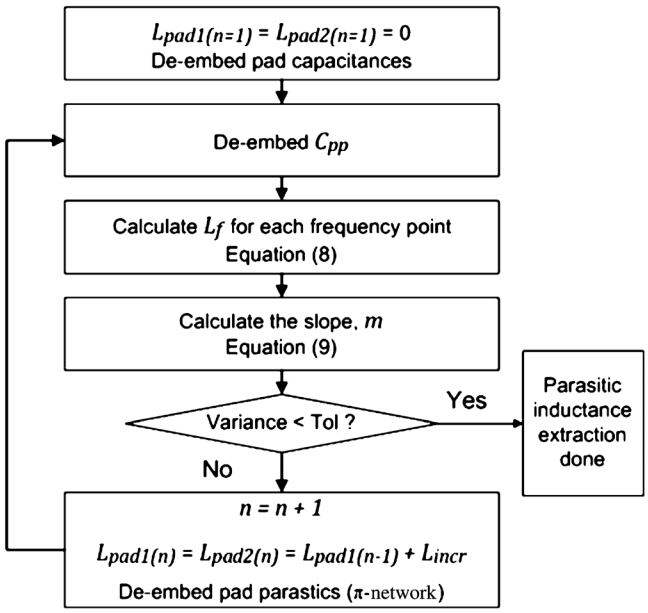


Fig. 3. Parasitic inductance extraction algorithm (*note:* n is the iteration number).

C. Step 3—Inductance Extraction

The parasitic inductances are extracted at high frequencies, e.g., hundreds of gigahertz range. For a diode in the forward-biased condition, the junction capacitance can be neglected. With this, a direct calculation of the finger inductance is possible upon a proper de-embedding of the pad parasitics and $C_{\rm pp}$ using

$$L_f = \frac{\mathrm{Im}\left(Z_{\rm branch}(\omega)\right)}{\omega} + \frac{C_{\rm fp}R_{\rm tot}^2}{1+(\omega R_{\rm tot}C_{\rm fp})^2} \tag{8}$$

where $Z_{\rm branch}$ is the equivalent impedance for the air-bridge finger branch [see Fig. 1(b)].

To de-embed the pad parasitics (π-networks), a similar method as in [18], via a sequence of Y–Z–Y matrix conversion, is used. Due to the lack of prior knowledge of $L_{\rm pad1}$ and $L_{\rm pad2}$, L_f is calculated through an iterative procedure, as shown in Fig. 3.

In this procedure, the pad inductances are assumed to be the same because of the relatively similar pad structures. Moreover, it is also known that a correct parasitic inductance value is constant across frequency range [19], [20], i.e., zero slope for a inductance versus frequency plot. However, there are statistical and modeling errors in the result. Thus, the procedure is iterated until a pre-set slope value, i.e., the convergence criterion, is met. The slope, m, can be calculated with a linear regression method [19]

$$m = \frac{N\sum_{k=1}^{N}\left(\omega_k L_f(\omega_k)\right) - \left(\sum_{k=1}^{N}\omega_k\right)\left(\sum_{k=1}^{N}L_f(\omega_k)\right)}{N\sum_{k=1}^{N}\omega_k^2 - \left(\sum_{k=1}^{N}\omega_k\right)^2} \tag{9}$$

where N is the number of frequency points.

At the beginning of this procedure, it is assumed that the pad inductances are zero. Prior to reaching the zero or pre-set slope value, the calculated slope is interpreted as a result of underestimated pad inductances. Thus, in each iteration loop, the pad inductances are increased, as in

$$L_{\rm incr} = 0.01 \times \frac{1}{N}\sum_{k=1}^{N} L_f(\omega_k). \tag{10}$$

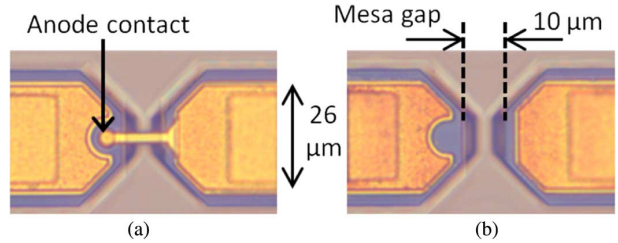


Fig. 4. Device geometry for measurement and simulation. (a) Planar Schottky diode. (b) Additional de-embedding structure.

D. Model Error Analysis

The accuracy of this method is evaluated by computing the errors between the S-parameters for the device-under-test (DUT) and the extracted model. The frequency and voltage dependent error function is written as

$$e(V,\omega_k) = \frac{1}{4}\sum_{j=1}^{2}\sum_{i=1}^{2}\left|S_{ij}^{\rm DUT}(V,\omega_k) - S_{ij}^{\rm mod}(V,\omega_k)\right|^2 \tag{11}$$

where $S_{ij}^{\rm DUT}(V,\omega_k)$ and $S_{ij}^{\rm mod}(V,\omega_k)$ are the DUT and model S-parameters at a kth frequency point for a voltage point, respectively.

The average error, $\overline{e(V)}$, is defined as

$$\overline{e(V)} = \frac{1}{N}\sum_{k=1}^{N} e(V,\omega_k). \tag{12}$$

IV. DUT S-Parameters

A. DUT Structure

The DUT structure is identical to a Schottky varactor diode operating in the 200-GHz range [see Fig. 4(a)]. The diode is fabricated on a 270-nm-thick active junction layer with n-type dopant (2×10^{17} cm^{-3}). The Schottky anode contact is 10 μm^2. For a measurement up to 110 GHz, the supporting substrate of the diode sample is 150 μm [24]. Fig. 4(b) shows the additional de-embedding structure, i.e., a diode structure without the air-bridge finger.

Similar diode structures are constructed for the 3-D EM full-wave simulation up to 110 GHz in a CPW configuration and up to 600 GHz in a suspended stripline configuration. For simulation in a suspended stripline configuration, the supporting substrate is 3-μm thick.

B. On-Wafer Measurements (5–110 GHz)

For on-wafer measurements, a CPW configuration without backside metallization is used (see Fig. 5). The conductor metallization thickness is 0.7 μm. The diode structure is probed with a pair of Cascade infinity ground–signal–ground (GSG) probes.

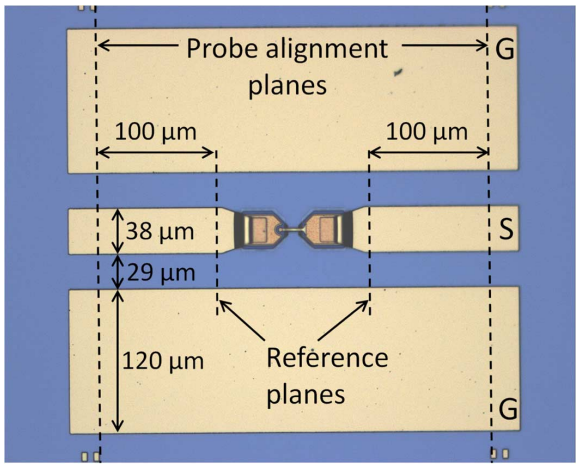


Fig. 5. Microscope image of a diode in the CPW configuration for the on-wafer S-parameter measurements.

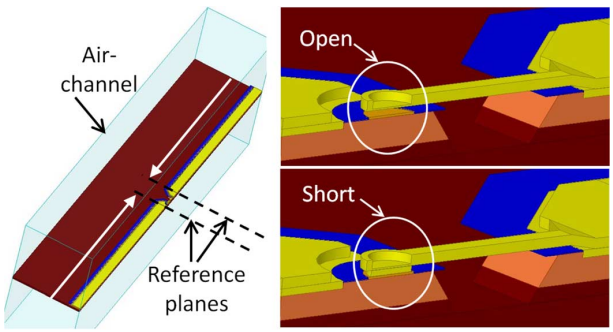


Fig. 6. (a) 3-D EM full-wave simulation setup. (b) Open- and short-circuited diode structures.

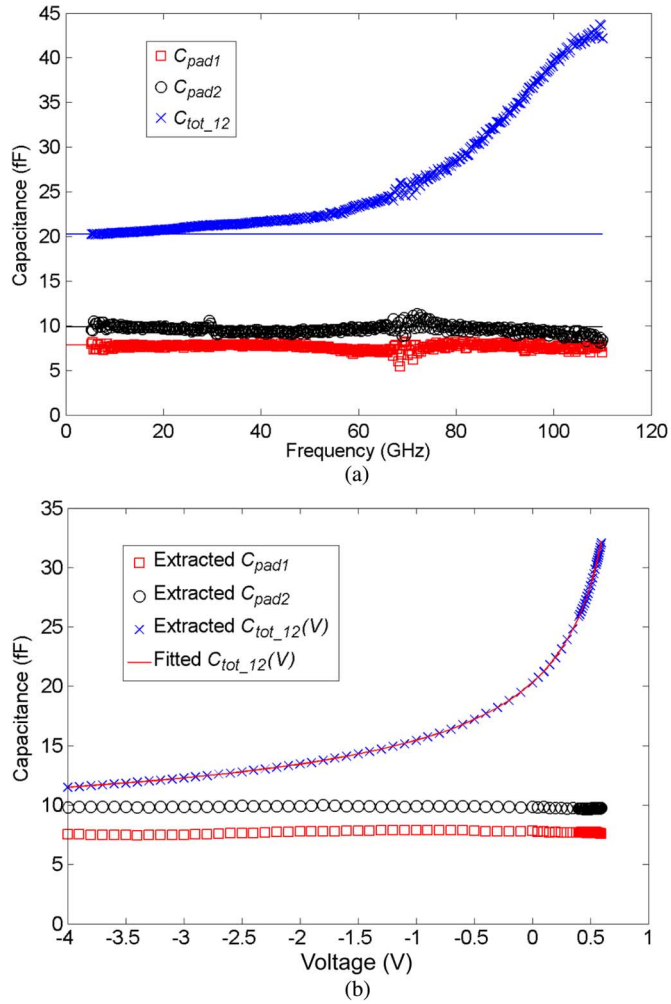


Fig. 7. Step 1: Capacitances extraction at a low-frequency range. (a) Plot of capacitance versus frequency at zero biasing voltage (markers show the extracted value and solid lines show the fitted capacitance in the 5–6-GHz range). (b) Plot of extracted capacitance versus voltage.

During measurement, the wafer is placed on top of a W-band microwave absorber.

The Agilent PNA N5250C and Keithley 2606A dual channel bias supply setups are used. The voltage difference applied across the diode terminals is varied from -4 to 1 V and the corresponding dc current is measured. For each voltage level, the frequency is swept from 5 to 110 GHz. The RF power for each port is -27 dBm.

The calibration is performed using a set of on-wafer thru-reflect-line (TRL) calibration structures, providing accurate measurement between 5–110 GHz. The reference planes [25] after calibration are placed close to the diode pads, as indicated in Fig. 5.

C. 3-D EM Full-Wave Simulations (5–600 GHz)

A 3-D EM full-wave diode model is useful for high-frequency diode geometry design optimization and for analyzing the geometry-dependent parasitics. For simulation up to 600 GHz, only half of the diode structure is constructed due to the symmetry property (see Fig. 6).

The S-parameters are calculated for an open-circuited and a short-circuited diode structure, as illustrated in Fig. 6(b). The diodes are placed in air channels and the reference planes are placed close to the intrinsic device. The conductive losses are not taken into account. The detail of the simulation setup is explained in [5]. The simulated suspended stripline mode characteristic impedance is approximately 120 Ω across the frequency band.

V. Result

In this section, the proposed method (Section III) is used to extract the diode model from the measured and simulated S-parameters. The MATLAB-Muwave toolbox [26] is used to handle the computations.

A. On-Wafer CPW Diode Model

The model capacitances are first calculated using (3) and (4) and the result is plotted in Fig. 7. At high frequencies, the total capacitance $(C_{\text{tot\_12}})$ increases to ∼45 fF. This indicates that the low-frequency equivalent-circuit assumption in Fig. 2 is not valid beyond ∼20 GHz and the influence of the inductance is observed. Thus, the capacitances are taken at the low-frequency asymptote, i.e., in the 5–6-GHz range. Equation (5) is then fitted to the extracted capacitance for a biasing voltage from -4 to 0.6 V by setting M to 0.5.

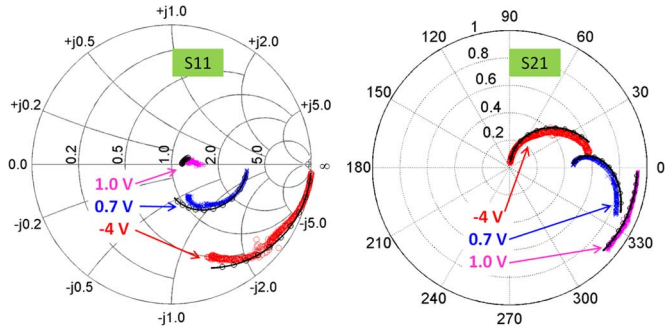


Fig. 8. Comparison of the measured and modeled S-parameter from 5 to 110 GHz (markers are the measurement data; solid lines are the corresponding model responses; dots on the solid lines indicate a range of frequency points from 10 to 100 GHz with a 10-GHz step).

From the curve-fitting procedure, C_{j0}, $\psi_{\rm bi}$, and $C_{\rm par}$ are extracted to be 15 fF, 0.87 V, and 5 fF, respectively. From the de-embedding structure measurement, the pad-to-pad capacitance is 3 fF. With (6), the finger-to-pad capacitance is deduced as 2 fF. The pad capacitances are constant across the biasing voltage.

After extracting the capacitances, the total diode resistance is calculated using (7) and the result is shown in Fig. 9. The series resistance is estimated to be approximately 8 Ω in the forward-biased cases. At the dc biasing voltage of 1 V, the diode current is ∼23 mA. Due to the high current level, the diode is subjected to self-heating. The estimated value is not corrected for the self-heating effect [9] and this is further discussed in Section VI-C.

For the parasitic inductances extraction, the S-parameters for a biasing voltage range of 0.9–1 V, within a frequency range of 20–110 GHz, are used. For a zero slope, the finger and pad inductance are relatively constant across the voltage range. The total finger and pad inductances are extracted as 60 pH. However, in this frequency range, it is difficult to distinguish between the finger and pad inductances. The sensitivity of finger and pad inductance extraction is discussed in Section VI-B.

With all the extracted parameters, the S-parameters between the measurement and model are compared for a frequency range of 5–110 GHz. In the model, the junction capacitance is neglected for the 0.8–1-V range. For the −4–0.7 V, the junction capacitance is modeled using the voltage-dependent term in (5) with the extracted C_{j0} and $\psi_{\rm bi}$.

A comparison of the S-parameters for three voltage points is plotted in Fig. 8. Only forward return loss (S_{11}) and transmission (S_{21}) are shown. This is because the reverse S-parameters (S_{22} and S_{12}) are similar to those in the forward direction. Fig. 10 shows the errors calculated using (11).

For the forward-biased case, there is a good agreement between the measured and modeled S-parameters. However, for the reverse-biased case, the model does not agree well with the measurement at frequencies higher than 30 GHz. This error is investigated to be attributed to the onset of parasitic propagation modes in the CPW measurement setup, i.e., energy loss due to radiation [27], [28]. The error is more pronounced for a more reverse-biased case. Despite the problems due to parasitic modes, the average error for all the bias voltages are still in the order of or below 10^{-2}.

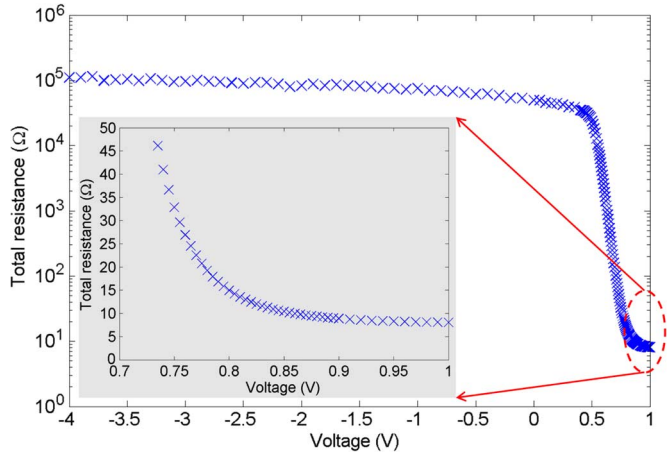


Fig. 9. Step 2: Total resistance extraction (inset: total resistance at forward-biased case for series resistance estimation).

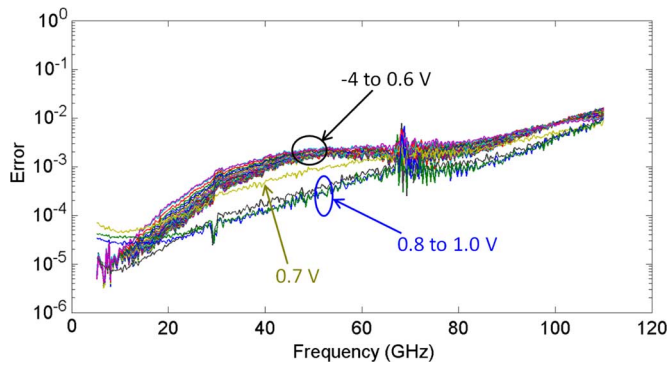


Fig. 10. Calculated errors between measurements and models.

B. 3-D EM Full-Wave Diode Parasitic Model in Suspended Stripline Configuration

The parasitic capacitances are extracted at 5 GHz. By using (4), the pad-to-pad capacitance is calculated using the de-embedded structure. A similar equation is used to calculate the capacitances using the S-parameters from the open-circuited diode structure. This yields a $C_{\rm pp}$ of 1.6 fF and a $C_{\rm fp}$ of 0.6 fF. $C_{\rm pad1}$ and $C_{\rm pad2}$ are 0.5 and 0.6 fF, respectively.

Since the simulation does not take into account the conductance losses, the resistance extraction steps are skipped. The pad and finger inductances are then calculated. The finger inductance slope is calculated for 20–600 GHz, and the tolerance is set to zero. The slope reached zero at the 42th iteration, resulting in a finger inductance of 10.8 pH and a pad inductance of 6.3 pH (see Fig. 11). Fig. 12 shows a comparison of the model and simulations, indicating good agreements have been achieved.

VI. Discussion

A. Parasitic Model Parameter Comparisons

Table I summarizes all of the extracted parasitic model parameters. For the DUT in the CPW configuration, several parameters extracted from measurement are verified with values extracted by other means. From the dc *I–V* data, the diode series resistance is extracted as 8 Ω, which is consistent with the

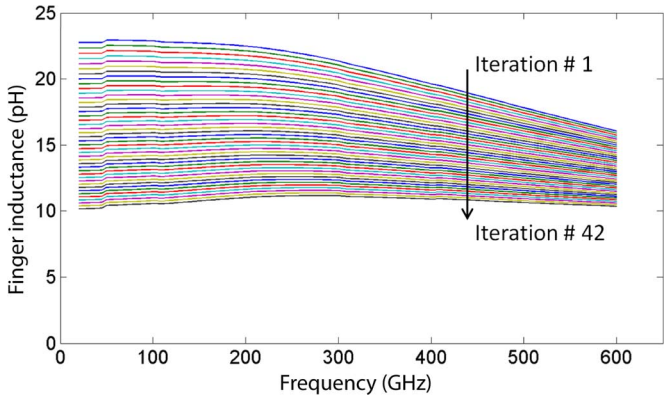


Fig. 11. Step 3: Inductance extraction at a high-frequency range.

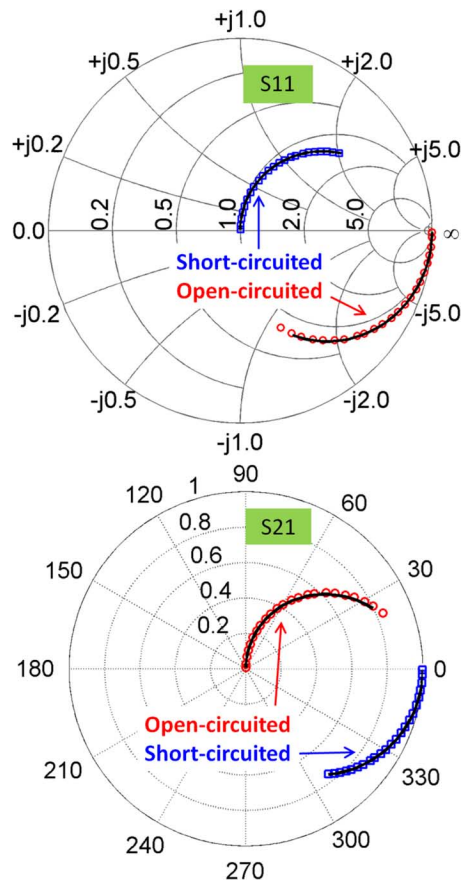


Fig. 12. Comparison of the simulated and modeled S-parameter from 5 to 600 GHz (markers are the simulated data; solid lines are the corresponding model responses).

value extracted in step 2. In addition to the diode with a mesa gap ($d_{\rm pp}$) of 10 μm, diodes with mesa gap of 8, 15, 20, and 30 μm are also measured. The $C_{\rm par}$ are extracted using a similar method.

For the diode model, as shown in Fig. 1, the pad-to-pad capacitance can be perceived as an analogy of two parallel plates separated by the distance of a mesa gap. Assuming a lumped model is valid ($d_{\rm pp} \ll \lambda_{\rm eff}$), the finger-to-pad capacitance can be estimated by fitting $C_{\rm par}$ as a function of the mesa gap. With this, the finger-to-pad capacitance is estimated as 2 fF (see Fig. 13).

TABLE I
EXTRACTED DIODE PARASITIC MODEL PARAMETERS

Parameter	DUT in CPW configuration (up 110 GHz)		DUT in suspended stripline configuration (up to 600 GHz)
	Measurement	Simulation	Simulation
C_{pp} (fF)	3	3	1.6
C_{fp} (fF)	2	0.8	0.6
L_f (pH)	-	-	10.8
R (Ω)	8	-	-
C_{pad1} (fF)	8	9	0.5
C_{pad2} (fF)	10	9	0.6
L_{pad1}=L_{pad2} (pH)	-	-	6.3
L_{tot} (pH)	60	60	23.4

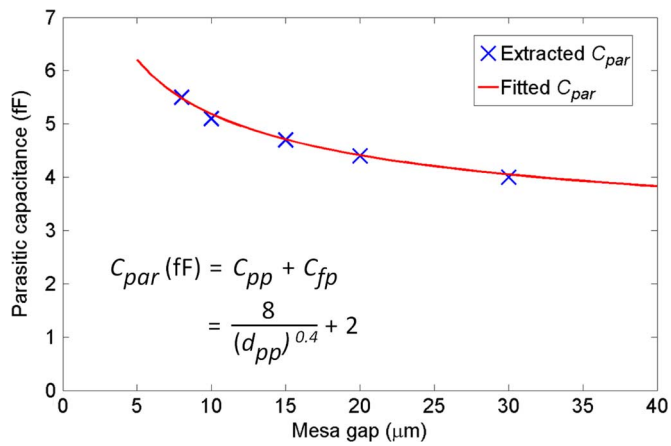


Fig. 13. Sum of pad-to-pad and finger-to-pad capacitances as a function of mesa gap ($d_{\rm pp}$ is in the unit of μm).

This agrees well with the finger-to-pad capacitance estimated with the assistance of the de-embedding structure.

A 3-D EM full-wave simulation is also performed for the DUT in the CPW configuration. The extracted parameters show a good agreement with those extracted from measurement, except for $C_{\rm fp}$. This is caused by the air-bridge finger bent near the anode contact during DUT fabrication, increasing the finger-to-pad coupling.

Between models of CPW and suspended stripline configuration, higher $C_{\rm pp}$ and $C_{\rm fp}$ are observed for the DUT in the CPW configuration. A higher $C_{\rm pp}$ is attributed to the thicker supporting substrate, i.e., 150 μm. Smaller pad parasitics are extracted for the model in the suspended stripline configuration. This is because of the difference in substrate thickness, as well as the reference planes placement, which are closer to the intrinsic device in the simulations of the suspended stripline configuration compared to the CPW configuration.

For the extraction of finger inductance, only the total inductance, defined as (13), is stated for the DUT in the CPW configuration. This is because of the lack of extraction accuracy in distinguishing the pad and finger inductances for the frequency

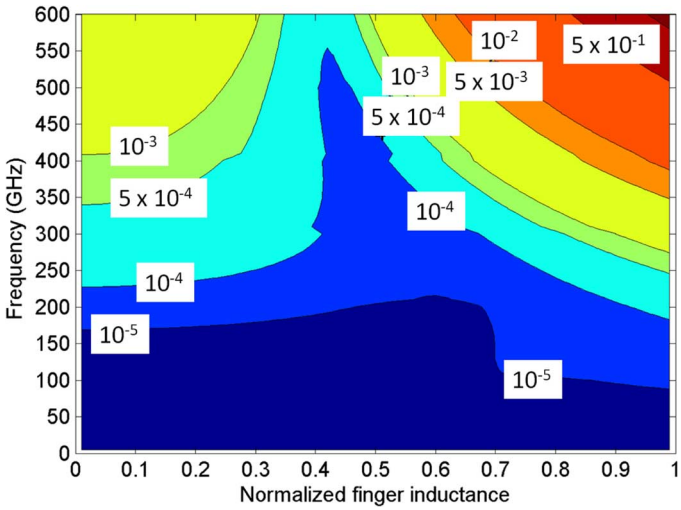


Fig. 14. Contour plot of the errors (e) as a function of frequency and normalized finger inductance.

range (up to 110 GHz). The extraction sensitivity is further analyzed and discussed in Section VI-B,

$$L_{\rm tot} = L_f + 2 \times L_{\rm pad}. \tag{13}$$

B. Finger Inductance Extraction Sensitivity Study

The finger inductance extraction sensitivity is analyzed by varying the finger inductance in the models, and the errors between the DUTs and models are studied. A normalized finger inductance $(L_{f\rm norm})$ is defined by dividing the varying finger inductance $(L_{f\rm var})$ to the total extracted inductance $(L_{\rm tot})$

$$L_{f\rm norm} = \frac{L_{f\rm var}}{L_{\rm tot}}. \tag{14}$$

For a $L_{f\rm norm}$ range of 0–1, the frequency-dependent errors (e) are calculated using (11) for the short-circuited DUT in the suspended stripline configuration. As shown in Fig. 14, below 300 GHz, there is no significant error variation across all the $L_{f\rm norm}$ values and the errors are below 10^{-3}. Moving from 300 to 600 GHz, the error has a clear minimum at a specific $L_{f\rm norm}$ value.

The errors averaged over frequency $(\overline{e})$, calculated using (12), exhibits a minimum value of 5×10^{-5} at the $L_{f\rm norm}$ of 0.43, which corresponds to a finger inductance of 10.1 pH. This agrees well with the extracted finger inductance in Section V-B.

For the measured DUT, the S-parameters at biasing voltage of 1 V are used for this sensitivity analysis. For the 5–110-GHz range, a similar frequency-dependent error trend, as in Fig. 14, is observed. For an $L_{f\rm norm}$ of 0–1, the errors averaged over frequency of 5–110 GHz $(\overline{e})$ increase monotonically from 1×10^{-3} to 2×10^{-3}. The error variation is relatively small. Thus, the extraction of finger inductance is not accurate at this frequency range.

At 300 and 600 GHz, the equivalent impedance of a 10-pH inductance is approximately 18 and 40 Ω, respectively. Thus, the frequency range for a proper finger inductance extraction should be high enough, which results in a corresponding reactance larger circa of 15% of the characteristic impedance.

C. Diode Intrinsic Impedance

By de-embedding all the parasitics, the diode intrinsic impedance $(Z_{\rm intrinsic})$ can be extracted. In this work, the series resistance is estimated to be 8 Ω from the forward-biased case at low frequencies. However, the extracted series resistance is subjected to errors due to self-heating from the forward conduction current. In addition, the measurement is performed with the wafer placed on a W-band microwave absorber and the thermal characteristic of diodes is not controlled. Under this circumstance, the diode series resistance tends to be underestimated. This can be circumvented by extracting the model parameters using pulsed S-parameters, instead of continuous biased S-parameters, in a well temperature-controlled environment.

Alternatively, the series resistance can be extracted from a reverse-biased case at high frequencies. For a proper series resistance extraction, the frequency has to be high enough where the junction conductance $(1/R_j)$ is relatively small compared to the junction capacitance susceptance (ωC_j). In addition, the junction capacitance reactance has to be comparable to the series resistance. For the measured DUT, the junction capacitance and resistance is approximately 15 fF and 50 kΩ at zero biasing voltage. For a series resistance within a tens Ω range, a frequency of >1 THz is required for a proper series resistance extraction under a reverse-bias condition. Today, S-parameter measurement equipment up to 1 THz is available. However, for measurement at such high frequency, the challenge lies in a proper calibration and high sensitivity to errors and tolerances [29], [30].

VII. Conclusion

We have proposed and evaluated a systematic and straightforward analytical method for high-frequency planar Schottky diode model parameter extraction. A step-by-step extraction has been demonstrated for three sets of S-parameter, i.e., 5–110-GHz measurement and 5–600-GHz simulations. The extracted models agree well with the DUT S-parameters. The method is robust and suitable for fast diode model extraction, which is useful for yield analysis. Moreover, the method can serve as a reliable technique to provide the initial parameters for further fine tuning using an optimization technique.

The challenges in extracting the air-bridge finger inductance and series resistance are addressed and the frequency range required for a proper parameter extraction is recommended. The proposed method is straightforward and applicable to other devices with a similar equivalent-circuit model.

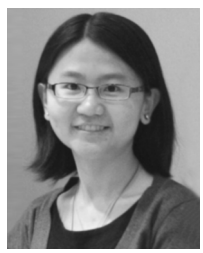
Acknowledgment

The authors would like to thank Dr. A. Vorobiev, Dr. M. Thorsell, and Dr. G. Moschetti for their help and discussions about the VNA measurement setup. The authors would also like to thank Prof. E. Kollberg for providing comments on this paper's manuscript.

References

[1] W. Bishop, K. McKinney, R. Mattauch, T. Crowe, and G. Green, "A novel Whiskerless Schottky diode for millimeter and submillimeter wave application," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 1987, pp. 607–610.

[2] P. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.
[3] T. Crowe, W. Bishop, D. Porterfield, J. Hesler, and R. Weikle, "Opening the terahertz window with integrated diode circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2104–2110, Oct. 2005.
[4] A. Maestrini, B. Thomas, H. Wang, C. Jung, J. Treuttel, Y. Jin, G. Chattopadhyay, I. Mehdi, and G. Beaudin, "Schottky diode-based terahertz frequency multipliers and mixers," *Comptes Rendus Phys.* , vol. 11, pp. 480–495, Aug. 2010.
[5] A. Y. Tang and J. Stake, "Impact of eddy currents and crowding effects on high-frequency losses in planar Schottky diodes," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3260–3269, Oct. 2011.
[6] J. L. Hesler, *Planar Schottky Diodes in Submillimeter-Wavelength Waveguide Receivers*. Charlottesville, VA, USA: Univ. Virginia, 1996.
[7] J. Zhang, P. Piironen, V. Mottonen, J. Louhi, A. Lehto, A. Simon, C. Lin, and A. Raisanen, "Model of quasi-vertical planar antiparallel Schottky diode," in *Proc. Int. Microw. Millimeter Wave Technol. Conf.*, 1998, pp. 130–133.
[8] T. Kiuru, K. Dahlberg, J. Mallat, A. V. Räisänen, and T. Närhi, "Comparison of low-frequency and microwave frequency capacitance determination techniques for mm-wave Schottky diodes," in *Eur. Microw. Integr. Circuits Conf.*, Manchester, U.K., 2011, pp. 53–56.
[9] T. Kiuru, J. Mallat, A. Räisänen, and T. Närhi, "Schottky diode series resistance and thermal resistance extraction from S-parameter and temperature controlled I–V measurements," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2108–2116, Aug. 2011.
[10] J. Liu, H. Morales, T. Weller, and L. Dunleavy, "Ultra-wideband nonlinear modeling of W-band Schottky diodes," *Microw. J.*, vol. 55, no. 9, p. 144, Sep. 2012.
[11] A. Tang, V. Drakinskiy, P. Sobis, J. Vukusic, and J. Stake, "Modeling of GaAs Schottky diodes for terahertz application," in *34th IEEE Int. Infrared, Millimeter, Terahertz Waves Conf.*, Piscataway, NJ, Sep. 21–25, 2009, 2 pp.
[12] J. Dieudonne, "Technology related design of monolithic millimeter-wave Schottky diode mixers," *IEEE Trans. Microw. Theory Techn.*, vol. 40, no. 7, pp. 1466–1474, Jul. 1992.
[13] H. Hjelmgren, E. Kollberg, and L. Lundgren, "Numerical simulations of the capacitance of forward-biased Schottky-diodes," *Solid State Electron.*, vol. 34, pp. 587–590, 1991.
[14] H. Hjelmgren, "Numerical modeling of hot electrons in n-GaAs Schottky-carrier diodes," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1228–1234, May 1990.
[15] R. Lipsey, S. Jones, J. R. Jones, T. Crowe, L. Horvath, U. Bhapkar, and R. Mattauch, "Monte carlo harmonic-balance and drift-diffusion harmonic-balance analyses of 100–600 GHz Schottky barrier varactor frequency multipliers," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1843–1850, Nov. 1997.
[16] B. Gelmont, D. Woolard, J. Hesler, and T. Crowe, "A degenerately-doped GaAs Schottky diode model applicable for terahertz frequency regime operation," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2521–2524, Dec. 1998.
[17] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 3, pp. 432–437, Mar. 1996.
[18] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determing the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.
[19] C. F. Campbell and S. A. Brown, "An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 7, pp. 1241–1247, Jul. 2001.
[20] K. Shirakawa, H. Oikawa, T. Shimura, T. Kawasaki, Y. Ohashi, T. Saito, and Y. Daido, "An approach to determining an equivalent circuit for HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 3, pp. 499–503, Mar. 1995.
[21] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear Transistor Model Parameter Extraction Techniques*. Cambridge, U.K.: Cambridge Univ. Press, 2012.
[22] J. Stake and H. Grönqvist, "An on-wafer method for C–V characterization of heterostructure diodes," *Microw. Opt. Technol. Lett.*, vol. 9, pp. 63–66, 1995.
[23] S. A. Maas, "Schottky-barrier diodes," in *Microwave Mixers*. London, U.K.: Artech House, ch. 2, pp. 11–59.
[24] R. Pucel, "Design considerations for monolithic microwave circuits," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-29, no. 6, pp. 513–534, Jun. 1981.
[25] R. Bauer and P. Penfield, "De-embedding and unterminating," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-22, no. 3, pp. 282–288, Mar. 1974.
[26] *"MATLAB–Muwave Toolbox,"* Chalmers Univ. Technol., Göteborg, Sweden, 2009.
[27] W. Haydl, "Resonanace phenomena and power loss in conductor-backed coplanar structures," *IEEE Microw. Guided Wave Lett.*, vol. 20, no. 12, pp. 514–516, Dec. 2000.
[28] M. Riaziat, R. Majidi-Ahy, and I. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 3, pp. 245–251, Mar. 1990.
[29] J. Stenarson, K. Yhland, T. Do, H. Zhao, P. Sobis, and J. Stake, "Influence of waveguide width errors on TRL and LRL calibrations," in *79th ARFTG Microw. Meas. Conf.*, Jun. 2012, pp. 1–3.
[30] D. F. Williams, "500 GHz–750 GHz rectrangular-waveguide vector-network-analyzer calibrations," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 2, pp. 364–377, Nov. 2011.



Aik Yean Tang (S'09) was born in Kedah, Malaysia. She received the B.Eng. degree in electrical-electronics engineering (honors) from the University Technology Malaysia, Johor Bahru, Malaysia, in 2002, the M.Eng. degree in nanoscience and nanotechnology from Katholieke Universiteit Leuven, Leuven, Belgium, in 2008, the M.Sc. degree in nanoscale science and technology from Chalmers University of Technology, Göteborg, Sweden, in 2008, and is currently working toward the Ph.D. degree in microtechnology and nanoscience at Chalmers University of Technology.

In 2002, she was a Silicon Validation Engineer with Intel Technology (M) Sdn. Bhd, Penang, Malaysia. In 2004, she joined Agilent Technologies (M) Sdn. Bhd., Penang, Malaysia, as an Analog IC Designer. From November 2010 to April 2011, she was a Visiting Research Ph.D. Student with the Submillimeter Wave Advanced Technology (SWAT) Group, Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, CA, USA. Her research interests include modeling, optimization, and integration of Schottky diodes for terahertz applications.

Ms. Tang was the recipient of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Graduate Fellowship Award in 2010.

Vladimir Drakinskiy was born in Kurganinsk, Russia, in 1977. He received the Diploma degree (with honors) in physics and informatics from the Armavir State Pedagogical Institute, Armavir, Russia, in 2000.

From 2000 to 2003, he was with the Physics Department, Moscow State Pedagogical University, Russia, as a Post-Graduate Student and Junior Research Assistant. Since 2003, he has been with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden. From 2003 to 2005, he was responsible for mixer-chip fabrication with the Herschel Space Observatory. Since 2008, he has been a Research Engineer with the Department of Microtechnology and Nanoscience, Chalmers University of Technology. His research interests include microfabrication and nanofabrication techniques, detectors for submillimeter and terahertz ranges, and superconducting thin films. He is currently responsible for the terahertz Schottky diode process line with MC2, Chalmers University of Technology.

Klas Yhland (M'07) received the M.Sc. degree in electronic engineering from the Lund University of Technology, Lund, Sweden, in 1992, and the Ph.D. degree in microwave electronics with Chalmers University of Technology, Göteborg, Sweden, in 1999.

From 1992 to 1994, he was with the Airborne Radar Division, Ericsson Microwave Systems. Since 1999, he has been Head of the National Laboratory for High Frequency and Microwave Metrology, SP Technical Research Institute of Sweden, Borås, Sweden. From 2000 to 2003, he was also with the Microwave Electronics Laboratory, Chalmers University of Technology. Since 2009, he has worked part time with the GigaHertz Centre, Chalmers University of Technolgy. Since September 2012, he has been an Adjunct Professor with the Terahertz

and Millimetre Wave Laboratory, Chalmers University of Technology. His research interests are microwave metrology, uncertainty analysis, new measurement techniques, planar measurement techniques, and design and modeling of microwave circuits.

Jörgen Stenarson (S'98–M'02) received the M.Sc. degree in engineering physics and Ph.D. degree in microwave electronics from Chalmers University of Technology, Göteborg, Sweden, in 1997 and 2001 respectively.

He is currently a Researcher with the SP Technical Research Institute of Sweden, Borås, Sweden, where his main interest is microwave metrology.

Tomas Bryllert was born in Växjö, Sweden, in 1974. He received the M.S. degree in physics and Ph.D. degree in semiconductor physics from Lund University, Lund, Sweden, in 2000 and 2005, respectively.

In 2006, he joined the Microwave Electronics Laboratory, Chalmers University of Technology, Göteborg, Sweden, where his main research interest was device and circuit technology for terahertz frequency multipliers. From 2007 to 2009, he was with the Submillimeter Wave Advanced Technology (SWAT) Group, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, USA, where he was involved with terahertz imaging and radar systems. He is currently with the Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, Göteborg, Sweden. He is also cofounder and Chief Executive Officer (CEO) of Wasa Millimeter Wave AB, a company that develops and fabricates millimeter-wave products.

Jan Stake (S'95–M'00–SM'06) was born in Uddevalla, Sweden, in 1971. He received the M.Sc. degree in electrical engineering and Ph.D. degree in microwave electronics from Chalmers University of Technology, Göteborg, Sweden, in 1994 and 1999, respectively.

In 1997, he was a Research Assistant with the University of Virginia, Charlottesville, VA, USA. From 1999 to 2001, he was a Research Fellow with the Millimetre Wave Group, Rutherford Appleton Laboratory, Didcot, U.K. He then joined Saab Combitech Systems AB, as a Senior RF/Microwave Engineer, until 2003. From 2000 to 2006, he held different academic positions with Chalmers University of Technology and, from 2003 to 2006, was also Head of the Nanofabrication Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology. During Summer 2007, he was a Visiting Professor with the Submillimeter Wave Advanced Technology (SWAT) Group, Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, CA, USA. He is currently Professor and Head of the Terahertz and Millimetre Wave Laboratory, MC2. He is also cofounder of Wasa Millimeter Wave AB, Göteborg, Sweden. His research involves sources and detectors for terahertz frequencies, high-frequency semiconductor devices, graphene electronics, and terahertz measurement techniques and applications.

Prof. Stake serves as a topical editor for the IEEE TRANSACTIONS ON TERAHERTZ SCIENCE AND TECHNOLOGY.