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A >120-GHz Bandwidth, >20-dBm P_{out}, <6-dB Noise-Figure Distributed Amplifier MMIC in a GaN-on-SiC HEMT Technology

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***Abstract*—This article demonstrates a distributed amplifier (DA) monolithic microwave integrated circuit (MMIC) with a 3-dB S_{21} bandwidth (BW) of 2–129 GHz fabricated in a gallium nitride (GaN) HEMT technology. Furthermore, the article investigates the prediction of the third-order intermodulation point (IP3) on device and DA level based on dc *I–V* measurements and compares two analytical approaches. The equations can be used as well as a design tool before the actual circuit design. The DA consists of eight cells based on common-source transistors with an average S_{21} of 6.7 dB. Within a frequency range from 2 to 110 GHz, the measured output-referred 1-dB compression point and saturated output power are between 17.9–20.2 dBm and 20.6–22 dBm, respectively. This is the first demonstration of an amplifier MMIC with an output power of more than 20 dBm over a 100-GHz BW. Up to 70 GHz, the measured output-referred IP3 is between 26.8 and 29.8 dBm. In addition to state-of-the-art large-signal performance, the DA exhibits also an excellent noise figure (NF) with values between 3.1 and 5.7 dB (2–110 GHz).**

***Index Terms*—Distributed amplifiers (DAs), distributed power amplifiers (DPAs), gallium nitride (GaN), high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), power amplifiers (PAs), silicon carbide (SiC), traveling-wave amplifiers (TWAs).**

I. Introduction

DUE to a wide bandgap, gallium nitride (GaN) high-electron-mobility transistor (HEMT) technologies provide the highest output power (P_{out}) densities in the millimeter-wave spectrum. Thus, generating RF power is always a major goal and driving force for further technology developments. Moreover, during the last years, GaN HEMTs demonstrated also an excellent noise figure (*NF*) with a very good *NF* up to *D*-band (110–170 GHz) frequencies [1]. Thus, GaN HEMTs can be considered today as the second-best low-noise technology, whereas only InGaAs HEMTs demonstrate a lower *NF*. However, the combination of an excellent noise performance, an outstanding P_{out}, and a good linearity make GaN HEMTs an optimum choice for many system applications, such as wireless communication and measurement equipment. In measurement equipment, the need for wideband amplifiers with state-of-the-art noise and large-signal performance is continuously growing. Especially in the context of new wireless communications standards, frequencies at 100 GHz and beyond are getting more and more important. Distributed amplifiers (DAs) are one of the most essential components in measurement equipment, where high relative and absolute bandwidths (BWs) are fundamental requirements. In addition, a low *NF* is needed for signal analysis or the generation of complex, highly modulated test signals with a low noise floor. Furthermore, a high P_{out} and low intermodulation products are important for the generation of clean test signal.

In GaN HEMT technologies, DA monolithic microwave integrated circuits (MMICs) have been demonstrated up to a BW of 120 GHz [2]. For frequencies below 39 GHz, the corresponding *NF* is reported with 4.8–6.8 dB. The saturated P_{out} (P_{sat}) is 19.4 dBm at 20 GHz. However, often both parameters degrade considerably toward the upper band edge. Even though the third-order intermodulation point (IP3) is besides the BW, commonly one of the most important requirements, it is rarely reported. In [3], the output-referred IP3 (OIP3) of a 65- GHz-BW DA is in excess of 34.1 dB. However, this excellent OIP3 is achieved at the expense of a high dc power consumption (P_{dc}) of 4.8 W. In general, InGaAs HEMT technologies demonstrate the best *NF* [4], [5], however, are commonly also limited in providing a high P_{out}. DA MMICs that are realized in InP double hetero-junction bipolar transistor (DHBT) technologies can achieve a P_{out} in excess of 20 dBm, however, have not reported this over a 100-GHz BW. Furthermore, the reported *NF* of InP DHBT DAs is, in general, the highest compared to all other technologies.

In this work, a GaN DA MMIC (Fig. 1) is demonstrated, which targets a >120-GHz BW with a lowest possible *NF* and a P_{out} of 20 dBm. The article is organized as follows. Section II shows a design tool based on dc transfer characteristics, which allows the estimation of the IP3 on the device level as well as on the DA level before an entire circuit design. The approach is adapted from device considerations, which are available in the open literature, and is transferred to DAs in this work. Furthermore, we compare two approaches with regard to the prediction of IP3 over bias. This design tool is also valuable in situations of rapid transistor technology developments where sophisticated models are not always available or are limited in their coverage. In Section III, the MMIC design including tradeoffs concerning the device bias, the noise performance, the linearity, and the BW is discussed. The measurements of the MMIC are presented in

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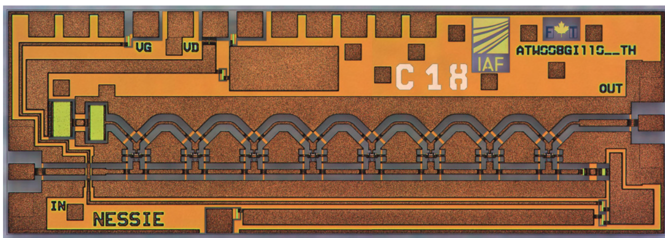

Fig. 1. Chip photograph of the fabricated DA MMIC with a total size of $2 \times 0.75\,\mathrm{mm}^2$.

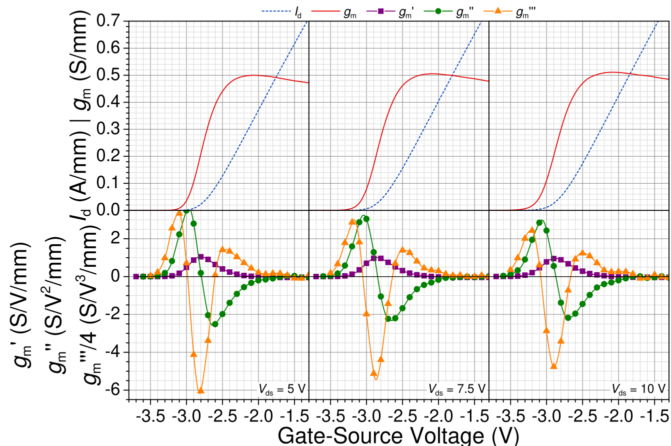

Fig. 2. Top row shows the measured dc I_d versus V_{gs} and, based on this, the extracted g_m for different V_{ds}. The bottom row gives the first, second, and third derivative of the measured g_m.

Section IV and include S-parameters, the NF at different backside temperatures, and single- and two-tone continuous-wave (CW) linearity measurements. A state-of-the-art comparison and discussion is given in Section V. Section VI concludes the article.

II. Device Bias and Linearity Considerations

The presented work is based on the Fraunhofer IAF GaN-on-SiC HEMT technology, which is described in more detail in [6]. The active layers are grown in-house by metal–organic vapor deposition on 100-mm semi-insulating 4H-SiC substrates. The process features different gate lengths, such as 70, 100, and 130 nm. The saturation dc drain current (I_d) is above 1.5 A/mm and the peak transconductance (g_m) exceeds 500 mS/mm. Fig. 2 depicts transfer characteristics of a 70-nm gate-length HEMT for different drain-source voltages (V_{ds}). 70-nm devices exhibit transition and maximum-oscillation frequencies (f_T and f_{max}) of up to 145 GHz and above 300 GHz, respectively. The back-end-of-line process features two interconnect gold layers. The second of which is a galvanic metal layer and can be realized in air-bridge technology. The backside process includes wafer thinning to a thickness of 75 μm and through-substrate vias.

In this work, 70-nm gate-length devices are used mainly due to high cut-off frequencies, f_T and f_{max}, over a wide range of bias conditions, also at moderate and low currents and voltages.

The choice of the correct bias conditions makes the design of DAs even more important than for other amplifier topologies since several critical design parameters depend directly on it and, in addition, are interconnected. The dependence of the RF performance of a DA on I_d is, in general, much stronger than the dependence on V_{ds}. Especially in a standard bias regime for amplifiers of approximately 50–500 mA/mm (for this technology), g_m has one of the strongest variations versus gate-source voltage (V_{gs}) and the corresponding I_d. This is also a reason why, commonly, g_m is considered to affect the intermodulation distortion in a weakly nonlinear regime most. Furthermore, g_m has a direct impact on the gain of a DA and, consequently, also on the NF. Based on a reactively matched low-noise amplifier (LNA), we investigated the NF bias dependence already in one of our previous works [6]. As a first approximation, we take the main conclusion also for this work, where no strong NF dependence on V_{ds} was observed. An optimum NF was achieved for an I_d of approximately 200 mA/mm with only minor degradation in the range of a few tenths of decibel for currents as high as 400 mA/mm.

For investigating the bias dependence of IP3, two approaches are used and compared in this work. Both are based on dc transfer characteristics and corresponding derivatives of I_d with respect to V_{gs}. Since IP3 is considered a measure of a weakly nonlinear regime, pulsed I–V curves are not considered in this work. The first equation is presented in [7] and is based on [8]. It describes IP3 at an available input power (AIP3) when terminating the device at the input and output with the real impedances Z_g and Z_d, respectively. This is very much the case of a DA where each transistor is embedded in an artificial transmission line (ATL) and Z_g and Z_d are the impedances of the input and output ATL of a DA. The input-referred IP3 (IIP3) and AIP3 differ since for IIP3 the impedance cannot necessarily be considered real. AIP3 and the well-known OIP3 are linked by the transducer gain (G_t) [7]

$$\mathrm{OIP3} = \mathrm{AIP3} \cdot G_t. \tag{1}$$

Based on Maas and Crosmun [8], AIP3 ($\mathrm{AIP3}_m$) is given as

$$\mathrm{AIP3}_m = \frac{1}{2|Z_g|}\left|\frac{\alpha_1(1+\alpha_1 R_s)^2}{(\alpha_3 - 2\alpha_2^2 R_s)(1-\alpha_1 R_s)}\right| \tag{2}$$

where R_s is the source resistance of a transistor and α_1 to α_3 are the following Taylor coefficients [8]:

$$\alpha_1 = \frac{\partial I_d(V_{gs})}{\partial V_{gs}} = g_m \tag{3}$$

$$\alpha_2 = \frac{1}{2}\frac{\partial^2 I_d(V_{gs})}{\partial V_{gs}^2} = \frac{g_m'}{2} \tag{4}$$

$$\alpha_3 = \frac{1}{6}\frac{\partial^3 I_d(V_{gs})}{\partial V_{gs}^3} = \frac{g_m''}{6}. \tag{5}$$

Equation (2) refers to a description with the intrinsic g_m (g_{mi}) and, when inserting (3), (4), and (5) into (2), $\mathrm{AIP3}_m$ results in

$$\mathrm{AIP3}_m = \frac{3}{|Z_g|}\left|\frac{g_{mi}(1+g_{mi}R_s)^2}{(g_{mi}'' - 3g_{mi}'^2 R_s)(1-g_{mi}R_s)}\right|. \tag{6}$$

If an extrinsic g_m is used, R_s can be set to zero and (6) simplifies to

$$\mathrm{AIP3}_m = \frac{1}{2|Z_g|}\left|\frac{\alpha_1}{\alpha_3}\right| = \frac{3}{|Z_g|}\left|\frac{g_m}{g_m''}\right| \tag{7}$$

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$$= 10\log\left(\frac{3}{|Z_g|}\left|\frac{g_m}{g_m''}\right|n\right) + 30. \quad (8)$$

It is obvious that in this equation, g_m'' is the dominant g_m distortion mechanism. However, Kobayashi et al. [3] add cross terms and replace the denominator in the following way to improve the prediction of IP3 over bias, especially for high currents. This modifies AIP3 to AIP3$_k$

$$\alpha_3 \Rightarrow \sqrt{\left|\alpha_3^2 + \frac{16}{9}\alpha_2\alpha_4\right|} \quad (9)$$

$$g_m'' \Rightarrow \sqrt{\left|g_m''^2 + \frac{4}{3}g_m' g_m'''\right|} \quad (10)$$

$$\Rightarrow \mathrm{AIP3}_k = \frac{3}{|Z_g|}\frac{g_m}{\sqrt{\left|g_m''^2 + \frac{4}{3}g_m' g_m'''\right|}} \quad (11)$$

$$= 10\log\left(\frac{3}{|Z_g|}\frac{g_m}{\sqrt{\left|g_m''^2 + \frac{4}{3}g_m' g_m'''\right|}}\right) + 30. \quad (12)$$

Since AIP3 is independent of the device periphery, the equations above illustrate also a major benefit of AIP3 compared to, for example, OIP3. This is the case for both version of AIP3, (7) and (11). Thus, AIP3 depends mainly on the general behavior of a device or technology itself and, of course, the bias condition, but less on the circuit design or implementation of a DA, such as the device size or the number of used transistors. This is advantageous since the gain of a DA depends on the absolute value of g_m as well as on the number of transistors. Especially at an early stage of a circuit design, these details might be unknown.

However, for approximating OIP3, one can estimate G_t of an n-cell DA by using an equation, which is given in [9]

$$G_t = \frac{g_m^2 Z_g Z_d}{4}\left(\frac{\exp(-\alpha_g l_g n) - \exp(-\alpha_d l_d n)}{\alpha_g l_g - \alpha_d l_d}\right)^2 \quad (13)$$

where α_g and α_d are the attenuation constants per unit cell of the gate and drain ATLs and l_g and l_d are the lengths of unit gate- and drain-line sections, respectively. α_g and α_d are given as [9]

$$\alpha_g = \frac{R_{\mathrm{in}}(\omega C_{\mathrm{in}})^2}{2l_g}Z_g = \frac{R_{\mathrm{in}}(\omega C_{\mathrm{in}})^2}{2l_g}\sqrt{\frac{L_g}{C_g + \frac{C_{\mathrm{in}}}{l_g}}} \quad (14)$$

$$\alpha_d = \frac{1}{2R_{\mathrm{out}}l_d}Z_d = \frac{1}{2R_{\mathrm{out}}l_d}\sqrt{\frac{L_d}{C_d + \frac{C_{\mathrm{out}}}{l_d}}} \quad (15)$$

where R_{in}, R_{out}, C_{in}, and C_{out} are the input and output resistances and capacitances of the used transistor in a DA unit cell, respectively. L_g, L_d, C_g, and C_d are the per-unit-length inductance and capacitance of the used transmission lines in the gate and drain line of a DA. Very often, the attenuation of the drain ATL is neglected, which simplifies (13) significantly. However, this is only valid if, for example, R_{out} is considerably large. For RF-cascode-based DAs, this might be the case. The R_{out} of a common-source (CS) device is, most likely, too small, and the attenuation of the drain ATL has to be considered as well. We can calculate OIP3 using two different equations, as in (16) and (17), shown at the bottom of the next page, by inserting (13) and (7) or (11) into (1). For a better readability, (16) (OIP3$_m$: describing OIP3 based on [8]) and (17) (OIP3$_k$: describing OIP3 based on [3]) are listed below.

Now, for investigating the bias dependence and its impact on IP3, the symbols in Fig. 3 (bottom row) show the calculated AIP3 versus I_d for a V_{ds} of 5, 7.5, and 10 V. For the calculation of AIP3$_m$ and AIP3$_k$, measured transfer characteristics and the corresponding derivatives of a 70-nm gate-length HEMT (depicted in Fig. 2) are used. It can be observed that up to an I_d of approximately 400 mA/mm AIP3$_m$ and AIP3$_k$ increase considerably and are almost identical. Above, AIP3 is flattening out, however, AIP3$_m$ predicts approximately 6 dB higher values as compared to AIP3$_k$. At high drain currents, the calculated AIP3 based on measured dc I–V curves tends to be slightly noisy, which is caused by measurement fluctuations in combination with considerably small values of the derivatives of g_m. However, the trends can still be observed. Simulations, using a large-signal transistor model, are not included since the available model is not verified for such a wide bias range.

From AIP3 (Fig. 3) and the two versions of predicting it, there are two major conclusions. First, within a usual bias range, the V_{ds} dependence is almost negligible. Second, the I_d where AIP3 saturates is different for AIP3$_m$ and AIP3$_k$. This is important since I_d is an important design parameter for the design of a DA. One might be interested in selecting a bias where I_d is considerably low, whereas AIP3 should be of course maximized. For AIP3$_k$, such a bias is at approximately 400 mA/mm with a predicted value of 24 dBm. At the same bias, AIP3$_m$ predicts a very similar value. However, when increasing I_d by 25%–50%, AIP3$_m$ gains roughly 6 dB. Therefore, it is interesting to further investigate and compare AIP3$_m$ and AIP3$_k$ with measurements of a real implementation of a DA.

III. Distributed Amplifier MMIC Design

The DA is based on CS devices using a gate length of 70 nm. In this design, we aim for a gain of 7–8 dB, which is a challenge for a CS DA. However, compared to an RF-cascode-based version, the achievable *NF* is expected to be better. A simplified schematic of the DA MMIC is illustrated in Fig. 4.

The first step is to determine the bias condition, which targets a tradeoff between *NF*, AIP3, G_t, and P_{sat}. As already discussed in the previous section, the *NF* depends only slightly on V_{ds} and I_d should be in a range of 150–400 mA/mm to prevent a noise degradation. g_m and thus G_t exhibit a peak performance at approximately 350 mA/mm almost independent of V_{ds}. For AIP3, it is at this moment unclear which, (7) or (11), is closer to the actual performance of the used device. Thus, it is also the goal of this work to further investigate the prediction of AIP3 since a major difference between the two discussed equations is expected at the upper part of the usable range of I_d. In any case, AIP3 is considerably increasing up to at least 400 mA/mm. Also for AIP3, only minor differences can be observed for a V_{ds} between 5 and 10 V. However, a higher P_{out} is expected for an increased V_{ds}. We know from previous work [6] that a major improvement of P_{out} can be achieved when increasing V_{ds} from 5 to 7.5 V, whereas

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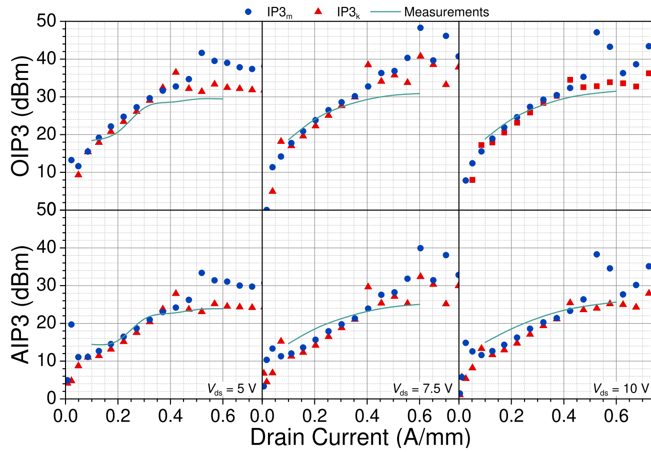

Fig. 3. Symbols show the extracted (bottom) AIP3 and (top) OIP3 based on the dc I–V curves as shown in Fig. 2. The green line indicates the actual measurement of AIP3 and OIP3 of the fabricated DA MMIC at 10 GHz.

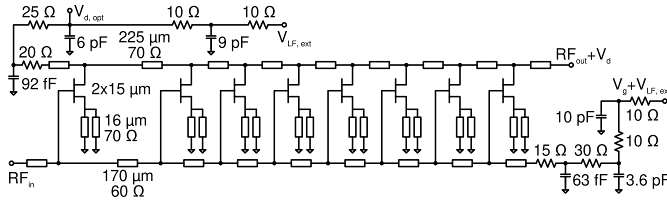

Fig. 4. Simplified schematics of the presented DA MMIC.

10 V provides only minor benefits. Thus, combining all pros and cons, the bias condition for the initial design is set to $V_{\text{ds}} = 7.5$ V and $I_d = 400$ mA/mm.

The next step is the choice of the total gate width (TGW). This is a fundamental parameter since, once the bias conditions are set, TGW heavily defines the achievable gain, though limiting the possible BW simultaneously. Thus, TGW is the result of a tradeoff in an iterative optimization procedure. The goal is to maximize TGW while achieving a BW of 120 GHz. In general, the main decision criterion is the Bragg frequency (f_{bragg}), which defines the cut-off frequency of an ATL. For the gate and drain ATL of a DA, f_{bragg} is defined as [10]

$$f_{\text{bragg},g} = \left(\pi\sqrt{L_g(C_g + C_{\text{in}})}\right)^{-1} \tag{18}$$

$$f_{\text{bragg},d} = \left(\pi\sqrt{L_d(C_d + C_{\text{out}})}\right)^{-1}. \tag{19}$$

However, since at f_{bragg}, the impedance of an ATL is zero and the attenuation highly increases, a DA has to be designed with a certain margin, which is difficult to estimate simply from f_{bragg}. A more sophisticated criterion is the impedance of the corresponding gate and drain ATLs [10]

$$Z_{0,g}(f) = \sqrt{\frac{L_g}{C_g + C_{\text{in}}}}\sqrt{1 - \frac{f^2}{f^2_{\text{bragg},g}}} \tag{20}$$

$$Z_{0,d}(f) = \sqrt{\frac{L_d}{C_d + C_{\text{out}}}}\sqrt{1 - \frac{f^2}{f^2_{\text{bragg},d}}} \tag{21}$$

and the resulting input and output matching

$$S_{11}(f) = 20\log\left|\frac{50 - Z_{0,g}(f)}{50 + Z_{0,g}(f)}\right| \tag{22}$$

$$S_{22}(f) = 20\log\left|\frac{50 - Z_{0,d}(f)}{50 + Z_{0,d}(f)}\right|. \tag{23}$$

In the end, TGW is set to 30 μm with a two-finger layout. For a CS configuration, this results in a simulated input and output impedance of (11.04 − 48.19i) and (37.38 − 102.15i) Ω, respectively. However, the first simulations indicate an instability at approximately 160 GHz. Since even an out-of-band instability might lead to an oscillating amplifier, short source lines (SLs) are integrated. This technique has to be treated carefully since the source inductance adds to the real part of the input impedance and, thus, increases α_g, as presented in (14). Hence, two 16-μm-short SLs in a symmetric layout are used. The transmission lines of the gate and drain ATL are designed to achieve matching and synchronism over the intended BW. The corresponding transmission lines have a length of 170 and 225 μm, as it is shown in Fig. 4. Based on (18)–(21), the resulting matching and impedance of the gate and drain ATL are given in Fig. 5. It is clearly shown that the gate ATL limits the BW, as is commonly the case for this type of DA. Furthermore, Fig. 5 indicates that the chosen TGW is at the upper limit since a 120-GHz BW achieving a matching of −10 dB is challenging. This results from an $Z_{0,g}$ that is already for low frequencies below 50 Ω. This is a common behavior of this class of DA and is evidence for a maximal TGW. Fig. 5 shows as well that using a small SL has almost no impact on the achievable BW, as long as matching is the main concern.

$$\begin{aligned}
\text{OIP3}_m = {} & \frac{3g_m^3}{|g_m''|}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\left(\exp\left(-nR_{\text{in}}(\omega C_{\text{in}})^2\sqrt{\frac{L_g}{C_g + \frac{C_{\text{in}}}{l_g}}}\right) - \exp\left(-\frac{n}{R_{\text{out}}}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\right)\right)^2 \\
& \times \left(R_{\text{in}}(\omega C_{\text{in}})^2\sqrt{\frac{L_g}{C_g + \frac{C_{\text{in}}}{l_g}}} - \frac{1}{R_{\text{out}}}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\right)^{-2}
\end{aligned} \tag{16}$$

$$\begin{aligned}
\text{OIP3}_k = {} & \frac{3g_m^3}{\sqrt{\left|g_m''^2 + \frac{4}{3}g_m' g_m'''\right|}}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\left(\exp\left(-nR_{\text{in}}(\omega C_{\text{in}})^2\sqrt{\frac{L_g}{C_g + \frac{C_{\text{in}}}{l_g}}}\right) - \exp\left(-\frac{n}{R_{\text{out}}}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\right)\right)^2 \\
& \times \left(R_{\text{in}}(\omega C_{\text{in}})^2\sqrt{\frac{L_g}{C_g + \frac{C_{\text{in}}}{l_g}}} - \frac{1}{R_{\text{out}}}\sqrt{\frac{L_d}{C_d + \frac{C_{\text{out}}}{l_d}}}\right)^{-2}
\end{aligned} \tag{17}$$

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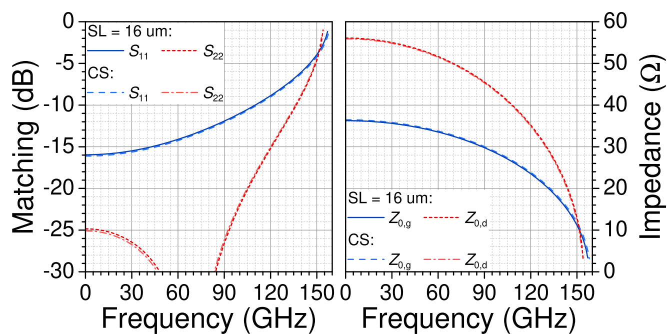

Fig. 5. Based on (18)–(21), calculated matching and impedance of the gate and drain ATL.

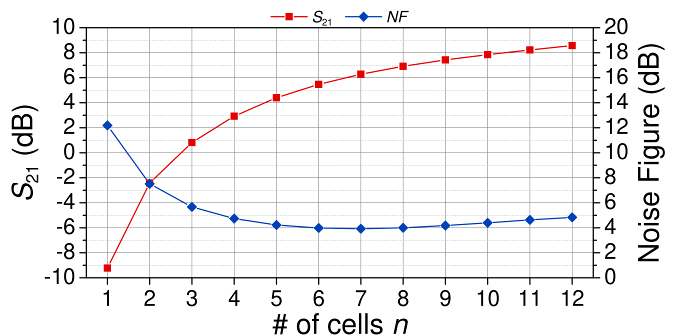

Fig. 6. Simulated S_{21} and NF versus n. The values are averaged over the intended 120- GHz BW.

n is again a tradeoff between different parameters, such as small-signal gain, NF, and P_{out}. As it can be seen in (13), the small-signal gain increases by increasing n. Though, due to α of the gate and drain ATL, the maximum n is limited. Furthermore, it is also important to mention that (13) does not consider losses of the transmission line itself, which adds frequency-dependent losses and further increases the falling gain slope over frequency that is already caused by α_g. Thus, in practice, the maximum n decreases with frequency. Concerning NF, we have to differentiate between the low-frequency (LF) behavior and, approximately, the upper half of the operating BW. We know from [11] that, for frequencies toward zero, the forward and reverse gain of a DA equals, which leads to the well-known NF increase at low frequencies. The increase is caused by the amplified noise power of the gate-line termination. The corner frequency of the increased NF is a function of n so that the corner frequency decreases by increasing n. Theoretically, as discussed in [11], also the NF of the upper part of the operating frequency range improves by increasing n. However, this is only true as long as frequency-dependent losses of the transmission lines and α_g are neglected. In practice, it has been shown [5] that, even when S_{21} still increases in the upper-frequency part, the corresponding NF increases as well with n. Concerning P_{out}, the discussion follows roughly the above-mentioned gain considerations. P_{out} increases as n increases. However, frequency-dependent losses commonly result in an increasing P_{out} slope over frequency as n increases. In general, this is even more pronounced for gain cells based on RF cascodes or more extreme stacks, which follow stack-specific reasons and is discussed in detail in [12] and [13]. Fig. 6 shows the simulated average S_{21} and NF versus number of cells. The average NF shows a minimum of six to eight cells and degrades to both sides. The increase of S_{21} flattens slightly toward more cells, but improves even up to 12 cells. Weighing up all the pros and cons, n is set to eight. It offers a simulated S_{21} of approx. 7 dB and balances the discussed noise aspects.

The last design part is dedicated to the resistive gate- and drain-line terminations. Their main purpose is to avoid reflections at the end of the gate and drain ATLs. As discussed above, the impedance of an ATL is dispersive, which results in degraded input and output matching, as long as a constant resistive load is used. In general, two possibilities can counteract this characteristic: first, a line–shunt-capacitor–line T-network at the input and output of a DA or, second, a termination that follows the frequency dispersion of the ATL impedance. The first of which is common practice, but introduces losses. Hence, the second option is realized using a distributed network of resistors and shunt capacitors as presented in Fig. 4. The main design goal for the terminations is to short-circuit higher operating frequencies earlier so that the effective resistance is lower as compared to lower frequencies. The gate-line termination is designed so that the DA can be biased via the termination. Even though it is not intended to supply the drain bias of the DA via the drain-line termination, the drain resistors are wide enough to allow also a bias via the termination. Since the dc shunt capacitors that can be realistically integrated on an MMIC are limited, both terminations include also an additional port to connect an LF extension.

IV. Measurement Results

The MMIC was measured on wafers with different setups. All setups are calibrated to the RF probe tips and for all measurements, V_{ds} is supplied via the RF output pad. Unless otherwise stated, the MMIC is biased with a V_{ds} of 7.5 V and an I_d of 96 mA (400 mA/mm).

The S-parameters are measured with an Anritsu VectorStar vector network analyzer up to 150 GHz. The calibration is done with a FormFactor impedance standard substrate and a corresponding FormFactor eLRRM calibration algorithm. The measured S-parameters are shown in Fig. 7. The DA MMIC exhibits an average S_{21} of 6.7 dB within a 3-dB BW from 2 to 129 GHz. The peak gain is 7.5 dB. For operating frequencies of up to 120 GHz, the measured S_{21} is better than 6 dB. Over the entire BW, the input and output return loss is better than 11.7 and 14.1 dB, respectively. Fig. 8 shows the group delay and the K-factor of the DA MMIC. The K-factor is always above 1.2 indicating unconditional stability. In the 3-dB BW, the group delay is within 14.3–30.5 ps.

The NF is measured with two Y-factor setups. Up to 45 GHz, the setup contains a Keysight coaxial noise source at the input and a Keysight PXA signal analyzer at the output. Before the PXA, a wideband amplifier module preamplifies the test signal. At W-band (75–110 GHz), the setup uses an ELVA-1 WR10 waveguide noise source at the input and a commercially-available mixer module at the output of the DUT. The actual noise power at intermediate frequencies is measured by a Keysight NF analyzer. A detailed description of the W-band on-wafer noise setup is given in [6]. The second-stage contributions are corrected in a preceding calibration step. In the frequency range from 2 to 110 GHz, the measured NF

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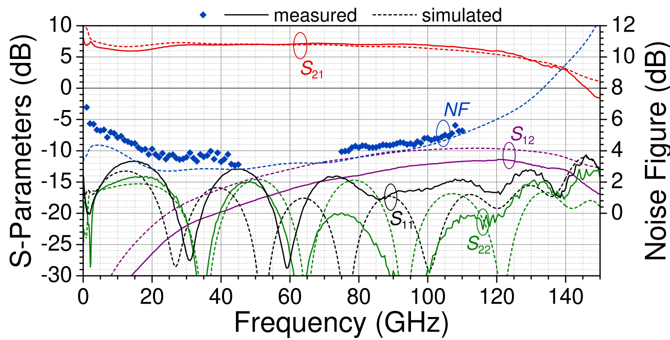

Fig. 7. Measured (solid lines) and simulated (dashed lines) S-parameters of the presented DA MMIC from 0.01 to 150 GHz. The measured NF is depicted by blue symbols.

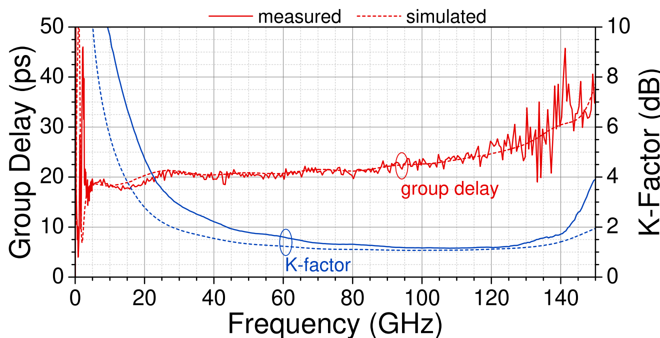

Fig. 8. Measured (solid lines) and simulated (dashed lines) group delay and K-factor of the presented DA MMIC from 0.01 to 150 GHz.

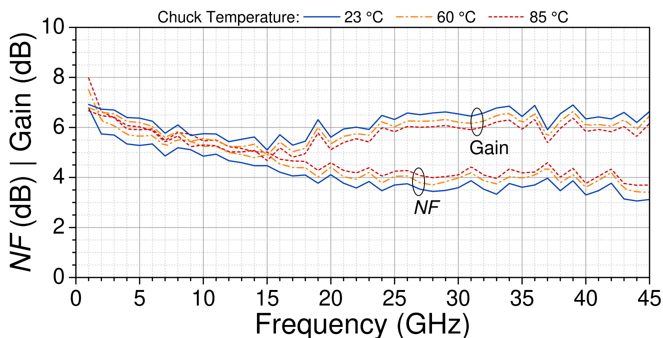

Fig. 9. Measured NF and gain of the presented DA MMIC for different chuck temperatures.

is between 3.1 and 5.7 dB. The NF is plotted together with the S-parameters in Fig. 7. The measurements over ambient temperature are shown in Fig. 9. On average, the gain and NF shows a temperature dependence of approximately −0.007 and 0.01 dB/K, respectively.

The large-signal performance of the DA is characterized by three setups, all in the CW mode. Up to 50 GHz, the single-tone performance is measured with a signal generator and a preamplifier at the input. Between the preamplifier and the RF input probe, the correct leveling of the input signal is verified in situ by using a 20-dB coaxial directional coupler and a power sensor at the coupled port. At the output, the fundamental frequency and the harmonic signals are measured by an Anritsu 110-GHz spectrum analyzer. A block diagram of the setup is illustrated in Fig. 10. In the W-band, the input of the setup consists of a signal generator, a multiplier-by-six

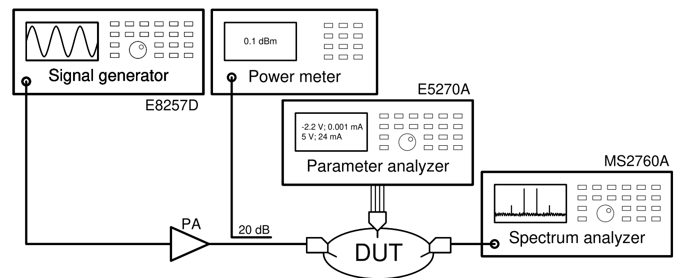

Fig. 10. Simplified block diagram of the large-signal single-tone setup including measurement of the harmonic contributions.

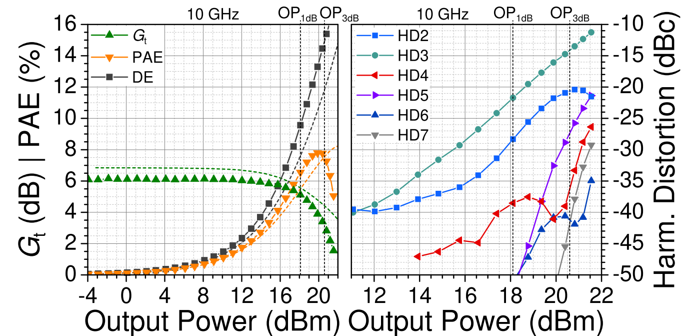

Fig. 11. Measured single-tone CW large-signal performance as a function of the fundamental P_{out} at an input frequency of 10 GHz.

module, and a waveguide amplifier module. The signal chain provides an input power (P_{in}) of up to 18 dBm. The output signal is damped by a 10-dB waveguide attenuator before it is measured by a waveguide power sensor. The two-tone setup contains two coupled signal generators at the input. The two 10-MHz-separated signals are combined by a coaxial power combiner. The output signal is again measured by an Anritsu 110-GHz spectrum analyzer.

Fig. 11 shows a power sweep at an input frequency of 10 GHz. The small-signal G_t is 6.1 dB. The P_{out} at 1- and 3-dB compression ($OP_{1\,dB}$ and $OP_{3\,dB}$) is in excess of 18 and 20 dBm, respectively. $OP_{3\,dB}$ is also considered as P_{sat}. The second harmonic distortion (HD2) at $OP_{1\,dB}$ and $OP_{3\,dB}$ is approximately −28 and −21 dBc, respectively. It is interesting to mention that the third harmonic distortion (HD3) is above HD2 and does not show the compression behavior HD2 shows in the range of P_{sat}. Close to saturation, a similar trend is also shown for the other harmonics so that, at least at an input frequency of 10 GHz, the odd harmonics are stronger than the preceding even harmonics.

The large-signal performance versus frequency is shown in Fig. 12. The Y-axis gives the provided P_{in} and the colored contour presents the measured P_{out}. The black dashed lines indicate the G_t compression at different levels. The DA exhibits an $OP_{1\,dB}$ of 17.9–20.2 dBm. The $OP_{3\,dB}$ is approximately 3 dB higher and lies between 20.6 and 22 dBm.

Figs. 13 and 14 compare the bias dependence of different linearity characteristics. $OP_{1\,dB}$ shows almost no V_{ds} dependence, but a much stronger I_d dependence. $OP_{3\,dB}$ exhibits as well a stronger improvement with I_d, but also a minor V_{ds} dependence. Furthermore, the variation of $OP_{3\,dB}$ is not as strong as for $OP_{1\,dB}$. HD2 shows a stronger bias dependence as compared to HD3. This is especially true for I_d and less

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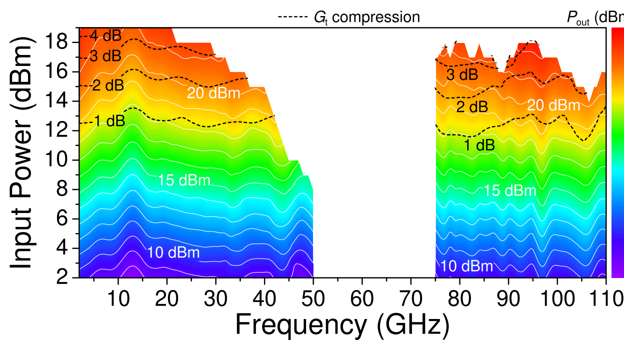

Fig. 12. Contour plot of the measured P_{out} as a function of operating frequency and input power, which are varied in steps of 1 GHz and 1 dB, respectively. White solid lines illustrate the contour of the measured P_{out}. Black dashed lines show an overlay of the G_t compression contour. White areas indicate the limits of the test capabilities.

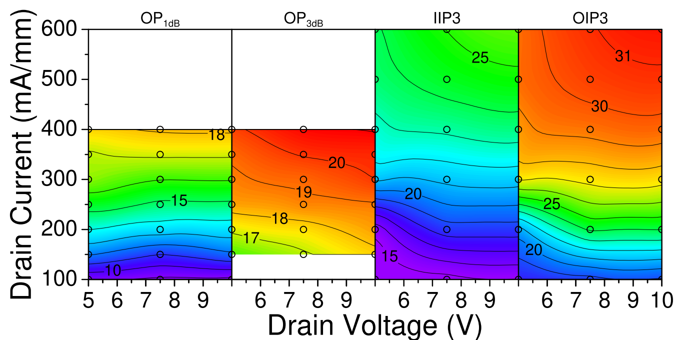

Fig. 13. Contour plot of the measured single-tone CW $\mathrm{OP1}_{1\,\mathrm{dB}}$ and $\mathrm{OP}_{3\,\mathrm{dB}}$ and two-tone OIP3 over V_{ds} and I_d at an operating frequency of 10 GHz. The black circles denote the bias points of the actual measurements.

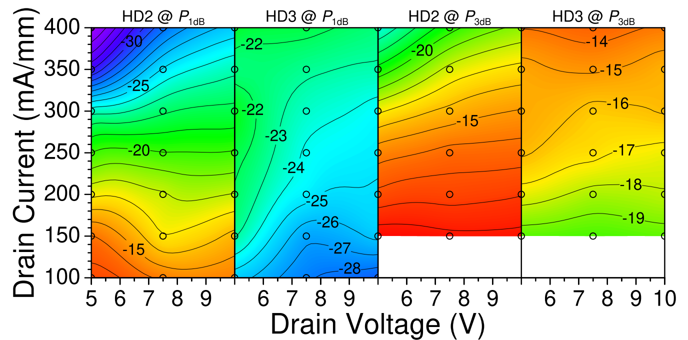

Fig. 14. Contour plot of the measured single-tone CW HD2 and HD3 at $P_{1\,\mathrm{dB}}$ and $P_{3\,\mathrm{dB}}$ over V_{ds} and I_d at an input frequency of 10 GHz. The black circles denote the bias points of the actual measurements.

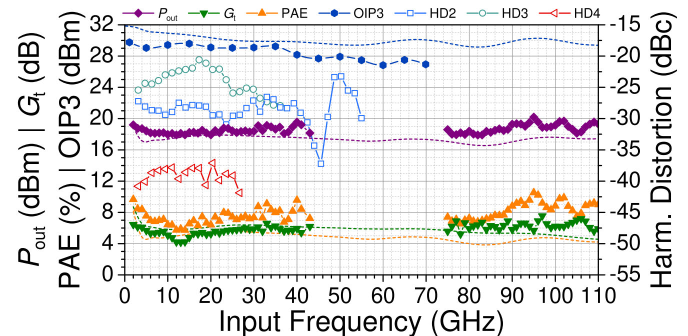

Fig. 15. Measured single-tone CW large-signal performance at $P_{1\,\mathrm{dB}}$ and OIP3 as a function of input frequency.

for V_{ds}. For instance, at 1-dB compression, HD2 improves from values in the range of −15 dBc, at 100 mA/mm, to values up to −30 dBc, at 400 mA/mm. It is important to mention that HD3 has an inverse bias dependence as HD2. Thus, a high I_d results as well in a high third harmonic content, leading to a general tradeoff. While second and third harmonic contents can be roughly at a similar power level, high or low drain currents pronounce more HD3 or HD2, respectively. IIP3 and OIP3 follow similar trends as HD2. As already predicted in Section II, IP3 shows only a minor V_{ds} dependence, but a strong influence by I_d. For a convenient comparison between the dc-based theoretical analysis and actual measurements, the IP3 values that are shown in the contours of Fig. 13 are also plotted in Fig. 3.

Finally, Fig. 15 shows the measured and simulated performance versus frequency of P_{out}, G_t, the power-added efficiency (PAE), and several harmonics at $P_{1\,\mathrm{dB}}$, in addition with OIP3. Up to 70 GHz, OIP3 is between 26.8 and 29.8 dBm.

V. Discussion

Comparing the IP3 values predicted simply by dc measurements of a single HEMT and measurements of the fabricated DA MMIC (as presented in Fig. 3) shows an excellent agreement. This is especially interesting since predicting an RF performance based on dc parameters is, commonly, considered rather challenging. This is even more the case for GaN HEMT technologies where LF dispersion is assumed to be considerably distinct. Also beyond investigations in this work, one might expect that the same set of equations leads to a similar good prediction for other technologies. The comparison between the two analytical approaches demonstrates the clear value of the improved equation with added cross terms as presented in [3]. As intended, the prediction of $\mathrm{AIP3}_k$ and $\mathrm{OIP3}_k$ at a high I_d is much closer to the measured values of the fabricated circuit. It is especially remarkable, how close the calculated and measured IP3 is over such a wide bias range. Even though slight deviations between calculated and measured IP3 can be observed in some cases, the gap is in a similar range as the simulations of the entire MMIC including a large-signal transistor model. In addition, also the simpler equations of $\mathrm{AIP3}_m$ and $\mathrm{OIP3}_m$ are very accurate over a smaller, but still, wide bias range, where the main advantage is that the first and third derivative of g_m is not needed. The simplicity of the required input values in combination with the accuracy of the predicted IP3 demonstrates the major benefit of the presented IP3 investigation and can be a valuable design tool also for other DA MMICs and technologies.

Table I summarizes the measured performance of the fabricated DA MMIC and compares it to state-of-the-art results, realized in different technologies. [2] presents the only GaN-based DA with a BW of above 100 GHz. Thus, the article includes also GaN references with a BW of at least 50 GHz. To the best of the authors' knowledge, this is the first demonstration of an amplifier MMIC with a P_{out} of 20 dBm or more over a 100-GHz BW, independent of the used transistor technology or amplifier topology. Moreover, this work achieves the highest BW among any GaN amplifier. Compared to the only GaN DA with a >100-GHz BW, it is interesting to see that this work exhibits a better NF and the

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TABLE I
OVERVIEW OF STATE-OF-THE-ART DA MMICS WITH >100- GHz BW

Reference, Year	Technology	BW (GHz)	S_{21} (dB)	$P_{dc,q}$ (mW)	*NF* (dB)	$OP_{1\,dB}$ (dBm)	OIP3 (dBm)	P_{sat} (dBm)
[14], (2020)	45-nm RFSOI	102 (2–104)	33	820	3.8–7.5 (<50 GHz)	15.9–21.3 (<70 GHz)	n/a	17.1–23.5 (<70 GHz)
[15], (2023)	InP DHBT	108 (7–115)	av 16	n/a	n/a	12.5–22 (<110 GHz)	n/a	16–24 (<110 GHz)
[4], (2017)	50-nm InGaAs mHEMT	119 (0–119)	av 19.7	541	2.5–6.4 (<98 GHz)	6.3–15.9 (<110 GHz)	n/a	12.2–20 (<110 GHz)
[16], (2016)	55-nm SiGe BiCMOS	130 (5–135)	5.5–8.5	99	5.5–7.5 (<90 GHz)	8.5 (@20 GHz)	n/a	10.7 (@20 GHz)
[17], (2020)	InP DHBT	159 (1–160)	av 10.5	288	10.1–20 (<110 GHz)	13.5–15.5 (<110 GHz)	n/a	14.6–17.8 (<110 GHz)
[18], (2015)	130-nm SiGe BiCMOS	169 (1–170)	10	108	4–6 (@50–67 GHz)	6.5–8.2 (<60 GHz)	20 (@30 GHz)	9 (<50 GHz)
[19], (2021)	35-nm InGaAs mHEMT	230 (75–305)	>17.5	500	n/a	n/a	n/a	10–14.9
[20], (2015)	250-nm InP DHBT	235 (2–237)	16 (14–18)	117	9–12.5 (<195 GHz)	n/a	n/a	n/a
[21], (2019)	250-nm InP DHBT	241 (1–242)	10	387	n/a	10 (@10 GHz)	n/a	10.5 (@10 GHz)
[22], (2023)	35-nm InGaAs mHEMT	150 (50–200)	>14	1075	5.1–11.6	8.2–9.7	18.4–25.2 (<165 GHz)	14.8–19.5
		252 (28–280)	>19.8	122	2.9–6.6 (<205 GHz)	2–8.2 (<220 GHz)	11.5–19.7 (<165 GHz)	8–10.7 (<220 GHz)
[5], (2021)	35-nm InGaAs mHEMT	314 (1–315)	av 14.1	128	2.3–10.9 (<308 GHz)	8.2–9.7 (<110 GHz)	15.4–18.8 (<50 GHz)	8.7–14.8 (<250 GHz)
		334 (1–335)	av 11	77	3.9–9.2 (<308 GHz)	6.8–8.5 (<110 GHz)	17.1–20.3 (<50 GHz)	6.4–11.5 (<250 GHz)
GaN >50 GHz								
[3], (2021)	90-nm ScAlN/GaN HEMT	65 (0.04–65)	10.8–13.9	4800	1.9–5.5 (<50 GHz)	n/a	34.1–37.6 (<45 GHz)	n/a
[2], (2016)	40-nm GaN HEMT	56 (1–57)	av 14.5	828	1.4–5.2 (<39 GHz)	22.5 (@20 GHz)	n/a	26 (@20 GHz)
		80 (5–85)	av 9.8	396	4–5.1 (<39 GHz)	24 (@20 GHz)	n/a	25.3 (@20 GHz)
		120 (5–125)	av 7.3	448	4.8–6.8 (<39 GHz)	15.5 (@20 GHz)	n/a	19.4 (@20 GHz)
This work*	70-nm GaN HEMT	127 (2–129)	av 6.7	720	3.1–5.7	17.9–20.2	26.8–29.8	20.6–22

* Single-tone power and *NF* are given for frequencies of up to 110 GHz; OIP3 up to frequencies of 70 GHz.

gain is almost identical, even though in [2] an RF cascode is used. In comparison to other technologies, this work shows an excellent *NF*, where only dedicated low-noise technologies show a better noise performance. However, these technologies yield a much lower P_{out} and linearity. As discussed in Section V, the on-wafer dc shunt capacitors are limited, which leads, in the presented work, to a 2-GHz lower band edge of the MMIC. Nevertheless, the MMIC features separate pads in the gate and drain line that are prepared to connect an LF extension, as described in [23]. This allows the extension of the performance close to dc without affecting the presented RF performance.

VI. CONCLUSION

This article demonstrates the first amplifier MMIC with a P_{out} of more than 20 dBm over a >100-GHz BW. The presented eight-cell DA MMIC is fabricated in a GaN-on-SiC HEMT technology and exhibits an average gain of 6.7 dB with a 3-dB BW ranging from 2 to 129 GHz. Furthermore, the measured *NF* is between 3.1 and 5.7 dB (<110 GHz). The measured OIP3 is between 26.8 and 29.8 dBm (<70 GHz). In addition to the DA MMIC, this work presents as well an IP3 investigation based on measured dc transfer characteristics and compares two possibilities to calculate the bias-dependent IP3 behavior. The achieved equations for AIP3 and OIP3 can be used as design tools for DAs before the actual circuit design, also using other semiconductor technologies than GaN HEMTs.

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