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InP DHBT Linear Modulator Driver With a 3-Vppd PAM-4 Output Swing at 90 GBaud: From Enhanced Transistor Modeling to Integrated Circuit Design

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***Abstract*—In this article, we report on the modeling, design, and characterization of indium phosphide (InP) double heterojunction bipolar transistor (DHBT) devices and integrated circuits (ICs) for next-generation optical communications. Critical aspects of transistors' modeling and their influence on the IC design are detailed, as well as the design and characterization of a lumped linear modulator driver featuring a 3-Vppd four-level pulse-amplitude modulation (PAM-4) output swing at 90 GBaud (GBd). In particular, we propose an electromagnetic (EM) simulation-based parasitic extraction method of the DHBT access structures, to refine the DHBT and IC performance prediction accuracy. It is shown to provide a better estimation of a canonical cascode gain and μ stability factor at millimeter-wave frequencies, as well as a better estimation of the driver IC gain in the 50–110 GHz frequency range. Furthermore, a high-frequency gain boosting (self-peaking) topology, based upon an emitter-degenerated paralleled-transistor cascode configuration, is analyzed using a simplified transistor model and leveraged to enhance the linear driver output-stage gain–bandwidth product with controlled amount of peaking gain. This self-peaking technique is shown to be inherent to cascode structures and can therefore be used with other technologies, with no added design complexity. The driver IC was implemented in a 0.5-μm InP-DHBT technology and features a bandwidth well in excess of 110 GHz, with 13 dB of peaking gain at 95 GHz. Besides, it achieves a 9.1-dBm single-ended output power at 1 dB of gain compression and a 2.7% root-mean-square total harmonic distortion (rms-THD) at a 3-Vppd output swing. The driver power consumption is 0.67 W, which is among the lowest in the state of the art and shows a 1.5-GBd driver figure of merit (FoM). To the best of our knowledge, this driver achieves the highest ≥64 GBd PAM-4 performances reported to date, without digital signal processing (DSP) or postprocessing.**

***Index Terms*—Four-level pulse amplitude modulation (PAM-4), high-speed integrated circuits (ICs), indium phosphide (InP) double heterojunction bipolar transistor (DHBT), large-swing linear modulator driver, Tb/s optical communications.**

Manuscript received 22 March 2023; revised 26 June 2023; accepted 29 July 2023. This work was supported in part by the European Commission through the H2020 ICT 2016-2017—Photonics Key Enabling Technologies (KET) QAMeleon, H2020-ICT-2018-2 TERIPHIC and H2020-ICT-2019-2 TWILIGHT projects, which are initiatives of the Photonics Public Private Partnership. *(Corresponding author: Romain Hersent.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2023.3305150.

Digital Object Identifier 10.1109/TMTT.2023.3305150

I. Introduction

In THE recent decades, the demand for communication traffic has exploded. This growth is expected to continue as shown by the forecast of massive deployment of 5G and beyond-5G mobile networks, the Internet of Things (IoT), cloud computing, and data centers [1]. As a consequence, all segments of optical networks face an urgent need to increase transmission capacities. Different challenges must be faced to meet this enormous traffic growth, respecting criteria like spectral efficiency, reach, complexity, power consumption, and cost. Intensive research is deployed to explore various alternatives in optical and electronic technologies, new systems with advanced transmission formats, and digital signal processing (DSP) algorithms, allowing higher transmission rate operations with increased spectral efficiency. In this context, multilevel coded transmission and m-ary quadrature amplitude modulation (m-QAM) are of particular interest [2].

The need for high-speed optical interfaces is driving research toward higher-and-higher symbol-rate all electronically generated signals, in order to minimize the number of parallel optoelectronic transmitters and receivers. The design of electronic integrated circuits (ICs) compatible with multilevel modulation formats brings additional requirements compared to circuits (only) operating in on-off keying (OOK) regimes. Not only high analog bandwidth should be achieved but also linearity should be maintained in order to ensure sufficient signal-to-noise ratio (SNR). As a consequence, although OOK-only operating circuits can benefit from compression in order to improve signal SNR [3], [4], the ICs operate in

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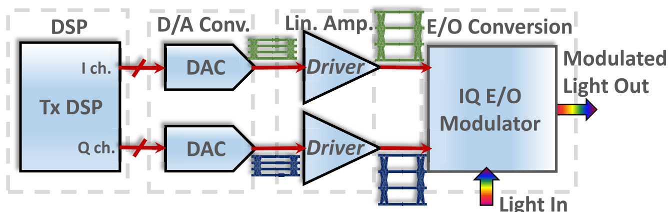

Fig. 1. Simplified digital coherent optical fiber transmitter block diagram.

the linear mode with limited distortion to support 4-/8- and above-pulse amplitude modulation (PAM) formats. To satisfy circuit specifications and preserve signal integrity, adequate methodology needs to be used, in particular linearized differential architectures (e.g., resistive emitter degeneration), controlled use of equalization techniques (e.g., inductive peaking), and very careful layout implementation. The design of linear electro-optical modulator drivers yet entails additional challenges related to the modulator characteristics. Among those, are their rather low input impedance that corresponds to the driver load, whereas the required driving swing (V_π) is conversely high.

To date, Mach–Zehnder modulators with record performances have shown 1.5–2.3 V V_π with 80-GHz bandwidth and 25–50 Ω (single-ended) impedances [5] and [6]. However, commercially available technologies tend to show over-3-Vppd V_π, thus requiring increased driver output swing, and much lower electro-optical bandwidth [7], [8], [9], [10], with losses well in excess of 6 dB beyond 60 GHz. Additionally, the interconnections between the driver and modulator also generate high-frequency losses and impedance mismatching which cause significant bandwidth degradations (see Fig. 1). To limit the use of power-hungry DSP, linear drivers with gain peaking can be used to compensate for the modulators' limited bandwidth, while providing large linear output swings. Such continuous-time linear equalization can thus prevent intersymbol interferences (ISIs) and preserve signal integrity. Besides, to facilitate its system integration and ease thermal dissipation of packaged devices, the driver power consumption should be kept well below 1 W per channel.

One technique for the design of broadband and large-output-swing modulator drivers is the distributed amplifier architecture [11]. Indium phosphide (InP) double heterojunction bipolar transistor (DHBT), silicon germanium (SiGe) bipolar-CMOS (BiCMOS)-, and silicon complementary metal oxyde semi-conductor (Si CMOS)-distributed linear drivers are, respectively, presented in [12], [13], and [14]. Beyond 100 GHz bandwidth with over 3 Vpp output swings has been achieved, while dissipated powers remain below 1 W. However, published PAM-4 signals cap at 56 GBd and none provide equalization capabilities. For a given technology, the main drawback of this approach is the inherent large footprint and subsequent integration challenges. On the other hand, lumped-architecture linear drivers implemented in InP DHBT technologies have already demonstrated bandwidths in excess of 80 GHz and large output swings, while featuring analog equalization (peaking gain) and limited power consumption. In [5], an over-110-GHz InP-DHBT with 1.5-Vppd 8-dB peaking gain analog multiplexer driver with a 0.99 W power consumption enables a 168-GBd 16-QAM optical transmission. The corresponding driver figure of merit (FoM) [as defined in (3) of this article] is 0.45 GBd. However, power-hungry DSP is required to reach this performance. The InP-DHBT linear driver presented in [15] has an 86.8 GHz bandwidth, 4.1 dB of peaking gain, and a 4.9-Vppd PAM-4 output swing at 50 GBd, yielding a 1.52 GBd FoM. Besides, in [16], a 106 GHz bandwidth linear driver with 6.2 dB peaking gain is reported, having a 3-Vppd PAM-4 linear output swing at 80 GBd, resulting in a 1.22 GBd FoM without DSP.

In this article, we present the design, modeling, and characterization of a lumped linear modulator driver implemented in III-V Lab's 0.5-μm InP DHBT technology. Compared to our previous works [15] and [16], this driver shows higher bandwidth, peaking gain, FoM, PAM-4 symbol rate, and linear dynamic at lower power consumption (see Table I). This article is an expanded version from the IEEE 2021 BiCMOS and compound semiconductor integrated circuits and technology symposium (BCICTS) paper [17].

This article is organized as follows. The main features of the InP DHBT technology and the transistor modeling are presented in Section II, along with the state-of-the-art of the high-speed transistor technologies. In particular, in Section II-B, the proposed InP DHBT modeling approach is detailed. It is shown to prevent the "over-deembedding" typically associated with the standard S-parameter measurement deembedding, resulting in a significant improvement of the high-speed IC gain prediction, both in small- and large-signal regimes (see Section IV). It is also shown that failing to account for the external parasitics in the DHBT model may cause overdimensioning (e.g., gain peaking, transistor bias) during the IC design phase and/or result in unexpected IC performance degradations (see Sections III and IV). The InP-DHBT linear driver design, architecture and simulation methodology are detailed in Section III. More specifically, several driver output stage amplifying cells are compared, and bandwidth enhancement is achieved in using the high-frequency gain boosting capability (later called self-peaking) of a paralleled-transistor resistively degenerated cascode differential pair. To the best of our knowledge, this self-peaking mechanism has not yet been explored in the literature and is analyzed in this article, in using a simplified transistor model to provide designers with more insight on the stemming bandwidth boosting capability. As a result, we show that self-peaking is inherent to the cascode architecture (with resistive emitter degeneration) and can therefore be used with various technologies, with no added complexity to the design. The influence of the InP-DHBT model precision on the driver design is also presented in Section III. Compared to previous works [15], [16], [17], the simulation methodology is improved, as presented in Section III-D, resulting in better IC performance prediction, as shown along with the InP-DHBT linear driver small- and large-signal characterisations in Section IV. Then in Section V, the proposed linear driver performances are compared to the state-of-the-art. Finally, Section VI concludes this article.

The 0.5-μm InP-DHBT driver shows a 3-Vppd linear output swing while operating at 90 GBd in PAM-4. The measured bandwidth is well in excess of 110 GHz with a 13-dB peaking

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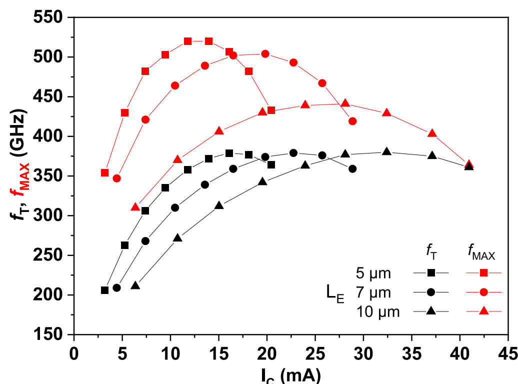

Fig. 2. 0.5-μm InP DHBT f_T and f_{MAX} versus collector current, I_C, at $V_{CE} = 1.6$ V, for the three available emitter lengths in the process.

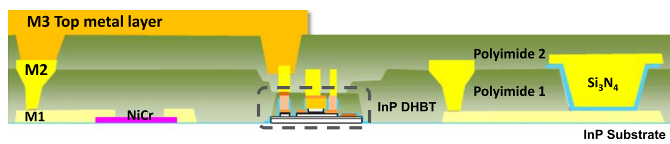

Fig. 3. 0.5-μm InP DHBT process' cross-sectional schematic.

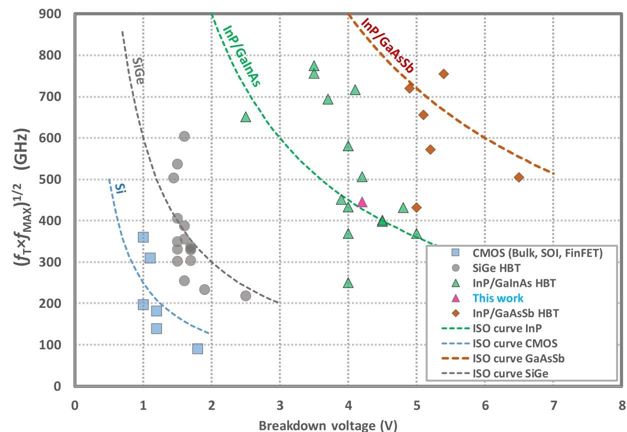

Fig. 4. High-speed technologies state of the art. The devices' cutoff frequency (in the form of f_T and f_{MAX} geometrical mean) is plotted versus their breakdown voltage (BV_{CE0}, V_{DD}). Green triangles refer to InP/GaInAs DHBTs and brown diamonds to InP/Ga(In)AsSb devices [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34]. SiGe BiCMOS and HBTs are plotted in gray circles [35], [36], [37], [38], [39]. Blue rectangles refer to Si CMOS technologies [40], [41]. For each technology, an indicative trend is plotted. Deviations from the trends appear due to process structural differences in terms of vertical profile and 2-D geometry, e.g., lower emitter widths for HBTs yield f_{MAX} improvements via parasitic reduction.

gain at 95 GHz. At a 3-Vppd output swing, the measured rms-THD is 2.7%, at 1 GHz.

II. InP DHBT Technology and Model

A. InP-DHBT Process and Performances

The 0.5-μm InP DHBT frequency performances are displayed on Fig. 2 versus the collector current, I_C, for the three available emitter lengths in the process (5, 7, and 10 μm). At $V_{CE} = 1.6$ V and $J_C \cong 7$ mA/μm^2, 0.5 μm × 5 μm devices feature 380- and 520-GHz peak f_T and f_{MAX}, respectively. The common-emitter breakdown voltage, BV_{CE0}, is 4.2 V (at a 0.05-mA/μm^2 collector current density, J_C). Besides, the DHBTs show an over 30 maximum static current gain (β). The InP DHBTs are integrated in a full circuit process which requires about 20 lithography steps. Fig. 3 depicts the process' cross-sectional view. This technology provides 40-Ω/square nichrome (NiCr) thin-film resistors and silicon nitride (SiN) metal–insulator–metal (MIM) capacitors, as well as three Au-based metalisation levels for interconnections. As shown in Fig. 3, the DHBT can be interconnected using the M2 level. For more information about this process, see [17] and [18].

Fig. 4 depicts the high-speed technologies state of the art [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], and [41], in comparing the tradeoff between f_T, f_{MAX}, and the breakdown voltage (BV_{CE0} for HBTs, V_{DD} for CMOS), which are key metrics for IC design. Note that f_{MAX} and BV_{CE0} are not systematically determined in using similar conditions and criteria [41], [42]. Additionally, reported results cover both cutting-edge research processes, which may not (yet) be fully compatible with high-speed IC design and more mature processes which imply different optimization targets and yield constraints. Fig. 4 shows a clear advantage of InP DHBTs over silicon-based technologies for the design of high-symbol-rate and large-output-swing ICs, as they achieve very high cutoff frequencies with large BV_{CE0}. In [25], InP DHBTs' high BV_{CE0} and early voltage as well as their gradual safe operating area limit are regarded as the main sources of superior linearity and output power in comparison to SiGe HBTs, in >100-GHz bandwidth power amplifiers, making InP DHBTs strong candidates for the design of large-swing modulator drivers.

Most InP DHBTs use either (type-I) InP/gallium–indium–arsenide (GaInAs) or (type-II) InP/gallium–arsenide–antimonide (GaAsSb) heterojunctions. As shown in Fig. 4, recent work on type-II devices has shown best-in-class performances, with proven capabilities for the design of large-swing modulator drivers (see [4] and [43]). Yet, to date, these processes show lower maturity compared to type-I technologies. The III-V Lab technology not only aims at high performances (see Fig. 4) but also targets high yield, reliability, and large output swing, which translates into higher constraints with respect to pure research processes. It allows the monolithic integration of few hundreds of DHBTs for the design of high-speed and high-performance ICs (see [3], [11], [18], and [44]).

B. InP DHBT Modeling

As the circuit operating frequencies are being pushed well into the millimeter-wave frequency range, it becomes progressively more important to accurately model the parasitic effects associated with the complete device structure. Though attempts have been made, e.g., [45], to extract these parasitic effects for InP DHBTs directly from on-wafer measured S parameters at high frequencies, this approach is of limited accuracy. This is not only due to the uncertainty associated with measured S parameters at high frequencies but also due to the fact that the parasitic elements model of standard deembedding procedure tends to overestimate the device parasitics. This process is often referred to as "over deembedding (ODmbD)". A more reliable approach for device

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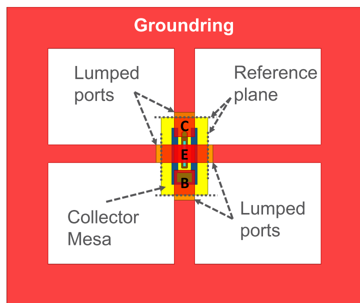

Fig. 5. Top-down view of *Ansys HFSS* 3-D EM model of the complete triple mesa InP DHBT structure with surrounding groundring. The reference planes for the device model are indicated by dashed lines. For clarity, the outer airbox and substrate layers are not shown.

parasitic effect extraction is based on electromagnetic (EM) simulation of the complete structure as reported for thin-film microstrip-connected transferred-substrate InP DHBTs in [46]. For the coplanar waveguide-connected triple-mesa InP DHBTs considered in this work, the EM simulation-based extraction approach is refined. The *Ansys HFSS* 3-D EM model of the complete triple-mesa InP DHBT structure is shown in Fig. 5. In this model, lumped ports (orange sheets) referenced to a surrounding groundring excite the transistor structure at its base–collector and emitter terminals. The groundring is implemented in M2, similar to that used at the external device access planes (see Fig. 3). The parasitics associated with the lumped ports and the surrounding groundring are removed by the L–2L calibration procedure [47] as these would otherwise mask the small-value parasitic elements of the device structure itself. In the EM model, the active part of the InP DHBTs is either short circuited or left open circuited. In the short-circuited device, the base, the emitter, and the collector are all connected together using a shorting bar. In the open-circuited device, the semiconductor layers within the active part are substituted by low dielectric constant ($\varepsilon_r \ll 1$) artificial materials. This allows the junction capacitances to be correctly allocated to the intrinsic device during the subsequent large-signal model parameter extraction procedure. Both structures are meshed at 325 GHz using an initial wavelength-based mesh setting of 0.03 λ. The skin effect due to the field penetration into conductors is accurately captured by employing an initial mesh seeding and solving for the fields inside the conductors. First, the simulated open- and short-circuited 3-D EM models allow frequency-dependent effective capacitances and effective inductances, respectively, to be extracted. The frequency-dependent effective capacitances are modeled by distributing frequency-independent capacitances along the device structure, following the straightforward iterative procedure described in [46]. For the triple-mesa DHBT structures considered here, the external parasitic network takes on the rather complicated form as shown in Fig. 6. Second, in this model, frequency-dependent impedances are defined as in the following equation:

$$Z_{\mathrm{pb}(e,c)}(f) = R_{\mathrm{pb}(e,c)}|_{f\to 0} + R_{\mathrm{pb}(e,c),\mathrm{ac}} \cdot \sqrt{f} \cdot (1+j) \quad (1)$$

where f is the frequency, $R_{\mathrm{pb}(e,c)}|_{f\to 0}$ are dc resistances, and $R_{\mathrm{pb}(e,c),\mathrm{ac}} \cdot \sqrt{f} \cdot (1+j)$ are terms describing the ac impedance

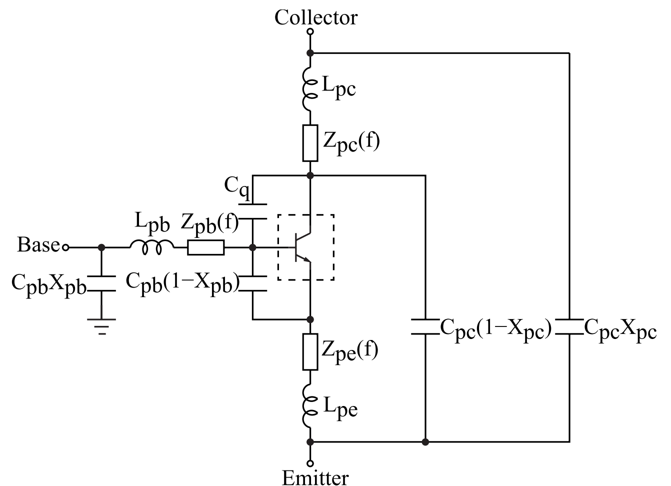

Fig. 6. Proposed large-signal model structure for InP DHBTs including external parasitics. The dashed box contains the InP DHBT intrinsic part modeled using the modified UCSD HBT model [48].

due to the field penetration into the conductors. The calculated skin depths at 1, 10, and 100 GHz are 2.76, 0.87, and 0.28 μm, respectively. This formulation of the skin effect is known to lead to a causal model response [49].

While comparing the S parameters of the obtained DHBT models, with and without considering the external parasitics' impact, with the device measurements, it is difficult to estimate the accuracy of one model over the other. This is because the standard deembedding procedure wrongly removes important parasitic effects from the device data, which is reflected in a simpler, but erroneous, model structure, leading to "ODmbD." Hence, to illustrate the InP DHBT external parasitic element modeling importance for high-symbol-rate linear driver designs, a canonical cascode configuration, as depicted in Fig. 7, is considered. For simplicity, only the dominating external parasitic elements are shown. The collector–emitter and base–collector capacitances of the common-emitter stage have been neglected due to the low impedance level at the common-emitter/common-base interstage node. This allows the parasitic collector access impedance to be added to the parasitic emitter access impedance of the common-base stage. Besides, the common-base stage parasitic collector access impedance is not considered as it can easily be absorbed into any load peaking network and will not greatly influence the maximum stable gain (MSG) or maximum available gain (MAG). Fig. 8 depicts the MAG/MSG and geometrically derived stability factor, μ, simulation comparison up to 325 GHz for the cascode configuration with and without external parasitic elements. The external parasitic elements cause an MSG reduction, already from low frequencies to about 220 GHz. At 110 GHz, the MSG already experiences an about 3.5-dB simulated discrepancy. This low-frequency MSG reduction originates from the common-base stage's collector–emitter capacitance, as also discussed in [50]. Above 178 GHz, the μ stability factor of the cascode configuration without parasitic elements rises above one, thus ensuring unconditional stability with a change in gain slope going from MSG to MAG. The cascode configuration with parasitic

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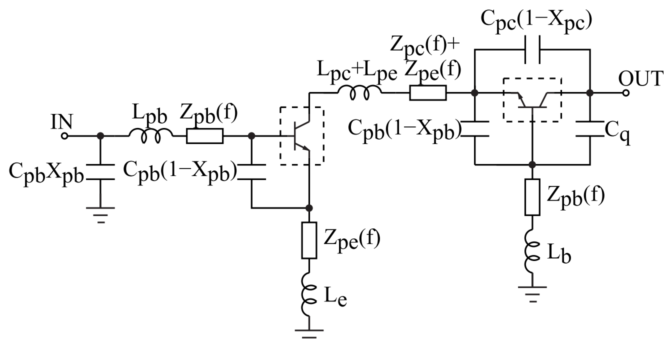

Fig. 7. Simplified schematic of the cascode configuration showing dominating parasitic elements (bias details not shown). The dashed boxes contain the intrinsic part of the InP DHBTs modeled using the modified UCSD HBT model [48].

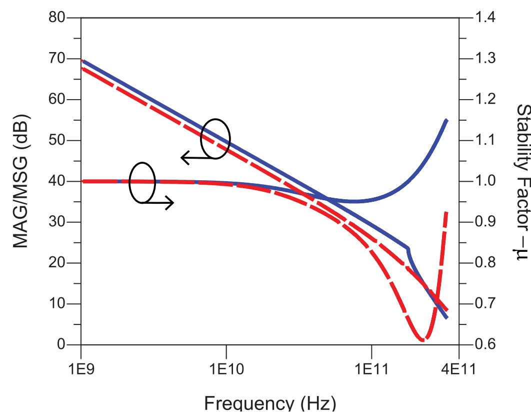

Fig. 8. Simulation comparison of MAG/MSG and the μ stability factor for the cascode configuration with (red broken curves) and without (blue solid curves) external parasitic elements.

elements, on the other hand, remains conditionally stable with a μ below one at all simulated frequencies. The external parasitic elements' influence on the DHBT's gain and stability, at higher millimeter-wave frequencies, will be shown to cause a strong gain discrepancy of the high-symbol-rate 0.5-μm InP-DHBT linear driver, both for small- and large-signal operations (see Section IV).

III. InP-DHBT Linear Driver Design

A. InP-DHBT Linear Output Stage Optimization

InP-DHBT-based multiple-paralleled-transistor cascode differential pairs with emitter resistive degeneration can combine very high gain–bandwidth product with large linear output swings, as shown in [15], [16], and [17]. However, for a given linear output swing and a given technology, the paralleled transistors' number and their dimensions should be carefully chosen for optimum performance. Indeed, using numerous smaller transistors may ease thermal management, as heat sources are spread on a larger area, yet it implies higher routing complexity that may alter signal integrity and limit maximum operating speed. Contrariwise, larger DHBTs show reduced frequency performances, especially regarding f_{MAX} (see Fig. 2). Additionally, a high number of paralleled transistors tend to alter signal integrity due to input, respectively output, parasitic capacitances' summation, which degrades the

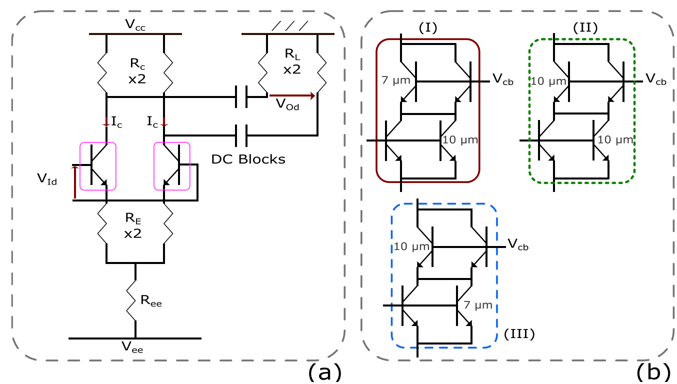

Fig. 9. Driver's output-stage amplifying cell performances' comparison. (a) Resistively degenerated cascode differential pair test structure schematic. (b) Paralleled-transistor amplifying cells' schematics. (c) Amplifying cells' small-signal differential gain comparison versus frequency. R_{E} is swept using a 5-Ω step, from 0 to 25 Ω. (d) Cascode configurations' large-signal differential static voltage input–output characteristic comparison. R_{E} is swept using a 5-Ω step from 0 to 25 Ω.

input, respectively output, impedance matching, and thus limit the achievable bandwidth. Hence, as shown in [15], [16], and [17], a two-paralleled-transistor cascode yields a good tradeoff between linear output swing, gain–bandwidth product, impedance matching, and power consumption.

1) Amplifying-Cell Comparison: Fig. 9 depicts a simulation comparison of three amplifying cell configurations based on a two-paralleled-transistor degenerated differential cascode [see Fig. 9(a) and (b)], implemented in the III-V Lab technology. In the amplifying-cell optimization discussion, the DHBT model does not account for the small-value external parasitics, in order to simplify the discussion and provide more insight on the mechanism at stake. Note that in III-V Lab process design kit (PDK), three DHBT emitter lengths are available (5, 7, and 10 μm). All DHBTs are biased at a 1.6 V V_{CE} and a 20 mA I_{C}, close to the 7- and 10-μm devices' f_{T} and f_{MAX}

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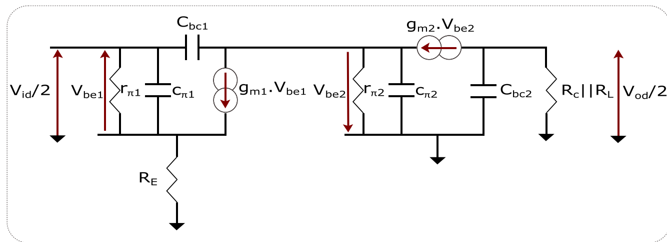

Fig. 10. Resistively degenerated cascode differential pair half-circuit small-signal equivalent circuit based on a simplified DHBT model.

peaks, while the tail resistance, R_{ee} in Fig. 9(a), is modified according to the degeneration resistance sweep, R_E, to keep bias conditions unchanged. Fig. 9(c) and (d), respectively, depicts the three amplifying cells' simulated differential small-signal gain versus frequency and large-signal voltage static transfer function, while R_E is swept from 0 to 25 Ω with a 5 Ω step. Using 7- and/or 10-μm emitter length, L_E, and 0.7-μm emitter width, W_E, DHBTs, an over 3-Vppd linear output swing (plus back-off) and a beyond-2-THz gain-bandwidth product can be conjugated. Note that 5-μm devices were not considered as at least three devices are required to maintain linearity at a 3-Vppd output swing, which may not be optimal in terms of signal integrity due to parasitics summation and higher routing complexity, as previously discussed. One can note that all three topologies achieve comparable large-signal performances, while the gain–bandwidth product of the 10-μm-L_E degenerated common-emitter 7-μm-L_E common-base cascode configuration [denoted (I) in Fig. 9(b)] is, respectively, 50 and 210 GHz higher than those of (II) and (III). This is achieved in benefiting from the resistively degenerated InP-DHBT-based paralleled-transistor cascode high-frequency gain boosting (later referred to as self-peaking), to design a large-linear-output-swing high-gain–bandwidth-product driver output stage. The self-peaking mechanism is theoretically analyzed in Section III-A2.

2) Analysis of the Self-Peaking for Bandwidth Boosting: The traditional cascode implementation enhances the bandwidth through minimizing the degenerated common emitter (CE) transistor voltage gain with a common-base (CB) transistor load, whose input impedance is designed as close as possible to the inverse of the common-emitter DHBT's transconductance. This often necessitates both transistors' dimensions to be alike. However, even higher performances can be obtained in benefiting from the cascode self-peaking effects, in leveraging the synergy between the paralleled-transistor cascode and resistive emitter-degeneration. As shown in Fig. 9, this may require the degenerated common-emitter and common-base transistors to be designed with different geometries (W_E, L_E).

$$A_{vd} = A_0 \cdot \frac{\left[1 - j\frac{f}{f_2} + \left(\frac{f}{f_4}\right)^2\right]}{\left(1 + j\frac{f}{f_1}\right)\cdot\left(1 + j\frac{f}{f_3}\right)\cdot\left(1 + j\frac{f}{f_5}\right)} \tag{2a}$$

$$A_0 = -g_{m1} \cdot \frac{K_2}{K_1} \cdot \frac{R_C \cdot R_L}{R_C + R_L} \tag{2b}$$

$$f_1 = \frac{1}{2\pi \cdot \frac{R_C \cdot R_L}{R_C + R_L} \cdot c_{bc2}} \tag{2c}$$

$$f_2 = \frac{g_{m1}}{2\pi \cdot c_{bc1} \cdot K_1} \tag{2d}$$

$$f_3 = \frac{K_1}{2\pi \cdot R_E \cdot c_{\pi 1}} \tag{2e}$$

$$f_4 = \frac{1}{2\pi \cdot \sqrt{R_E \cdot c_{\pi 1} \cdot \frac{c_{bc1}}{g_{m1}}}} \tag{2f}$$

$$f_5 = \frac{g_{m2}}{2\pi \cdot K_2 \cdot (c_{\pi 2} + c_{bc1})} \tag{2g}$$

$$K_1 = 1 + \left(g_{m1} + \frac{1}{r_{\pi 1}}\right) \cdot R_E \tag{2h}$$

$$K_2 = \frac{g_{m2} \cdot r_{\pi 2}}{1 + g_{m2} \cdot r_{\pi 2}}. \tag{2i}$$

This gain–bandwidth product improvement can be analyzed using a basic cascode differential half-circuit model, as depicted in Fig. 10. The degenerated CE and CB transistors' components are, respectively, indexed 1 and 2. c_{bci}, $c_{\pi i}$, $r_{\pi i}$, and g_{mi} represent the base–collector and base–emitter capacitances, the base–emitter resistance, and the transconductance, respectively. R_C and R_L are the collector's back termination and resistive load, respectively. Note that for a given I_C, $g_{m1} \approx g_{m2}$, as the transconductance only slightly varies with the emitter geometry. g_{m1} and g_{m2} may yet differ at high I_C values where other effects become significant (e.g., Kirk effect, thermal, parasitic voltage drop). The differential small-signal voltage gain can be expressed as in (2a). This equation shows that f_2 and f_4 can provide high-frequency gain boosting to enhance the output stage's bandwidth, in mitigating the poles' cutoff frequencies [see (2c)–(2i)]. The cascode self-peaking is obtained in leveraging the effects of emitter degeneration (R_E) and the CE capacitances (c_{bc1}, $c_{\pi 1}$). It, however, necessitates f_2 and f_4 to fall within the frequency band of interest, i.e., to increase f_2 and f_4 denominators, while keeping f_1, f_3, and f_5 unaltered. This can be achieved with a large R_E, however to the detriment of the low-frequency gain, according to (2b). Indeed, as depicted in Fig. 9(c), increasing R_E increases all-three cascode configurations' high-frequency gain (self-peaking) and hence their bandwidths accordingly. Additionally, according to (2b)–(2i), increasing R_E reduces A_0, f_2, and f_4, while f_3 is almost unchanged, and f_1 and f_5 are unaffected. This achieves the expected objectives yet in sacrificing the low-frequency gain (A_0), which is a well-known effect of resistive emitter degeneration.

Nevertheless, to maintain sufficient low-frequency gain while ensuring a sufficient shift of f_2 and f_4 toward lower frequencies, c_{bc1} and $c_{\pi 1}$ may also be increased. Large parasitic capacitances can be achieved in using large DHBT devices, yet potentially to the overall performance detriment, as large DHBTs usually face low frequency cutoff [as defined by (2a) poles]. Another option is to use multiple-paralleled fast transistors and to benefit from the subsequent parasitic capacitances (c_{bc} and c_π) summation. As shown in Fig. 9, this can yield improved high-frequency performances if interconnection parasitics are handled. This litigates for a limited number of paralleled transistors to be used, while transistor

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dimensions need to be carefully considered (see previous discussion). One should, however, note that excessive c_{bc1} and $c_{\pi 1}$ values would decrease f_3 and f_5 and degrade impedance matching with neighboring stages and thus reduce the overall bandwidth.

One can note that configuration (I) shows much higher bandwidth improvement than (II) and (III), especially while $R_E \leq 15\ \Omega$. This is due to the following effects. First, compared to configuration (III), (I) and (II) benefit from increased c_{bc1} and $c_{\pi 1}$, thanks to the 10-μm degenerated CE paralleled devices, which induce more pronounced shifts of their respective f_2 and f_4 toward lower frequencies than that of (III). Additionally, f_5, which accounts for the CB transistor transconductance bypassing under $c_{\pi 2}$ and c_{bc1} actions, is not significantly affected while switching between 7- and 10-μm-L_E (CE) DHBTs. Likewise, while using a 10-μm degenerated CE device as in configurations (I) and (II), f_3's degradation is not significant, with respect to that of (III), as both g_{m1} and $c_{\pi 1}$ are increased, while $r_{\pi 1}$ is reduced. Hence, the expected gain boost provisioned by f_2 and f_4 down shift is not concealed by f_3 and f_5 effects, while 10-μm degenerated CE devices are used to increase c_{bc1} and $c_{\pi 1}$ values. Additionally, compared to (II) and (III), configuration (I) is significantly favored thanks to a lower c_{bc2} [see (2c)] of its 7-μm CB DHBTs, with respect to that of (II) and (III) which are 10-μm devices. Hence, configuration (I) shows higher amplitude self-peaking as it is less concealed by the low-pass filtering of f_1 [see (2c)] than those of configurations (II) and (III). This is even more pronounced that the paralleled-transistor architecture is causing the summation of the CB base–collector capacitances, c_{bc2}. Besides, (III) has a slightly reduced low-frequency gain, as 10-μm transistors have higher $r_{\pi 1}$, and thus lower K_1, than those of the 7-μm devices [see (2b)].

Therefore, in comparison to using R_E only, and trade low-frequency gain for bandwidth enhancement, a better compromise may be achieved in benefiting from the cascode self-peaking. Hence, compared to the standard cascode implementation [e.g., configuration (II) in Fig. 9], for a given bandwidth objective, benefiting from the cascode self-peaking may preserve low-frequency gain, as smaller R_E is required, which yields a higher gain–bandwidth product. Besides, since most current linear driver designs use resistively degenerated cascode architectures to support PAM-4/8 signals, the proposed cascode self-peaking technique can be achieved without additional design complexity. Furthermore, the basic theoretical study of the self-peaking bandwidth enhancement shows that it is inherent to cascode architectures with emitter degeneration and thus allows its implementation with other technologies.

B. Linear Driver Architecture and Design

The proposed InP-DHBT linear driver design aims at compensating for significant modulator losses (≥6 dB at 60 GHz), to support high-symbol-rate operation with limited DSP usage. An over-3-Vppd linear output swing is targeted with a power consumption well below 1 W. The driver implements a fully differential lumped architecture composed of two amplifying stages, a preamplifier and an output stage, as depicted in Fig. 11(a). Other than the input offset controls ($V_{\text{offh/b}}$), separate voltage supplies were used for the preamplifier and output stage in order to provide better control on the circuit and to decrease the driver overall power consumption. An increased number of external controls, however, complicates system integration. Nevertheless, the driver total number of dc supplies and controls remains limited. The InP-DHBT linear driver schematic is shown in Fig. 11(b).

The preamplifier provides input impedance matching, voltage gain, and common-mode rejection, achieved through two stages of emitter followers and a linear differential cascode amplifier that features emitter-resistive degeneration. It also features some inductive peaking to extend the preamplifier bandwidth in improving its impedance matching with downstream stages. Custom emitter degeneration has been implemented using a mixed T-Π configuration. Compared to the standard T configuration, the resulting differential degeneration resistance is R_{E1} in parallel with $R_{\text{dege1}}/2$, while both have an R_{E1} common-mode degeneration resistance. Although slightly complicating implementation, it further improves common-mode rejection and adds an additional degree of freedom in the design. All preamplifier DHBTs are $0.5 \times 5\ \mu\text{m}^2$ devices, thus ensuring a good tradeoff between power consumption and frequency performances. The cascode differential pair tail current is set to 15 mA while emitter followers are biased below 6 mA to limit the overall driver power consumption.

The output stage design leverages the cascode self-peaking bandwidth enhancement discussed in Section III-A. It provides most of the voltage and power gains, as well as output impedance matching and large peaking gain. It is based on a two-paralleled-transistor fully differential cascode architecture with resistive emitter degeneration. The 7-μm-length common-base and 10-μm-length "common-emitter" DHBTs have been used. The differential degeneration resistance, i.e., R_{ee2} in parallel with $R_{\text{dege2}}/2$ [see Fig. 11(b)], was chosen slightly larger than 5 Ω to ensure a combined 3-Vppd output swing (plus back-off) and a high gain–bandwidth product, as shown in Fig. 9. To limit power consumption, a Π-degeneration configuration has been used. The output stage differential cascode pair transistors are biased close to the f_T and f_{MAX} peaks (i.e., about 42 mA per side) to ensure very-high-speed operation while supporting large linear output swings. Besides, inductive peaking is implemented in the output stage [see L_C and L_{cs} in Fig. 11(b)]. These inductances can mitigate some of the driver output capacitance effects and thus improve the output impedance matching, while providing additional gain peaking. L_C inductances have been implemented as high-impedance transmission lines using the M2 metal layer, with large distance to the neighboring M2 ground planes (see Fig. 3). It allows a direct connection to the output coplanar transmission lines and avoids using vias, thus preventing extra layout parasitics and limiting thermal stress. While L_C's width is fixed to limit electromigration that could cause failure, its length optimization is depicted in Fig. 12(a) and (b). The gain and output reflection S parameters, S_{21} and S_{22}, respectively, are simulated from 10 kHz to 160 GHz, based on the driver schematic (no layout parasitic),

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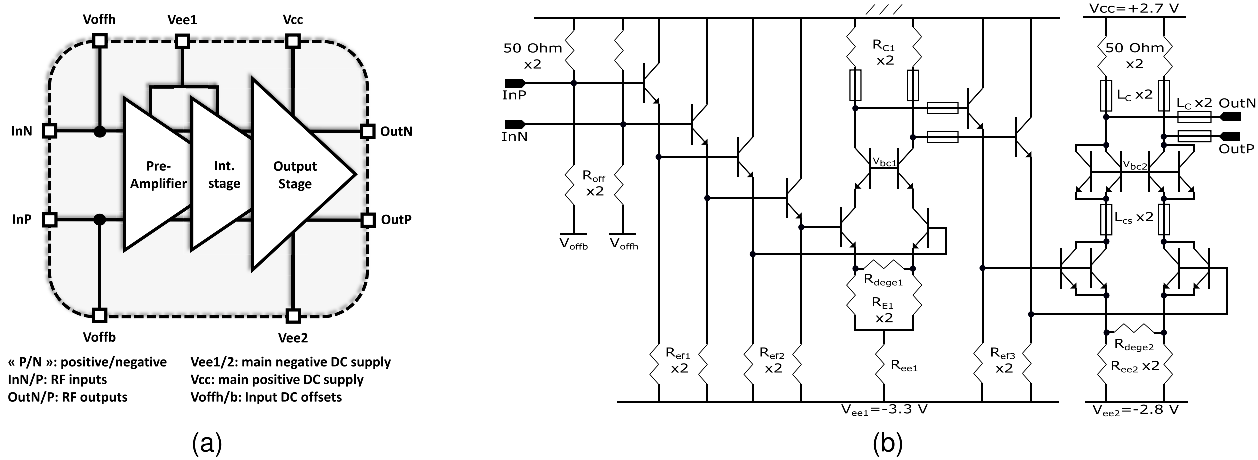

Fig. 11. InP-DHBT linear driver. (a) Block diagram. (b) Schematic.

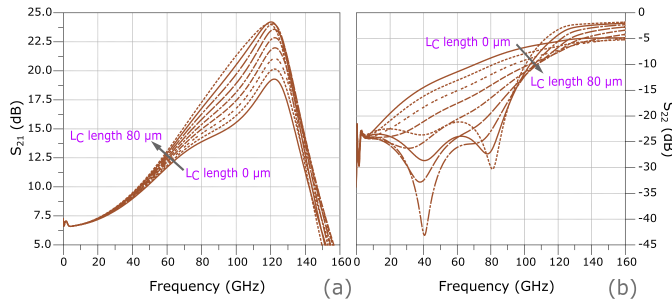

Fig. 12. InP-DHBT linear driver output inductive peaking optimization. L_C's length is varied from 0 to 80 μm with a 10-μm step. (a) S-parameter gain, S_{21}. (b) S-parameter output reflection coefficient, S_{22}.

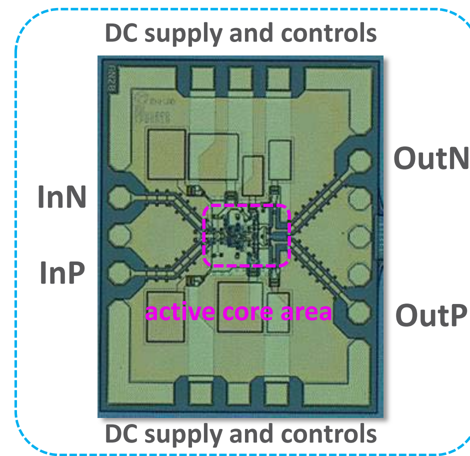

Fig. 13. 0.5-μm InP-DHBT linear driver chip microphotograph.

using the proposed InP-DHBT EM-based model. L_C is shown to have a significant impact on both the driver peaking gain and output impedance matching. Although a significant output impedance matching improvement can be obtained at intermediate frequencies with lengths of 30 μm and beyond, values in excess of 40 μm produce noticeable $|S_{22}|$ degradations above 100 GHz. Excessive high-frequency gain (peaking) and poor impedance matching are not desirable as this may alter the driver performance and stability. As a tradeoff, L_C's length is set to 35 μm, providing about 2-dB extra peaking and about 8-dB improvement in $|S_{22}|$, in the 30–70 GHz frequency range, without noticeable degradations of $|S_{22}|$ at high frequencies.

Furthermore, to improve the overall bandwidth, an emitter–follower stage is interposed between the preamplifier and the output stage to mitigate the capacitive loading introduced by the paralleled-transistor topology on the preamplifier. The 0.5×7-μm^2 DHBTs have been used with a 13-mA tail current to ensure high linearity. Moreover, the driver is biased using voltage sources through resistances, as it reduces power consumption with respect to traditional transistor-based current sources, although it yields lower common-mode rejection and less resilience to power supply, temperature, and resistance variations.

The driver chip microphotograph is shown in Fig. 13. Its dimensions are 1.2×1.5 mm^2 while the core active area is 0.32×0.4 mm^2. On-chip R–C damped decoupling networks have been used to ensure proper biasing of the driver. Finally, the driver core and pads are connected through low-loss coplanar transmission lines to ensure very high bandwidth.

C. InP-DHBT Modeling Technique Comparison

Fig. 14(a) and (b) depicts the impact of the external parasitics on the driver simulated S_{21} and S_{22}, respectively. The driver schematic has been simulated in the same conditions as in Fig. 12(a) and (b) using the DHBT model with "ODmbD" model and the EM-based DHBT modeling. At a given L_C, $|S_{22}|$ experiences some degradations above 70 GHz due to the DHBT external parasitics, while $|S_{21}|$ shows a discrepancy of more than 8 dB at 120 GHz. Furthermore, increasing L_C is expected to provide some bandwidth extension, which is indeed obtained with the ODmbD model. However, Fig. 14(a) shows that when considering the EM-based InP-DHBT modeling, the driver bandwidth is almost unaffected, and increasing L_C only provides more gain peaking then. This can be attributed to the transistors access base inductance [see Fig. 7], and in particular that of the output stage CB DHBTs, which already provides significant gain peaking, compensating for the output capacitance low-pass filtering. Hence, as shown in Fig. 14(a), when the DHBT model does not account

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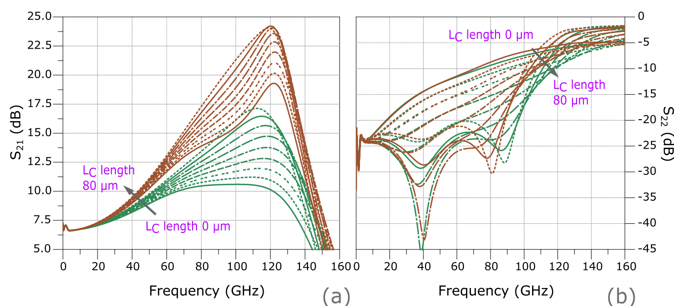

Fig. 14. InP-DHBT modeling impact on the linear driver performances. The brown curve network corresponds to the EM-based DHBT modeling while the green curve network corresponds to the ODmbD DHBT modeling. L_C's length is varied from 0 to 80 μm with a 10-μm step. (a) S-parameter gain, S_{21}. (b) S-parameter output reflection coefficient, S_{22}.

for the external parasitics, designers willing to extend the driver bandwidth may increase the inductive peaking (e.g., L_C's length) and end up with an unexpected behavior of the fabricated device, as a result of excessive peaking gain above 40 GHz. Hence, failing to account for such parasitics in the InP-DHBT model may strongly impact the driver design and alter its performances in terms of peaking gain and bandwidth. This may also force designers to overdimension gain peaking or transistor biasing currents, to cope with a limited bandwidth, which is actually underestimated. These observations are further discussed and confirmed in Section IV, with the driver small- and large-signal measurements and EM-circuit cosimulation results.

D. InP-DHBT Driver Integrated Circuit EM Simulation

To reach a 3-Vppd linear output-swing driver with an over 110 GHz bandwidth, a fine modeling of its behavior across the entire frequency range is mandatory. This was achieved through intensive 2.5-D EM-circuit cosimulation using *Momentum-ADS*. Based on the circuit's layout, an S-parameter model of all the passive elements is generated and then used along with the DHBTs' large-signal model. This allows to accurately account for the circuit's layout parasitics and behavior, which helps in alleviating bandwidth limitations. At least a 20-cell/λ mesh accuracy is used, along with additional cells at the driver layout shapes' edges, as a compromise between simulation resources, time and precision. λ is determined based on the upper EM-simulation frequency bound, which was 160 GHz. Note that the driver IC input–output pads have a 150-μm pitch and were simulated separately using the *Ansys HFSS* 3-D EM-simulator. This prevents limitations in the driver-model frequency-range definition associated with low λ/pad-pitch ratio simulations in *Momentum-ADS*. The pads' S parameters are then used along with the driver model for EM-circuit cosimulation. Additionally, EM-simulation ports' ground references are defined using nearby "ground" ports, directly attached to surrounding ground planes. This prevents high-frequency EM-simulation artifacts that would otherwise occur beyond 40–50 GHz, when the simulation port ground reference is located below the InP substrate. Such technique is particularly well suited for differential integrated circuit architectures, as virtual grounds are inherently present along the layout. Ground reference ports can then be placed along symmetry axes and connected to (perfect) electrical ground during cosimulation.

This yields a very accurate model of the driver behavior and performances, as shown in Section IV's small- and large-signal measurement-simulation comparisons. Note that the proposed EM-circuit cosimulation technique has also been used in [15], [16], and [17] and was validated on InP-DHBT circuits with significantly higher number of integrated transistors (see [44]) using the same technology.

IV. Driver IC Experimental Results

A. S-Parameter Characterisations

The linear driver on-wafer (before wafer thinning and dicing) S-parameter measurements were conducted with a two-port *Anritsu* ME7838A vector network analyzer (VNA) and a 3739A frequency extender, from 70 kHz to 110 GHz. A single-band calibration was performed, covering the entire frequency range. Fig. 15(a) depicts the driver single-ended S-parameter gain, S_{21}, and input reflection coefficient, S_{11}. $|S_{21}|$ shows a 6-dB (12-dB differential) low-frequency gain, together with a -3 dB bandwidth (with respect to the low-frequency gain) well beyond 110 GHz, exceeding the VNA upper bound frequency. A 13-dB equalization gain is obtained at 95 GHz. Fig. 15(b) depicts the single-ended output reflection coefficient S parameter, S_{22}. S_{11} and S_{22}, respectively, remain better than -10 dB up to 92 and 95 GHz, testifying of a broadband 50-Ω impedance matching. The reverse gain S parameter, S_{12}, does not exceed -35 dB over 110 GHz, as depicted in Fig. 15(d), thus showing a good input–output isolation. Together with the good impedance matching, the low reverse gain highly improves the driver stability, as shown in the μ stability factor of Fig. 15(c), which remains above 1 from 0.1 to 110 GHz. μ was retrieved from the S-parameter measurements. Fig. 15(e) shows the driver group delay retrieved from the S_{21} measurement. The group delay ripple is smaller than 9 ps across 110 GHz, although degraded by resonances. The common-mode rejection ratio (CMRR), as depicted in Fig. 15(f), was also retrieved from the single-ended S-parameter measurements. The CMRR exceeds 48 dB around 89 GHz and remains above 17 dB across 110 GHz. This shows that a reasonable CMRR can be obtained with the driver biasing scheme choices presented in Section III, while saving power consumption.

Besides, Fig. 15 presents a comparison of the driver-measured and simulated performances. The corresponding simulation flow is described in Section III-D. One can note an accurate modeling of the linear driver behavior, with enhanced precision on the gain prediction above 50 GHz, while using the proposed small-value external parasitic elements' extraction technique, compared to the ODmbD model. This enhanced precision is critical to properly account for the driver high-frequency gain and stability responses. Indeed, as shown in Fig. 15(a), the standard approach errs up to more than 6 dB in the 50–110 GHz range, which may result in unforeseen excessive peaking gain, with potential subsequent linearity and/or stability degradations in the fabricated device. Besides, the proposed modeling shows much higher accuracy compared

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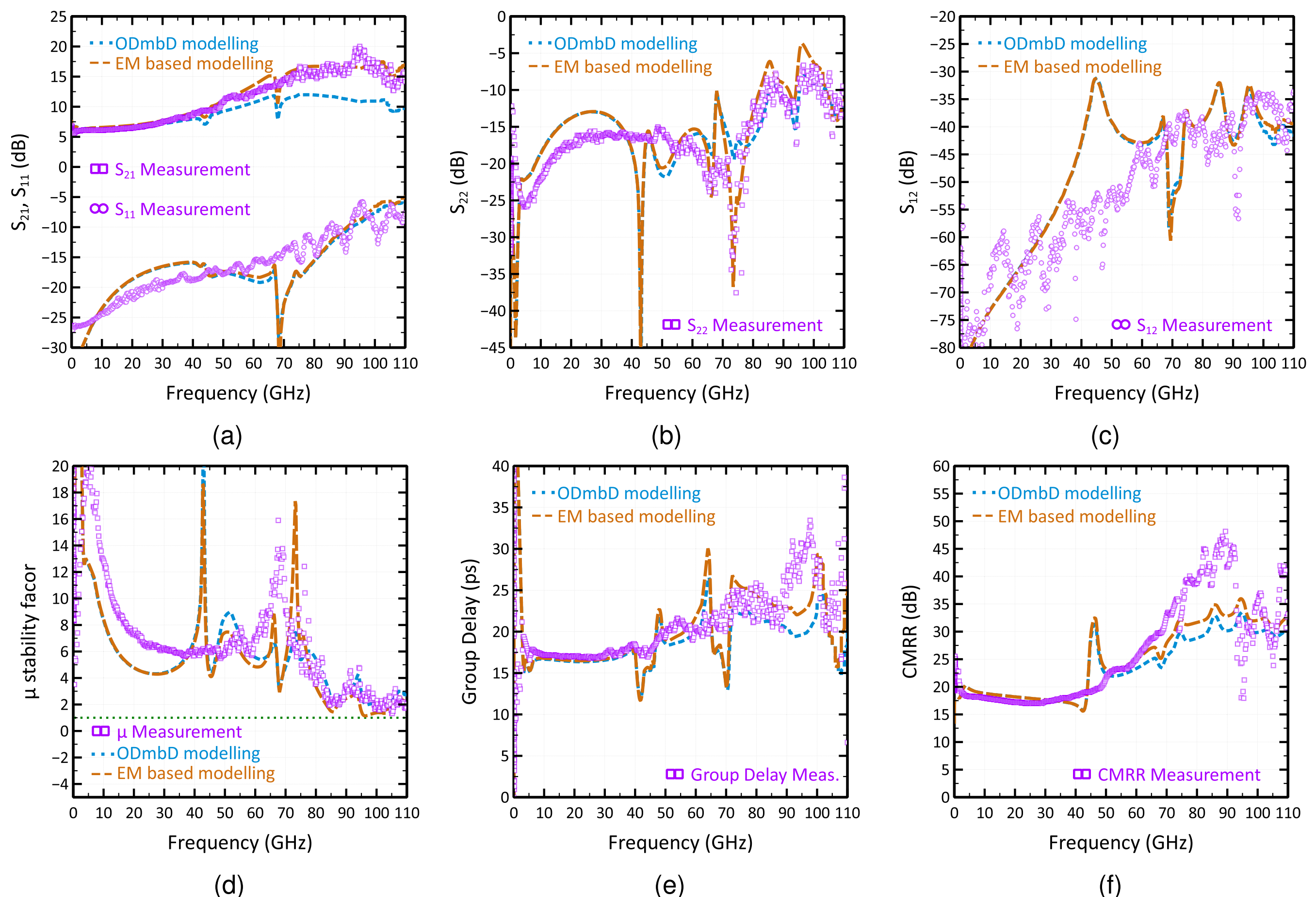

Fig. 15. InP-DHBT linear driver single-ended S-parameter measurements. Measurements are displayed in magenta symbols. The EM-circuit cosimulation using the proposed EM-based InP-DHBT modeling is displayed in orange broken lines and the EM-circuit cosimulation using the ODmbD InP-DHBT modeling is displayed in blue dotted lines. (a) Gain, S_{21}, and input reflection, S_{11}, S parameters. (b) Output reflection S parameter, S_{22}. (c) Reverse gain, S_{12}, S parameter. (d) μ stability factor retrieved from S-parameter measurements. (e) Group delay, retrieved from S parameter measurements. (f) Common mode rejection ratio, retrieved from S parameter measurements.

to previous works, originating from an overall improved simulation flow (see [15], [16], [17]).

As shown in Fig. 15(a)–(c), resonances occur on S_{22} and S_{12} around 44 GHz and on S_{11} and S_{21} around 68 GHz, yet are strongly attenuated in measurement. These resonances could originate from parallel plate coupling between the driver M2 ground planes and the perfect conductor ground plane beneath the InP substrate, considered by default in *Momentum* simulations. Indeed, *Momentum* uses a laterally open method-of-moments formulation with infinite substrate width and length. The electromagnetic waves, coupled to the parallel plate modes, reflect at the IC edges and create a resonant cavity, which yields parasitic substrate mode excitation at the driver input and output ports. The resonance frequency is in good agreement with the theory for the (1, 1, 0) and (1, 2, 0) modes, as defined in [51, eq. (1)]. Note that in simulation, a 160-μm-thick substrate is considered, corresponding to the diced InP IC substrate thickness, to prevent frequency limitations of the *Momentum* Green functions calculation. Only a weak substrate mode excitation can be observed in the measurements, because S parameters were measured on-wafer, which substrate is 600 μm thick and thus significantly reduces the parallel plate coupling.

The S_{22} low-frequency rise could originate from an insufficient decoupling in the measurement setup. Finally, the S_{11} and S_{22} measurement versus simulation low-frequency discrepancy indicate a small process variation during thin film NiCr resistance fabrication.

Apart from the group delay and CMRR, on which some averaging was applied to reduce noise, postprocessing, averaging, and retro-fitting were not applied to the measured and simulated data, for fair comparison. Only measured and simulated driver current consumption were matched in adjusting the (external) voltage supplies during simulation.

B. Large-Signal Continuous Wave (CW) Characterisations

The linear driver continuous wave large-signal measurements have been performed on the wafer, using the standalone ME7838A VNA. The single-ended output power and power gain were measured at 1 and 30 GHz excitation frequencies and are, respectively, plotted in Fig. 16(a) and (c) versus the single-ended input injected power. At 1 GHz, a 5.8-dB linear power gain is obtained, which is consistent with the S_{21} measurement (see Section IV-A). At 1 dB of

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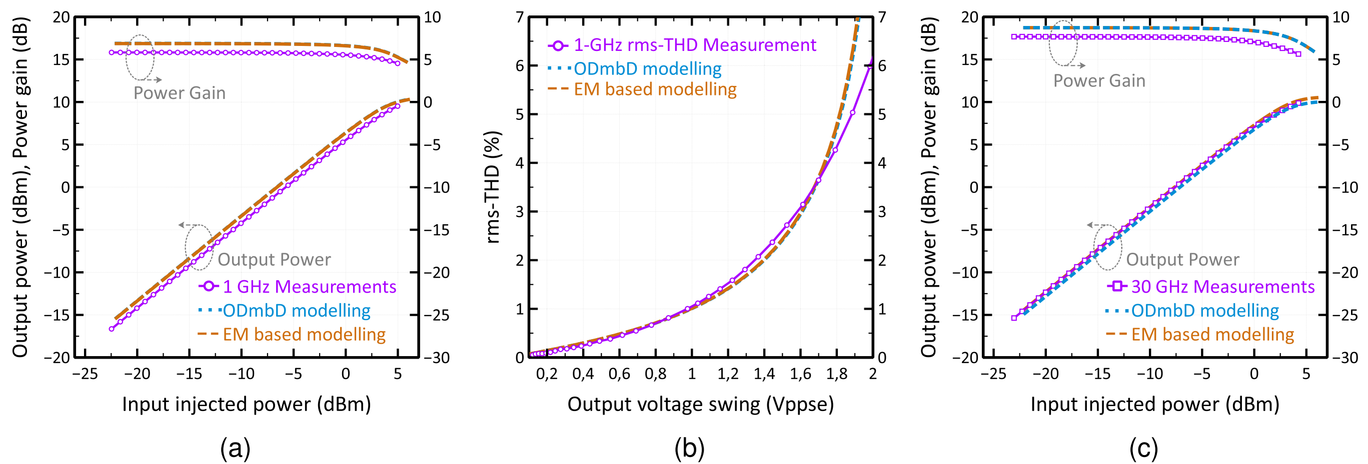

Fig. 16. InP-DHBT linear driver single-ended large-signal continuous wave measurements. Measurements are displayed in magenta solid lines with symbols. EM-circuit cosimulation using the proposed EM-based InP-DHBT modeling is displayed in orange broken lines and the ODmbD InP-DHBT modeling is displayed in blue dotted lines. (a) Output power and power gain versus the input injected power at 1 GHz. (b) RMS-total harmonic distortion versus the single-ended output voltage swing at a 1 GHz excitation frequency. (c) Output power and power gain versus the input injected power at 30 GHz.

gain compression, the measured output power is 9.1 dBm, corresponding to a 3.6-Vppd voltage output swing, which testifies of a large-linear-output dynamic of the InP DHBT driver. The corresponding input injected power is 4.2 dBm. At 30 GHz, because of the driver peaking, a 1.4-dB power gain increase is observed compared to the 1 GHz gain. Besides, Fig. 16(a) and (c) shows the driver large-signal single-ended EM-circuit cosimulated output power and power gain at 1 and 30 GHz, respectively. A high large-signal driver behavior modeling accuracy is obtained. Some shift can, however, be observed between the measured and simulated gains ($\leq$1 dB at 30 GHz).

Fig. 16(b) depicts the linear driver rms-THD measurement versus the driver single-ended output swing. This characterization was performed with the same VNA. The rms-THD measurement has been conducted at a 1 GHz excitation frequency and accounts for the ten first harmonics. At a 1.5-Vppse (3-Vppd) output swing, the rms-THD is 2.7%, testifying of a high driver linear output dynamic. At a 5% rms-THD, the differential output swing is >3.7 Vppd. Nonetheless, as it is based on single-ended measurements, the driver linear dynamic estimation may be pessimistic compared to a true differential measurement.

Additionally, Fig. 16(b) shows a comparison of the measured and simulated driver THD performances, using the EM-circuit cosimulation methodology. A high linear-driver large-signal-response modeling accuracy is observed up to an about 5% THD. This validates the InP DHBTs' large-signal modeling up to moderate-distortion-level regimes. Beyond the 1-dB gain compression point, simulations seem pessimistic, likewise on the power transfer characteristics of Fig. 16(a) and (c). The DHBT model could thus benefit from more intensive small-signal characterisations in the transistor Kirk-effect area, to improve prediction accuracy in deeper compression regimes. However, one should note that this linear driver is not intended to be used in such nonlinear regimes. For fair measurement/simulation comparison, postprocessing, averaging, and retro-fitting were not applied to the measured and simulated data, only measured and simulated driver current consumptions were matched.

Furthermore, Fig. 16 depicts a comparison between the proposed EM-based InP-DHBT modeling and the ODmbD InP-DHBT modeling (see Section II-B). No significant difference is observable at 1 GHz, which is consistent with the driver-simulated small-signal gain of Fig. 15(a). However, the precision on the output power prediction is slightly enhanced at 30 GHz with the proposed EM-based InP-DHBT modeling technique. Moreover, as the excitation frequency increases beyond 30 GHz, more discrepancies between the measured and simulated results may be expected while using the ODmbD InP-DHBT modeling. Indeed, according to the small-signal gain measurement of Fig. 15(a), when using this DHBT model, the higher the fundamental frequency is, the more erroneous the gain prediction becomes, for both the fundamental and the harmonics.

Higher frequency continuous wave characterisations were not possible due to an insufficient VNA output power.

C. Large-Signal Digital Characterisations

To generate high-symbol-rate PAM-4 input signals with sufficient quality, after the InP wafer was thinned and diced, the driver chip was placed on a mockup, along with an in-house-developed InP-DHBT 2-bit active combiner integrated circuit, as shown in Fig. 17. The chips were connected through 50-μm-wide, 300–350-μm-long gold ribbons bonding. All the mounting process was performed at III-V Lab. The 2-bit active combiner is fed with high-quality 75- and 90-Gb/s (2^{15}-1)-bit NRZ signals to, respectively, generate the driver 75- and 90-GBd PAM-4 input signals. For more information on the active combiner operation, see Konczykowska et al. [4]. Driver's output signals were captured using a DCA-X 86100D sampling oscilloscope with two 122-GHz remote heads, connected to the chip through 67-GHz probes, 65-GHz dc blocks, and 10-dB attenuators to protect the sampling heads, and V-to-W adapters. Fig. 18(a) and (b), respectively, depicts the linear driver's output differential

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TABLE I
HIGH-SYMBOL-RATE LINEAR DRIVER STATE OF THE ART

	[52]	[53]	[5]	[54]	[44]	[55]	[16]	[15]	This work
Year of publication	2017	2013	2019	2019	2022	2017	2020	2019	2023
Material	SiGe	InP	InP	SiGe	InP	Si	InP	InP	InP
Technology	BiCMOS	HBT	DHBT	BiCMOS	DHBT	CMOS	DHBT	DHBT	DHBT
f_T/f_{MAX} (GHz)	320/370	290/320	460/480	250/-	360/450	-/-	370/430	380/340	380/520
Architecture Type	Lumped	Lumped	Lumped	Lumped	Lumped	Lumped	Lumped	Lumped	Lumped
Output type	diff	diff	diff	diff	diff	diff	diff	diff	diff
Output impedance matching (Ω)	(¶)	100	100	100	100	100	100	100	100
-3 dB Bandwidth (GHz)	57.5	37.8	>110	>40	108	32	106	86.4	>110
Gain (<1 GHz) (dB)	18.5	16.2	10.5	20	25.7	28‡	14.3	15.3	12
Equalisation gain/frequency (GHz)	4.2/47	3/28‡	8/85‡	2/23‡	11/86.6	4/24	5.7/75.8	4.4/51.6	13/95
PAM-4									
Symbol-rate, D_S (GBd)	64	28	168	34	100	40	80	50	90
Voltage swing, V_{Opp} at D_S (V)	4.8	3	1.5	6	2.4	2‡	3	4.9	3
DC Power consumption (W)	0.82	0.73	0.99	1	1.3	0.18	0.74	0.99	0.67
FoM/Output-stage FoM (GBd)	2.2/3.1	0.43/0.74	0.48/-	1.8/-	0.55/-	1.6/-	1.22/2.3	1.52/2	1.5/2.4
DSP used/required	Yes	No	Yes	No	No	No	No	No	No
THD at V_{Opp} (%)/ $P_{O\,1\,dB}$ (dBm)	-/12	1.2/-	3/-	-	-	5/-	4.2/8.2	-/9.8	2.7/9.1
freq. at THD at V_{Opp}/ $P_{O\,1\,dB}$ (GHz)	10	1	1	-	-	1	1	1	1

‡ Estimated from published measurements. (¶) Low output impedance

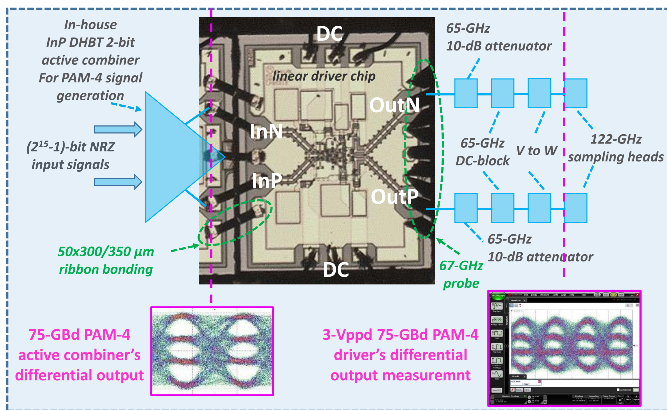

Fig. 17. InP-DHBT linear driver high-symbol-rate PAM-4 characterization environment.

PAM-4 eye diagrams at 75 GBd (150 Gb/s) and 90 GBd (180 Gb/s) with a 3-Vppd linear output swing. At 75 GBd, clear eye opening is obtained, while some degradations can be observed at 90 GBd. A significant part of the output signal quality impairment may come from lower quality input signals, as shown in Fig. 18's insets, as well as the ribbon bonding and the setup bandwidth limitations. Bit error rate (BER) could, however, not be measured due to the lack of necessary equipment. Moreover, one should note that active combiner's output signals were measured prior to connection to the driver chip and do not account for the ribbon bonding degradations. An important part of the driver peaking gain was absorbed to compensate for the ribbons and setup losses. Additionally, note that neither DSP nor postprocessing was used; thus, presented eye diagrams directly reflect the driver plus measurement setup raw performances.

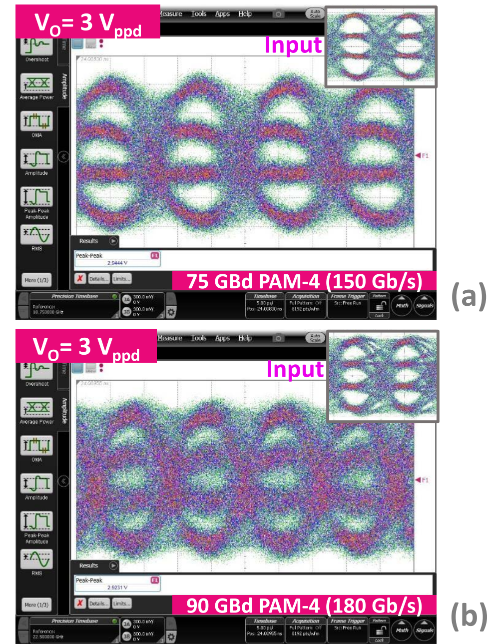

Fig. 18. InP-DHBT linear driver differential PAM-4 output eye diagrams. (a) 3-Vppd 75-GBd (150-Gb/s) output signal. Inset: active combiner's 830-mVppd 75-GBd output signal measured prior to connection with the driver. (b) 3-Vppd 90-GBd (180-Gb/s) output signal. Inset: active combiner's 830-mVppd 90-GBd output signal measured prior to connection with the driver.

Fig. 19 depicts a comparison of the InP-DHBT linear driver 75-GBd PAM-4 measured eye diagram with the transient EM-circuit cosimulated results, using both the OdmbD-based and the EM-based InP DHBT models. For easier comparison, simulated and measured eye diagrams are partly superimposed. Both simulations use the same environment and are based on the EM-circuit cosimulation methodology used in

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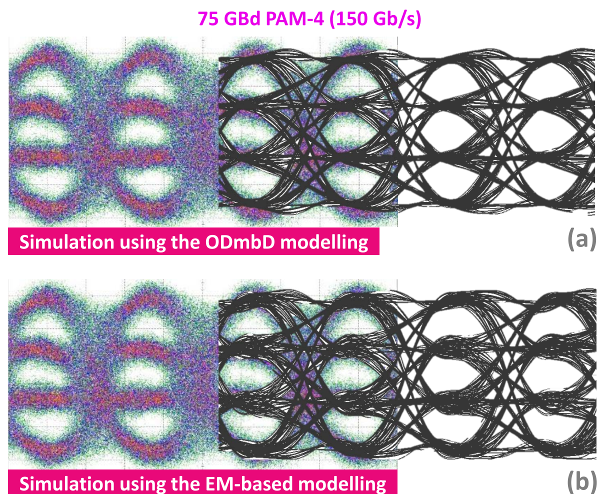

Fig. 19. InP-DHBT linear driver large-signal digital measurements and transient EM-circuit cosimulation comparison at 75 GBd in PAM-4. Simulations use (a) ODmbD InP-DHBT modeling and (b) EM-based InP-DHBT modeling.

Sections IV-A and IV-B. Simulations account for the input ribbon bonding using lumped elements, while a fifth-order *Bessel* filter accounts for the low-pass filtering effects of the output probe, the dc blocks and attenuators, the adapters, and the oscilloscope remote sampling heads at the driver's output (see Fig. 17). Fig. 19 shows that the EM-based modeling yields a qualitatively more consistent simulated driver large-signal PAM-4 behavior. Indeed, as shown in Fig. 15(a), the ODmbD modeling does not seem to capture the driver's high-frequency gain response (peaking gain amplitude). This is noticeable by the reduced amount of overshoots in the corresponding eye diagram [see Fig. 19(a)], predicting very clear eye opening. Contrariwise, in Fig. 19(b), the simulation predicts residual overshoots, originating from a higher peaking gain that is not fully absorbed in the setup losses, which is consistent with measurements. As shown in Fig. 19, gain prediction inaccuracies may become problematic, particularly at high symbol rate, with respect to signal integrity estimation. One should, however, note that finely reproducing the measured input signals in simulation is complex, considering the sophisticated input signal path of the measurement environment. This may explain some discrepancies between the simulated and measured eye diagrams of Fig. 19. Additionally, simulations do not account for noise.

V. Discussion

The linear driver FoM is defined in the following equation:

$$\text{FoM} = \frac{D_S \cdot V_{\text{Opp}}^2}{8 \cdot Z_0 \cdot P_{\text{dc}}} \tag{3}$$

where D_S is the PAM-4 symbol rate, V_{Opp} is the single-ended or differential output swing at D_S, Z_0 is the single-ended or differential output impedance matching, and P_{dc} is the dc power consumption at V_{Opp}. This InP DHBT driver total power dissipation is 0.67 W, of which 0.43 W originate from the output stage, hence corresponding to a 1.5-GBd driver FoM and 2.4-GBd FoM for the standalone output stage. To the best of our knowledge, the proposed lumped linear driver shows the highest >64 GBd PAM-4 performances reported to date. Indeed, the driver combines a 3-Vppd output swing at 90 GBd (180 Gb/s) with a bandwidth well beyond 110 GHz and record 13-dB equalization capabilities at 95 GHz. Table I presents a detailed state of the art of high-symbol-rate lumped linear drivers. Besides, despite a low total power consumption, which is among the lowest in current state of the art, this driver features a high linearity.

VI. Conclusion

This article reports on the modeling, design, and characterization of InP-DHBT-based devices and an integrated circuit. At the transistor level, an improved InP DHBT modeling technique is proposed in order to prevent the "ODmbD" associated with standard *S*-parameter measurement deembedding procedures. It relies on the device access structure external parasitic extraction using EM simulations. With this technique, a significant improvement of simulation accuracy is shown. In particular, better prediction of a canonical cascode gain and stability factor are obtained at millimeter-wave frequencies, as well as an enhanced precision of the proposed linear modulator driver simulated gain in the 50–110 GHz range. This increased accuracy on the peaking gain prediction is shown to have an impact on the driver design choices in relation with its bandwidth, impedance matching, and large-signal modulated signals' integrity.

At the driver IC level, high-frequency gain boosting is used and theoretically detailed to design a large-swing output stage based on a paralleled-transistor cascode with emitter degeneration. We thus propose a theoretical analysis of this cascode self-peaking, which is shown to provide significant gain–bandwidth product enhancement in comparison to the standard cascode implementation with homogeneous transistor dimensions, without increasing the architecture complexity. Additionally, self-peaking is also shown to be inherent to cascode structures and is therefore applicable to other technologies. Besides, the proposed 0.5-μm InP-DHBT linear driver shows a 3-Vppd PAM-4 output swing at 75 and 90 GBd. To the best of our knowledge, these are the highest PAM-4 performances reported to date, without any use of DSP or postprocessing. At a 3-Vppd output swing, the driver shows a 2.7% rms-THD. It also achieves a bandwidth well in excess of 110 GHz. The driver features a 13-dB peaking gain at 95-GHz, which can compensate for the electro-optical modulators' bandwidth limitations. The driver power consumption is among the lowest in the state of the art, achieving a 1.5-GBd driver FoM, which is the highest linear driver performance reported to date without DSP, for ≥64-GBd PAM-4.

Hence, InP DHBTs could bridge the performance gap and empower next generation beyond 1-Tb/s/channel optical transceivers [56], [57], as well as enabling sub-THz power generation [58] for beyond 5G/6G applications. Although, to date, they remain niche-market technologies, regarding communication applications, intense research activities are conducted to combine InP DHBTs' potential with the high-maturity silicon technologies [59], [60], [61], [62]. Such approaches pave the way for InP DHBTs to penetrate industrial

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applications, with the ultimate goal of a direct integration of InP-based high-performance analog front ends with silicon digital/mixed-signal functions (data converters and DSP).

REFERENCES

[1] Cisco. *Cisco Annual Internet Report (2018–2023) White Paper*. Accessed: Jan. 5, 2023. [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.pdf

[2] S.-A. Li et al., "Enabling technology in high-baud-rate coherent optical communication systems," *IEEE Access*, vol. 8, pp. 111318–111329, 2020, doi: 10.1109/ACCESS.2020.3003331.

[3] A. Konczykowska, J.-Y. Dupuy, F. Jorge, M. Riet, V. Nodjiadjim, and H. Mardoyan, "Extreme speed power-DAC: Leveraging InP DHBT for ultimate capacity single-carrier optical transmissions," *J. Lightw. Technol.*, vol. 36, no. 2, pp. 401–407, Jan. 15, 2018, doi: 10.1109/JLT.2017.2760507.

[4] A. Konczykowska et al., "112 GBaud (224 Gb/s) large output swing InP DHBT PAM-4 DAC-driver," in *Proc. 24th Int. Microw. Radar Conf. (MIKON)*, Sep. 2022, pp. 1–4, doi: 10.23919/MIKON54314.2022.9924653.

[5] M. Nagatani et al., "A beyond-1-Tb/s coherent optical transmitter front-end based on 110-GHz-bandwidth 2:1 analog multiplexer in 250-nm InP DHBT," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2301–2315, Sep. 2020, doi: 10.1109/JSSC.2020.2989579.

[6] C. Wang et al., "Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages," *Nature*, vol. 562, no. 7725, pp. 101–104, Oct. 2018, doi: 10.1038/s41586-018-0551-y.

[7] Fujitsu. *100G/400G LN Modulator*. Accessed: Jan. 4, 2023. [Online]. Available: https://www.fujitsu.com/jp/group/foc/en/products/devices/ln/indexgig5.html

[8] Eospace. *40+ Gb/s Modulators*. Accessed: Jan. 6, 2023. [Online]. Available: https://www.eospace.com/40-gb/s-modulators

[9] iXblue. *MXIQ-LN-30 Modulator*. Accessed: Jan. 4, 2023. [Online]. Available: https://www.ixblue.com/wp-content/uploads/2022/02/MXIQ-LN-30_0.pdf

[10] Lumentum Holdings. *High-Bandwidth Coherent Driver Modulator (HB-CDM) with SOA, 69 Gbaud Symbol Rate*. Accessed: Jan. 4, 2023. [Online]. Available: https://www.lumentum.com/en/products/high-bandwidth-coherent-driver-modulator

[11] J.-Y. Dupuy et al., "A large-swing 112-Gb/s selector-driver based on a differential distributed amplifier in InP DHBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 517–524, Jan. 2013, doi: 10.1109/TMTT.2012.2226057.

[12] H. Wakita, M. Nagatani, K. Kurishima, M. Ida, and H. Nosaka, "An over-67-GHz-bandwidth 2 V_{ppd} linear differential amplifier with gain control in 0.25-μm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–3, doi: 10.1109/MWSYM.2016.7540045.

[13] P. Rito, I. G. López, A. Awny, M. Ko, A. C. Ulusoy, and D. Kissinger, "A DC-90-GHz 4-V_{pp} modulator driver in a 0.13-μm SiGe:C BiCMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5192–5202, Dec. 2017, doi: 10.1109/TMTT.2017.2757927.

[14] O. El-Aassar and G. M. Rebeiz, "A DC-to-108-GHz CMOS SOI distributed power amplifier and modulator driver leveraging multi-drive complementary stacked cells," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3437–3451, Dec. 2019, doi: 10.1109/JSSC.2019.2941013.

[15] H. Romain et al., "Over 70-GHz 4.9-V_{ppdiff} InP linear driver for next generation coherent optical communications," in *Proc. IEEE BiCMOS Compound semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, pp. 1–4, doi: 10.1109/BCICTS45179.2019.8972779.

[16] R. Hersent et al., "106-GHz bandwidth InP DHBT linear driver with a 3-V_{ppdiff} swing at 80 GBd in PAM-4," *Electron. Lett.*, vol. 56, no. 14, pp. 691–693, Jul. 2020, doi: 10.1049/el.2020.0654.

[17] R. Hersent et al., "Design, modelling and characterization of a 3-V_{ppd} 90-GBaud over-110-GHz-bandwidth linear driver in 0.5-μm InP DHBTs for optical communications," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Monterey, CA, USA, Dec. 2021, pp. 1–4, doi: 10.1109/BCICTS50416.2021.9682463.

[18] V. Nodjiadjim et al., "0.7-μm InP DHBT technology with 400-GHz f_T and f_{MAX} 4.5-V BV_{CE0} for high speed and high frequency integrated circuits," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 748–752, 2019, doi: 10.1109/JEDS.2019.2928271.

[19] M. Urteaga et al., "A 130 nm InP HBT integrated circuit technology for THz electronics," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 29.2.1–29.2.4, doi: 10.1109/IEDM.2016.7838503.

[20] R. Driad et al., "InP DHBT-based IC technology for 100-Gb/s Ethernet," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2604–2609, Aug. 2011, doi: 10.1109/TED.2011.2157927.

[21] N. G. Weimann et al., "InP DHBT circuits for 100 Gb/s Ethernet applications," in *Proc. 20th Int. Conf. Indium Phosph. Rel. Mater.*, Versailles, France, May 2008, pp. 1–4, doi: 10.1109/ICIPRM.2008.4702916.

[22] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130 nm InP DHBTs with f_T >0.52 THz and f_{MAX} >1.1 THz," in *Proc. 69th Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 2011, pp. 281–282, doi: 10.1109/DRC.2011.5994532.

[23] V. Jain et al., "1.0 THz f_{MAX} InP DHBTs in a refractory emitter and self-aligned base process for reduced base access resistance," in *Proc. 69th Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 2011, pp. 271–272, doi: 10.1109/DRC.2011.5994528.

[24] M. Urteaga et al., "InP HBT integrated circuit technology for terahertz frequencies," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Monterey, CA, USA, Oct. 2010, pp. 1–4, doi: 10.1109/CSICS.2010.5619675.

[25] K. W. Kobayashi and Y. Z. McCleary, "Baseband to 140-GHz SiGe HBT and 100-GHz InP DHBT broadband triple-stacked distributed amplifiers with active bias terminations," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2336–2344, Sep. 2020, doi: 10.1109/JSSC.2020.2988420.

[26] N. Bin et al., "Common base four-finger InGaAs/InP DHBT with 535 GHz f_{MAX}," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Suzhou, China, Jul. 2015, pp. 1–3, doi: 10.1109/IMWS-AMP.2015.7324993.

[27] C. Monier et al., "High-speed InP HBT technology for advanced mixed-signal and digital applications," in *IEDM Tech. Dig.*, Washington, DC, USA, 2007, pp. 671–674, doi: 10.1109/IEDM.2007.4419033.

[28] A. M. Arabhavi et al., "InP/GaAsSb double heterojunction bipolar transistor emitter-fin technology with f_{MAX} = 1.2 THz," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2122–2129, Apr. 2022, doi: 10.1109/TED.2021.3138379.

[29] C. R. Bolognesi, H. Liu, O. Ostinelli, and Y. Zeng, "Development of ultrahigh-speed InP/GaAsSb/InP DHBTs: Are terahertz bandwidth transistors realistic?" in *Proc. Eur. Microw. Integr. Circuit Conf.*, Amsterdam, The Netherlands, Oct. 2008, pp. 107–110, doi: 10.1109/EMICC.2008.4772240.

[30] Y. Shiratori, T. Hoshi, and H. Matsuzaki, "Ultra-high speed InP/GaAsSb-based type-II double-heterojunction bipolar transistors and transfer technology onto SiC substrate," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Monterey, CA, USA, Nov. 2020, pp. 1–4, doi: 10.1109/BCICTS48439.2020.9392903.

[31] W. Quan, A. M. Arabhavi, R. Flückiger, O. Ostinelli, and C. R. Bolognesi, "Quaternary graded-base InP/GaInAsSb DHBTs with f_T/f_{MAX} = 547/784 GHz," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1141–1144, Aug. 2018, doi: 10.1109/LED.2018.2849351.

[32] T. Shivan et al., "High output power ultra-wideband distributed amplifier in InP DHBT technology using diamond heat spreader," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 401–404, doi: 10.1109/IMS30576.2020.9223893.

[33] H. Xu, B. Wu, E. W. Iverson, T. S. Low, and M. Feng, "0.5 THz performance of a type-II DHBT with a doping-graded and constant-composition GaAsSb base," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 24–26, Jan. 2014, doi: 10.1109/LED.2013.2290299.

[34] V. Nodjiadjim et al., "InP/GaInAs DHBT with TiW emitter demonstrating f_T/f_{MAX} ≈340/400 GHz for 100 Gb/s circuit applications," in *Proc. Int. Conf. Indium Phosph. Rel. Mater.*, Santa Barbara, CA, USA, Aug. 2012, pp. 192–195, doi: 10.1109/ICIPRM.2012.6403355.

[35] P. Chevalier et al., "Si/SiGe:C and InP/GaAsSb heterojunction bipolar transistors for THz applications," *Proc. IEEE*, vol. 105, no. 6, pp. 1035–1050, Jun. 2017, doi: 10.1109/JPROC.2017.2669087.

[36] P. Chevalier et al., "Towards THz SiGe HBTs," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Atlanta, GA, USA, Oct. 2011, pp. 57–65, doi: 10.1109/BCTM.2011.6082749.

[37] D. Manger et al., "Integration of SiGe HBT with f_T = 305 GHz, f_{MAX} = 537 GHz in 130 nm and 90 nm CMOS," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, San Diego, CA, USA, Oct. 2018, pp. 76–79, doi: 10.1109/BCICTS.2018.8550922.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[38] R. A. Camillo-Castillo et al., "SiGe HBTs in 90 nm BiCMOS technology demonstrating 300 GHz/420 GHz f_T/f_{MAX} through reduced Rb and Ccb parasitics," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Bordeaux, France, Sep. 2013, pp. 227–230, doi: 10.1109/BCTM.2013.6798182.

[39] H. Rücker and B. Heinemann, "Device architectures for high-speed SiGe HBTs," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nashville, TN, USA, Nov. 2019, pp. 1–7, doi: 10.1109/BCICTS45179.2019.8972757.

[40] M. H. Wakayama, "Nanometer CMOS from a mixed-signal/RF perspective," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 17.4.1–17.4.4, doi: 10.1109/IEDM.2013.6724648.

[41] S. P. Voinigescu et al., "A study of SiGe HBT signal sources in the 220–330-GHz range," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, Sep. 2013, doi: 10.1109/JSSC.2013.2265494.

[42] W. Quan, A. M. Arabhavi, R. Flueckiger, O. Ostinelli, and C. R. Bolognesi, "Iterative de-embedding and extracted maximum oscillation frequency f_{MAX} in mm-Wave InP DHBTs: Impact of device dimensions on extraction errors," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, San Diego, CA, USA, Oct. 2018, pp. 110–113, doi: 10.1109/BCICTS.2018.8550904.

[43] C. R. Bolognesi et al., "InP/GaAsSb DHBTs: THz analog performance and record 180-Gb/s 5.5 V_{ppd}-swing PAM-4 DAC-driver," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Phoenix, AZ, USA, Oct. 2022, pp. 112–119, doi: 10.1109/BCICTS53451.2022.10051763.

[44] R. Hersent et al., "160-GSa/s-and-beyond 108-GHz-bandwidth over-2-V_{ppd} output-swing 0.5-μm InP DHBT 2:1 AMUX-driver for next-generation optical communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 752–755, Jun. 2022, doi: 10.1109/LMWC.2022.3161706.

[45] T. K. Johansen, R. Leblanc, R. Poulain, and V. Delmouly, "Direct extraction of InP/GaAsSb/InP DHBT equivalent-circuit elements from *S*-parameters measured at cut-off and normal bias conditions," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 115–124, Jan. 2016, doi: 10.1109/TMTT.2015.2503769.

[46] T. K. Johansen, N. Weimann, R. Doerner, M. Hossain, V. Krozer, and W. Heinrich, "EM simulation assisted parameter extraction for the modeling of transferred-substrate InP HBTs," in *Proc. 12th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2017, pp. 240–243, doi: 10.23919/EuMIC.2017.8230704.

[47] T. K. Johansen, C. Jiang, D. Hadziabdic, and V. Krozer, "EM simulation accuracy enhancement for broadband modeling of on-wafer passive components," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Oct. 2007, pp. 447–450, doi: 10.1109/EMICC.2007.4412745.

[48] T. K. Johansen et al., "Large-signal modeling of multi-finger InP DHBT devices at millimeter-wave frequencies," in *Proc. Integr. Nonlinear Microw. Millimetre-Wave Circuits Workshop (INMMiC)*, Apr. 2017, pp. 1–3, doi: 10.1109/INMMIC.2017.7927301.

[49] J. Zhang et al., "Causal RLGC(f) models for transmission lines from measured *S*-parameters," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 1, pp. 189–198, Feb. 2010, doi: 10.1109/TEMC.2009.2035055.

[50] V. K. Paidi et al., "G-band (140–220 GHz) and W-band (75–110 GHz) InP DHBT medium power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 598–605, Feb. 2005, doi: 10.1109/TMTT.2004.840662.

[51] K. Eriksson, S. E. Gunnarsson, P.-Å. Nilsson, and H. Zirath, "Suppression of parasitic substrate modes in multilayer integrated circuits," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 3, pp. 591–594, Jun. 2015, doi: 10.1109/TEMC.2015.2393359.

[52] A. Zandieh, P. Schvan, and S. P. Voinigescu, "Linear large-swing push-pull SiGe BiCMOS drivers for silicon photonics modulators," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5355–5366, Dec. 2017, doi: 10.1109/TMTT.2017.2768028.

[53] M. Nagatani, Y. Bouvier, H. Nosaka, and K. Murata, "A 3-V_{ppd} 730-mW linear driver IC using InP HBTs for advanced optical modulations," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Monterey, CA, USA, Oct. 2013, pp. 1–4, doi: 10.1109/CSICS.2013.6659193.

[54] A. H. Ahmed et al., "A 6 V swing 3.6% THD >40 GHz driver with 4.5× bandwidth extension for a 272 Gb/s dual-polarization 16-QAM silicon photonic transmitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 484–486, doi: 10.1109/ISSCC.2019.8662318.

[55] S. Nakano et al., "A 2.25-mW/Gb/s 80-Gb/s-PAM4 linear driver with a single supply using stacked current-mode architecture in 65-nm CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. 322–323, doi: 10.23919/VLSIC.2017.8008525.

[56] C. Zervos et al., "A new generation of high-speed electro-optical transceivers and flexible bandwidth wavelength selective switches for coherent DCI: The QAMeleon project approach," *Proc. SPIE*, vol. 10924, Mar. 2019, Art. no. 109240E, doi: 10.1117/12.2509454.

[57] M. Spyropoulou et al., "The path to 1Tb/s and beyond datacenter interconnect networks: Technologies, components, and subsystems," *Proc. SPIE*, vol. 11712, Mar. 2021, Art. no. 117120G, doi: 10.1117/12.2582920.

[58] B. Debaillie et al. *European Core Technologies for Future Connectivity Systems and Components: D3.3 Initial COREnect Industry Roadmap*. Accessed: Aug. 5, 2022. [Online]. Available: https://www.corenect.eu/publications

[59] M. Urteaga et al., "THz bandwidth InP HBT technologies and heterogeneous integration with Si CMOS," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Sep. 2016, pp. 35–41, doi: 10.1109/BCTM.2016.7738973.

[60] W. Heinrich et al., "Connecting chips with more than 100 GHz bandwidth," *IEEE J. Microw.*, vol. 1, no. 1, pp. 364–373, Jan. 2021, doi: 10.1109/JMW.2020.3032879.

[61] T. E. Kazior et al., "A high performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1113–1116, doi: 10.1109/MWSYM.2009.5165896.

[62] C. Besancon et al., "Fabry Perot laser arrays covering C+L band obtained by selective area growth on InP-SiO_2/Si substrate," in *Proc. Conf. Lasers Electro-Optics (CLEO)*, May 2020, pp. 1–2.

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This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

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