32–36-GHz Single-Chip Front-End MMIC Featuring 35-dBm Output Power and 3.2-dB Noise Figure With 60- and 100-nm GaN/Si HEMTs

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***Abstract*— The design, realization, and test of a *Ka*-band gallium nitride (GaN) monolithic microwave-integrated circuit (MMIC) single-chip front-end (SCFE) is presented. The MMIC, realized in OMMIC's 100- and 60-nm gate length GaN on Silicon process, integrates high-power and low-noise amplification together with transmit or receive selection switches in a 4.7 × 3.0 mm chip area. The SCFE is conceived for active electronically scanned antenna applications operating from 32 to 36 GHz. In RX mode, a typical noise figure of 3.2 dB and gain better than 3B have been measured. In TX mode, the typical output power and the power-added efficiency (PAE) are 35 dBm and 16%, respectively. A drain bias point trade-off analysis is performed so the power amplifier's transistors channel temperature remains below 160° while design charts are provided for the synthesis of the low-noise amplifier (LNA) block. Finally, 100- and 60-nm gate length transistors are combined on the MMIC to improve its performance in terms of receive noise figure and transmit gain and output power. To the best of the authors' knowledge, this GaN SCFE features the highest operating frequency reported in the open literature regarding integrated GaN/Si solutions and compares well with GaN/SiC MMICs especially considering the CW test condition here reported while concurrently fulfilling the FET's channel temperature requirement.**

***Index Terms*— Active phased arrays, gallium nitride (GaN), millimeter wave integrated circuits, monolithic microwave integrated circuit (MMIC) design, transmit–receive modules (TRMs).**

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I. Introduction

THE portion of spectrum at *Ka*-band is well exploited in various applications such as radar seekers [1] and Earth observation (EO) satellites [2] Regarding the latter application, *Ka*-band has established itself, for significant improvements in detection performance in the ice phase, accurate quantitative precipitation of light to moderate rainfall, and observations [3]. The main applications in EO are civil, security, and scientific measurements. When focusing on urban areas, EO is helpful in monitoring the development of urban settlements or providing support and analysis during crises, such as floods and earthquakes. These services are enabled by compact, lightweight, and high-resolution instruments. Moreover, *Ka*-band enables accurate imaging, using real-time interferometry. Space-borne antennas incorporate an active electronic scanning array (AESA) as key building-block of the radar system. A main constraint, at *Ka*-band, is to minimize the size of transmit–receive (TR) modules (TRMs) to avoid grating lobes, since the array lattice spacing should be less than 1 cm in this band. Consequently, the numerous microwave front-end functionalities should be integrated as much as possible in a single-chip device.

Advanced integrated TRM solutions now require only two monolithic microwave integrated circuits (MMICs): a high-power and low-noise robust, known as single-chip front-end (SCFE) [4], [5], [6], and a circuit for signal shaping: the core-Chip [7], [8]. In the past, gallium arsenide (GaAs) was the reference technology at *Ka*-band thanks to its superior performance in terms of f_T and f_{MAX}. Today, gallium nitride (GaN) technologies have reached 100 nm gate lengths, or even less, becoming an attractive solution in this band.

In this context, some GaN SCFE or transmit/receive MMICs operating at *Ka*-band have been proposed in the open literature. A TR chip, designed for the 28–34 GHz band, featuring 3 dB receive NF and 3.5 W output power when operated at 12 V drain voltage is reported in [9]. A moderately wide-band solution is presented in [10], where 1.8 W output power and 3.6 dB receive NF are demonstrated between 24 and 31 GHz. Other interesting demonstrators, in the upper portion of the *Ka*-band, are reported in [11], [12], and [13]. The first two references demonstrate performance in the 33–37 GHz

band while the latter in the 37–40 GHz bandwidth. The demonstrated output power is between 2 and 3 W while the receive NF is 4 dB. Except for [9], realized in GaN/Si technology, the other references are all realized in GaN/SiC. The latter circuits, in TX mode, are designed to operate at 18–20 V drain voltage. Even the GaN/Si MMIC reported in [9] operates at a drain voltage above 10 V.

The goal of the proposed design is to demonstrate the state-of-the-art performance, i.e., 3 W output power in TX mode and less than 3.5 dB NF in RX mode, concurrently minimizing the channel temperature of the high-power amplifier (HPA) section transistors. The latter feature is fundamental in high-reliability applications, such as satellite payloads, when the selected MMIC substrate is the less performing, but cheaper, silicon. Therefore, an uncommon design approach orientated to minimizing the HPA transistor channel temperature is applied.

In RX mode, a systematic approach for designing the 4-stage low-noise amplifier (LNA) circuit is applied, discussing the fundamental design steps with the relevant design charts. Finally, dual gate length technology (60- and 100-nm gate length transistors) is used to improve RX NF and transmit mode gain without sacrificing other critical parameters of MMIC such as output power and reliability metrics.

The article is organized as follows. Section II describes the requirements at the system and circuit level and the key features of the selected technology. Section III describes the SCFE synthesis focusing on the design methodologies applied to its sub-circuits. As stated previously, an unusual HPA design methodology targeting maximum channel temperature operation is presented. For the low-noise section, a synthesis procedure and the relevant design charts to identify the optimum feedback inductor value on all transistors of the four-stage amplifier, to obtain a perfect match at its external ports in conjunction with amplifier noise figure minimization and a specified gain requirement, are presented. Linear and nonlinear design considerations are also provided for the T/R switching blocks. Finally, Section IV provides MMIC characterization data and benchmark with similar circuits reported in the open literature.

This manuscript significantly expands some design and simulation guidelines of an "all" 100-nm SCFE reported in [14] and the preliminary disclosure of some details of the 60–100-nm SCFE presented at IMS 2022 [15]. Detailed design descriptions, including schematics, design charts, and simulations of the four building blocks: LNA, HPA, and input and output switches are provided here. Moreover, supplementary characterization is presented both in terms of additional measurements and in terms of number of measured devices.

II. AESA and SCFE Architecture and Technology

The system demonstrator is for advanced satellite equipment, for EO, and in particular active antennas for a synthetic aperture radar (SAR) based on AESA topology, a type of phased array antenna, in which the beam of radio waves can be electronically steered to point in different directions without moving the antenna [16].

A. System Architecture

The active antenna's key electrical performances are 3.5 kW (approx. 65 dBm) radiated peak power and 55 dBi antenna directivity. The timing of the instrument is governed by a 15% duty cycle with pulse repetition frequency (PRF) of 10 kHz. The antenna size is 200 × 50 × 15 cm for a total mass around 200 kg.

The targeted AESA system is based on an architecture comprising 3456 (432 × 8) TRMs. A pair of TRMs (one for horizontal polarization and the other for vertical polarization) is connected, using a pair of eight-way power divider/combiners, to eight radiating elements evenly spaced at a distance $d < 0.85\lambda = 7.1$ mm. In other words, one TRM is connected to 8 radiating elements. In this condition, there are no grating lobes for scanning angles less than $\pm 10°$. The overall AESA is divided into 432 tiles, each tile having 64 radiating elements in a 8 × 8 configuration. To fulfill system-level requirements, the TRM's NF is maximum 4.0 dB with a target specification of 3.5 dB. The minimum output power of the TRM is 1.5 W (32 dBm) with a target specification of 3.0 W (35 dBm), while its target efficiency is 20%. At minimum saturated output power condition (32 dBm), 7 W TRM peak power consumption (one transmit polarization at a time is considered) is expected at a 15% duty cycle. The average dissipation per tile during the pulse period is expected to be 14 W accounting for radiating element losses and accounting for the consumption of two receive polarizations for up to 85% of the period. The target TRM power consumption in the RX mode is 500 mW. This is a considerable amount of power to be dissipated for a surface 56.8 × 56.8 mm and implies constraints from the mechanical point of view, especially the cooling system. The latter is based on micro heat pipes, for cooling space avionics, realized exploiting additive manufacturing techniques (i.e., 3-D printing of metallic parts) in the beam-forming network and TRMs.

As stated previously, the peak antenna radiated power is 3.5 kW. This figure is obtained by multiplying the minimum output power of the single TRM (32 dBm) by the number of active elements (3456) while considering 2 dB losses of the eight-way power divider/combiners and radiating elements. The 55 dBi antenna directivity figure is obtained considering the array-effect of 8 × 8 × 432 radiating elements when each antenna element has 10 dBi directivity. Therefore, the overall system effective isotropic radiated power (EIRP) is in the order of 120 dBm, when considering the minimum TRM output power condition (32 dBm).

Essentially, a TRM is realized by cascading the SCFE described here with an MMIC core chip, and in particular OMMIC's Ka-band phase and amplitude setting circuit commercially available off-the-shelf. The SCFE block diagram is shown in Fig. 1. dark red triangles indicate where the D006GH (presented in Section II-B) FETs are inserted. From a functional point of view, it is worth to point out that the amplifiers along the TX chains are requested to operate in compression zone to maximize their efficiency and avoid possible amplitude modulation of the transmitted signals. On the contrary, the RX amplifier shall work linearly to

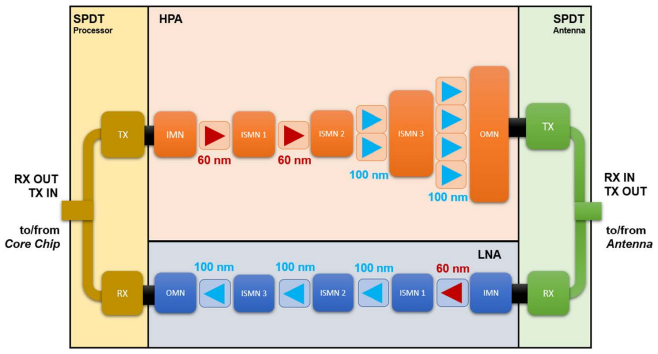

Fig. 1. SCFE simplified block diagram. The core-chip side SPDT is shown on the left while the antenna side SPDT appears on the right side of the block diagram. HPA is on the top side while LNA on the bottom. Both amplifiers are implemented in a four-stage topology while the HPA employs a corporate power recombination of the output stage transistors. For the amplifying FETs, shorter gate length transistors (60-nm tech.) are represented by dark red triangles, while 100-nm tech FETs with light blue triangles.

preserve as much as possible the echoes amplitude and phase characteristics.

B. Technology

The technology selected for the design of the SCFE is OMMIC's GaN on Silicon depletion mode HEMT. This technology features several interesting points. First, it is conceived to provide adequate power density, around 3 W/mm at millimeter-wave [17], in conjunction with advanced noise performance [18]. Second, it is endowed with the distinctive feature of providing two different gate length transistors on the same epitaxial structure or even MMIC. The two gate lengths are, respectively, 100 and 60-nm, the latter featuring advanced performance in terms of noise figure [19] and operating frequency [20]. The two technologies are identified as D01GH and D006GH, respectively, and their figures-of-merit are reported in Table I. The process is built on a Silicon substrate, with the possibility of 100- and 60-nm mushroom gate length without field plate. The double-heterojunction AlN/GaN/AlGaN HEMT process, based on a 3-in high-resistivity (5 kΩ/cm) silicon substrate thinned down to 100 μm with a dielectric constant (ϵ_r) of 11.7 and a loss tangent [tan(δ)] of 0.015. The process employs in situ passivation to avoid memory effects and regrown non-alloyed ohmic contacts to minimize access resistance. The thin AlN barrier serves to diminish short-channel effects, whereas the AlGaN back barrier improves electron confinement. The asymmetrical positioning and the mushroom shape of the gate contact is studied to raise the cutoff frequency (f_T) of the devices by lowering the intrinsic gate to source resistance R_i to 0.6 Ω · mm which also reduces the knee voltage allowing better power-added efficiency (PAE). With the high transconductance (g_m) of 850 mS/mm, it is possible to reduce the number of stages of the amplifier section. Several SiN and thick SiO_2 dielectric layers are used for passivation, isolation, and for two densities of MIM capacitors (400 and 50 pF/mm^2). Regarding reliability, according to the foundry manual, there is no difference in the maximum ratings of the 60- and 100-nm FETs, or, stated differently, a unique worst case value is given for the two technologies. The 100-nm technology is finalizing space qualification, while the 60-nm is still in prototype phase. Apart from the gate length, there is an additional difference between the two technologies. D006GH technology contains only FETs for amplification, while D01GH technology provides FETs for amplification and switching.

TABLE I
D01GH AND D006GH TECHNOLOGIES FIGURES-OF-MERIT

	L_g (nm)	f_T - f_{MAX} (GHz)	I_{DSS} (mA/mm)	g_m (mS/mm)	V_{BGD} (V)
D01GH	100	110 - 180	1200	850	36
D006GH	60	150 - 190	1200	950	36

III. SCFE SUB-SECTIONS DESIGN

Output power (P_{out}) in TX mode and the noise figure in RX mode are two key requirements of the SCFE. Their performances are greatly influenced by the losses of the antenna-side single-pole double-throw (SPDT) switch. Therefore, these losses should be minimized while guaranteeing sufficient power-handling performance in TX mode. When starting the design, 1 dB insertion loss (IL) is initially allocated to the switch, as verified in previous experiments [21]. Consequently, the HPA P_{out} and LNA NF requirements are adjusted by 1 dB with respect to the corresponding SCFE requirement. Finally, the side switch of the core-chip [in Fig. 1 (left)] is designed to improve T/R isolation and help to resolve layout issues, as described below.

A. SPDT Design and Simulations

OMMIC's GaN/Si process features the possibility to select either 60- or 100-nm gate length transistors for active (amplifying) FETs. This double gate length feature is not applicable to switch-mode FETs and consequently only 100-nm gate length technology is available for switching transistors.

The selected topologies of the two switches are shown in Fig. 2 while the switches' positions in the SCFE are given in Fig. 1. The critical requirements for the antenna SPDT are linearity and IL. The SCFE isolation requirement is obtained in conjunction with the core-chip SPDT and anyhow the unused amplifier is switched off to additionally increase isolation.

A quarter-wave transformation topology is selected since the thru branch has a switched-off device and the signal does not have to be transferred via a switched-on device, thus improving the switch's IL [22]. This solution features limited bandwidth behavior, due to the $\lambda/4$ transmission line, but is acceptable in this case since the operating bandwidth is limited. For this topology, power handling is slightly influenced by device size since P_{max} is approximated by

$$P_{\text{max}} = \frac{(V_{\text{bd}} - V_{\text{th}})^2}{2Z_0} \approx \frac{2(V_{\text{cntrl}} - V_{\text{th}})^2}{Z_0} \quad (1)$$

being V_{bd} the gate-to-drain breakdown voltage, V_{th} the threshold voltage, V_{cntrl} the gate control voltage, and Z_0 the impedance level at the switch device. To prevent device failure,

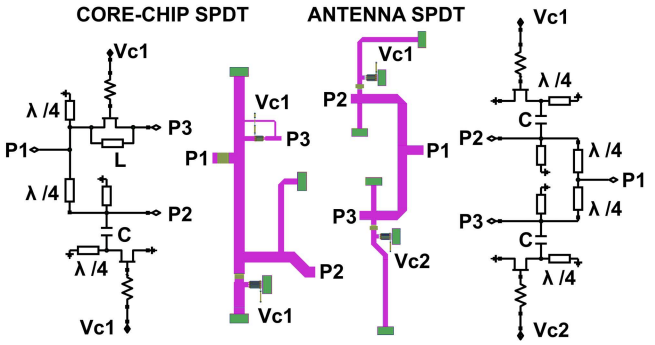

Fig. 2. SPDT switches schematics and layout. (Right) Antenna-side SPDT and (left) core-chip side SPDT.

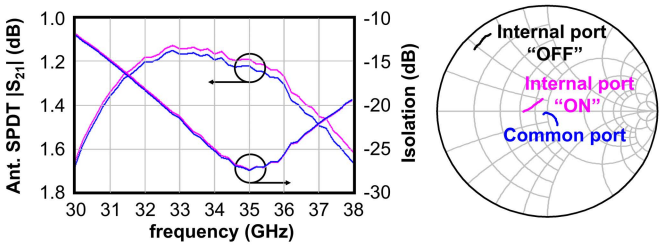

Fig. 3. Antenna port simulated linear performance. (Left) IL and isolation. (Right) Smith chart data provided from 32 to 36 GHz.

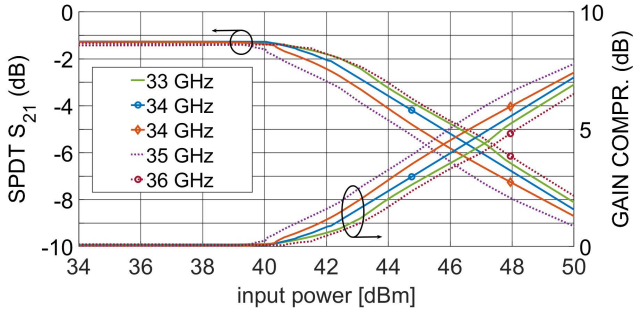

Fig. 4. Antenna SPDT simulated insertion gain (left axis) and gain compression (right axis) versus input power. Traces are given from 32 to 36 GHz at 1 GHz step.

it is necessary that $|V_{\text{cntrl}}| \leq |V_{\text{bd}} + V_{\text{th}}|/2$ [21]. A pair of opposite control voltages are required for SPDT operation: 0 V for FET ON-state and -15 V for FET OFF-state are preliminarily selected. The negative value is slightly less than half the technology's breakdown voltage (36 V) to implement some margin with respect to breakdown limit quantified in (1). Moreover, the negative control voltage value has an impact on SPDT switching time. Recent studies on OMMIC's D01GH have shown that switching occurs with negligible delay when the positive voltage $V_{\text{cntrl,pos}}$ is set equal to or below 0 V, as in the proposed design, and the negative voltage is higher than -20 V. Taking into account this indication also, -15 V for $V_{\text{cntrl,neg}}$ is imposed [23]. Finally, the overall MMIC switching speed is largely influenced by the large OFF-chip capacitor ($\geq$1 nF) that is inserted to improve HPA low-frequency stability.

A critical figure of merit to evaluate RF switching technologies is its $R_{\text{ON}} \times C_{\text{OFF}}$ product (or alternatively its inverse) that measures the ability of the switch arm to transmit with minimal IL in the ON-state while maintaining high isolation in the OFF-state. This FoM is invariant to switch geometry since C_{OFF} is directly proportional to the transistor size while R_{ON} is inversely proportional to its size [24]. For the selected technology, the unitary width ON-state resistance of a series FET is $R_{\text{ON}} = 1\ \Omega\cdot$ mm, while the unitary width OFF-state capacitance of a series FET is $C_{\text{OFF}} = 300$ fF/mm. Consequently, the technology's figure of merit for switching functionalities is computed to be in excess of 3 THz.

To simultaneously guarantee linear and nonlinear performance, the transistor geometry in the antenna SPDT is fixed in 6×70 μm. The latter value is a compromise between minimizing IL while simultaneously accepting 15 dB isolation, keeping in mind power-handling requirements. For the selected transistor geometry R_{ON} is calculated to be 2.4 Ω while C_{OFF} is 120 fF. 1.2 dB in band IL is obtained with this device, slightly worse than the target value of 1 dB, and 15 dB in band isolation, as seen in Fig. 3 (left). A slight IL improvement can be obtained at expense of isolation; however, this solution is discarded since 15 dB is considered, after a system-level analysis, the lowest acceptable value. A negligible discrepancy between the behavior of the RX and TX paths is observed since the Antenna SPDT layout is not perfectly symmetrical as can be noted in Fig. 2. Even if the layout is slightly asymmetrical, the electrical lengths and component values appearing in TX and RX branch of the antenna SPDT are identical and therefore there is no practical difference in the two paths electrical behavior, especially the internal reflection coefficients. The antenna SPDT is also designed to show an impedance—at the interface of the internal ports between the switch and the amplifiers, ports P2 and P3 in Fig. 2—close to 40 Ω to ease the synthesis of the HPA and LNA matching networks. The latter pair, in fact, requires optimal terminations having a real part around 40 Ω with a slightly inductive behavior. Consequently, moving the SPDT internal reflection coefficient to 40 Ω will reduce the distance between these impedances and the optimum amplifier terminations, thus reducing the complexity of matching network design. The simulated reflection coefficients of the antenna SPDT are depicted in Fig. 3 (right).

Focusing on nonlinear analysis, the simulated gain compression versus input power is provided in Fig. 4 and exhibits a 0.1 dB compression point at 40 dBm input power, guaranteeing 4 dB margin with respect to the maximum output power of the HPA. This power level is compatible with the maximum power level predicted in (1), considering 50 Ω termination and -2 V threshold voltage (V_{th}).

The core-chip side SPDT is designed also to accommodate layout constraints, thus easing connection to the adjacent core-chip MMIC. Consequently, an asymmetrical layout solution is adopted with a series FET for the TX path and a shunt FET with $\lambda/4$ transformer on the RX path. The effect of this choice on the SPDT layout is clearly visible in Fig. 2 (right). The geometry of the TX path FET is 4×50 μm. This asymmetrical SPDT can be controlled by applying the same voltage value to both transistors. An inductive element,

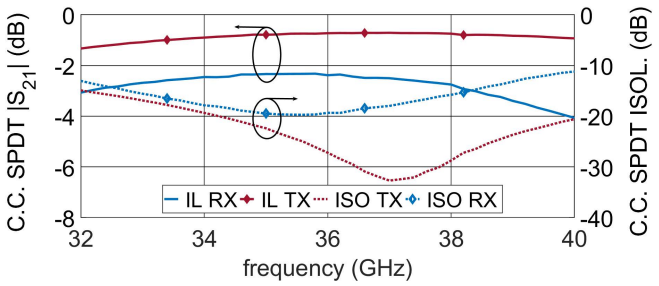

Fig. 5. Core-chip port simulated IL and isolation performance.

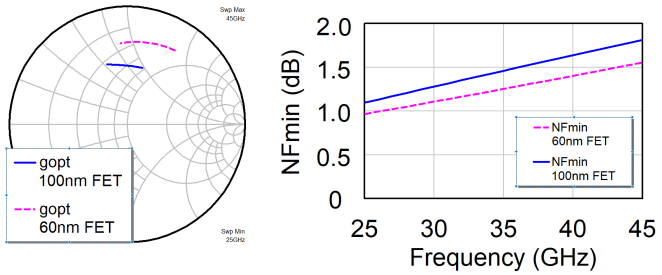

Fig. 6. Optimum input impedance for noise, gopt (left) and minimum noise figure, NF_{min} (right) of two transistors in D006GH and D01GH technologies. Smith chart data are given from 25 to 45 GHz.

L in Fig. 2, is inserted to resonate the series FET's OFF-state capacitance so maximizing isolation. Since the LNA's gain is greater than the HPA's one, a second design choice for the core-chip side SPDT consists in sacrificing the RX ON IL to improve the TX ON IL. This effect can be seen in Fig. 5. Isolation is better than 15 dB in both cases over the operating bandwidth.

Switching time is mainly governed by the OFF-chip capacitors. Transistor parasitic capacitances are very small (around 0.1–0.2 pF) and therefore the switching time associated with these parasitics is very low even when using 3 kΩ series gate resistors. Finally, the MMIC switching time must be governed at system level to avoid unwanted transient effects. Consequently, the system timing is implemented by first turning off one amplifier, then changing the switch position, and finally turning on the other amplifier.

B. LNA Design and Simulations

The LNA is designed to provide approximately 2 dB NF and more than 30 dB gain. As stated previously, OMMIC's GaN/Si process has the distinctive feature of providing two different gate length transistors on the same MMIC. Given the stringent noise figure goal we opted for the 60-nm (D006GH) technology on the first stage transistor, whose NF is critical for the overall LNA NF. This performance improvement is depicted in Fig. 6, where we plot transistors' noise figures-of-merit, at optimum noise bias point, versus frequency. The noise figure improvement of the 60-nm technology is rather clear, although it is obtained at the expense of the optimum noise termination being further away from the center of the Smith chart. NF_{min} value plotted in Fig. 6 is coherent with the LNA's 2 dB NF specification considering the ohmic

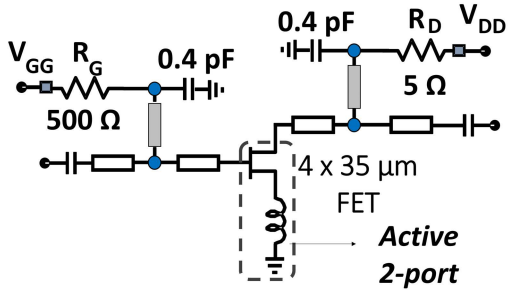

Fig. 7. Single stage low-noise simplified schematic. Only elements that have a practical effect on the operating bandwidth are reported.

losses of the passive embedding (mainly the input matching network and source degeneration) and some residual noise contribution from the following stages. Subsequent analysis suggests that there is no significant NF degradation when using 100-nm HEMTs after the first stage, so we opted to use the 100-nm technology for the following stages, given the higher maturity of the process. The bias point is selected keeping in mind the limitation of total dc power in RX mode (max 500 mW) and the foundry's suggested bias point for low-noise/high-gain operation. Consequently, the selected drain bias voltage is +5 V. Device geometry is chosen as a trade-off of linear, noise, and nonlinear requirements. At Ka-band the optimum solution is a device periphery around 150 μm. This analysis comes from previous experience in designing LNAs at a slightly lower frequency (27–31 GHz). In practice, larger devices have larger parasitics causing them to have low available gain, while smaller devices exhibit high gain but with optimum terminations closer to the open circuit region, making simultaneous signal-noise matching rather problematic. In the higher portion of the K_a, a four-finger by 30–40 μm devices exhibit sufficient gain and practically matchable optimum terminations. A 4×35 μm device is therefore selected as optimum trade-off between contrasting goals [25]. Gate bias voltage is chosen so that the drain current is 10% of the maximum value as typically required for low-noise operation. The drain current is 15 mA per stage (drain current density 110 mA/mm) ant the corresponding gate voltage value −1.1 V. The same gate voltage is applied at all stages. While this choice eases routing issues of the dc voltage in the TRM it does not allow the designer to tune the gate voltage at every stage to obtain better overall linear and nonlinear performance. A four-stage topology is determined to be necessary to satisfy the gain requirement.

Inductive source degeneration, schematically indicated as an inductive element connected between the transistor's source terminal and ground seen in Fig. 7, is a well-established technique applied in LNA design and its beneficial effects have been extensively reported in the open literature [26], [27], [28]. Recently, design methodologies for two-stage [29] and N-stage [30] LNAs have been proposed. The latter provides design charts that allow one to determine the value of the feedback inductor applied on each stage ($L_{S,k}$ in Fig. 8) as a function of the stage's mismatch level (IM_k and OM_k in Fig. 8). Essentially, a synthesis procedure is provided with

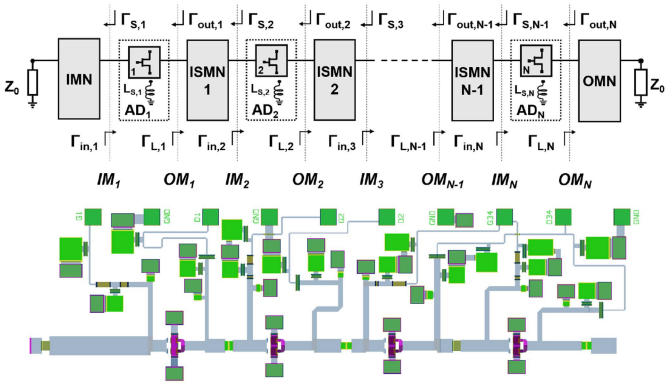

Fig. 8. LNA schematic for $N = 4$ (top) and layout (bottom).

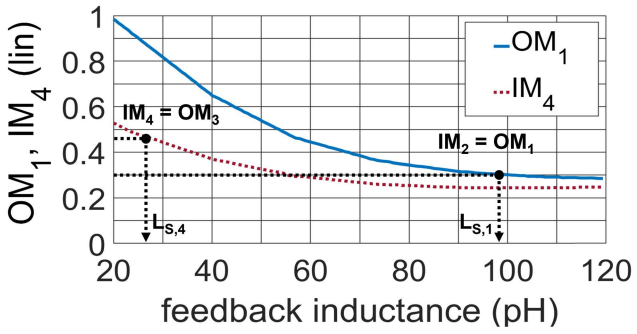

Fig. 9. OM_1 and IM_4 versus feedback inductance value at 34 GHz.

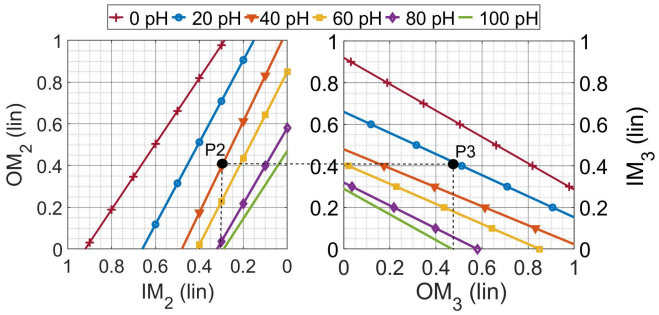

Fig. 10. LNA interstage mismatch levels versus feedback inductance value at 34 GHz.

the relevant design charts to identify the optimum feedback inductor value on all transistors of an N-stage amplifier. The method is applicable to arbitrary N values. The design methodology allows the designer to synthesize a conjugately matched N-stage LNA with optimum noise performance, while simultaneously controlling gain and in-band stability. This is accomplished by selecting appropriate mismatch levels and, consequently, specific feedback inductance values. Following the proposed design methodology, the LNA's first and last stage are matched to the terminating impedance, implementing a conjugate match condition at the LNA's I/O ports, while some controlled mismatch is accepted at the intermediate sections of the LNA. Additionally, the optimum termination for noise is presented at the FETs input port to minimize the LNA's NF while the output terminations are synthesized to provide an imposed mismatch level at all sections.

The preliminary design of the matching networks is performed using this method and is applied at 34 GHz (central frequency), not having to perform matching to the output and input sections toward the canonical 50 Ω, but toward the reflection coefficients shown at the internal ports of the antenna SPDT switch, shown in Fig. 3 (right). Once the bias point is selected, the optimum termination for noise measure condition is imposed on the input section of each of all stages ($\Gamma_{S,k} = \Gamma_{\mathrm{OPT},k}$), together with a null mismatch value for IM_1 and OM_4 representing, respectively, the LNA's input and output mismatch levels. The trend of OM_1 and IM_4, respectively, the mismatch in the output section of the first FET and the mismatch in the input section of the fourth (final) FET, is then plotted as a function of the source inductive feedback value, and is shown in Fig. 9. Finally, an additional design chart is created relating the second and third stage mismatches as a function of feedback inductance, seen in Fig. 10. The final step consists of determining an adequate level of mismatch in all internal LNA sections. As a general rule, higher mismatch is associated with lower feedback and consequently higher stage gain. However, mismatch levels should be controlled since they may cause instability issues, especially in adjacent bands, when they are close to becoming unitary at design frequency. Mismatch levels at the three intermediate sections of the 4-stage LNA are set at 0.30, 0.41, and 0.47 for this design. These mismatch levels are identified with dashed lines in Figs. 9 and 10 and allow us to graphically select the corresponding feedback inductance value. As explained previously, the input termination at each stage ($\Gamma_{S,k}$) in Fig. 8 is designed to satisfy the minimum noise measure condition, while the output termination on each stage ($\Gamma_{L,k}$) in Fig. 8, is designed to satisfy the mismatch levels reported in Table II. The proposed design flow is a starting point for identifying the optimum terminations and feedback values by applying a theoretical method. Afterward, some minor tuning is applied on the third and fourth stages to improve gain and return loss over the operating bandwidth.

The four-stage LNA is essentially a cascade of four similar low-noise amplifying networks whose simplified schematic is reported in Fig. 7. The active two-port is a source-degenerated transistor and the choice transistor geometry and feedback elements is described previously. The series capacitors appearing in the schematic act as dc-block and matching elements. Series and shunt transmission lines are used for bias injection and their geometry is designed to optimize RF performance. Resistors are added to the bias lines to improve low-frequency stability, while 0.4 pF shunt capacitors are inserted to conceal the resistor's noise contribution in the operating bandwidth.

The layout of the four-stage LNA is reported in Fig. 8 (bottom), while Fig. 11 reports the LNA section simulated NF and gain. The simulated values agree well with the requirements expressed at the system level. The simulated NF is slightly higher than the synthesized value, as the data given in Fig. 11 consider a termination of 50 Ω. A 0.15 dB improvement is observed in simulation when the input termination is set at $(40 + 5 \cdot j)$ Ω being the SPDT's internal port impedance. The gain level is aligned with the 30 dB requirement.

TABLE II
LNA MISMATCH LEVELS AT 34 GHz AND SYNTHESIZED FEEDBACK INDUCTOR VALUE

Stage	$L_{S,k}$ feedback inductor value (pH)	IM_k	OM_k
k=1	97	0	0.30
k=2	40	0.30	0.41
k=3	22	0.41	0.47
k=4	27	0.47	0

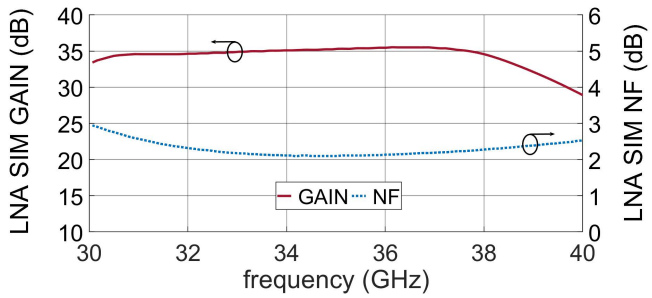

Fig. 11. Simulated noise figure of the standalone LNA section (dotted line) and linear gain (solid line). The design bandwidth is 32–36 GHz.

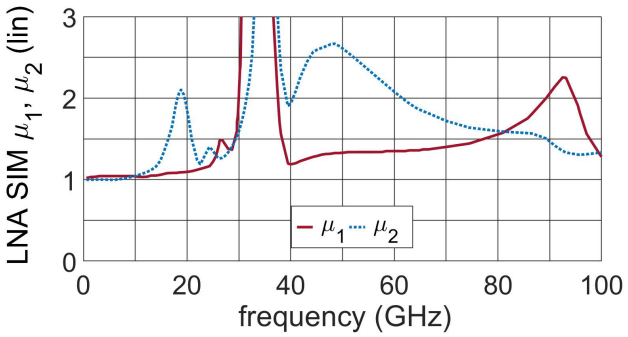

Fig. 12. Standalone LNA section simulated input (dotted line) and output (solid line) geometrical stability factors.

LNA in-band stability is accounted for at design frequency since all sections mismatch levels are imposed to be smaller than unity, guaranteeing at the very least in-band conditional stability [31], [32]. The out-of-band active device unconditional stability is obtained by adding resistive elements, in the biasing lines, whose stabilizing (and noisy) effects are negligible at operating frequency but, thanks to the shunt capacitor, but become apparent at lower and higher frequencies. In addition, the inherent stability analysis (i.e., on standard loads) is checked by applying Ohtomo's test [33] and finally LNA external stability is confirmed through geometrical stability factors, [34], shown in Fig. 12.

C. HPA Design and Simulations

Reliability is a critical aspect in space components. Regarding electronic front-end functionalities, the HPA is possibly the most critical circuit since it incorporates large power transistors, which add to a significant total gate periphery value. The HPA section is designed to guarantee 10^8 h mean time to failure (MTTF) and some form of de-rating is to be applied as recently recommended by the European Space Agency [35]. OMMIC's 100-nm GaN technology is capable of delivering in excess of 3.5 W/mm output power when operated in the maximum power condition bias point, i.e., $V_{DS} = 15$ V. However, at this bias point to maximize output power, the channel temperature will be in excess of 200 °C. This high temperature value is in contrast to the requirements expressed in [35] that advise maintaining the channel temperature below 160 °C to improve reliability and therefore the system's MTTF. A careful trade-off between the HPA's contrasting goals of maximizing output power and minimizing channel temperature has to be carried out. The first and fundamental decision in the classical HPA design flow is to determine the number of transistors and the total periphery of the final (output) stage. Typically, in single-ended and narrowband designs, this task is accomplished considering the maximum power density of the technology at the operating frequency as the input parameter for the decision. However, the maximum power density cannot be the only input when the transistor's maximum channel temperature is also a critical requirement. Consequently, a trade-off between power density and operating channel temperature has to be accepted. OMMIC's D01GH PDK is equipped with two different transistor thermal models. The first is a simplified quasi-static mono-dimensional heat flow model, while the second is a 3-D thermal that can be used within FEM-based numerical thermal simulators. The latter possibility is more precise and can account for marginal effects within the same device. However, it requires extensive computational resources and time, making the simplified model an attractive solution for preliminary evaluation in fast design and optimization cycles. Accurate electro-thermal simulations, on the other hand, can be used for a final layout verification. The key factors which affect the channel temperature of the transistor are as follows.

1) Form factor of the transistor, quantified by the unitary gate width.
2) Bias point, V_{GS} and V_{DS}.
3) Extrinsic load seen by the active device.

The geometry used for this analysis is selected with the following assumptions. The technology power density, in de-rated configuration to fulfill the maximum channel temperature operation, is preliminary set around 2.0 W/mm. The requested HPA RF output power is 36 dBm. Additionally, an approximately 1 dB loss of the output matching network of the amplifier must be considered. Supposing to recombine the output of four transistors to obtain the desired total output power, the single transistor periphery shall be at least 750 μm. Initially, a 6×125 μm device is selected to guarantee the 4 W HPA output power. The traces depicted in Fig. 13 report the channel temperature (T_j) and the corresponding drain voltage V_{DS} as a function of the output power of a single transistor at a fixed input power of 27 dBm at mid-band frequency. In practice, this graph reports the best (=lowest) V_{DS} and T_j pair that can be obtained at a fixed output power level by tuning the output impedance. In other terms, higher output power can be obtained from this device (6×125 μm), however, at the

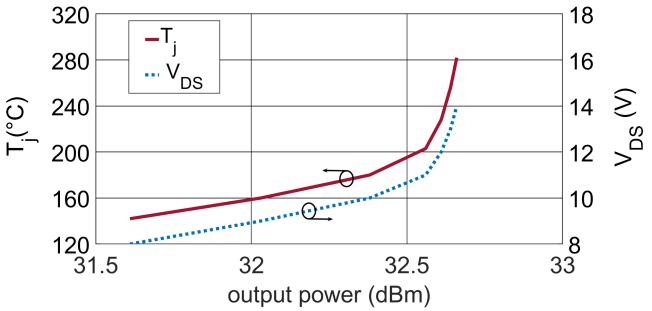

Fig. 13. Channel temperature T_j (left) and required V_{DS} (right) of a 6×125 μm device as a function of output power.

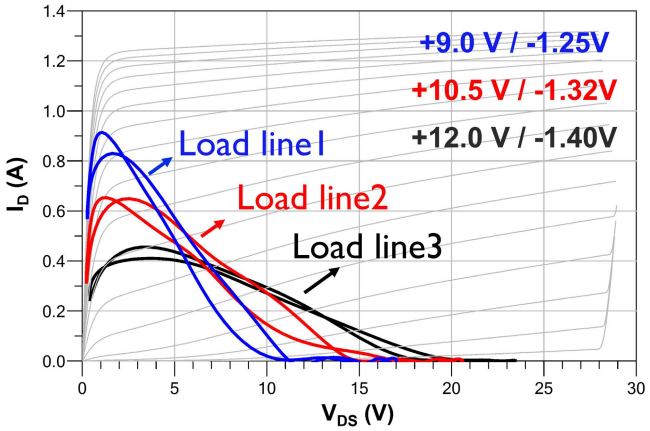

Fig. 14. Load lines corresponding to biases reported in Table III for a 6×125 μm device. Bias conditions are reported in the legend. Positive values are drain voltages, while negative values are gate voltages.

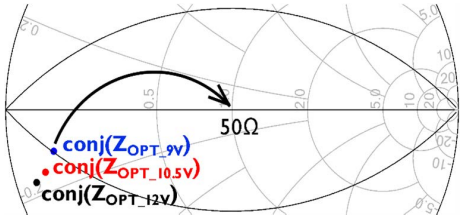

Fig. 15. Conjugate of the optimum power load (Z^*_{OPT}) of a 6×125 μm as function of drain voltage. Bias conditions are reported in Table III.

TABLE III
BIAS CONFIGURATION FOR THE THREE LOAD LINES REPORTED IN FIG. 14

Load line	V_{GS} (V)	V_{DS} (V)	P_{OUT} (dBm)	T_j (°C)
1 (blue curve)	−1.25	9.0	32.01	160
2 (red curve)	−1.32	10.5	30.98	160
3 (black curve)	−1.40	12.0	30.13	160

expense of a higher T_j while requiring higher V_{DS}. In this analysis, the base plate temperature is fixed at +80 °C. The transistor is biased in class AB corresponding to a gate voltage of −1.2 V. The channel temperature is estimated through

$$T_j = T_{\text{bottom}} \exp\left(R_{\text{th@}T_{\text{ref}}} \frac{P_D}{T_{\text{ref}}} \right) \tag{2}$$

being T_{bottom} the base plate absolute temperature. OMMIC's PDK provides, for any device periphery, the value of $R_{\text{th@}T_{\text{REF}}}$ at 20 °C. The total thermal resistance $R_{\text{th@}T_{\text{REF}}}$ of the substrate evaluated at the reference temperature T_0^a (superscript "a" denotes absolute temperatures in Kelvin) is

$$R_{\text{th@}T_{\text{ref}}} = \frac{H}{A} \frac{1}{K_{\text{th}} T_{\text{ref}}} \tag{3}$$

being H the substrate thickness, A the area of the device footprint and $K_{\text{th}}(T_0^a)$ the thermal conductivity at T_0^a. The dissipated power (P_D) is a result of design solutions, while the other parameters are available from OMMIC's PDK.

A design trade-off between contrasting goals, i.e., minimizing the thermal resistance of the device and the dissipated power, must be enforced to guarantee the maximum +160 °C channel temperature when base plate temperature is fixed at +80 °C.

In principle, a higher output power could be obtained by increasing the drain voltage V_{DS}. However, this choice would lead to an increase in channel temperature, which might be unacceptable for space applications. A similar phenomenon occurs when V_{DS} is fixed and V_{GS} is modified. In this second case, there is an adjustment of drain current that has an impact on output power and channel temperature, although less dramatic than the case in which V_{DS} is swept. The curves in Fig. 13 are obtained for a fixed output termination. This is not the optimum case, since output terminations should be retuned when V_{DS} changes. Fig. 14 shows the load lines for three values of V_{DS}. V_{GS} is adjusted to modulate the drain current and obtain always 160 °C channel temperature. The input signal is 27 dBm at the mid-band frequency while the base plate temperature is set at +80 °C.

Table III indicates the bias configurations used for the three cases reported in Fig. 14. It appears that by increasing V_{DS} it is necessary to decrease V_{GS} to minimize the dissipated power. Furthermore, by increasing V_{DS} and decreasing V_{GS} the conjugate of the optimum power load (Z^*_{OPT}) moves toward the edge of the Smith chart, as shown in Fig. 15, thus complicating signal matching at the HPA output [36]. Consequently, the optimum engineering choice, in this design, is to select a lower V_{DS} value in conjunction with higher V_{GS} to simultaneously fulfill nonlinear requirements and reliability constraints (maximum T_j).

The analysis previouly reported justifies the choice of the final stage total periphery. After stabilization elements are applied, as shown in Fig. 16(a), the final stage transistor available gain is 6 dB over the operating bandwidth. A four-stage topology, schematically depicted in Fig. 17, is adopted to obtain the prescribed 26 dB gain. The first and second stage employ 60-nm gate length devices to increase HPA gain, with respect to an all 100-nm version, thus helping saturate the final stage transistors. Shorter gate length FETs (60-nm tech.) are inserted only in the first and second stages since the 100-nm technology features, at the moment, better reliability and failure analysis models. Therefore, the latter technology is selected for the final stages where reliability is critical and a device model of higher accuracy is necessary. The typical FET periphery scaling, increasing from input to output, is adopted to meet nonlinear requirements, especially PAE.

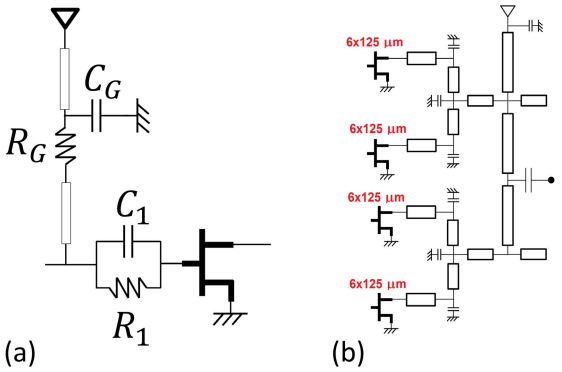

Fig. 16. (a) HPA transistor with its stabilizing elements at the gate terminal and (b) simplified schematic of the HPA's final stage.

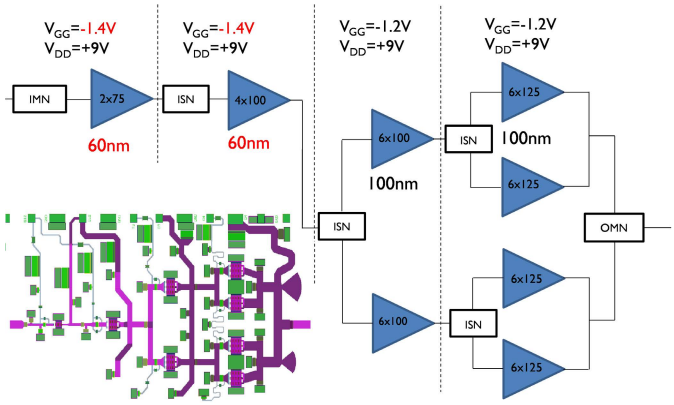

Fig. 17. Schematic and layout of the HPA section.

The final stage overall periphery is determined to be 3.0 mm. This geometry is chosen to deliver just above 4 W RF output power, considering the power density of the technology under the minimized drain voltage condition (1.8 W/mm averaged throughout the operating bandwidth) and the inevitable losses, quantified at approximately 0.8 dB, of the 4-to-1 output combining structure (OMN in Fig. 17). Transistors geometry and bias points are selected to fulfill nonlinear and linear requirements. In the HPA, the gate to source voltages of the two first stages are lower than the two last, since the 60-nm gate length technology has higher transconductance than the 100-nm FETs, as reported in Table I. Consequently, the gate voltage of the 60-nm FET is lower than the 100-nm FETs.

The third stage transistor is slightly smaller and its available gain is 7 dB. The first and second stage transistors are implemented in the 60-nm technology and their available gain is higher than the final stages one, also due to the smaller transistor periphery: 9 and 7 dB, respectively. Consequently, the cascade available gain of the four-stage HPA adds up to 29 dB. The HPA transducer gain is 3 dB lower than this figure, consequently 26 dB, considering the inevitable losses of the matching networks and some mismatch loss at the HPA output section.

Particular care is devoted to obtain in-band and out-band stability (geometrical stability factor $\mu > 1$ in dc-80 GHz).

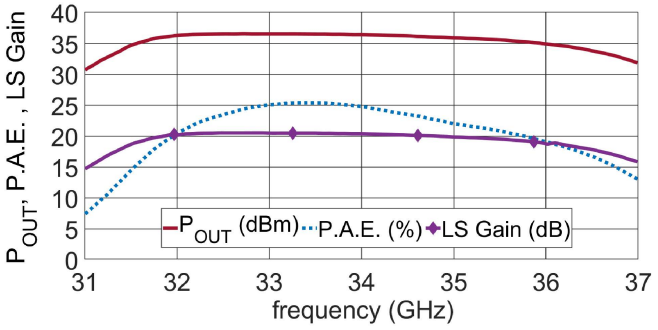

Fig. 18. Standalone HPA simulated nonlinear performance over frequency at 16 dBm input power.

This feature is obtained by applying the schematic reported in Fig. 16(a). This topology ensures unconditional stability adopting a parallel-*RC* (C_1 and R_1 elements) and a series-*RL* network (R_G and shunt transmission line ac-grounded through C_G) connected in series and in parallel to the gate terminal, respectively. The appropriate selection of the resistive and reactive elements also allows reaching a rather flat response for the gain. This solution represents a robust stability network, but affects gain, causing a light reduction.

The output combiner's design goals are: symmetrical structure so as to provide in-phase signal recombination, provide Z_{OPT} load to each FET when the output port is terminated on Z_0, and to minimize ILs. The simplified schematic of the 4-to-1 output section combiner is shown in Fig. 16(b).

Note that an asymmetrical drain voltage injection topology, from the top side only, is applied targeting HPA integration in the SCFE. The interstage matching networks and input matching network topologies are similar to those reported in Fig. 16.

Finally, overall PA stability is evaluated at first in a linear regime applying Othomo's test [33], and subsequently in periodic large-signal regime through [37] and [38]. No stability issues are identified.

The simulated nonlinear performance of the HPA section is given in Fig. 18 in the nominal bias condition. In saturation, the output power reaches 36 dBm. while the linear gain is 26 dB, considering 6 dB gain compression and 20 dB large signal (LS) gain. The typical PAE in band is 22%.

The maximum channel temperature, seen in Fig. 19, is verified to be below +160 °C in saturated power condition and over the entire operating bandwidth. The requirement on channel temperature would not have been fulfilled if a higher V_{DS} had been chosen, as seen in the same figure. However, in the latter case, the output power would have increased by about 0.7 dB.

D. SCFE Design and Layout

The SCFE is designed implementing the schematic reported in Fig. 1. The expected key electrical performance (RX NF and TX output power) is approximately 1.1 dB worse than the HPA and LNA stand-alone values reported in Sections III-B and III-C at sub-circuit level. The reduction is due to the ohmic losses of the antenna SPDT switch, considering on average

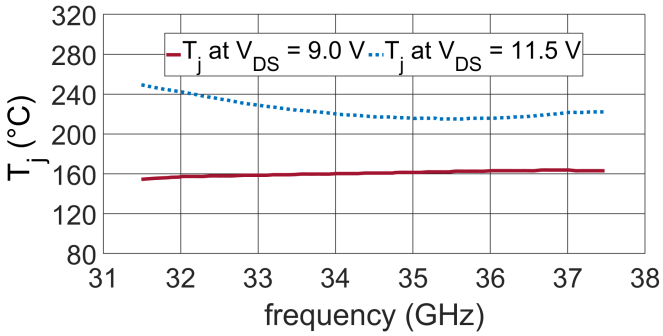

Fig. 19. Standalone HPA final-stage transistors channel temperature versus frequency at maximum input power while varying V_{DS}.

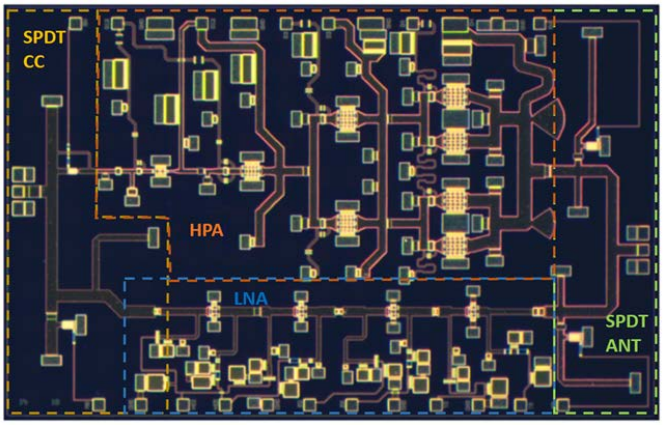

Fig. 20. Picture of the realized SCFE. RF pads are on the left side (core-chip port) and on the right side (antenna port). DC pads are placed at the upper (HPA bias) and lower (LNA bias) sides. Chip size is 4.7 × 3.0 mm^2.

1.2 dB IL and some expected improvement since the internal circuits are optimized for 40 Ω termination. Fig. 20 reports the micro-photograph of the MMIC. The size of the chip is 4.7 × 3.0 mm^2. The HPA is biased only from the top side pads. While this choice eases internal routing issues, it sets a lower limit on the drain bias linewidth and, consequently, on its characteristic impedance, making HPA synthesis slightly more complicated. The LNA is biased from the bottom-side pads and finally the four switch FETs are controlled from the pads in the four corners of the MMIC.

IV. Experimental Results

Two-port measurements have been performed on-wafer both for the RX and TX mode. All presented performance refers to the entire SCFE, not individual functionalities. Linear and nonlinear characterizations are performed at ambient temperature without external cooling. A comparison of the proposed GaN SCFE with other TR MMICs in the open literature is reported in Table IV.

A. SCFE RX Mode Characterization

Measurements have been performed under the bias conditions of the LNA indicated in Section III-B, in detail (V_{DD} = 5 V, V_{GG} = −1.2 V, linear drain current I_D = 60 mA), while the HPA is turned off by pinching-off the gate and maintaining the drain bias ON. Fig. 21 shows the measured and simulated SCFE RX gain and NF. The gain is higher than 30 dB and well covers the operating bandwidth from 32 to 36 GHz. The same figure shows the measured and simulated SCFE RX Noise Figure (NF50). The average NF value is 3.2 dB as expected by analysis. In fact, the LNA's NF is approximately 2.0 dB (on a 40 Ω input termination), while the antenna port SPDT IL is around 1.2 dB, slightly increasing above 35 GHz.

SCFE RX mode return loss is better than 8 dB at the antenna-side port and better than 12 dB at the core-chip side port, see Fig. 22. The agreement between the simulated and measured data is very good at the output port. There is some discrepancy between measurements and simulation at the input port due to the preliminary PDK electrical model of the 60-nm HEMT. The reason of s_{11} discrepancy is related to source degeneration in the first stage. To accurately simulate source degeneration, a correct de-embedding of inductive/capacitive/resistive parasitic effects at the three transistor terminals is required. If this de-embedding is not

TABLE IV
State-of-the-Art Table *Ka*-Band TR MMICs

REF. \ PARAM.	[9]	[12]	[10]	[11]	[13]	T.W.
tech.	GaN/Si 100-nm	GaN/SiC 150-nm	GaN/SiC GaAs 150-nm	GaN/SiC 150-nm	GaN/SiC 150-nm	GaN/Si 60/100-nm
config.	TR CHIP	CHIP-SET	CHIP-SET	CHIP-SET	TR CHIP	TR CHIP
FREQ. (GHz)	28-34	33-37	24-31	33-37	37-40.5	32-36
$P_{out,TX}$ (dBm)	35.5 pulsed	35 pulsed	32.5	30	33 pulsed	35 CW
PAE_{TX} (%)	N/R	20	19	6	18	16
NF_{RX} (dB)	2.9	4	3.6	4.2	4.2	3.2
HPA V_{DD} (V)	12	19	18	18	20	9
Gain TX / RX (dB)	18 / 21	14 / 20	36 / 20	13 / 14	23 / 18	25 / 30
AREA (mm^2)	11	N/A	QFN4	N/A	QFN4	14.1

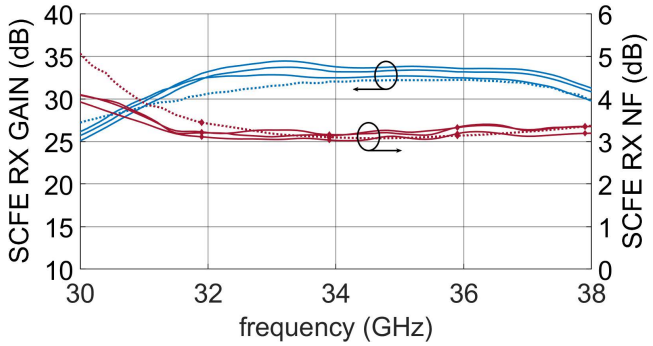

Fig. 21. SCFE RX mode (LNA plus I/O switches) gain (left axis) and NF (right axis). Measured (three samples, solid lines) and simulated (dotted lines).

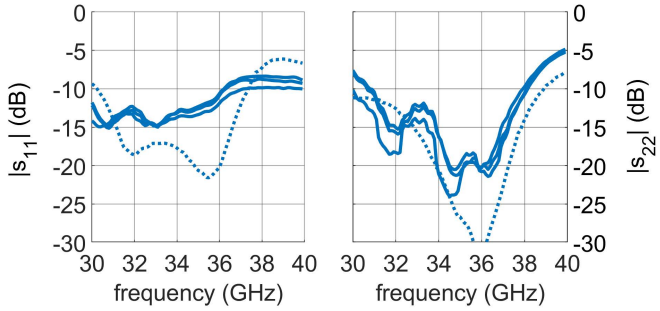

Fig. 22. SCFE RX mode (LNA plus I/O switches) I/O return loss, left $|s_{11}|$, right $|s_{22}|$. Measured (three samples, solid lines) and simulated (dotted line).

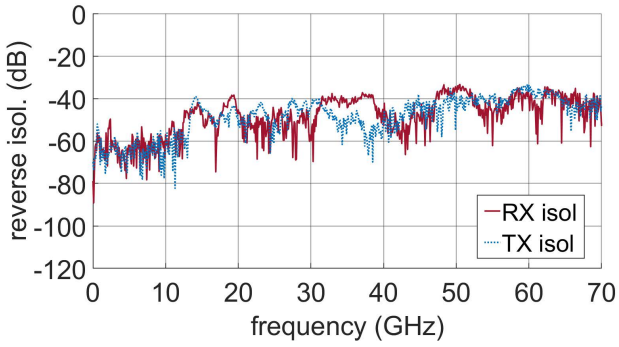

Fig. 23. SCFE RX and TX mode measured reverse isolation.

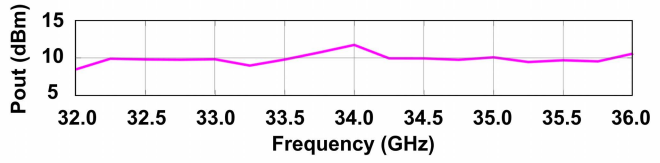

Fig. 24. SCFE RX mode (LNA plus I/O switches) measured output power versus frequency at 1 dB compression point.

well implemented, as may happen with preliminary transistor models, then there will be a difference between simulated and measured results. Reverse isolation is reported in Fig. 23.

Finally, the nonlinear performance of the SCFE in RX mode is reported. Fig. 24 shows the output power, at 1 dB gain compression condition, over the operating bandwidth. The typical value is 10 dBm under nominal bias conditions, reaching 20 dBm when the drain current is increased to 250 mA.

B. SCFE TX Mode Characterization

Linear characterization of SCFE in TX mode is carried out at the bias point indicated in Section III-C, in detail (V_{DD} = 9 V, V_{GG} = −1.0 V), while LNA is turned off by pinching-off the gate and maintaining the drain bias ON. At this bias voltage, the linear drain current is I_D = 900 mA. The simulated and measured SCFE gain and I/O return loss in TX mode are shown in Fig. 25. The comparison highlights a good agreement between the measured and simulated data. The input return loss is again worse than the output return loss due to the preliminary electrical PDK models of the 60-nm

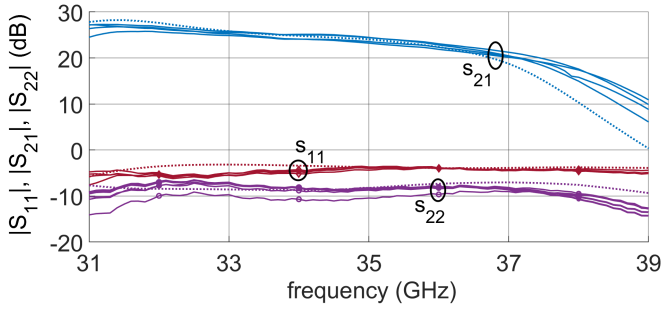

Fig. 25. SCFE TX mode (HPA plus I/O switches) linear behavior. Measured (five samples, solid colored lines), and simulated (dotted lines).

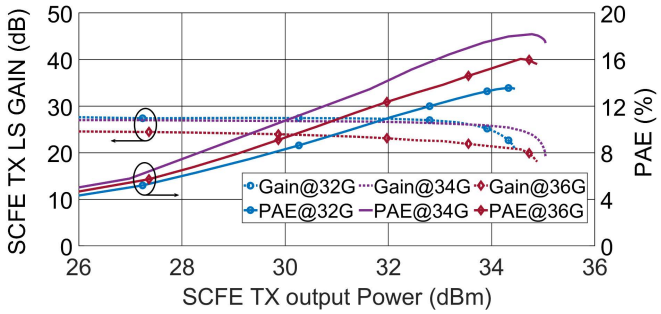

Fig. 26. SCFE TX mode (HPA plus I/O switches) measured PAE and gain as functions of the output power under the nominal bias condition and at 32, 34, and 36 GHz. Dotted lines report large signal gain, while solid lines PAE.

HEMTs and a design choice that consists of selecting higher available gain for the first two HPA stages while sacrificing input return loss. This design choice has a small impact on the performance of the TRM, since this port is connected to an internal section of the TRM and in particular a passive circuit. However, the discrepancy between simulated and measured IRL is less evident in TX ON mode, since the source terminal of HPA FETs are grounded directly without any degeneration.

Power measurements, in CW mode, are performed by an Agilent E4448A Power Spectrum Analyzer, in this case, coupled with an absolute power reference provided by a Keysight USB power sensor. The test signal is realized by an Agilent N5183A Synthesizer. Fig. 26 reports the measured nonlinear characteristics versus input power at 32, 34, and 36 GHz.

The MMIC shows a P_{out} level of 32 dBm at 9 dBm input power (worst case), while the saturated output power reaches 35 dBm in most parts of the bandwidth. The saturated PAE is typically 16%, however a slightly better value is expected. The reason for the small discrepancy is the higher measured drain current than the corresponding simulated value due to the preliminary PDK nonlinear model. However, it is fair to say that for the entire SCFE the simulated PAE is 17% while the measured value is 16%. This simulation versus measurement discrepancy is tolerable considering the employed technology and the corresponding PDK model is not fully released for production. Finally, Fig. 27 reports the nonlinear performance versus frequency. The output power is given at 6 dB gain compression. The input power is adjusted to obtain this condition and is also plotted together with PAE and nonlinear gain.

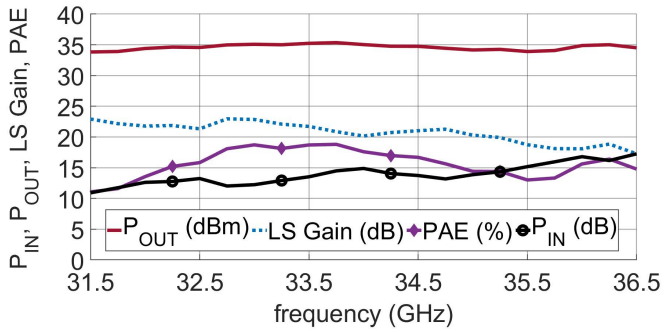

Fig. 27. SCFE TX mode (HPA plus I/O switches) measured output power, PAE, and gain at 6 dB gain compression condition. The input power is also provided as a reference. The operating bandwidth is 32–36 GHz.

The saturated output power practically reaches 35 dBm over the entire operating bandwidth, with a small roll-off below 32 GHz. The input power is adjusted to compensate for the gain slope versus frequency. PAE is between 14% and 19%. When the output power reaches saturation, the drain current varies between 1.9 and 2.5 A over frequency, in a manner inversely proportional to the PAE value. The measured results are in good agreement with the expected ones. In fact, the HPA's simulated output power, shown in Fig. 18 is slightly above 36 dBm. This value is consistent with the SCFE TX mode measured data considering the antenna-side SPDT switch IL just above 1 dB.

C. Benchmark

Table IV reports the comparison between the SCFE MMIC presented here and other circuits available in the open literature. The focus is Ka-band multifunctional front ends, both as integrated solutions or as chipsets. The SCFE here presented compares well with previously published GaN TR MMICs and chipsets operating at Ka-band. To the best of the author's knowledge, it reaches the highest operation frequency, at least for integrated solutions in GaN/Si, and compares well with GaN/SiC, as seen in Table IV. In fact, $P_{out,TX}$ is in line with other contributions, however, obtained at lower V_{DD} and channel temperature, thus improving the device reliability. Moreover, the tests described here are carried out in CW mode, while the power performance reported in [11], [12], and [13] is in pulsed mode. Finally, the receive mode NF is noteworthy considering the relatively high operating frequency. These results provide interesting feedback on OMMIC's GaN/Si technology proving it can be gainfully employed for integrated low-noise and power circuits, comprising switching functionality.

V. Conclusion

Design and characterization of a SCFE MMIC operating at 32–36 GHz and implemented in industrial grade GaN/Si technology are given in this article. Several interesting design solutions have been sought, such as HPA drain voltage trade-off study to minimize channel temperature, and novel design charts for the LNA synthesis. Moreover, a gainful combination of 100- and 60-nm gate length FETs is applied on the MMIC to improve the performance with respect to an all 100-nm version. In RX mode, the MMIC features NF = 3.2 dB and Gain $\geq$30 dB. In TX mode, P_{out} = 35 dBm and typical PAE = 15% are measured in CW operation. The measured performance is noteworthy considering the rather low drain voltage and the use of the less preforming, from the electro-thermal point of view, Silicon substrate rather than Silicon Carbide. The SCFE RX mode NF is also excellent, thanks to the use of advanced 60-nm gate length technology in the LNA section.

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