A 21.8–41.6-GHz Low Jitter and High FoM$_j$ Fast-Locking Subsampling PLL With Dead Zone Automatic Controller

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***Abstract*— In this article, a wideband millimeter-wave (mm-wave) fast-locking subsampling phase-locked loop (FL-SSPLL) with low jitter and high jitter-power figure of merit (FoM$_j$) is proposed. A quadrature subsampling phase detector (QSSPD)-based dead zone automatic controller (DZAC) is introduced for fast locking. Such DZAC eliminates the long locking time caused by the dead zone of frequency-locked loop (FLL) while maintaining low in-band phase noise of subsampling loop (SSL). The mm-wave quad-mode oscillator is integrated in the FL-SSPLL to achieve a wide frequency range. The proposed FL-SSPLL is fabricated in a 40-nm CMOS technology and occupies a core area of 0.18 mm^2. Measurements exhibit a wide output frequency range of 62.5% from 21.8 to 41.6 GHz with a 100-MHz reference. The FL-SSPLL achieves a 62.7–79.1-fs root-mean-square (rms) jitter across the whole frequency range. The total power consumption is 18.3–23.6 mW, leading to FoM$_j$ from −248.3 to −251.4 dB. Meanwhile, the FL-SSPLL features a robust lock acquisition and achieves less than 1.5-μs locking time.**

***Index Terms*— Fast locking, jitter, millimeter wave (mm-wave), subsampling phase-locked loop (SSPLL), wideband.**

I. Introduction

THE millimeter-wave (mm-wave) multiple-band operations for 5G wireless and point-to-point backhaul communication (such as 24, 28, 37, and 39 GHz) require phase-locked loops (PLLs) with wide output frequency range. To support the high data rate at the Gb/s level, complex modulation schemes are demanded, which put stringent requirements on the phase noise of PLL. Meanwhile, the short locking time is an important design requirement of PLL [1], [2], [3], [4], [5], [6], especially for massive users with high data-rate requirement or fast vehicles traveling among cities and towns. To support a quick transition between channels, the output frequency of PLL jumps from one frequency to another quickly. Besides, the fast-locking PLL relaxes the timing conditions for the transceiver communication. At the same time, robust lock acquisition with short relock time is an essential design requirement because voltages can change quite rapidly on-chip. PLLs using multiple oscillators are reported to cover a wide mm-wave frequency range [7]. In the sacrifice of large chip area, this kind of PLL still faces the challenge of low phase noise at mm-wave due to the large division ratio. Recently, different types of mm-wave PLLs with low phase noise are reported [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. The mm-wave PLLs utilizing high-frequency crystal and large loop bandwidth have demonstrated low phase noise [15], [16], [17]. However, such crystal is expensive and increases the system cost. Another way to relax the tradeoff is cascading injection-locked frequency multiplier (ILFM) after the PLL [18], [19], [20], enabling the PLL and voltage-controlled oscillator (VCO) to operate at a lower frequency. Nevertheless, such ILFMs suffer from limited locking range and high power consumption and require high injecting power from VCO.

Subsampling PLL (SSPLL) is promising to achieve low in-band phase noise without divider [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37]. The intrinsically high gain of the subsampling phase detector (SSPD) can suppress in-band phase noise significantly. Thus, SSPLL can achieve low in-band phase noise when operating at mm-wave. However, due to its dividerless characteristics, the SSPLL lacks frequency detection capability. Thus, an auxiliary frequency-locked loop (FLL) with a dead zone of half the REF cycle is often used for frequency locking [21]. Until the phase error at the input of the phase/frequency detector (PFD) exceeds the dead zone, the FLL is active. In general, such an operation requires a long acquisition time. To shorten the locking time, removing the dead zone from the FLL is a choice [23]. However, the revised FLL injects its PFD and charge pump (CP) noise into the loop filter, which deteriorates the in-band phase noise. A soft loop switching in [26] reduces the dead zone to half the VCO cycle for achieving quick relocking and low in-band phase noise

Manuscript received 27 November 2023; revised 22 January 2024; accepted 18 February 2024. Date of publication 27 February 2024; date of current version 5 September 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 61934001 and Grant 62161160310. *(Corresponding author: Xun Luo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2024.3368190.

Digital Object Identifier 10.1109/TMTT.2024.3368190

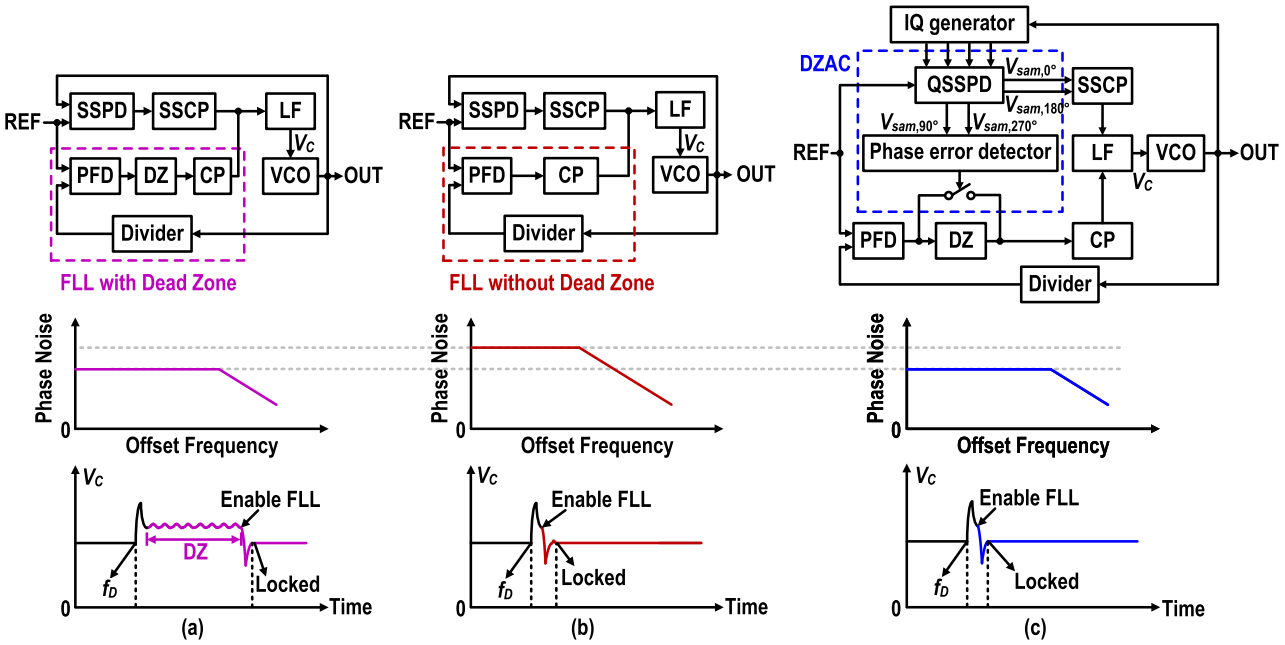


Fig. 1. Architecture comparisons of (a) SSPLL with dead zone in FLL [21], (b) combined PLL without dead zone in FLL [23], and (c) proposed FL-SSPLL with DZAC.

simultaneously. However, once the propagation delay of phase error between subsampling loop (SSL) and FLL exceeds the detection range of FLL, false lock may occur. Hence, an extra off-chip propagation delay calibration is required. Therefore, the design of mm-wave PLL with merits of the wide output frequency range, low jitter, and fast locking still remains a great challenge.

In this article, a wideband mm-wave fast-locking SSPLL (FL-SSPLL) with low jitter and high jitter-power figure of merit (FoM$_j$) is proposed [35]. A quadrature SSPD (QSSPD)-based dead zone automatic controller (DZAC) is introduced to automatically trigger the FLL for fast locking. Here, the long locking time waiting for exceeding the dead zone of FLL is avoided. The proposed FL-SSPLL is fabricated in a 40-nm CMOS technology, which exhibits a wide output frequency range of 62.5% from 21.8 to 41.6 GHz. The integrated root-mean-square (rms) jitter within the whole frequency range is from 62.7 to 79.1 fs, which leads to a PLL FoM$_j$ from -248.3 to -251.4 dB. Meanwhile, the FL-SSPLL features a robust lock acquisition and achieves less than 1.5-μs locking time. This article is organized as follows. In Section II, the architecture and operation of the wideband FL-SSPLL are presented, while the locking time improvement for activating FLL is analyzed. The implementations of the proposed FL-SSPLL and building blocks are provided in Section III. Besides, the locking time under different initial conditions and phase noises of the FL-SSPLL is discussed. In Section IV, measurements of the FL-SSPLL are provided and compared. Finally, a conclusion is given in Section V.

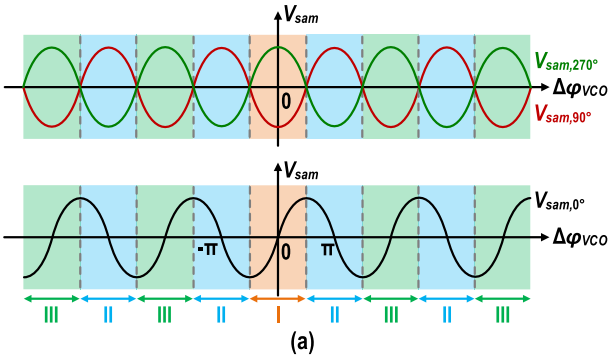
II. Architecture and Principle

A. FL-SSPLL Architecture

Fig. 1(a)–(c) compares the conventional SSPLL with dead zone [21], the combined PLL without dead zone in FLL [23], and the proposed FL-SSPLL with DZAC, respectively. V_C is the control voltage of VCO. The proposed FL-SSPLL consists of two feedback loops (i.e., SSL and FLL). The SSL is used for close-in phase lock to achieve low in-band phase noise. The FLL is introduced to ensure correct frequency locking. Note that the QSSPD-based DZAC is implemented to achieve fast switching between the two loops. An IQ generator is introduced to generate quadrature signals, which are sampled by a sample-and-hold circuit of the QSSPD. Then, four sampling voltages (i.e., $V_{\text{sam},0^\circ}$, $V_{\text{sam},90^\circ}$, $V_{\text{sam},180^\circ}$, and $V_{\text{sam},270^\circ}$) are obtained. $V_{\text{sam},0^\circ}$ and $V_{\text{sam},180^\circ}$ are the inputs of differential subsampling CP (SSCP). The phase error detector processes $V_{\text{sam},90^\circ}$ and $V_{\text{sam},270^\circ}$ of the QSSPD outputs. The result is used to enable or disable the dead zone and control the FLL. Here, the FLL is active when the phase error exceeds the QSSPD phase-detecting range of $\pi/2$. Compared to the architecture of Fig. 1(a), the proposed FL-SSPLL avoids the long locking time waiting for exceeding dead zone. Compared to the architecture of Fig. 1(b), the FLL in the proposed FL-SSPLL is disabled during the locking state, which does not introduce additional noise. Therefore, the FL-SSPLL achieves the low in-band phase noise and fast locking simultaneously. Meanwhile, the DZAC is determined by the QSSPD in the SSL and is not related to the FLL. The phase error propagation delay between FLL and SSL does not exist. Compared to [26] and [30], the proposed FL-SSPLL does not need an extra propagation delay calibration circuit. Moreover, the extra propagation delay calibration circuit varies from frequency and the design complexity is increased, especially for VCO at mm-wave. Thus, the proposed QSSPD-based DZAC is suitable for wideband mm-wave fast-locking applications.

B. Operation and Block Diagram of DZAC

As depicted in Fig. 2(a), the phase error between VCO and reference (i.e., $\Delta\phi_{\text{VCO}}$) is divided into three kinds of regions (i.e., region I: marked in orange, region II: marked in blue, and



Region	Characteristic	Phase Error
I	$V_{sam,90°}<V_{sam,270°}$	$\lvert\Delta\varphi_{VCO}\rvert<\pi/2$
II	$V_{sam,90°}>V_{sam,270°}$	$2k\pi+\pi/2<\lvert\Delta\varphi_{VCO}\rvert\leq 2k\pi+3\pi/2$
III	$V_{sam,90°}<V_{sam,270°}$	$2k\pi+3\pi/2<\lvert\Delta\varphi_{VCO}\rvert\leq 2k\pi+5\pi/2$

(b)

Fig. 2. (a) Operation and characteristic of the proposed QSSPD. (b) Definitions of the three regions.

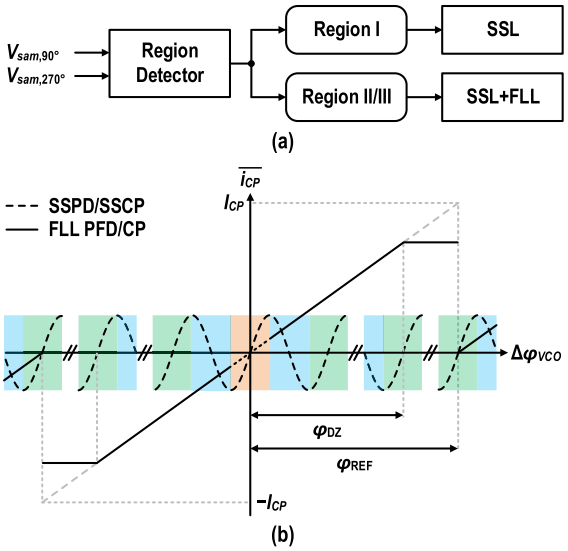


Fig. 3. (a) Region detection for activating the FLL. (b) Transfer characteristics of the proposed SSL and FLL.

region III: marked in green). The three regions are defined as follows:

$$\begin{aligned}&\text{Region I}: |\Delta\phi_{\text{VCO}}| \leq \frac{\pi}{2}\\ &\text{Region II}: 2k\pi + \frac{\pi}{2} < |\Delta\phi_{\text{VCO}}| \leq 2k\pi + \frac{3\pi}{2}\\ &\text{Region III}: 2k\pi + \frac{3\pi}{2} < |\Delta\phi_{\text{VCO}}| \leq 2k\pi + \frac{5\pi}{2}\end{aligned} \quad (1)$$

where k is a natural number. The relationships between $V_{\text{sam},90^\circ}$ and $V_{\text{sam},270^\circ}$ in three regions are arranged in Fig. 2(b). In regions I and III, $V_{\text{sam},90^\circ}$ is less than $V_{\text{sam},270^\circ}$, while $V_{\text{sam},90^\circ}$ is larger than $V_{\text{sam},270^\circ}$ in region II. Note that $\Delta\phi_{\text{VCO}}$ of region I is in the detecting range of QSSPD, which can be removed only by SSL. However, $\Delta\phi_{\text{VCO}}$ in region III is out of such detecting range and requires activating the FLL. The three regions are used to automatically enable or disable the

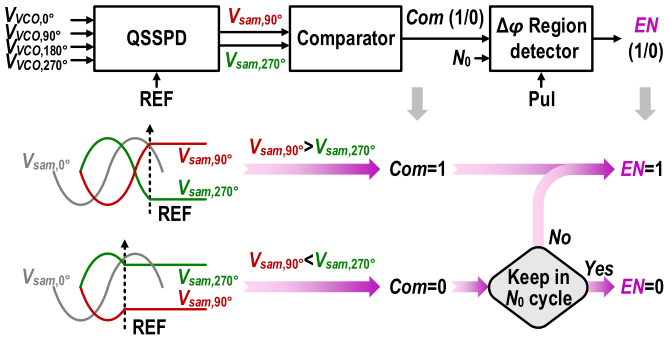


Fig. 4. Block diagram of the proposed QSSPD-based DZAC.

dead zone of FLL. As shown in Fig. 3(a), when $\Delta\phi_{\text{VCO}}$ is in region I, only the SSL is active. Once $\Delta\phi_{\text{VCO}}$ is in region II or III, the FLL and SSL are active. The transfer characteristics of the phase detector in SSL and FLL are shown in Fig. 3(b). When the phase error is in region I, the transfer characteristic of the proposed FL-SSPLL is the same as SSL. However, for the phase error in region II or III, such transfer characteristic is formed by summing the characteristics of PFD and SSPD. To retain the same frequency locking ability of the PFD, the zero output of the proposed phase detector should only occur at $\Delta\phi_{\text{VCO}} = 0$. Then, the proposed phase detector is designed to produce positive currents for all positive $\Delta\phi_{\text{VCO}}$ and negative currents for all negative $\Delta\phi_{\text{VCO}}$.

Fig. 4 depicts the block diagram of the proposed QSSPD-based DZAC. A comparator and a phase error region detector are united to automatically control the dead zone. The output of comparator (i.e., Com) is determined by $V_{\text{sam},90^\circ}$ and $V_{\text{sam},270^\circ}$. Com is 1 once $V_{\text{sam},90^\circ}$ is larger than $V_{\text{sam},270^\circ}$. Thus, for the phase error $\Delta\phi_{\text{VCO}}$ in regions I–III, Com is 0, 1, and 0, respectively. Then, Com is processed by the region detector with a predefined threshold number N_0. Only Com keeps 0 within N_0 cycle of clock (i.e., Pul), and EN is 0. To balance the time of inactivating the FLL and the times of triggering the FLL, N_0 is optimized. Smaller N_0 may cause the FLL to be triggered more times, while larger N_0 results in a longer time of inactivating the FLL. The output EN of the region detector is utilized to control the dead zone of the FLL. EN = 1 indicates that the dead zone is disabled and the FLL is active. The phase error in region I is within the phase-detecting range of the QSSPD, which is removed only by the SSL. Thus, when phase error is in region I, EN is 0. However, the phase error in region II or III needs to be reduced by the FLL. Therefore, EN is 1 in region II or III.

Fig. 5(a) shows the flowchart of the proposed QSSPD-based DZAC. Once $V_{\text{sam},90^\circ}$ is larger than $V_{\text{sam},270^\circ}$, EN is equal to 1 and the FLL is active instantly. Meanwhile, N_p is reset to 0. Here, N_p is the cycle number of clock Pul. To keep the FLL active until $\Delta\phi_{\text{VCO}}$ entering in region I, the comparator compares $V_{\text{sam},90^\circ}$ and $V_{\text{sam},270^\circ}$ at the next Pul cycle (i.e., $N_p = N_p + 1$). The output of the region detector EN is determined by counting N_p of continuous Com = 0. For the phase error entering region III, the FLL keeps changing $\Delta\phi_{\text{VCO}}$. Then, $N_p \geq N_0$ cannot hold. This transition is shown as Case 1 in Fig. 5(b). The FLL maintains active until $\Delta\phi_{\text{VCO}}$ entering region I. For Case 2 in Fig. 5(b), once N_p is no less

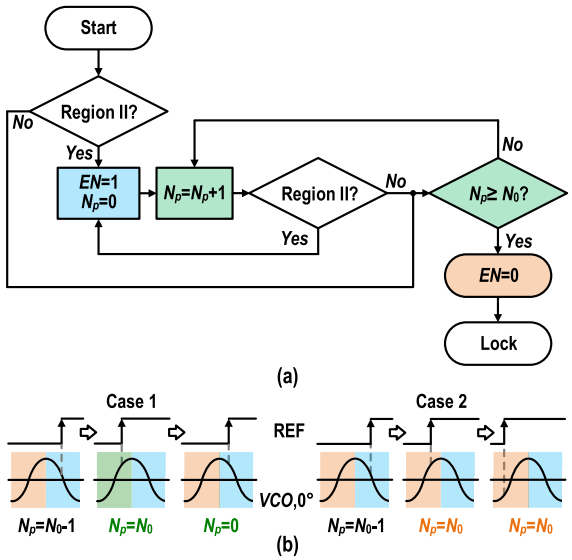
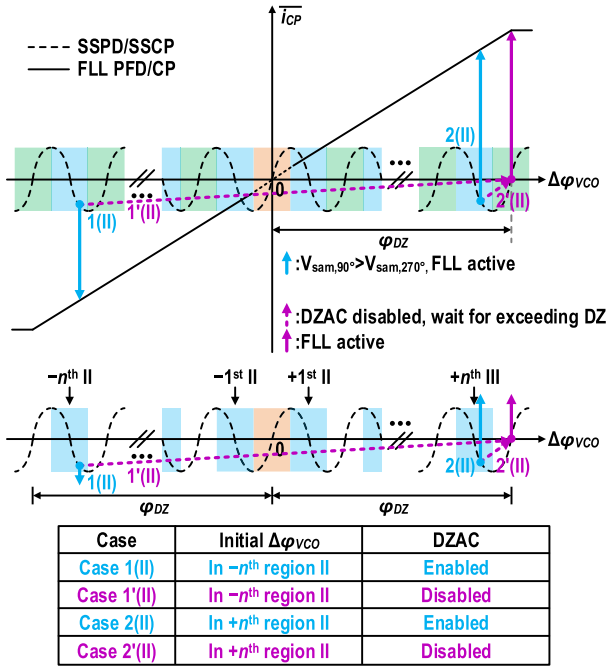


Fig. 5. (a) Flowchart of the proposed QSSPD-based DZAC. (b) Two possible transitions of detection region.



Case	Initial $\Delta\varphi_{VCO}$	DZAC
Case 1(II)	In $-n^{th}$ region II	Enabled
Case 1'(II)	In $-n^{th}$ region II	Disabled
Case 2(II)	In $+n^{th}$ region II	Enabled
Case 2'(II)	In $+n^{th}$ region II	Disabled

Fig. 6. Locking behavior of the proposed FL-SSPLL for the initial phase error in region II.

than N_0, EN is set to 0. Then, the FLL is inactive and the SSL removes the small phase error to achieve locking.

C. Locking Time Improvement in Region II

To analyze the locking behavior under the different initial phase error region, for convenience, the frequency error at initial time is assumed to be positive, causing an increase of $\Delta\phi_{\mathrm{VCO}}$. The value of dead zone (i.e., ϕ_{DZ}) is set as half of the REF cycle (i.e., $\phi_{\mathrm{REF}}/2$). Therefore, the numbers of whole regions II and III within the dead zone are n and $n-1$, respectively. n is expressed as

$$n = \frac{\phi_{\mathrm{DZ}}}{\phi_{\mathrm{VCO}}} \tag{2}$$

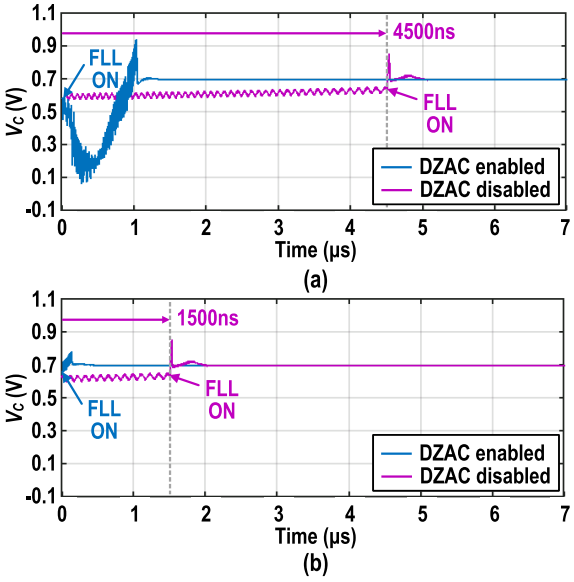


Fig. 7. Simulated time for activating the FLL with enabled and disabled DZAC when initial phase errors are (a) $-0.9\phi_{\mathrm{DZ}}$ and (b) $+0.47\phi_{\mathrm{DZ}}$ in region II.

where ϕ_{VCO} is the phase cycle of VCO signal. Here, the initial phase error within the dead zone is investigated. For the initial phase error exceeding the dead zone, the FLL triggering behavior is the same as conventional SSPLL in [21]. Fig. 6 shows the locking behavior of the proposed FL-SSPLL, when the initial phase error is in region II. For the DZAC enabled, the FLL is immediately active regardless of $\Delta\phi_{\mathrm{VCO}}$ is in which number of region II (i.e., the blue line in Fig. 6). The initial phase errors of Case 1(II) and Case 2(II) are in the $-n$th and $+n$th region II, respectively. The time for activating FLL of Case 1(II) and Case 2(II) is

$$t_{1(\mathrm{II})} = t_{2(\mathrm{II})} = 0. \tag{3}$$

However, for the DZAC disabled, the FLL remains inactive until the phase error exceeds the dead zone (i.e., magenta dotted line in Fig. 6). Once the phase error exceeds the dead zone, the FLL is active (i.e., magenta line in Fig. 6). The FL-SSPLL requires time of $t'_{(\mathrm{II})}$ to active the FLL. The condition that phase error exceeds dead zone after $t'_{(\mathrm{II})}$ is represented as

$$\frac{t'_{(\mathrm{II})}}{t_{\mathrm{REF}}}\Delta(\Delta\phi_{\mathrm{VCO}}) + \Delta\phi_0 > \phi_{\mathrm{DZ}} \tag{4}$$

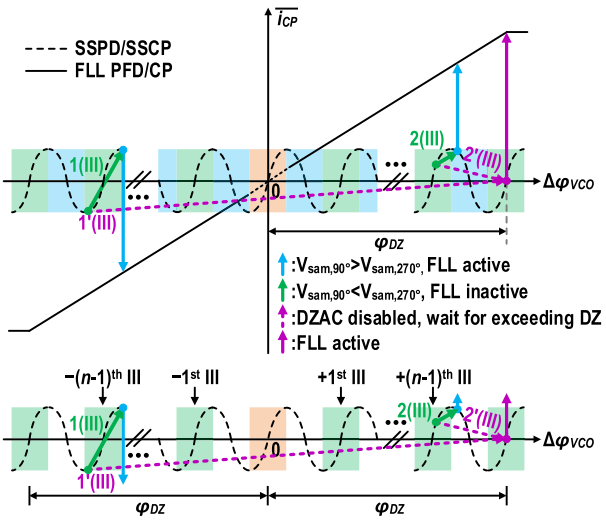
where $\Delta(\Delta\phi_{\mathrm{VCO}})$ is the VCO phase error changed by SSL in one REF cycle and is assumed to be constant and t_{REF} is the period of REF signal. The initial phase error $\Delta\phi_0$ is derived as

$$\Delta\phi_0 = \alpha\left(\frac{\phi_{\mathrm{VCO}}}{4} + \Delta\phi_{\mathrm{II}} + k\phi_{\mathrm{VCO}}\right) \tag{5}$$

where α is expressed as

$$\alpha = \begin{cases} -1, & \Delta\phi_{\mathrm{VCO}} < 0 \\ +1, & \Delta\phi_{\mathrm{VCO}} > 0 \end{cases} \tag{6}$$

and $\Delta\phi_{\mathrm{II}}$ is the phase error within the $(k+1)$th region II. Therefore, the time of activating the FLL with disabled DZAC



Case	Initial $\Delta\varphi_{VCO}$	DZAC
Case 1(III)	In −(n-1)th region III	Enabled
Case 1'(III)	In −(n-1)th region III	Disabled
Case 2(III)	In +(n-1)th region III	Enabled
Case 2'(III)	In +(n-1)th region III	Disabled

Fig. 8. Locking behavior of the proposed FL-SSPLL for the initial phase error in region III.

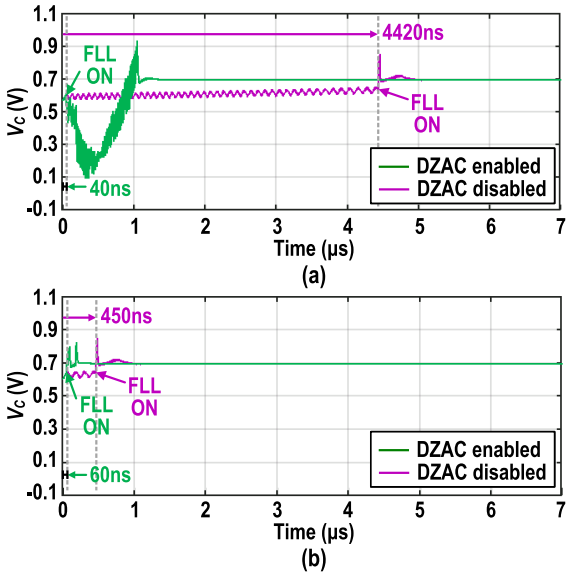


Fig. 9. Simulated time for activating the FLL with enabled and disabled DZAC when initial phase errors are (a) $-0.86\phi_{DZ}$ and (b) $+0.86\phi_{DZ}$ in region III.

is derived as

$$t'_{(II)} = \frac{t_{REF}}{\Delta(\Delta\phi_{VCO})}\left(\frac{4n-4k\alpha-\alpha}{4n}\phi_{DZ} - \alpha\Delta\phi_{II}\right). \quad (7)$$

Here, $t'_{(II)}$ is maximum when $k = n-1$ and $\alpha = -1$. Therefore, the maximum time for activating FLL occurs when the initial $\Delta\phi_{VCO}$ is in the $-n$th region II (i.e., $-2(n-1)\pi - 3\pi/2 < \Delta\phi_{VCO} \le -2(n-1)\pi - \pi/2$).

The behavior of triggering the FLL is shown as Case 1'(II) in Fig. 6. According to (7), such maximum time is approximated as

$$t_{1'(II)} \approx \frac{2\phi_{DZ}}{\Delta(\Delta\phi_{VCO})}t_{REF}. \quad (8)$$

For the initial $\Delta\phi_{VCO}$ in the $+n$th region II (i.e., $2(n-1)\pi + \pi/2 < \Delta\phi_{VCO} \le 2(n-1)\pi + 3\pi/2$), the time for activating FLL is minimum, which is expressed as

$$t_{2'(II)} = \frac{\pi}{2\Delta(\Delta\phi_{VCO})}t_{REF}. \quad (9)$$

The locking behavior is depicted as Case 2'(II) in Fig. 6. Here, k is $n-1$ and α is $+1$. Then, the range of $t'_{(II)}$ is derived as

$$\frac{\pi}{2\Delta(\Delta\phi_{VCO})}t_{REF} < t'_{(II)} < \frac{2\phi_{DZ}}{\Delta(\Delta\phi_{VCO})}t_{REF}. \quad (10)$$

Therefore, according to (3) and (10), no matter which one of region II the initial phase error is in, the FLL is triggered faster with enabled DZAC.

To verify the effect of the proposed QSSPD-based DZAC, transient simulations using behavioral models are conducted. The FL-SSPLL is driven by a reference frequency of 100 MHz. The output frequency of VCO is 24 GHz. The loop filter consists of a parallel capacitor 5 pF and a resistor 2 kΩ in series with a capacitor 100 pF. The bias current of the FLL CP is set to 200 μA so that the FLL dominates the loop control. Here, the FLL is triggered one time for convenient discussion. The timing dead zone is set to 5 ns. Fig. 7 depicts the transient simulations with enabled and disabled DZAC, while the initial phase error is in region II. In Fig. 7(a), the initial phase error is $-0.9\phi_{DZ}$. For the DZAC enabled, the FLL is active immediately. However, with the disabled DZAC, the FLL is inactive until the phase error exceeds $+\phi_{DZ}$. The simulated time of waiting dead zone is 4.5 μs. Fig. 7(b) shows the transient simulation under the initial phase error of $+0.47\phi_{DZ}$. Similar to Fig. 7(a), the FLL with enabled DZAC is active at 0 μs. Nevertheless, with disabled DZAC, the simulated time of 1.5 μs is required to activate the FLL. The transient simulations in Fig. 7 are consistent with the locking behavior analysis in Fig. 6.

D. Locking Time Improvement in Region III

Fig. 8 shows the locking behavior of the proposed FL-SSPLL for the initial phase error in region III. Similarly, the initial frequency error is assumed to be positive, leading to an increase in $\Delta\phi_{VCO}$. When the DZAC is enabled, once the phase error changes from region III to region II, the FLL is active immediately (i.e., the green line in Fig. 8). The FL-SSPLL requires the time of $t_{(III)}$ to active the FLL. The condition that phase error enters region II after $t_{(III)}$ is represented as

$$\frac{t_{(III)}}{t_{REF}}\Delta(\Delta\phi_{VCO}) + \Delta\phi_0 > \frac{\phi_{VCO}}{2}. \quad (11)$$

Here, the adjacent region II is assumed to enter. For the initial phase error at $+(2k\pi + 3\pi/2)$ or $-(2k\pi + 5\pi/2)$ of region III, the time for activating the FLL is maximum. In order to enter adjacent region II, the phase error is required to exceed $\phi_{VCO}/2$. Such locking behavior is depicted as Case 1(III). The time for activating FLL is expressed as

$$t_{1(III)} = \frac{\pi}{\Delta(\Delta\phi_{VCO})}t_{REF}. \quad (12)$$

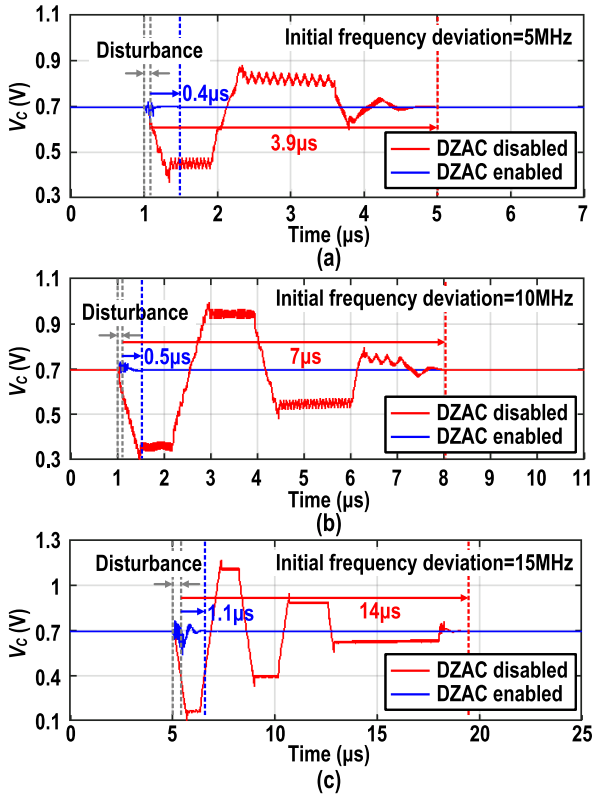


Fig. 10. Simulated locking time of FL-SSPLL operating at 24 GHz under different initial frequency deviations. (a) 5 MHz. (b) 10 MHz. (c) 15 MHz.

The minimum time for activating the FLL occurs when the initial phase error is at $+(2k\pi + 5\pi/2)$ or $-(2k\pi + 3\pi/2)$. The phase error enters adjacent region II at the next REF cycle. The locking behavior is shown as Case 2(III) in Fig. 8. The time for activating FLL in Case 2(III) is derived as

$$t_{2(\mathrm{III})} = t_{\mathrm{REF}}. \tag{13}$$

However, for DZAC disabled, the time of activating the FLL is expressed as

$$t'_{(\mathrm{III})} = \frac{t_{\mathrm{REF}}}{\Delta(\Delta\phi_{\mathrm{VCO}})}\left(\frac{4n - 4k\alpha - 3\alpha}{4n}\phi_{\mathrm{DZ}} - \alpha\Delta\phi_{\mathrm{III}}\right). \tag{14}$$

The maximum time to activate FLL occurs at Case 1'(III). Here, the initial $\Delta\phi_{\mathrm{VCO}}$ is in the $-(n-1)$th region III (i.e., $-2(n-2)\pi - 5\pi/2 < \Delta\phi_{\mathrm{VCO}} \leq -2(n-2)\pi - 3\pi/2$). k is $n-2$ and α is -1. Such maximum time is approximated as

$$t_{1'(\mathrm{III})} \approx \frac{2\phi_{\mathrm{DZ}}}{\Delta(\Delta\phi_{\mathrm{VCO}})}t_{\mathrm{REF}}. \tag{15}$$

The minimum time for activating FLL occurs when $\Delta\phi_{\mathrm{VCO}}$ is in the $+(n-1)$th region III (i.e., $2(n-2)\pi + 3\pi/2 < \Delta\phi_{\mathrm{VCO}} \leq 2(n-2)\pi + 5\pi/2$), which is expressed as

$$t_{2'(\mathrm{III})} = \frac{3\pi}{2\Delta(\Delta\phi_{\mathrm{VCO}})}t_{\mathrm{REF}}. \tag{16}$$

k is $n-2$ and α is $+1$. Such locking behavior is shown as Case 2'(III). Therefore, when the initial phase error is in region III, the locking time improvement of activating FLL with enabled DZAC is set as

$$\frac{3}{2} < \frac{t'_{(\mathrm{III})}}{t_{(\mathrm{III})}} < \frac{2\phi_{\mathrm{DZ}}}{\Delta(\Delta\phi_{\mathrm{VCO}})} \tag{17}$$

where $t'_{(\mathrm{III})}$ and $t_{(\mathrm{III})}$ are the time with disabled and enabled DZAC, respectively.

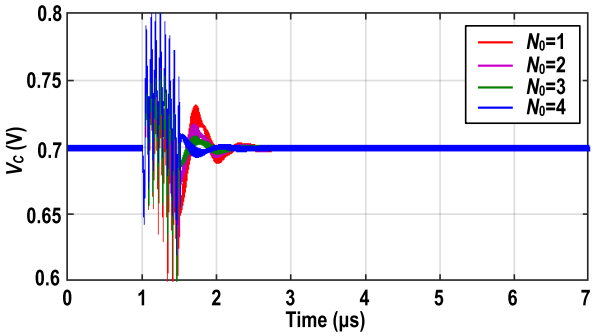


Fig. 11. Simulated locking time under different N_0's.

Fig. 9 shows the simulated time for activating FLL with enabled and disabled DZAC when the initial phase error is in region III. Here, N_0 is set as 2. In Fig. 9(a), the initial phase error is $-0.86\phi_{\mathrm{DZ}}$. For the DZAC enabled, the FLL is active after 40 ns. However, with the disabled DZAC, the simulated time of waiting dead zone is 4420 ns. Fig. 9(b) shows the transient simulation when the initial phase error is $+0.86\phi_{\mathrm{DZ}}$. The FLL with enabled DZAC is active at 60 ns. Nevertheless, the simulated time of 450 ns is required to activate the FLL with disabled DZAC. The transient simulations in Fig. 9 are consistent with the locking behavior analysis in Fig. 8. Therefore, according to the simulations in Figs. 7 and 9, the time for activating the FLL with enabled DZAC is faster regardless of initial phase error.

E. Analysis of the Robustness of the Proposed FL-SSPLL

When the FL-SSPLL is pushed out of lock by a disturbance, the FLL engages the relocking process once the phase error exceeds region I (i.e., $\pi/2$ referring to VCO). To investigate the relocking behavior, transient simulations using behavioral models are introduced. As shown in Fig. 10, a disturbance is injected into the loop to observe the locking operation of the FL-SSPLL at 24 GHz. When the initial frequency deviation is 5 MHz, the simulated locking time of the FL-SSPLL with disabled DZAC is 3.9 μs. On the other hand, under the same disturbance, the FL-SSPLL with enabled DZAC recovers to a steady state within 0.4 μs. The simulated locking time is improved more than 9× with the enabled DZAC. Besides, when the initial frequency deviations are 10 and 15 MHz, the locking time is 7 and 14 μs with DZAC disabled, respectively. However, the locking times are reduced to 0.5 and 1.1 μs by enabling the DZAC. Thus, the proposed FL-SSPLL achieves robust lock acquisition. Fig. 11 shows the locking time under different N_0's. The larger N_0 leads to shorter locking time in sacrifice of more components and power consumption.

Fig. 12 shows the impact of phase error ϕ_e from the IQ generator and QSSPD on DZAC. The sampling voltages $V_{\mathrm{sam},90^\circ}$ and $V_{\mathrm{sam},270^\circ}$ are changed to $V'_{\mathrm{sam},90^\circ}$ and $V'_{\mathrm{sam},270^\circ}$

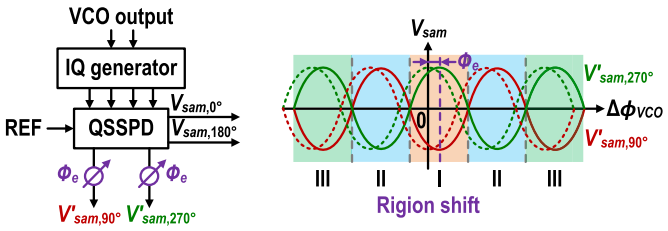


Fig. 12. Effects of quadrature phase error on DZAC.

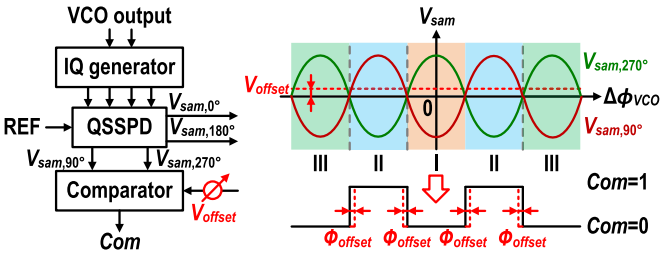


Fig. 13. Effects of comparator offset on DZAC.

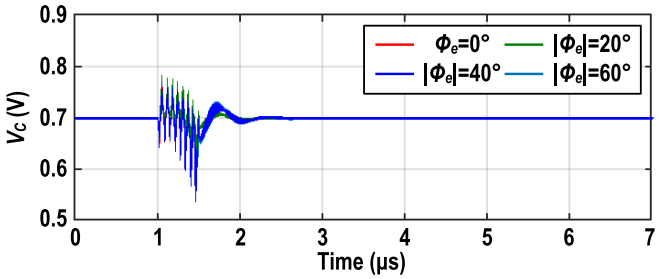


Fig. 14. Simulated locking time under different quadrature phase errors.

with phase error ϕ_e, respectively. Thus, the region detection is shifted ϕ_e. The three regions are updated from (1) as follows:

$$\begin{aligned}
&\text{Region I}' : -\frac{\pi}{2}+\phi_e < \Delta\phi_{\text{VCO}} \le \frac{\pi}{2}+\phi_e \\
&\text{Region II}' : 2k\pi+\frac{\pi}{2}+\phi_e < \Delta\phi_{\text{VCO}} \le 2k\pi+\frac{3\pi}{2}+\phi_e \\
&\text{and} \quad -2k\pi-\frac{3\pi}{2}+\phi_e \le \Delta\phi_{\text{VCO}} < -2k\pi-\frac{\pi}{2}+\phi_e \\
&\text{Region III}' : 2k\pi+\frac{3\pi}{2}+\phi_e < \Delta\phi_{\text{VCO}} \le 2k\pi+\frac{5\pi}{2}+\phi_e \\
&\text{and} \quad -2k\pi-\frac{5\pi}{2}+\phi_e \le \Delta\phi_{\text{VCO}} < -2k\pi-\frac{3\pi}{2}+\phi_e.
\end{aligned} \tag{18}$$

Fig. 13 shows the impact of comparator offset on DZAC. Com = 1 is resulted by $V_{\text{sam},90°} > V_{\text{sam},270°}$. Due to the comparator offset, the range of Com = 1 reduces twice of ϕ_{offset}, where ϕ_{offset} is the offset of region II caused by comparator offset. Then, (1) is updated as follows:

$$\begin{aligned}
&\text{Region I}'' : -\frac{\pi}{2}-\phi_{\text{offset}} < \Delta\phi_{\text{VCO}} \le \frac{\pi}{2}+\phi_{\text{offset}} \\
&\text{Region II}'' : 2k\pi+\frac{\pi}{2}+\phi_{\text{offset}} < |\Delta\phi_{\text{VCO}}| \\
&\qquad \le 2k\pi+\frac{3\pi}{2}-\phi_{\text{offset}} \\
&\text{Region III}'' : 2k\pi+\frac{3\pi}{2}-\phi_{\text{offset}} < |\Delta\phi_{\text{VCO}}|
\end{aligned}$$

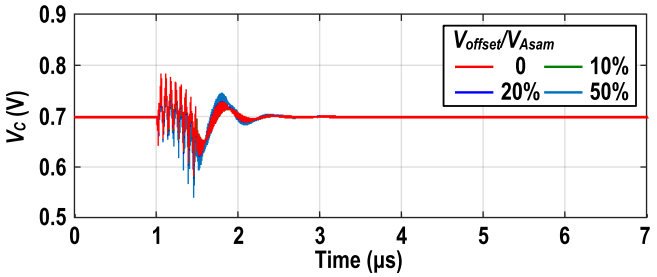


Fig. 15. Simulated locking time under different comparator offsets.

$$\le 2k\pi+\frac{5\pi}{2}+\phi_{\text{offset}}. \tag{19}$$

From (18) and (19), when the SSPLL is locking, the phase error is detected in region I and the DZAC inactivates the FLL. Thus, the in-band phase noise performance is not influenced by ϕ_e and V_{offset}. Besides, ϕ_e and V_{offset} affect the first time of activating FLL. Once the FLL is active, ϕ_e and V_{offset} have less influence on the locking time. Figs. 14 and 15 show the simulated locking time under different quadrature phase errors and comparator offsets, respectively. The phase error ϕ_e shows less influence on relock time within 60° quadrature phase error. Meanwhile, the comparator offset V_{offset} introduces less influence on relock time within $V_{\text{offset}}/V_{\text{Asam}}$ of 50%.

III. Circuit Implementation

Based on the principle investigated in Section II, a wideband low jitter FL-SSPLL with DZAC is implemented using a conventional 40-nm CMOS technology. Fig. 16 shows the diagram of the proposed FL-SSPLL. For convenient test, an on-chip divider-by-2 is used for output of lower frequency. In order to fully verify the performance of the proposed FL-SSPLL architecture in wideband mm-wave operation, a quad-mode mm-wave oscillator is integrated in the FL-SSPLL. In this architecture, a quadrature frequency divider is introduced to generate quadrature signals.

A. Quad-Mode Oscillator

The schematic of the quad-mode oscillator is shown in Fig. 17. A quad-core oscillator using the electric-magnetic (E–M) mixed-coupling resonance boosting technique is used [38], which achieves quad-mode operation frequency and low phase noise simultaneously. The E–M mixed-coupling resonator is investigated to generate four reconfigurable resonances. The 2-D mode switch array is introduced to achieve the quad-mode switching and avoid the concurrent oscillation without introducing loss to the resonator. The switching circuits lock the output phases of the four coupled cores in different states, thus forcing the LC network to work in the corresponding modes [39], [40]. The mode switches are realized by pMOS operated at ON/OFF states. The size of pMOS is 6 μm/40 nm corresponding to an ON-conductance around 5 mS, which effectively avoids the multiresonance oscillation.

B. DZAC and FLL With Controllable Dead Zone

Fig. 18 shows the schematic of the quadrature frequency divider and QSSPD. Such quadrature frequency divider

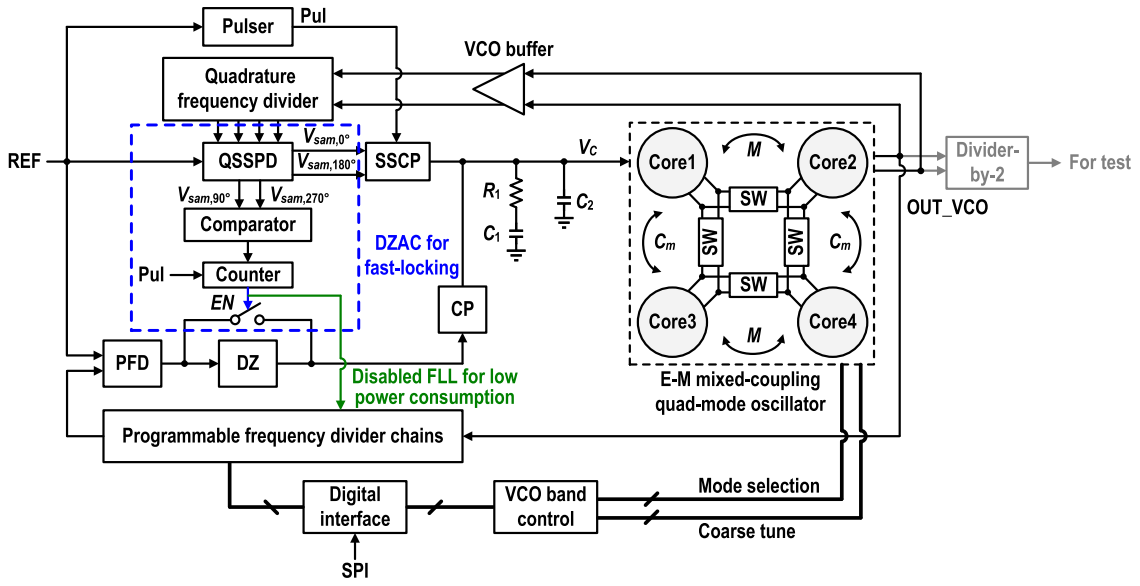


Fig. 16. Block diagram of the proposed wideband FL-SSPLL architecture.

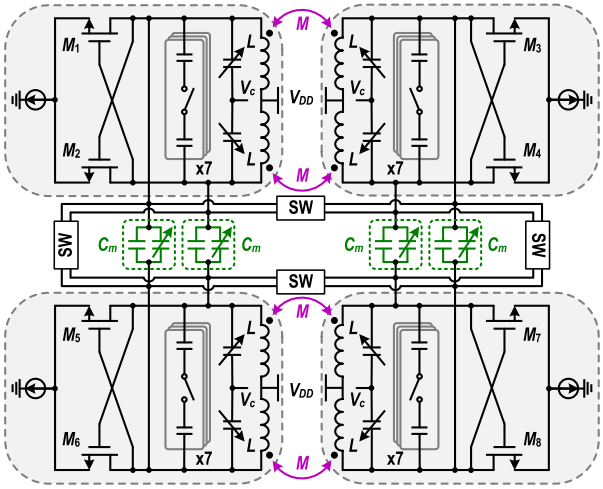


Fig. 17. Schematic of the proposed quad-mode oscillator.

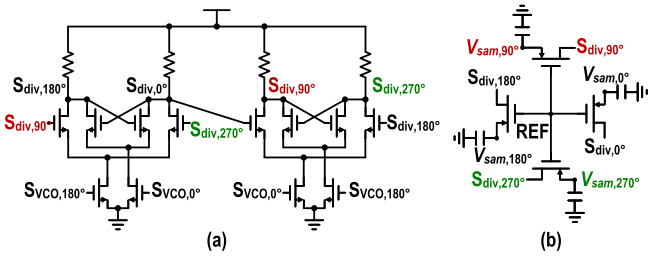


Fig. 18. Schematic of (a) quadrature frequency divider and (b) QSSPD.

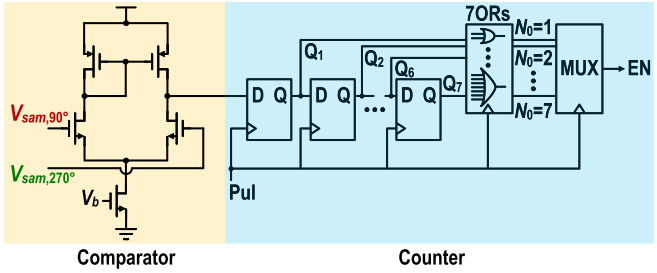


Fig. 19. Schematic of the comparator and counter.

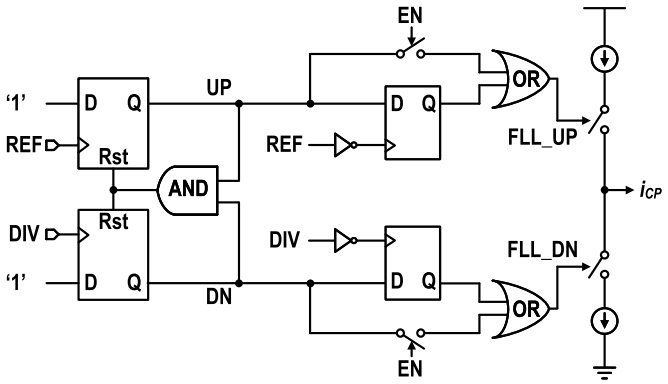


Fig. 20. Proposed PFD/CP with controllable dead zone.

consisting of two current-mode logic (CML) latches is used to generate the IQ signals over the wide operation frequency range. The latch circuit comprises two differential transistor pairs with common loads and a differential current source. The simulated quadrature phase error is within 0.02° over the input frequency range from 20 to 50 GHz. The QSSPD is implemented simply with four pMOS transistors and capacitors to sample the outputs of quadrature frequency divider. Meanwhile, the output of the divider is square wave, while subsampling techniques require sine wave. An *RC* low-pass filter is hence deployed in series of divider to shape square wave to sine wave. Four source follower buffers isolate the QSSPD from the divider. Fig. 19 depicts the schematic of the comparator and counter. The comparator is used to compare the sampling voltages $V_{\text{sam},90^\circ}$ and $V_{\text{sam},270^\circ}$. Afterward, the result of comparison is utilized for counter to generate the dead zone control signal EN. The counter consists of seven D-flip-flops, seven OR logic gates, and a multiplexer. Here, the multiplexer is programmable for selecting optimized N_0 to distinguish regions I and III. The simulated power consumption of counter is from 28.5 to 199.5 μW with N_0 increased

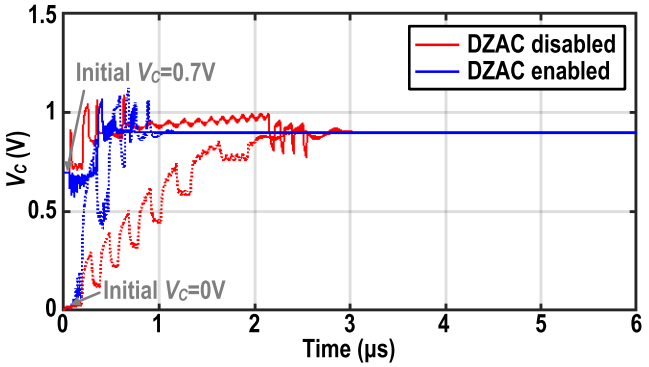


Fig. 21. Simulated locking transient under different initial V_C's.

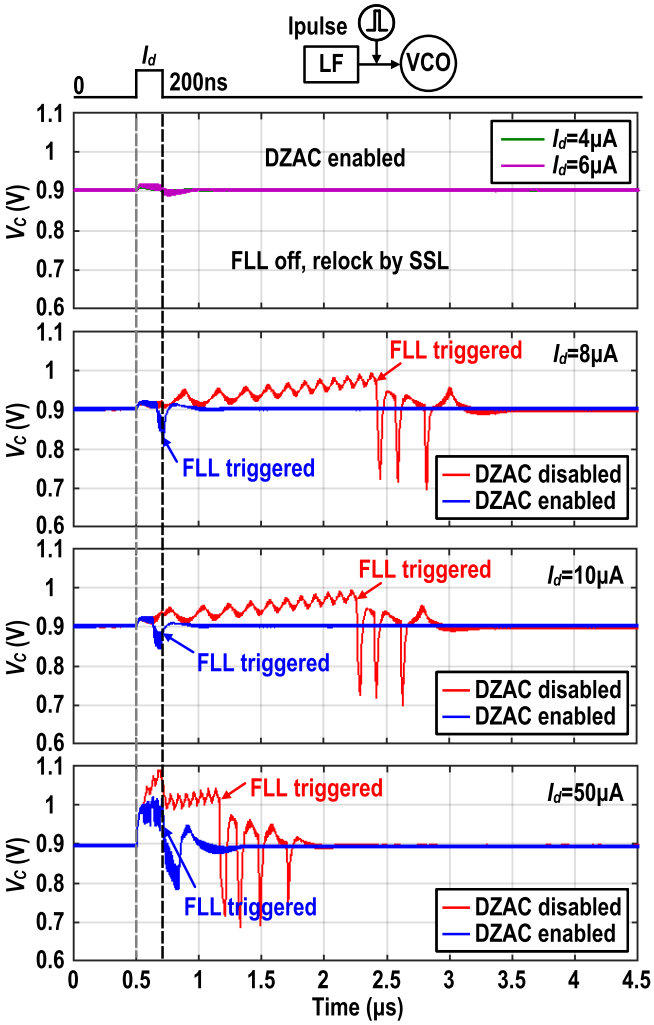


Fig. 22. Simulated relock transient under different disturbances.

from 1 to 7. The proposed FLL consists of a wideband frequency divider chain, a three-state PFD with controllable dead zone, and a CP. Such wideband frequency divider chain is composed of two CML frequency dividers, two dual-mode (i.e., divide-by-2 or divide-by-3) true single phase clock (TSPC) dividers, and a programmable TSPC divider. Fig. 20 shows the schematic of the proposed three-state PFD/CP with controllable dead zone. Compared to the conventional PFD in [21], two switches and OR gates are inserted to control the

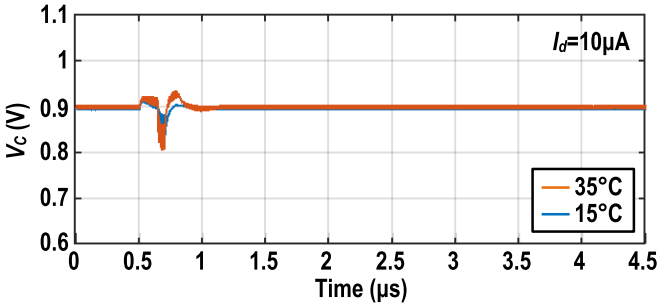


Fig. 23. Simulated relock transient under different temperatures.

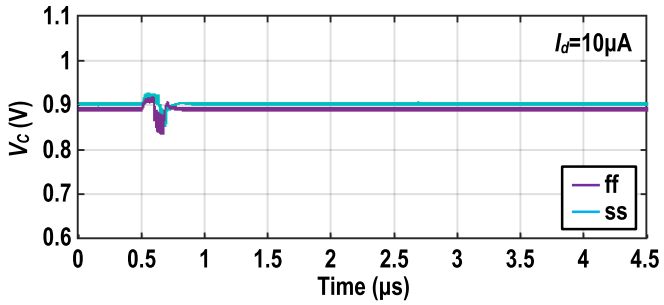


Fig. 24. Simulated relock transient under different corners.

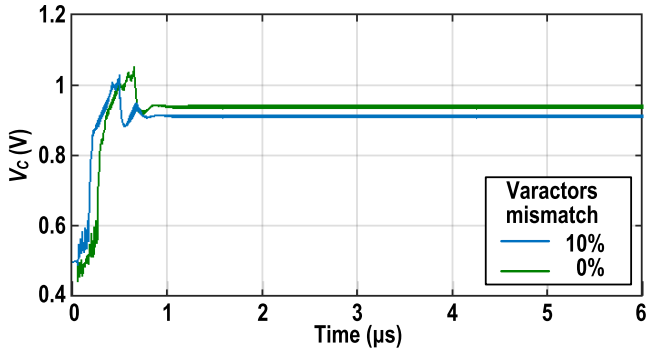


Fig. 25. Simulated locking time with mismatches between four varactors.

dead zone. The control signal EN is generated by the DZAC in Fig. 19.

C. Locking Time Discussion

Fig. 21 shows the simulated locking transient under different initial V_C. The locking time is shorter with DZAC enabled under different initial V_C's. Fig. 22 depicts the simulated relock transient under different disturbances. When the phase error is within the SSL range, the relock time with and without DZAC is the same. However, once the frequency mismatch exceeds 8 μA, the relock time of SSPLL with DZAC disabled soars rapidly, due to its poor capture ability. In contrast, the relock time of SSPLL with DZAC enabled can always maintain a relatively low value across the whole disturbance range. The simulated relock time under 10-μA disturbance with DZAC enabled at 35 °C and 15 °C is shown in Fig. 23. The proposed FL-SSPLL with DZAC enabled shows robust locking versus temperature variation. Fig. 24 shows the simulated relock time under 10-μA disturbance with DZAC enabled at ff and ss corners. The simulated relock time is less than 0.3 μs. The mismatch of the capacitance in varactor

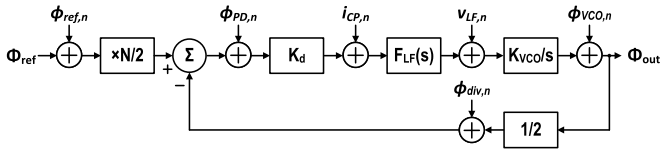


Fig. 26. Phase-domain model of the proposed FL-SSPLL with quadrature frequency divider-by-2.

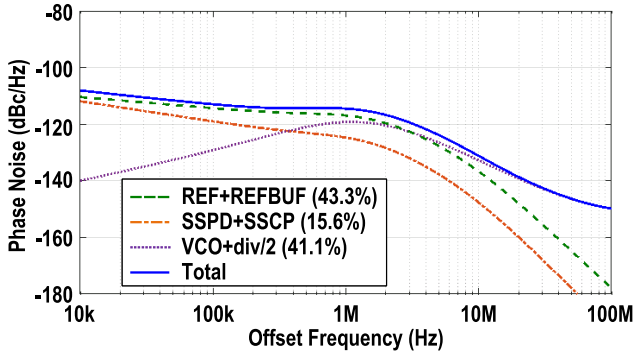


Fig. 27. Simulated phase noise contribution of different FL-SSPLL blocks at 12 GHz after divider-by-2.

leads to the change of VCO output frequency variation. Fig. 25 depicts the simulated locking time with the mismatch of 10% between the varactors. V_C is changed due to such a mismatch, while the target locking frequency is the same. In this work, by using the proposed DZAC-based FLL, the PLL achieves fast locking, while the locking time has low variation.

D. Phase Noise Analysis

When the reference clock samples the $f_{\mathrm{VCO}}/2$ output, the phase error between $f_{\mathrm{VCO}}/2$ and f_{REF} is half of that between f_{VCO} and f_{REF}. VCO-divided-by-2 is considered as a single VCO as a whole; thus, the frequency-locking range of the VCO-divided-by-2 sampling PLL is increased by two times [6]. Fig. 26 shows the phase-domain model of the proposed FL-SSPLL with quadrature frequency divider-by-2. The open-loop phase transfer function of the FL-SSPLL at a steady state can be derived as

$$H_{\mathrm{OL}}(s) = K_d \cdot F_{\mathrm{LF}}(s) \cdot \frac{K_{\mathrm{VCO}}}{s} \cdot \frac{1}{2} \tag{20}$$

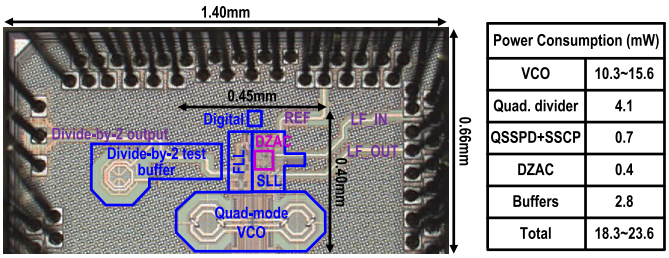
where K_d is the SSCP feedback gain, $F_{\mathrm{LP}}(s)$ is the transimpedance of the loop filter, and K_{VCO} is the gain of the VCO. According to Fig. 26, the following shows the noise transfer functions of the current noise associated with the SSCP to the output phase noise:

$$H_{n,\mathrm{CP}}(s) = \frac{1}{K_d} \frac{2H_{\mathrm{OL}}(s)}{1 + H_{\mathrm{OL}}(s)}. \tag{21}$$

In the steady state, the VCO phase error is small, and (21) can be rewritten as

$$H_{n,\mathrm{CP}}(s) = \frac{T_{\mathrm{REF}}}{2g_m A_{\mathrm{div}} t_{\mathrm{pul}}} \frac{2H_{\mathrm{OL}}(s)}{1 + H_{\mathrm{OL}}(s)}. \tag{22}$$

The noise contribution of the SSCP increases with 2 according to (22). From (22), it can be seen that it is possible to reduce the noise contribution of the SSCP by increasing the output amplitude of divider-by-2 (A_{div}) and pulsewidth of pulser (t_{pul}).



Power Consumption (mW)	
VCO	10.3~15.6
Quad. divider	4.1
QSSPD+SSCP	0.7
DZAC	0.4
Buffers	2.8
Total	18.3~23.6

Fig. 28. Chip micrograph and power breakdown table.

In this design, A_{div} is 0.3 V and t_{pul} is tunable between 0.6 and 2.4 ns. Since noise from the CP is suppressed by the relatively high phase detection gain when transferred to the PLL output, the in-band phase noise is dominated by reference and reference buffer. The reference buffer in this work is implemented by a chain of CMOS buffers with its first stage being sized large enough to convert a sine wave into a quasi-square wave. The buffer chain consumes a total power of 0.56 mW to keep the SSPLL in-band phase noise lower than −110 dBc/Hz.

Fig. 27 depicts the simulated phase noise contribution of different FL-SSPLL blocks at 12-GHz output frequency after divider-by-2. R_1, C_1, and C_2 of loop filter are 2 kΩ, 5 pF, and 100 pF, respectively. The integrated phase noise contribution of the reference with reference buffer, SSPD with SSCP, and VCO with divide-by-2 is 43.3%, 15.6%, and 41.1%, respectively.

IV. Fabrication and Measurement

The proposed FL-SSPLL is designed and fabricated in a conventional 40-nm CMOS technology. The chip micrograph and the power breakdown table are shown in Fig. 28. The active area of FL-SSPLL is 0.18 mm^2. In order to reserve the capacity of modifying loop bandwidth, the loop filter is off-chip in this work. In the measurement, the value of loop filter is not adjusted. The power consumption is 18.3–23.6 mW, excluding the test buffer. The proposed DZAC consumes only 0.4 mW, which is 1.7% of the overall power consumption. The typical power consumption of the FLL is 6.2 mW. The FLL is disabled after the FL-SSPLL is locked. The reference frequency is 100 MHz. The proposed FL-SSPLL achieves a 62.5% tuning range from 21.8 to 41.6 GHz. The frequency ranges of each mode are 21.8–25.5, 23.8–29.2, 28.6–33.2, and 32.7–41.6 GHz. All the overlaps between the adjacent modes are wider than 0.5 GHz.

Fig. 29 shows the measured phase noise in the four modes. At the 100-kHz frequency offset, the measured phase noises are −106.01 dBc/Hz at 21.8 GHz in mode 1, −105.44 dBc/Hz at 24 GHz in mode 2, −101.67 dBc/Hz at 32.4 GHz in mode 3, and −96.2 dBc/Hz at 41.6 GHz in mode 4. The measured output integrated jitters are 62.7, 69.6, 74.9, and 79.1 fs at 21.8, 24, 32.4, and 41.6 GHz, respectively. Fig. 30 depicts the measured spectrums in the four modes. The measured reference spurs are −53.2, −54.1, −52.8, and −46.1 dBc at 21.8, 24, 32.4, and 41.6 GHz, respectively. Fig. 31 shows the measured jitter and spur level over the operating frequency. The measured output integrated jitter is from 62.7 to 79.1 fs

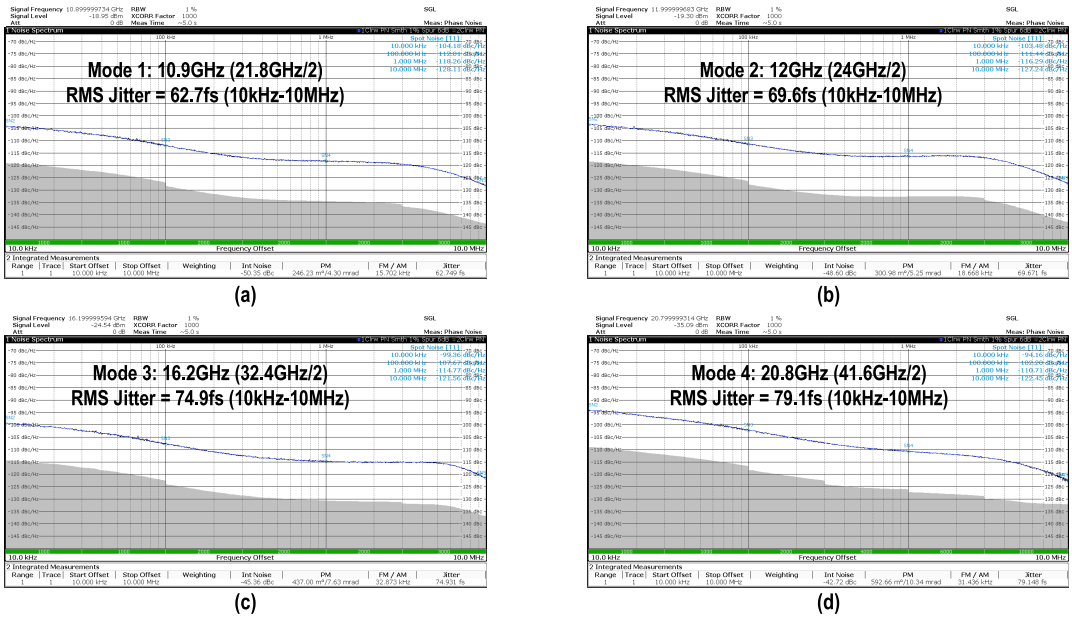


Fig. 29. Measured phase noise of the FL-SSPLL in four oscillator modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

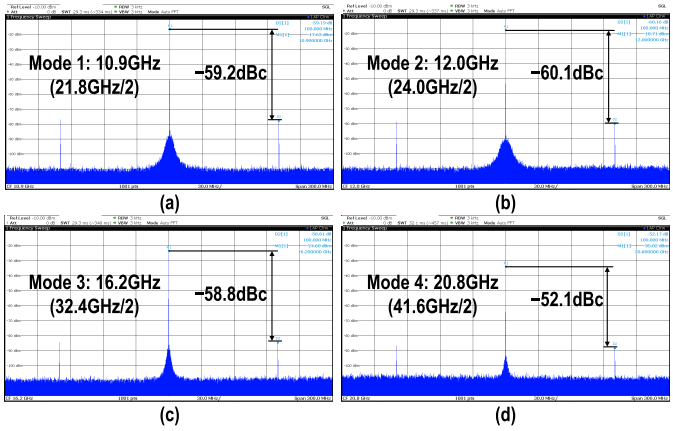


Fig. 30. Measured spectrum of the FL-SSPLL in four oscillator modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

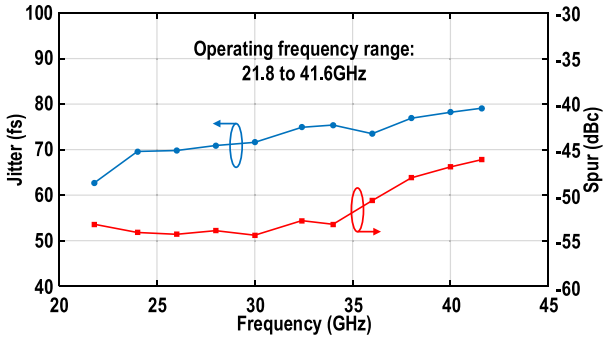


Fig. 31. Measured jitter and spur level over the operating frequency.

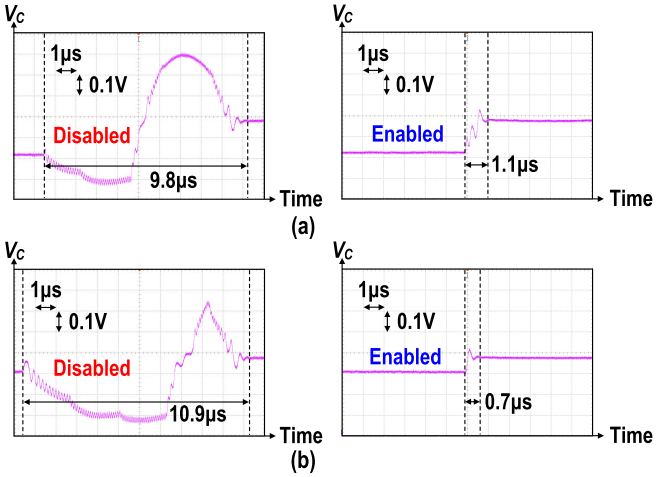


Fig. 32. Measured locking transient behavior of the FL-SSPLL under 100-MHz initial frequency deviation with DZAC disabled and enabled. (a) Locking at 24 GHz. (b) Locking at 40 GHz.

within the operation frequency range, leading to FoM$_j$ from −248.3 to −251.4 dB. The measured reference spur is from −54.4 to −46.1 dBc, which is restored from the measured output with on-chip divider-by-2. The reference spur may be further suppressed by using more stages of VCO buffers for isolation or utilizing improved phase detectors such as in [41] and [42].

Fig. 32 shows the measured locking behaviors of the proposed FL-SSPLL under 100-MHz initial frequency deviation. As shown in Fig. 32(a), the divide ratio N is switched from 240 to 241. The output frequency changes from 24 to 24.1 GHz. The measured locking time is 9.8 μs when the DZAC is disabled. Note that the long locking time due to the dead zone is clearly demonstrated. However, the locking time is reduced to 1.1 μs with enabled DZAC. The proposed FL-SSPLL achieves 8.9× locking time improvement with enabled DZAC. Similarly, as shown in Fig. 32(b), the divide ratio N is switched from 400 to 401. The locking time is 10.9 and 0.7 μs with disabled and enabled DZAC, respectively. The locking time improvement of the proposed FL-SSPLL is 15.5×. Fig. 33 depicts the measured locking time across the operating frequency range with different initial frequency deviations of 100, 200, and 300 MHz. The locking time is less than 1.5 μs with the enabled DZAC.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS

Ref.	TCAS-I'15 [23]	JSSC'18 [26]	JSSC'20 [9]	JSSC'20 [5]	TMTT'21 [31]	TMTT'22 [13]	JSSC'23 [36]	**This Work**
Architecture	PFD+SSPD	SSPLL	RSPLL+ILFM	BB-DPLL	SSPLL	QS-PFD PLL	SSPLL	**FL-SSPLL**
Technology	65nm CMOS	130nm CMOS	45nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	**40nm CMOS**
Output Frequency (GHz)	2.05 to 2.2	2.39 to 2.46	33.6 to 36	22.5 to 27.7	40.5	36.4 to 40.6	7.9 to 14.3	**21.8 to 41.6**
Tuning Range (%)	7	3	6.8	20.7	N/A	10.9	57.7	**62.5**
REF Frequency (MHz)	50	50	80	216	100	280 to 320	100	**100**
RMS Jitter (fs) @f_{out}(GHz) (Integ. Range)	484 @2.2 (10k-10M)	158 @2.4 (10k-10M)	251 @35.84 (10k-10M)	220 @24 (10k-20M)	228 (10k-100M)	121.9 to 169.4 (10k-100M)	77.0 to 84.6 (1k-30M)	**62.7 to 79.1 (10k-10M)**
Locking Time (μs) (Disturbance)	0.9 (9.1MHz f_{out})	20 (150mV V_{DD})	N/A (has FTL)	45 (27MHz f_{out})	3.2 (300mV V_C)	6 (20MHz f_{out})	N/A (has DZ)	**<1.5 (300MHz f_{out} or 100mV V_{DD})**
Reference Spur (dBc)	−41.6 @2.2GHz	−72 @2.4GHz	−60 @35.84GHz	−65 @24GHz	−42	−75 @38.4GHz	−46.4 to −54	**−46.1 to −54.4**
Power Consumption (mW)	8.8	21	20.6	25	9.6	23.6	14.1 to 17.2	**18.3 to 23.6**
FoM_j*(dB)	−236.9	−242.8	−238.9	−239	−243	−241.7 to −244.5	−249.4 to −250.5	**−248.3 to −251.4**
$FoM_{j,T}$**(dB)	−225.3	−227.6	−227.2	−232.3	N/A	−232.1 to −234.9	−247.1 to −248.1	**−246.3 to −249.4**
$FoM_{j,N}$***(dB)	−253.3	−259.6	−265.4	−259.6	−269.1	−263 to −265.6	−269.5 to −271	**−273.7 to −274.9**
Core Size (mm^2)	0.24	0.43	0.41	0.09	0.6	0.34	0.18	**0.18**

*FoM_j=10log((σ_t/1s)²×P_{DC}/1mW) **$FoM_{j,T}$=10log((σ_t/1s)²×P_{DC}/1mW/TR) ***$FoM_{j,N}$=10log((σ_t/1s)²×P_{DC}/1mW×f_{ref}/f_{out}))

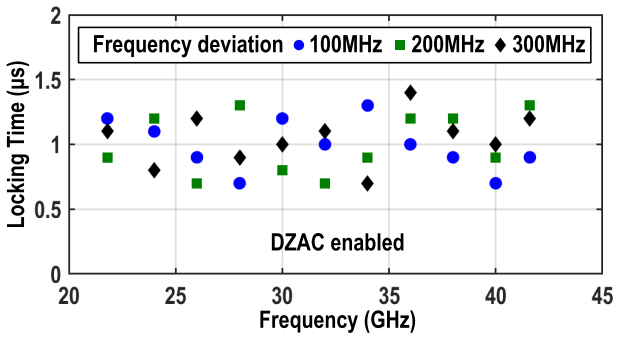


Fig. 33. Measured locking time with the variation of frequency.

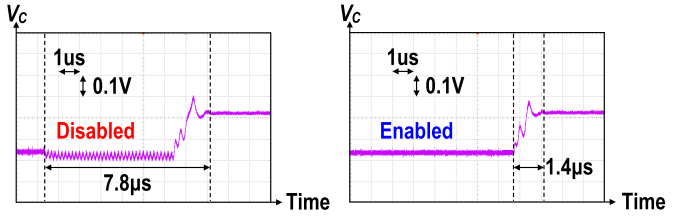


Fig. 34. Measured locking transient behavior of the FL-SSPLL operating at 24 GHz with VCO supply variation of −10%.

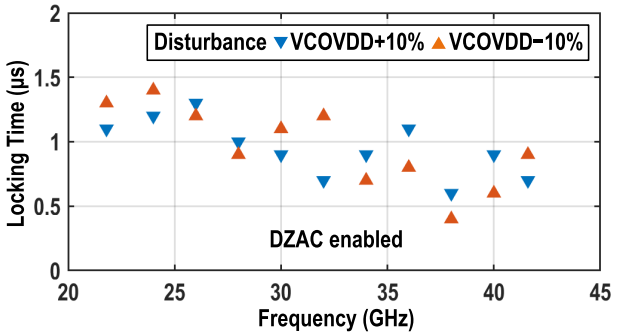


Fig. 35. Measured influence of VCO supply variation on locking time of the FL-SSPLL with DZAC enabled.

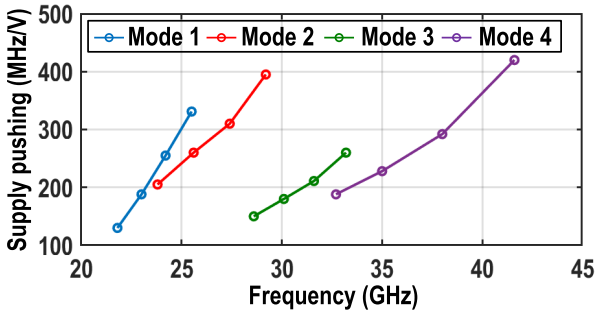


Fig. 36. Measured VCO supply pushing.

Fig. 34 experimentally verified that the proposed FL-SSPLL has good robustness to disturbances on the power supply. The disturbance is generated by changing the VCO supply. The measured locking transient is operating at 24 GHz with VCO supply variation of −10% (i.e., from 1.1 to 0.99 V). As shown in Fig. 34, after the perturbation has been injected, the PLL is out of lock. For DZAC disabled, the FLL still remains inactive because the phase error at this time is not large enough to reach the threshold of DZ. Thus, the PLL needs to wait for an accumulation of phase error to activate the frequency loop and regain locking. The locking time is 7.8 μs. However, the locking time reduces to 1.4 μs with DZAC enabled. Fig. 35 depicts the measured influence of VCO supply variation on locking time across the operating frequency range. Thanks to the DZAC enabled, the locking time is less than 1.5 μs within the VCO supply variation of 10%. Fig. 36 shows the measured VCO supply pushing in each mode. The supply pushing ranges from 130 to 420 MHz/V in the operating frequency.

The experimental results are summarized and compared with the relevant state-of-the-art PLLs in Table I. The proposed

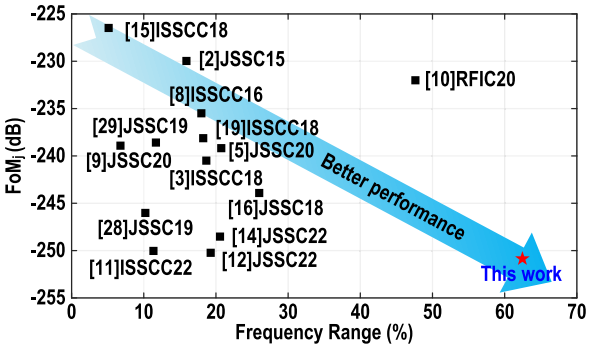


Fig. 37. Comparison of FoM$_j$ versus frequency range in state-of-the-art mm-wave PLLs.

FL-SSPLL achieves the superior jitter performance over the 62.5% frequency range. Besides, this FL-SSPLL exhibits competitive FoM$_j$ and locking time. Fig. 37 compares the performance of this article with the state-of-the-art mm-wave PLLs. The proposed FL-SSPLL operates at a wide frequency range of larger than 50% and simultaneously achieves a good FoM$_j$.

V. Conclusion

In this article, a wideband FL-SSPLL with low jitter and high FoM$_j$ is proposed. A QSSPD-based DZAC is introduced to automatically trigger the FLL for fast locking. The FL-SSPLL is fabricated in a 40-nm CMOS technology. Measurements exhibit a 62.5% output frequency range from 21.8 to 41.6 GHz. The FL-SSPLL achieves a 62.7–79.1-fs rms jitter within the whole frequency range. Besides, the power consumption is 18.3–23.6 mW, leading to FoM$_j$ from −248.3 to −251.4 dB. Moreover, the FL-SSPLL achieves a locking time improvement over the wide frequency range compared to the conventional SSPLL.

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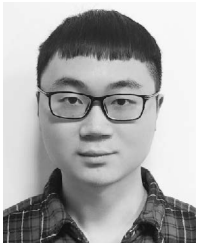

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