Over 200-GHz-Bandwidth InP DHBT Baseband Amplifier ICs and Ultrabroadband Modules With 1-/0.8-mm Coaxial Connectors

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Abstract— Wideband baseband amplifier ICs were designed and fabricated in in-house 250-nm indium phosphide (InP) double-heterojunction bipolar transistor (DHBT) technology for the emerging needs of over 100–150-GHz bandwidth applications. We propose combining an *RC* degeneration (RCD) circuit and a cascode stage peaking (CSP) circuit to achieve a broadband peaking characteristic and a wide bandwidth. The fabricated amplifier IC achieved a bandwidth of over 200 GHz. To use the amplifier ICs in practical applications, we packaged the amplifier ICs as amplifier modules with 1-mm coaxial connectors as well as 0.8-mm coaxial connectors. The amplifier ICs were mounted onto quartz glass-based module substrates by flip-chip bonding to avoid large reflection and loss. Ground blocks (GBs) were used at the connection part between the module substrates and the coaxial connectors to suppress radiation loss. The fabricated amplifier module with 1-mm coaxial connectors achieved a 7.3-dB gain with a bandwidth over 130 GHz. The fabricated amplifier module with 0.8-mm coaxial connectors achieved an 8.3-dB gain with a 165-GHz bandwidth, which is the widest ever reported thus far.

Index Terms— Amplifier module, coaxial connector, distributed amplifier (DA), flip-chip bonding, indium phosphide (InP) double-heterojunction bipolar transistor (DHBT), quartz glass.

I. INTRODUCTION

WIDEBAND baseband amplifiers are needed in various applications, such as measurement equipment and optical communications. In recent years, ultrawideband over 100–150 GHz has started to become necessary. For example, several optical transmission experiments with around 200 GBaud have been demonstrated [1], [2], and the symbol rate is expected to further increase to sustain the ever-growing traffic. Moreover, the commercialization of measurement equipment with bandwidths of over 100 GHz [3], [4] has begun. For the above applications, baseband amplifier ICs with bandwidths exceeding 100–150 GHz will be essential components.

Distributed amplifier (DA) topology is a common technique for designing wideband amplifiers. The first DA was proposed in 1936 [5]. Since then, DAs have been fabricated by various technologies, such as indium phosphide (InP) double-heterojunction bipolar transistor (DHBT)s [6], [7], [8], [9], [10], [11], [12], InP HEMTs [13], [14], SiGe BiCMOS [15], [16], [17], and CMOS [18], [19]. The bandwidth of a DA increases as the maximum oscillation frequency (f_{max}) of the technology increases. The DA bandwidth has reached over 200 GHz [6], [7], [8], [9], [13], [14] by using technologies with f_{max} of over 400 GHz. In our previous work [6], we designed and fabricated a DA using our developed in-house 250-nm-emitter-width InP DHBT technology [20]. In the amplifier IC, we proposed combining an *RC* degeneration (RCD) circuit and a cascode stage peaking (CSP) circuit to achieve a broadband peaking characteristic. The fabricated amplifier IC achieved a bandwidth of over 200 GHz. In this article, as an expansion of our previous work [6], we first discuss and analyze the details of the amplifier IC, specifically with respect to the peaking method.

Packaging technology with coaxial connectors is also important for the practical application of the amplifier IC. Some amplifier modules with coaxial connectors have achieved bandwidths of around 100 GHz [6], [21], [22], [23]. In our previous work [6], we developed a baseband amplifier module with 1-mm coaxial connectors and achieved a bandwidth of over 130 GHz, the widest reported thus far. However, the upper limit frequency that a single mode can propagate in a 1-mm coaxial connector is around 133 GHz [24], [25] which limits the bandwidth of the amplifier module. To achieve a wider bandwidth, 0.8-mm coaxial connectors must be used, as the upper limit frequency can ideally be extended to around 166 GHz [24], [25].

In this article, as an expansion of our previous work [6], we discuss and analyze the details of our amplifier module with 1-mm coaxial connectors (hereinafter, "1-mm module"), particularly its stability, group delay, noise figure (NF), and power characteristic. In addition, we have devised a new amplifier module with 0.8-mm coaxial connectors (hereinafter, "0.8-mm module") to ease the limit caused by the connectors and to further increase the bandwidth of the amplifier module.

To develop an amplifier module with a bandwidth that reaches the upper limit frequency of the connectors, the amplifier IC was designed to have a broadband peaking characteristic to compensate for packaging losses. The amplifier IC was mounted onto a quartz glass-based module substrate by
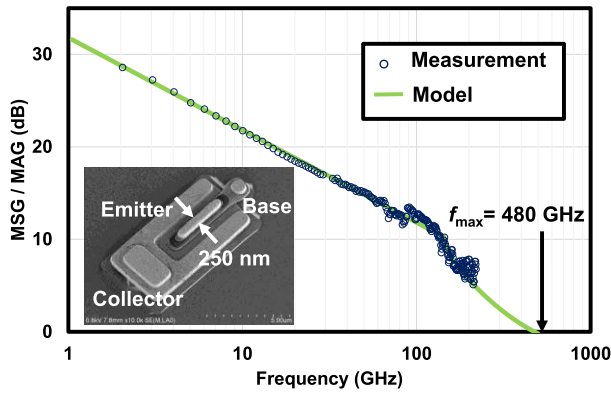
Fig. 1. Scanning microscope image and measured MSG/MAG of fabricated InP DHBT.

Fig. 2. Simplified cross section of InP DHBT IC.

flip-chip bonding to avoid large loss and reflection. At the connection part between the module substrate and coaxial connectors, we used ground blocks (GBs) to suppress the radiation loss. The fabricated 1-mm module achieved a 7.3-dB gain with a bandwidth of over 130 GHz. The fabricated 0.8-mm module achieved an 8.3-dB gain with a 165-GHz bandwidth, the widest bandwidth ever reported.

II. TECHNOLOGY

In this work, we designed and fabricated a DA using our developed in-house 250-nm-emitter-width InP DHBT technology [20]. Fig. 1 shows the measured maximum stable gain (MSG) and maximum available gain (MAG) of the InP DHBT for an emitter length of 2 μm, collector–emitter voltage V_{ce} of 1.5 V, and collector current density of 10 mA/μm^2. The measurement frequency is from 2 to 220 GHz using a VNA (Anritsu VectorStar ME7838G). We used the through-reflect-line (TRL) calibration method to de-embed the pads and the lead line to the transistor. f_{max} is estimated to be 480 GHz. The breakdown voltage, BVCEO, is over 3.5 V. We designed the DA using an accurate large-signal transistor model that agrees well with the measurement result. We also used well-modeled passive components, such as transmission lines. Fig. 2 shows a simplified cross-sectional view of our InP DHBT process including passive components. It has three interconnect metal layers, thin-film resistors, and metal–insulator–metal capacitors. All metal layers are made of Au. The top metal layer is the thickest (2.4 μm), so we mainly used this layer to compose coplanar waveguide (CPW) transmission lines with low loss and design our DA.

III. CIRCUIT DESIGN

A schematic of the amplifier IC is shown in Fig. 3. We utilized a DA topology to achieve wideband frequency characteristics. The DA consists of six unit cells, input CPW transmission lines (TLi), output CPW transmission lines (TLo), and input and output termination resistors. Both the input and output are coupled from the dc signal. The input/output CPW only consists of the third metal layer and is connected to the transistors via a short lead line in the second metal layer. The basic concept of the
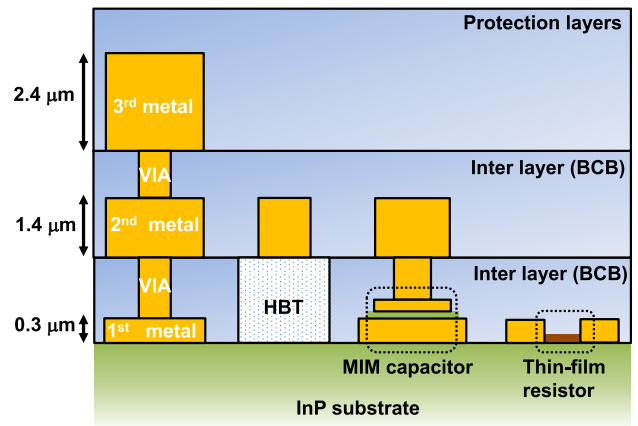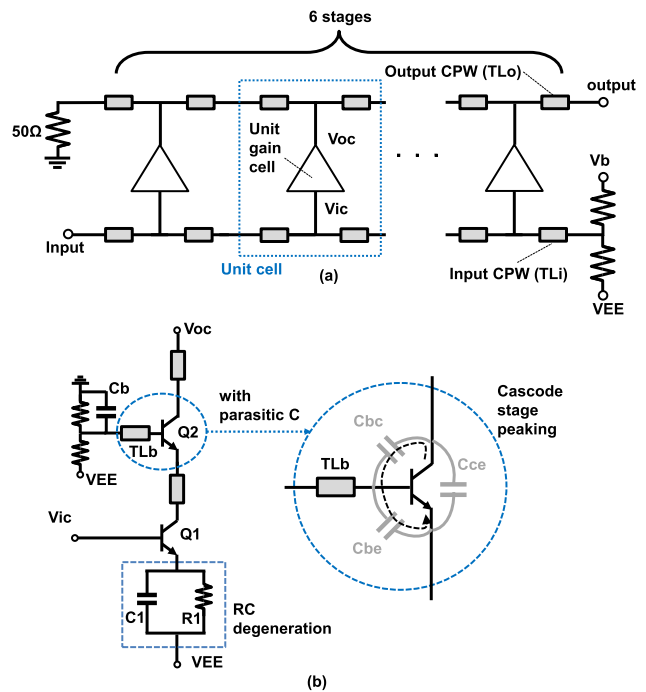

Fig. 3. Schematic of (a) overall configuration of amplifier IC and (b) unit gain cell.

DA is as follows. The input and output transmission lines with the parasitic components of the transistors in the unit gain cells comprise input and output artificial transmission lines (ATLs). The impedance of the ATLs is designed to be the same as the termination (generally 50 Ω). Furthermore, by matching the phase velocities between the input and output ATLs, the signals can be amplified over a wideband.

When designing the ATLs, it is desirable to handle the transistors in the unit gain cell as pure capacitance which has high impedance. In addition, the transmission lines should only include inductance and capacitance. However, since actual transistors include parasitic conductance, the input and output impedance of the unit gain cell decreases, which increases the loss of the ATLs. Moreover, the actual transmission lines also include resistance, which increases the loss of the

TABLE I
DESIGN PARAMETERS OF AMPLIFIER IC COMPONENTS

	Parameters for 1-mm module	Parameters for 0.8-mm module
Impedance of TLi	~67 Ω	~50 Ω
Length of TLi	45 μm	45 μm
Impedance of TLo	~79 Ω	~72 Ω
Length of TLo	45 μm	45 μm
Emitter length of Q1 & Q2	2 μm	2 μm
Collector current of Q1 & Q2	~5 mA	~5 mA
Capacitance of C1	50 pF	80 pF
Resistance of R1	23 Ω	20 Ω
Impedance of TLb	~30 Ω	~30 Ω
Length of TLb	35 μm	20 μm
Capacitance of Cb	200 fF	200 fF

ATLs. There is also packaging loss in addition to the loss inside the IC. Therefore, to fabricate a wideband amplifier module, the amplifier IC should have a peaking characteristic to compensate for these losses. In this work, we propose a broad peaking method that combines RCD and CSP circuits in a unit gain cell. The design parameters of each component are shown in Table I.

The RCD circuit consists of a resistor and capacitor connected to the emitter of the input transistor Q_1, as shown in Fig. 3(b). The RCD circuit is used for two main purposes. The first is to improve the input impedance of the unit gain cell and reduce the loss of the input ATL. As shown in Fig. 4(a) and (b), the input impedance of the unit gain cell increases and the loss of the unit input ATL decreases by using the RCD circuit compared with the simple common-emitter topology. Fig. 4(c) and (d) shows the simulation results of the characteristic impedance and the group delay of the input ATL in the unit cell. The use of the RCD circuit improves the transmittance of the input ATL but does not significantly affect the characteristic impedance or group delay.

The second purpose for using the RCD circuit is to provide a peaking characteristic to the unit gain cell. Because the input transistor is based on a common-emitter amplifier, a lower impedance on the emitter provides higher gain. The impedance of the emitter can be decreased, and the gain can be increased at high frequency by the RCD circuit. Fig. 5(a) shows the simulation results of dc-normalized gain for the entire amplifier IC, which demonstrates that the RCD circuit increases the gain at high frequency.

On the output side of the unit gain cell, we added a cascode stage above the input transistor. As shown by the simulation results in Fig. 6(a), the use of the cascode stage increases the output impedance of the unit gain cell, which reduces the loss of the output ATL compared with the single-stage configuration. In this study, we also propose a CSP circuit, where a transmission line (TLb) is added to the base of the cascode stage transistor. As shown in Fig. 6(a) and (b), this configuration can further reduce the loss of the output
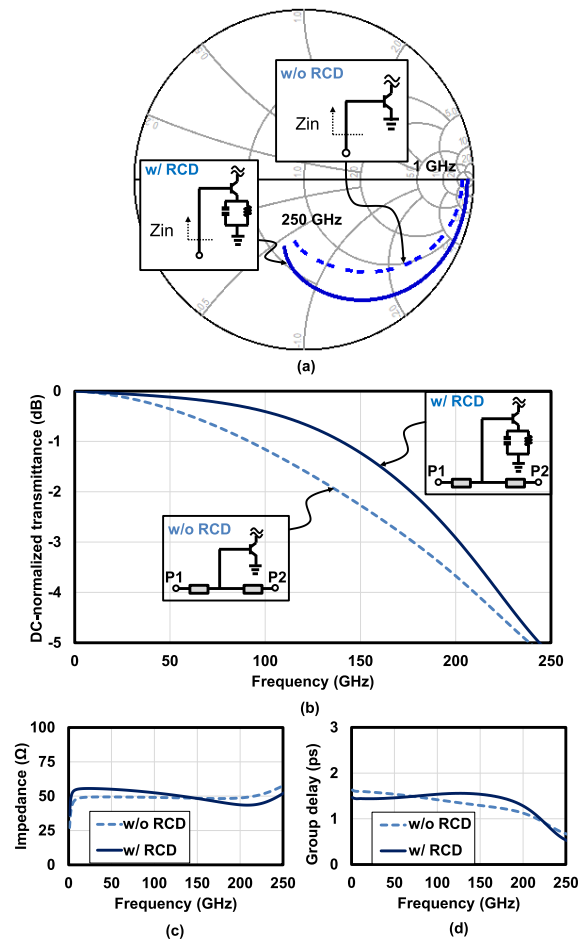

Fig. 4. (a) Simulation result of the input impedance of unit gain cell with and without RCD. Simulation result of (b) dc-normalized transmittance, (c) characteristic impedance, and (d) group delay of input ATL in the unit cell with and without RCD.

ATL compared with the simple cascode stage configuration. Fig. 6(c) and (d) shows the simulation results of the characteristic impedance and group delay of the output ATL of the unit cell. We verified that the use of the CSP circuits does not significantly affect either characteristic impedance or group delay.

Note that by using the cascode stage, the real part of the output impedance Z_{out} can be negative as shown in Fig. 6(a). This is because the signal at the collector node of the cascode transistor goes around to the emitter node through the parasitic capacitance and is amplified by the cascode transistor. Therefore, the real part of Z_{out} becomes negative, which can decrease the stability. However, since the collector node of the cascode transistor is connected to an output transmission line that has loss, the negative real part of Z_{out} does not necessarily mean that the entire amplifier can oscillate. When designing the amplifier, the K-factor of the entire amplifier must be verified so that the amplifier does not oscillate.

The use of the CSP circuit also provides a peaking characteristic to the unit gain cell. The additional baseline TLb in the CSP circuit increases the impedance of the base at high frequency. Therefore, the signal at the collector of the cascode
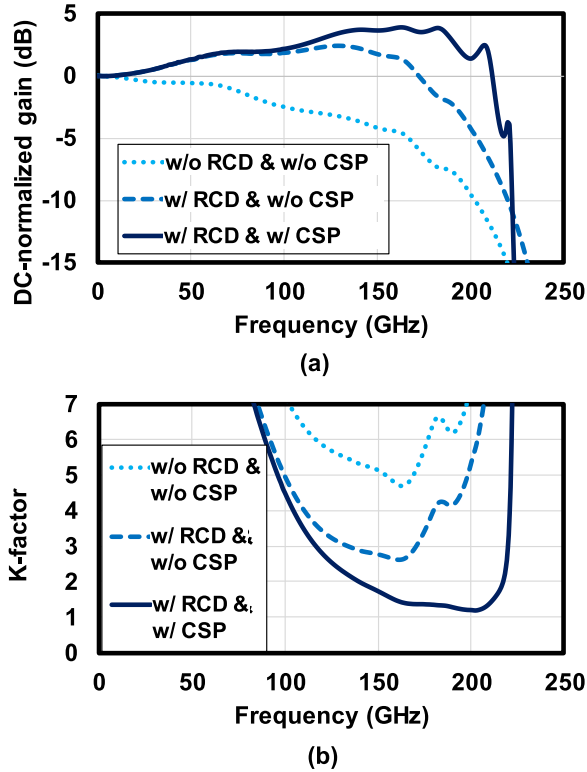
Fig. 5.   Simulation result of (a) dc-normalized gain and (b) K-factor of overall amplifier IC.
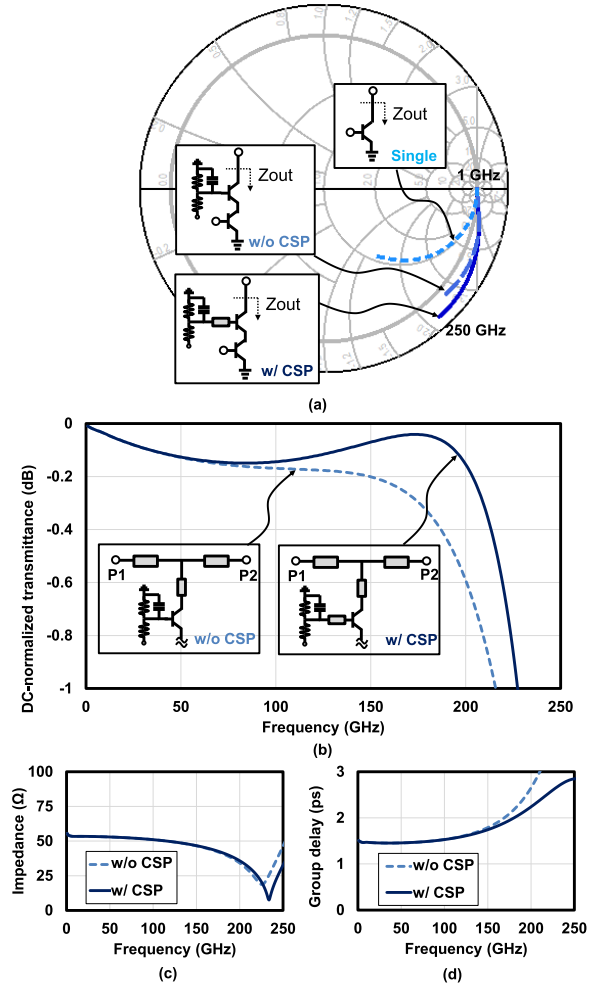

Fig. 6.   (a) Simulation result of the output impedance of unit gain cell. Simulation result of (b) dc-normalized transmittance, (c) characteristic impedance, and (d) group delay of output ATL in the unit cell with and without CSP.

stage transistor is positively fed back to the emitter through the parasitic capacitance, resulting in the increased gain at high frequency. As shown in Fig. 5(a), the use of the CSP circuit with the RCD circuit can achieve broader peaking than when using only the RCD circuit.

However, using the RCD and CSP circuits may degrade the amplifier stability, as shown in Fig. 5(b). In particular, because the CSP circuit uses positive feedback, the K-factor is highly sensitive to the length of TLb in the CSP circuit. Fig. 7 shows the simulation results when the length of the TLb is varied. If the length is too short, the peaking may be insufficient, and if it is too long, the K-factor may be below 1 at high frequency, which can cause oscillation. In addition, the stability when using the CSP circuit is also sensitive to the impedance of the bias circuit of the cascode stage and the length of the lead line to the output transmission line from the collector of the cascode stage transistor. For example, the gain profile and K-factor when varying the capacitor, C_b, in the bias circuit of the cascode stage is shown in Fig. 8. Therefore, it is necessary to design the peaking and K-factor characteristics of the entire amplifier considering all these factors. In this work, we used a well-modeled transistor and electromagnetic simulation of transmission lines to design an optimum peaking characteristic that takes stability into consideration and can compensate for the loss including packaging loss. "Optimal" in this work refers to a state where the K-factor is over 1, and the peaking gain is larger than the amount that can compensate for package loss and is the maximum value. The packaging loss will be discussed in the next section.

IV. MODULE DESIGN

Fig. 9(a) and (b) shows the simplified overall configuration of the 1- and 0.8-mm module, respectively. We used edge-mount-type coaxial connectors as the interfaces of the input and output. In the 1- and 0.8-mm connectors, only the lowest order TEM mode can ideally propagate up to 133 and 166 GHz, respectively [24], [25]. The amplifier IC was mounted onto the module substrate by flip-chip bonding, which yields a shorter wire length and lower inductance than that of wire bonding, and, as a result, lower loss and lower reflection. A cross-sectional view around the flip-chip bonding of the signal pads is shown in Fig. 9(c). The bumps for flip-chip bonding are made of Au, and their height after bonding is around 30 μm. An underfill was inserted between the module substrate and the amplifier IC to maintain the strength of the flip-chip bonding. The impedance of the RF lines on the module substrate was designed with consideration of the relative permittivity and loss tangent of the underfill. The module substrate is made of quartz glass, which has a loss tangent of 0.0001 and a relative permittivity of 3.8 at 10 GHz. The low-loss tangent contributes to reducing the loss of the packaging. The RF lines on the module substrate are based on
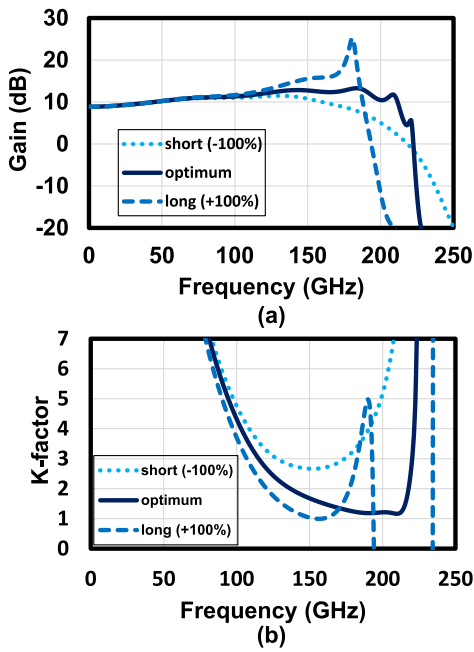
Fig. 7. Simulation result of (a) gain and (b) K-factor of overall amplifier IC when varying length of TLb of CSP.
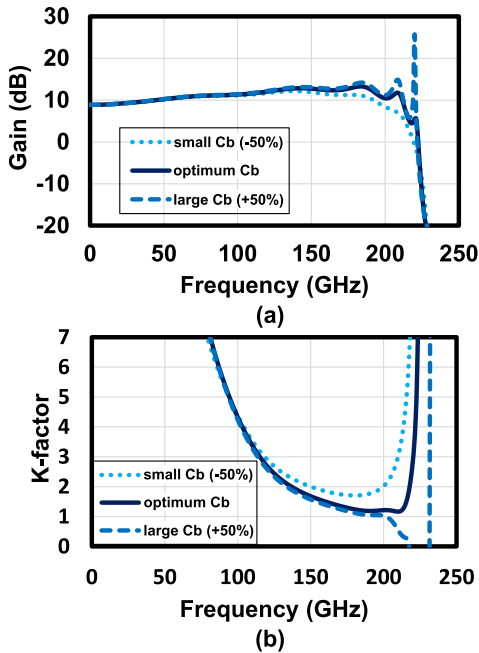

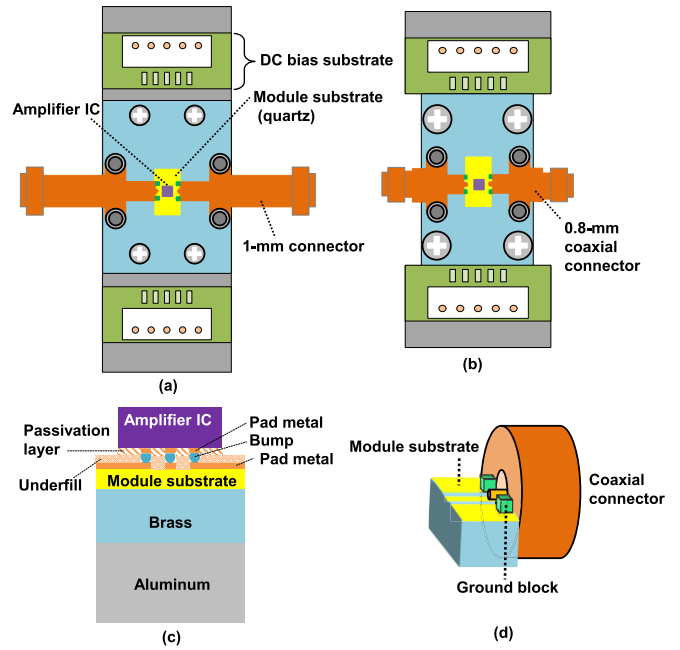Fig. 8. Simulation result of (a) gain and (b) K-factor of overall amplifier IC when varying C_b of CSP.

Fig. 9. Simplified configuration of amplifier module. (a) 1-mm module, (b) 0.8-mm module, (c) cross-sectional view around flip-chip bonding, and (d) connecting part between the coaxial connector and module substrate.
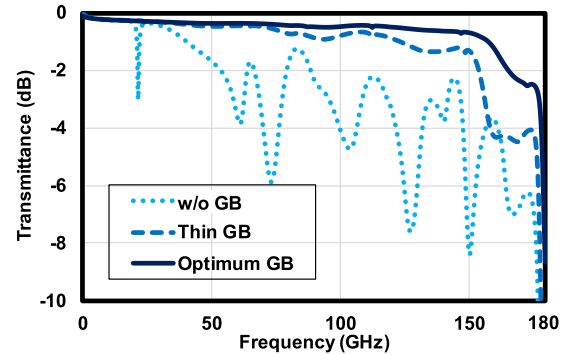

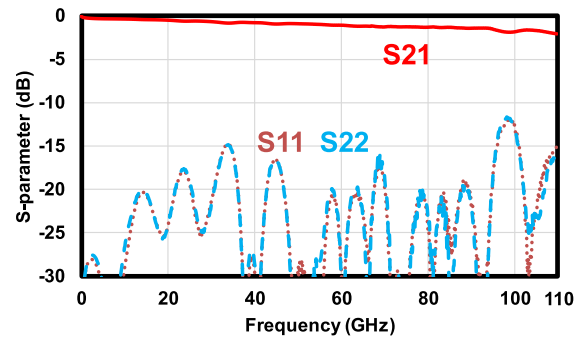Fig. 10. Simulation result of thru-line TEG module.

Fig. 11. Measured S-parameters of thru-line TEG module with 1-mm connectors.

CPW. (The layout of the RF lines is not shown in this article). In the module, there is also a dc bias network consisting of decoupling capacitors to suppress the resonance at low frequencies caused by the inductance of wires. (The circuit of the dc bias network is not shown in this article.) At the connection part between the connector and the module substrate, a GB was placed on either side of the signal line, as shown in Fig. 9(d). The GBs were used to communize the ground between the coaxial connector and the module substrate for the loss reduction and to enable a smooth

transition from the lowest order TEM mode of the coaxial structure to a quasi-TEM mode of the planar transmission line structure. If the GBs are not used, multiple reflections and unnecessary radiation will occur at the connection part due to the uneven mode transition, causing ripples and losses even at low frequencies. The GB thickness should be optimized to
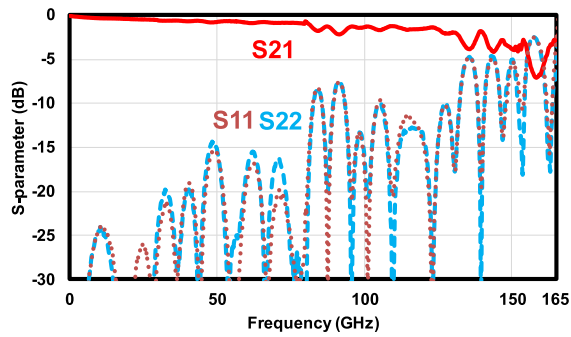
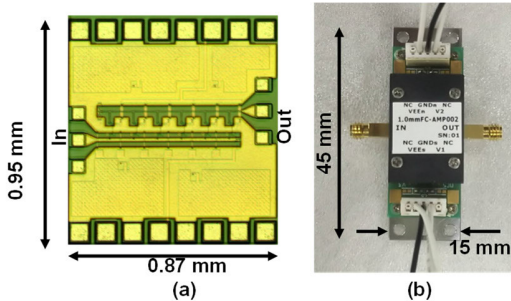Fig. 12.   Measured S-parameters of thru-line TEG module with 0.8-mm connectors.

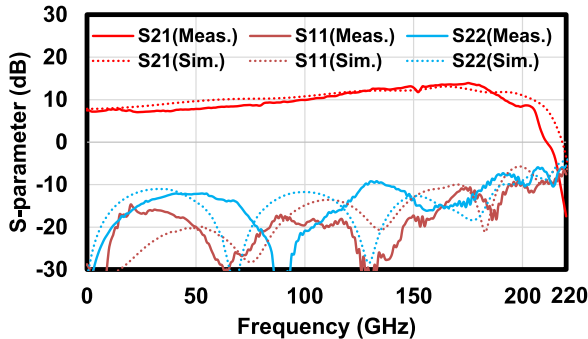Fig. 13.   Photographs of (a) amplifier IC for 1-mm module and (b) 1-mm module.

Fig. 14.   Measured S-parameters of amplifier IC for 1-mm module.
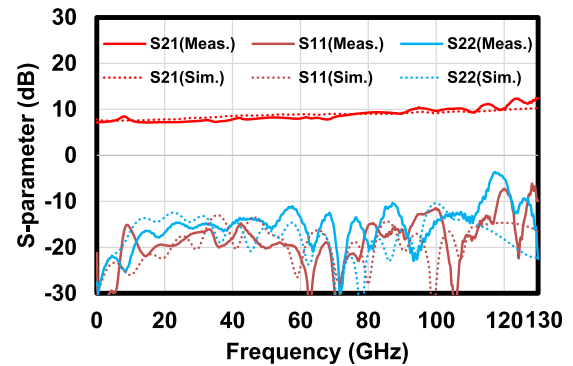

Fig. 15.   Measured S-parameters of 1-mm module.
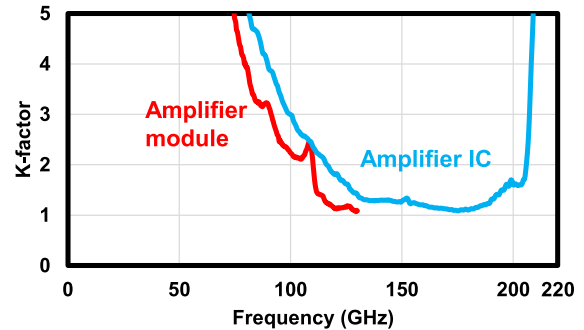

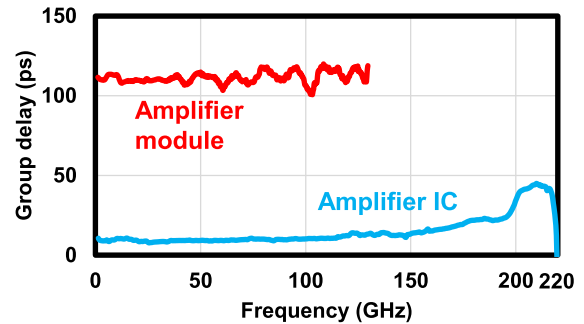Fig. 16.   Measured K-factor of amplifier IC and 1-mm module.

Fig. 17.   Measured group delay of amplifier IC and 1-mm module.

achieve low loss over a wideband. Fig. 10 shows the simulated transmittance of a thru-line test elementary group (TEG) module where a thru-line-substrate around 2 mm in length and coaxial connectors are connected. It can be seen that low loss is feasible over 160 GHz by using GBs that are of optimum thickness. Figs. 11 and 12 show the measured S-parameter of the thru-line TEG modules with 1- and 0.8-mm coaxial connectors. For the 1-mm thru-line TEG module, the loss has a slope of around −2 dB toward 110 GHz. For the 0.8-mm thru-line TEG module, the loss has a slope of around −4 dB toward 165 GHz. The amplifier ICs are designed with peaking characteristics to compensate for these losses.

V. MEASUREMENT RESULTS

A. 1-mm Module

A photograph of the 1-mm module and the amplifier IC for the 1-mm module are shown in Fig. 13. The size of the

amplifier IC is 0.87×0.95 mm, and that of the amplifier module is 15×45 mm. Both the IC and the module consume a current of 120 mA with a supply voltage VEE of −4.5 V, which corresponds to a power consumption of 540 mW. As a breakdown of the current consumption, 30 mA flows to the transistors in the six-stage unit gain cells. Each transistor consumes 5 mA corresponding to the current density of 10 mA/μm^2. The other currents flow into the bleeder resistors of the bias circuits in the unit gain cells and the input termination resistors.

To operate the amplifier IC, it is necessary to supply the bias voltage (V_b in Fig. 3) and the power supply voltage (VEE in Fig. 3) from outside. These voltages are supplied through the dc pads placed at the upper and lower sides of the IC [Fig. 12(a)]. DC blocks must be used to connect the amplifier module to other equipment because the signal input and output are dc coupled.
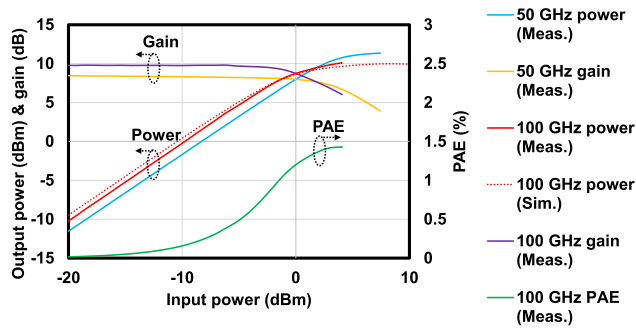
Fig. 18.   Measured input and output power characteristics of 1-mm module at 50 and 100 GHz.
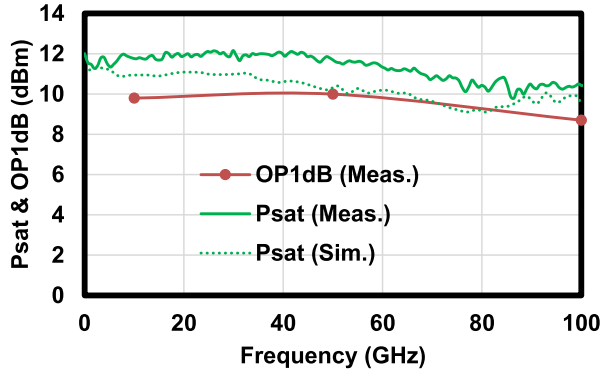

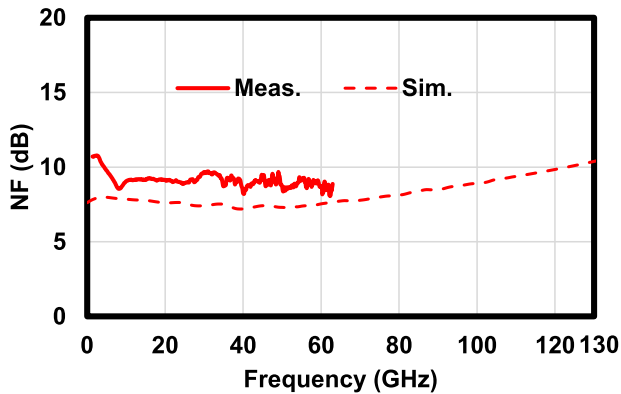Fig. 19.   Measured frequency characteristic of saturation power and OP1dB of 1-mm module.

Fig. 20.   Measured NF of 1-mm module.

(a)

(b)

Fig. 21.   Measured input and output waveforms of (a) 128-GBaud NRZ (128 Gb/s) and (b) 112-GBaud PAM4 (224 Gb/s) and Y-axis: 100 mV/div and X-axis: 5ps/div.
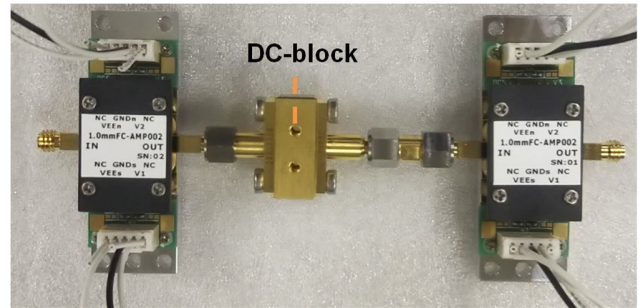
Fig. 22.   Photograph of the dual module.
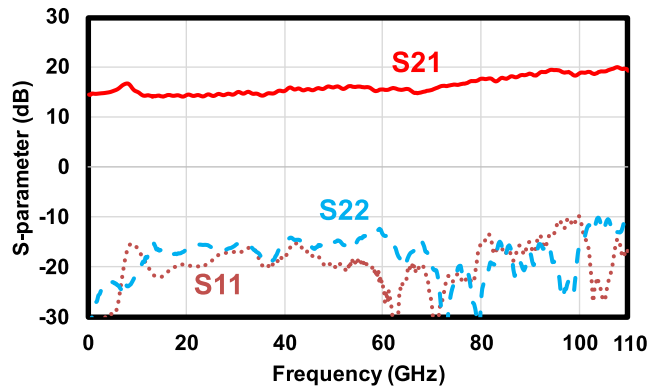
Fig. 23.   Measured S-parameters of dual module.

The amplifier module is designed to operate normally within a temperature rise of 50° above the ambient temperature. A thermal simulation of the flip-chip packaging under severe conditions without inserting an underfill showed that the temperature rise on the chip surface (flip-chip surface) was less than 50° above the ambient temperature (room temperature). Furthermore, since the underfill is actually placed between the chip and the module substrate, the heat from the chip diffuses more easily to the module substrate. Therefore, it is assumed that the actual temperature rise does not significantly affect the operation of the amplifier module.

Fig. 14 shows the S-parameters of the amplifier IC for the 1-mm module measured using a VNA (Anritsu VectorStar ME7838G) in an on-wafer environment. The gain measured at 100 MHz is 7.5 dB. Note that 100 MHz is a frequency we set in the measurement equipment and is not the lower limit of the amplifier because the signal ports of our amplifier are dc coupled. The −3-dB bandwidth is 208 GHz. The maximum peaking gain is +6.4 dB around 175 GHz. The return loss up to 125 GHz is less than −12 dB.

The measured S-parameters of the 1-mm module up to 130 GHz are shown in Fig. 15. The gain at 100 MHz and the −3-dB bandwidth are 7.3 dB and over 130 GHz, respectively.
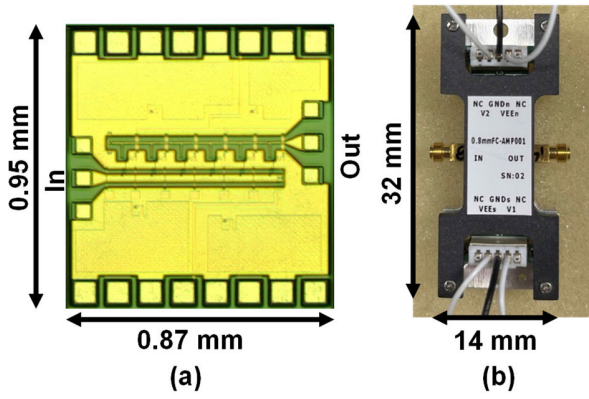
Fig. 24. Photographs of (a) amplifier IC for 0.8-mm module and (b) 0.8-mm module.
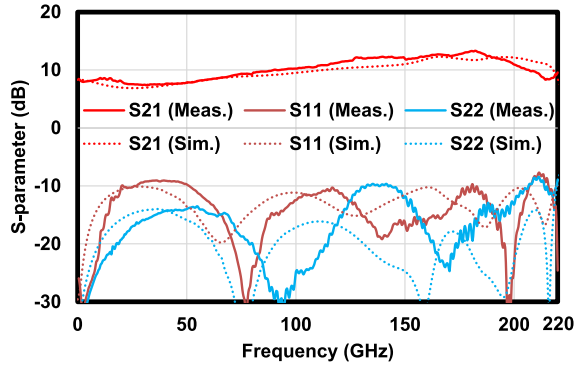
Fig. 25. Measured S-parameters of amplifier IC for 0.8-mm module.
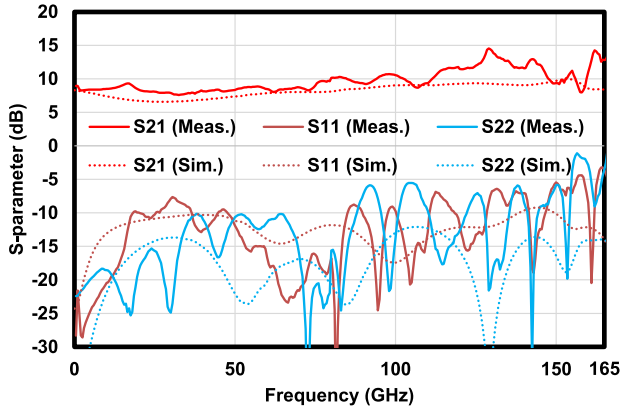
Fig. 26. Measured S-parameters of 0.8-mm module.

The return loss is less than −10 dB up to 110 GHz. The peaking gain is +5 dB at 130 GHz, which indicates that an additional loss of components connected to the amplifier module can be further compensated for. Fig. 16 shows the measured K-factor of the amplifier IC and the 1-mm module. Due to the use of peaking circuits, the K-factor of the amplifier IC decreases to around 180 GHz but remains over 1. In contrast, the K-factor increases above 200 GHz as the amplifier gain decreases. Both the K-factors of the amplifier IC and amplifier module are over 1 through their band, which indicates that they are stable.

Fig. 17 shows the measured group delay of the amplifier IC and the 1-mm module. The group delay variation of the amplifier IC and the 1-mm module are less than ±1.5 and ±7.5 ps, respectively, up to 100 GHz.
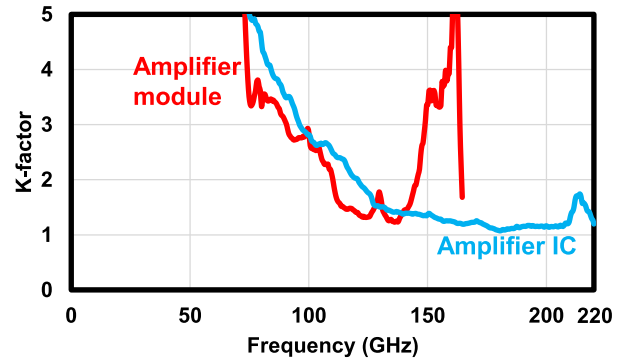
Fig. 27. Measured K-factor of amplifier IC and 0.8-mm.

Fig. 28. Measured group delay of amplifier IC and 0.8-mm module.

Fig. 29. Measured power characteristic of 0.8-mm module at 50 and 100 GHz.

Fig. 30. Measured frequency characteristic of saturation power and OP1dB of 0.8-mm module.

Fig. 18 shows the power characteristics of the 1-mm module at 50 and 100 GHz measured using the VNA (Keysight N5291A) and power meter (Keysight U8489A). The saturation

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF AMPLIFIER ICs

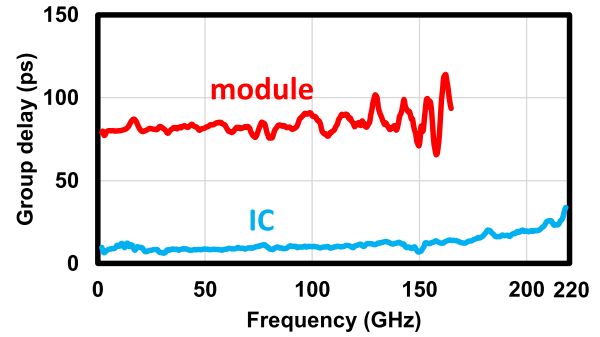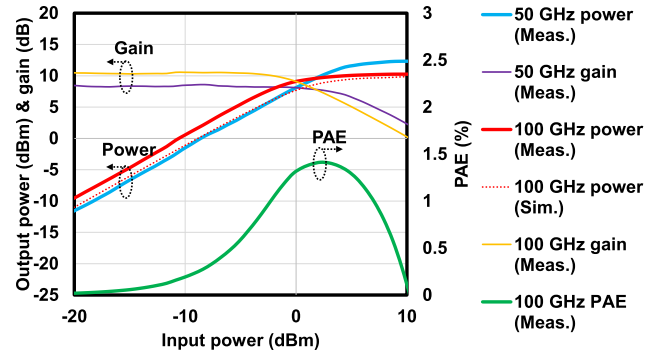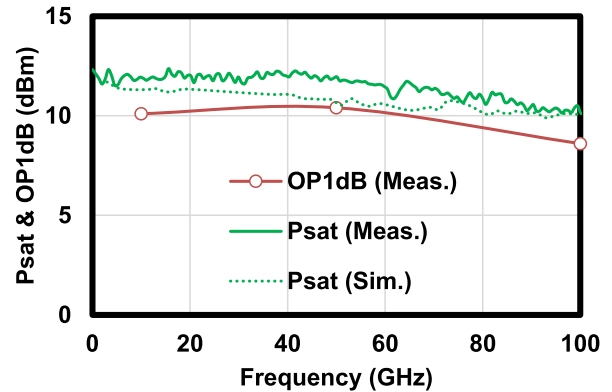|	BW* (GHz)	f_{LOW}* (GHz)	f_{High}* (GHz)	Gain (dB)	Peaking gain (dB)	NF (dB)	DC power (mW)	OP1dB (dBm)	Max. PAE (%)	Chip Size (mm²)	Technology
[14]	334	1	335	11	-	3	215	7.6 (~110 GHz)	4 @ 100 GHz	0.62	35-nm InGaAs mHEMT (f_{max} >1000 GHz)
[9]	241	1	242	10	-	N.A.	387	10 @ 10 GHz	2 @ 10 GHz	0.82	250-nm InP DHBT (f_{max} =480 GHz)
[7]	235	2	237	16	-	<10	117	N.A.	N.A.	0.41	250-nm InP DHBT (f_{max} =650 GHz)
[13]	230	75	305	19	-	N.A.	500	10 @ 95 GHz	3 @ 100 GHz 6 @ 200 GHz	1.68	35-nm InGaAs mHEMT (f_{max} >1000 GHz)
[8]	207	0	207	13.5	-	N.A.	210	5 @ 50 GHz 3.7 @ 100 GHz	N.A.	0.28	250-nm InP DHBT (f_{max} =650 GHz)
[17]	180	0.5	181	18.7	-	6	86	0 @100 GHz	N.A.	0.61	130-nm SiGe BiCMOS (f_{max} =450 GHz)
[15]	175	45	220	16	+ 4 (~200 GHz)	14	360	4.5 @ 130 GHz	N.A.	0.38	130-nm SiGe BiCMOS (f_{max} =450 GHz)
[10]	170	1	171	12	-	8 (~50 GHz)	180	8.4 @ 150 GHz	6	0.97	500-nm InP DHBT (f_{max} = 490 GHz)
[16]	160	90	250	13	-	N.A.	74	N.A.	N.A.	0.22	130-nm SiGe BiCMOS (f_{max} =500 GHz)
[11]	159	1	160	10.5	-	10.1	N.A.	15 @ 55 GHz	12.5 @ 110 GHz	1.28	InP HBT (f_{max} = 390 GHz)
[18]	92	0	92	9.7	-	N.A.	73	N.A.	N.A.	0.45	45-nm SOI CMOS (f_{max} =300 GHz)
[19]	87	4	91	4	-	4.2	90	10 @ 20 GHz	N.A.	0.8	45-nm SOI CMOS (f_{max} >200 GHz)
[12]	85	60	145	6.5	-	10.5 @ 65 GHz	440	18.5 @ 75 GHz	19.2 @ 110 GHz	0.96	InP HBT (f_{max} = 390 GHz)
This work [6]	208	<0.1 (DC coupled)	208	7.5	+6.4 (~ 175 GHz)	9	540	>6.8 @ 100 GHz	1.4 @ 100 GHz	0.82	250-nm InP DHBT (f_{max} =480 GHz)
This Work	> 220	<0.1 (DC coupled)	> 220	8.3	+ 4.3 (~ 165 GHz)	N.A.	540	>10.4 @ 50 GHz >8.6 @ 100 GHz	1.4 @ 100 GHz	0.82	250-nm InP DHBT (f_{max} =480 GHz)

BW: -3 dB bandwidth f_{LOW}: Low-frequency cut-off f_{High}: High-frequency cut-off

power (P_{sat}) and output 1-dB gain compression point (OP1dB) at 50 GHz are 11.4 and 10 dBm, respectively. P_{sat} and OP1dB at 100 GHz are 10.4 and 8.7 dBm, respectively. The frequency characteristic of the P_{sat} is also measured as shown in Fig. 19. P_{sat} is almost over 10 dBm up to 100 GHz. We also measured the NF of the 1-mm module using a VNA (N5291A) and the cold source method. The result is shown in Fig. 20. The NF is approximately 9 dB up to 64 GHz. The upper frequency of the measured NF was limited by our measurement setup.

Fig. 21(a) and (b) shows two waveforms 128-GBaud NRZ and 112-GBaud PAM4, respectively, at the input and output of the 1-mm module with two dc blocks. To generate the input signals and observe the output signals, we used a PAM4 multiplexer (SHF 616B) and a sampling oscilloscope (Keysight N1045B). The signals were linearly amplified, and a sufficient eye opening was attained at the output of the amplifier module.

We also measured the S-parameter of a dual module consisting of two 1-mm modules and a dc block (Fig. 22). The dc block used is the SHF DCB110R, the usable frequency range of which is 150 kHz–110 GHz as stated in the catalog. The results of the measured S-parameter are shown in Fig. 23.

The gain at 100 MHz is 14.6 dB with a bandwidth of over 110 GHz. The peaking gain including loss of the dc block is +5.6 dB at 110 GHz. The return loss is less than −10 dB through the band. Due to the low reflection of the single module, the dual module also achieved a small gain ripple characteristic.

B. 0.8-mm Module

Photographs of the 0.8-mm module and the amplifier IC for the 0.8-mm module are shown in Fig. 24. The die area of the amplifier IC including the pads is 0.87×0.95 mm, and the 0.8-mm module is 14×32 mm. The power supply voltage and dc power consumption are −4.5 V and 540 mW, respectively. The amplifier IC for the 0.8-mm module was optimized from the one used in the 1-mm module. Its S-parameters were measured up to 220 GHz in an on-wafer probing environment using a VNA (Anritsu VectorStar ME7838G). The measurement results are shown in Fig. 25. The gain at 100 MHz is 8.3 dB, which is 0.8 dB higher than that of the amplifier IC for the 1-mm module. The bandwidth is over 220 GHz, which is 12 GHz higher than that of the amplifier IC for the 1-mm module. The peaking gain at 165 GHz is +4.3 dB. We also

TABLE III
PERFORMANCE SUMMARY AND COMPARISON OF AMPLIFIER MODULES

	Amplifier Module								
Ref.	BW (GHz)	Gain (dB)	DC power (mW)	Psat (dBm)	OP1dB (dBm)	Module substrate	Bonding	Connector	Package loss (dB)
[22]	110	16.4	420	N.A.	N.A.	Quartz glass	wire	1 mm coaxial	3.1 @ 110 GHz
[23]	108	8	585	10 @ 100 GHz	7.6 @ 100 GHz	N.A.	Flip-chip	Push-on-type	N.A.
[21]	97	7.8	N.A.	N.A.	N.A.	Polyimide	Flip-chip	-	3 @ 110 GHz
This work [6]	130	7.3	540	11.4 @ 50 GHz 10.4 @ 100 GHz	10 @ 50 GHz 8.7 @ 100 GHz	**Quartz glass**	**Flip-chip**	1 mm coaxial	2 @ 110 GHz
This work	165	8.3	540	12 @ 50GHz 10.2 @ 100 GHz	10.4 @ 50 GHz 8.6 @ 100 GHz	**Quartz glass**	**Flip-chip**	0.8 mm coaxial	1.3 @ 110 GHz 4 @ 165 GHz

used the VNA to measure the S-parameters of the 0.8-mm module up to 165 GHz. As shown in Fig. 26, the 0.8-mm module achieved a gain of 8.3 dB at 100 MHz and a bandwidth of 165 GHz. We determined that the loss from packaging was sufficiently compensated for by the peaking characteristic of the amplifier IC. Fig. 27 shows the measured K-factor of the amplifier IC and the 0.8-mm module. Both have a K-factor over 1 throughout their band and are stable. Fig. 28 shows the measured group delay of the amplifier IC and the 0.8-mm module. The group delay variation of the amplifier IC and the 0.8-mm module are less than ± 3.5 and ± 8 ps, respectively, up to 100 GHz.

Fig. 29 shows the power characteristics of the 0.8-mm module at 50 and 100 GHz, measured with the VNA (Keysight N5291A) and the power meter (Keysight U8489A). The P_{sat} and OP1dB at 50 GHz are 12 and 10.4 dBm, respectively. The P_{sat} and OP1dB at 100 GHz are 10.2 and 8.6 dBm, respectively. The frequency characteristic of the P_{sat} is also measured as shown in Fig. 30. P_{sat} is almost over 10 dBm up to 100 GHz.

Table II shows a comparison of our amplifier IC with other state-of-the-art amplifier ICs. Ours is one of the amplifiers that exceeds the 200-GHz bandwidth. Among them, it achieves the highest peaking gain of over +6 dB. Table III shows a comparison of our module with other state-of-the-art amplifier modules. Among the other amplifier modules with a 1-mm connector, ours achieved the widest bandwidth of over 130 GHz and the lowest return loss of -10 dB up to 110 GHz. Our 0.8-mm module is the first ever amplifier module with 0.8-mm connectors, and its bandwidth of 165 GHz is also the widest ever reported.

VI. CONCLUSION

Wideband baseband amplifier ICs were designed and fabricated in our in-house developed 250-nm InP DHBT

technology for 100–150-GHz bandwidth applications. In addition, we proposed combining RCD and CSP circuits to achieve a broadband peaking characteristic and a wide bandwidth. The fabricated amplifier ICs achieved a bandwidth of over 200 GHz. Furthermore, we applied the amplifier ICs to amplifier modules with 1-mm coaxial connectors and 0.8-mm coaxial connectors. The amplifier ICs were mounted on a quartz glass-based substrate by flip-chip bonding to avoid large reflection and loss. A GB was used at the connection part between the module substrate and the coaxial connector to suppress radiation loss. The fabricated amplifier module with 1-mm coaxial connectors achieved a 7.3-dB gain with a 130-GHz bandwidth. The fabricated amplifier module with 0.8-mm connectors achieved an 8.3-dB gain with a 165-GHz bandwidth, which is the widest reported thus far.

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