A Multipurpose *D*-Band Vector Modulator for FMCW and PMCW Sensing Applications in 130 nm SiGe

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***Abstract*— The increased deployment of radar systems raises concerns about mutual interference among radar sensors sharing the same frequency band. Phase-modulated continuous wave (PMCW) techniques with orthogonal transmit codes can mitigate those problems. Moreover, many applications require 3-D detection, which needs either a steerable antenna beam (analog beamforming) or independent receive channels (digital beamforming). In this article, we present a 125 GHz vector modulator (VM) that can either shift the phase for phased-array operation or can be turned off for time-division multiple-input multiple-output (MIMO) operation. Phase-shifting is possible using analog (slow but fine-stepped) and digital (fast but course-stepped) control signals. Also, both interfaces can be used simultaneously to create steerable PMCW beams. The VM was fabricated using the B11HFC technology from Infineon Technologies AG and consists of four compactly interconnected power amplifiers (PAs): Two are fed with an in-phase (I) signal, and two are fed with a quadrature (Q) signal. Within the PA pairs, the PAs are cross-connected to a common inductive load so the I and Q signals can be inverted, generating output phases between 0° and 360°.**

***Index Terms*— B11HFC, BiCMOS, BPSK, code division multiplexing (CDM), *D*-band, joint radar-communication (RadCom), multiple-input multiple-output (MIMO), phase-coded, phase-modulated continuous wave (PMCW), phase-shifter, phased-array, power amplifier (PA), pseudo-noise (PN), radar, silicon-germanium (SiGe), time-division multiplexing (TDM), vector modulator (VM).**

I. INTRODUCTION

THE field of radar systems has undergone significant changes in recent decades: Increasing center frequency and more bandwidth have often been primary objectives for improving the range resolution of an FMCW radar system [1] [2, p. 8], and reducing its size. Pursuing higher center frequencies than *E*-band, used for 77 GHz automotive radar systems, results in more free-space path loss and atmospheric attenuation [3, p. 5], along with higher phase noise [4, p. 75]. Recent studies have highlighted both the challenges and capabilities of *D*-band components and systems [1], [5], [6], [7], [8]. Furthermore, an increasing number of researchers are exploring THz frequencies, utilizing silicon technologies to shrink system size and enhance bandwidth even further [9], [10], [11], [12].

In addition to bandwidth and center frequency, radar systems have also evolved in terms of antenna technology. The virtual array concept enabled by the multiple-input multiple-output (MIMO) approach reduces hardware overhead, with its accuracy scaling with the antenna count [13]. It enables better object detection compared to the phased-array approach when using the same number of antennas [14, p. 2]. Unlike the frequently employed time-division MIMO radar approach, the phased-array approach offers a decisive advantage: By combining the individual transmit antennas (i.e., fully connected arrays) into a joint and steerable beam, the detection range can be significantly increased, in contrast to the often-used time-division MIMO radar approach [15], [16], [17]. Especially for high-frequency systems in the *D*-band, this can mitigate the increased free-space path losses. Besides the phased-array approach for 3-D sensing, hybrid methods like phased-MIMO radar using partially connected arrays are gaining popularity [18], [19], [20], [21].

Nevertheless, the widespread use of radar systems results in issues related to jamming, specifically mutual interference among distinct radar sensors. In response to this challenge, phase modulation offers an alternative approach, utilizing binary sequences as orthogonal codes instead of frequency-modulated chirps. This technique is known as phase-modulated continuous wave (PMCW) or pseudo-noise (PN) radar. To minimize mutual interference from multiple radar sensors, these binary codes must exhibit high autocorrelation and low cross correlation [22]. It is worth noting that PMCW radar systems, while highly effective in minimizing interference, have their limitations. Due to the inherent constraints of orthogonal transmit codes, their isolation is typically limited to ≈ 30 dB [23]. Also, high-speed ADCs are needed to sample the phase-modulated signal. However, these systems offer distinct advantages, including enhanced capabilities

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for achieving higher maximum unambiguous velocity measurements and enabling joint radar-communication (RadCom) functionalities using phase-modulated signals [24], [25].

In general, phase shifters are needed to create a combined and steerable beam, i.e., analog beamforming [26, p. 303], or to invert the phase for phase modulation. Circuit concepts such as the Gilbert cell are often used for this purpose [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42]. Variable power amplifiers (PAs) combined with multiple couplers [43], [44], [45], [46], [47], [48], switchable delay lines [49], [50], reflection-type phase shifters [51], [52], [53], [54], [55], Doherty amplifiers [56], or tunable attenuators [57] can also be used to manipulate the output phase.

In our prior work, presented in [58], we introduced a vector modulator (VM) containing a purely digital interface, enabling rapid digital on-off switching and ≈ 45° phase shifts compared to the capabilities outlined in [59]. In this article, we build upon the foundation laid by [58], enhancing its circuitry by incorporating three significant improvements featured in two newly introduced monolithic microwave integrated circuits (MMICs).

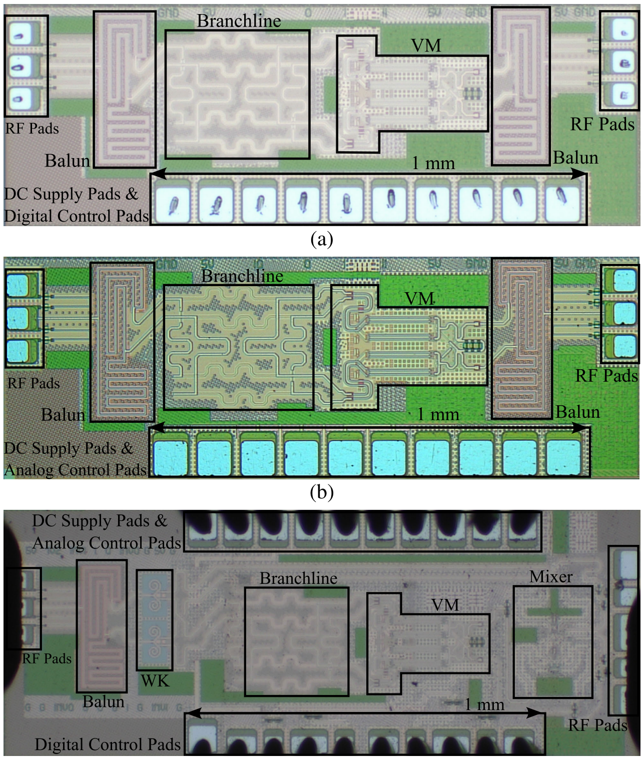
First, we extend the VM circuit to facilitate fine-stepped analog vector modulation. Second, we introduce a 125 GHz mixer designed to handle intermediate frequency (IF) signals in the GHz range. At last, we showcase the modulator's PMCW capabilities using a dedicated breakout MMIC. In summary, the modulator presented herein offers a versatile circuit for phase and frequency modulation techniques developed for 3-D sensing applications. These include fast-switched PMCW radar and precise FMCW phased-array radar, enhancing the versatility and performance of such systems. Moreover, by combining the analog and digital interface, one can create steerable PMCW beams.

We start by presenting the circuit concepts and the breakout MMICs (Section II). Afterward, we show the vector network analyzer (VNA) measurement results in Section III, including a deep analysis of the tuning behavior and the investigation of the PMCW properties. After presenting the key features and parameters, we analyze the phased-array properties in Section IV using the measured VNA data. Finally, we proceed to a comparative analysis of our VM with those found in published works, which is set out in Section V. Section VI summarizes the key findings and concludes the article.

II. CIRCUIT DESIGN AND BREAKOUT MMIC

Each of the three breakout MMICs described below contain a branchline coupler (BLC) and a VM and are therefore based on the same operating principle: A differential signal is converted into an *IQ* signal using the BLC, which is then connected to the VM. The VM is based internally on four amplifier circuits that can be controlled independently of each other. This allows the *I* and *Q* signals to be superimposed in a weighted manner to obtain the desired output amplitude and phase. However, each MMIC serves a distinct purpose.

The first breakout MMIC employs four digital control inputs to achieve a phase shift of approximately ≈ 45°, as previously described in [58] [Fig. 1(a)]. The second breakout MMIC



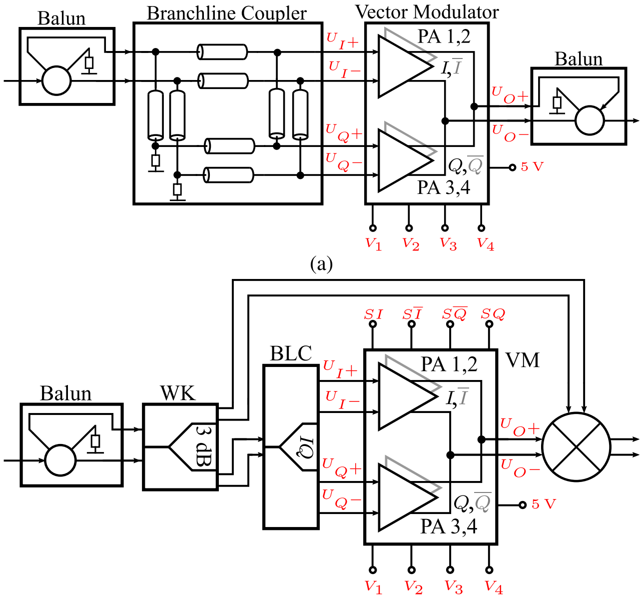
(a)
(b)
(c)

Fig. 1. These photographs depict three distinct breakout MMICs, each serving specific functions. (a) MMIC introduced in [58] is designed for digital control. (b) Second MMIC offers an analog control interface, providing an analog adjustment of the VM's output. (c) Third MMIC is engineered to provide both analog and digital control capabilities. Additionally, it incorporates a mixer at the output of the VM to showcase its ability to demonstrate PMCW capabilities.

shares similarities with the first but differs by utilizing four analog control signals to tune both amplitude and phase of the VM's output [Fig. 1(b)]. Both breakout MMICs integrate a rat-race balun at the input and output, facilitating single-ended VNA measurements. The block diagram showing all relevant building blocks, valid for the first and second MMIC, is depicted in Fig. 2(a).

While the second MMIC has the same top-level structure as the one in [58], the third MMIC is significantly different. Following the input balun, we divide the signal using a lumped-element Wilkinson (WK) divider. Instead of employing a balun after the VM, we have incorporated a mixer to analyze the PMCW capabilities. This mixer is fed by both the VM's output and the split signal from the WK divider, which serves as the local oscillator (LO) signal. Since both input signals of the mixer originate from the same source and consequently share the same center frequency, the phase difference between the LO signal and the VM's output determines the mixer's output signal. This setup allows for analyzing the VM's digital switching behavior. In addition to the described MMIC in [58], the new architecture is detailed in the block diagrams [Fig. 2(b)], and a comprehensive view of the complete design is provided in the chip photograph [Fig. 1(c)], highlighting all circuit components.

The third MMIC incorporates laser fuses that provide the capability to establish a connection between the VM and either the mixer or the pads. In the former scenario, the mixer's



(a)

(b)

Fig. 2. Block diagram of the breakout MMICs (without pads) for measuring the S-parameters (MMICs 1 and 2: (a) - based on [59]) and for measuring the PMCW capabilities (MMIC 3: (b)).

output is connected to the pads, while in the latter, the mixer is entirely disconnected.

At the center of all MMICs, a TRL-based BLC generates *IQ* signals essential for the VM's operation. Operating at a center frequency of 125 GHz, the BLC shows a simulated input matching performance exceeding -30 dB. Additionally, it provides an *IQ* amplitude and phase difference of 1.2 dB and 92.7°, respectively.

A. VM Design

The complete schematic of the VM is depicted in Fig. 3, where differences between the three MMICs are highlighted using purple dotted boxes (included in MMIC 1 & 3) and green dashed-dotted boxes (included in MMIC 2 & 3). Therefore, only MMIC 3 has both the analog and the digital interface. Signal names written in red link external signals between the circuit and block diagram, including the 125 GHz input and output signals, the 5 V supply voltage, the digital control signals (SI, $S\overline{I}$, SQ, and $S\overline{Q}$), and the analog control signals (V_1 to V_4).

The VM consists of four PAs (PA 1–4), each utilizing common-emitter and common-base topologies and featuring a current mirror. Within each common-emitter and common-base stage, 4 μm BEC transistors of the B11HFC technology are employed [60]. Two of the four PAs use the in-phase input signal (U_I — PA 1 & 2), while the other two use quadrature-phase input signal (U_Q — PA 3 & 4). The matching networks directly divide the input signals without a dedicated power divider (e.g., Wilkinson divider), resulting in a significantly more compact circuit. Although all four PAs are identical, the outputs of PA 1 & 2 and PA 3 & 4 are cross-connected to the output U_O to invert the I and Q input signals by 180°, respectively. This enables output phases ranging from 0° to 360°. The output matching of the VM can be adjusted via laser fuses. The TRL-based inductive load extends by removing these fuses, causing a downward shift in the center frequency. However, no fuses needed to be removed for the targeted center frequency of 125 GHz.

The digital switching within the I and Q paths is achieved through switchable current mirrors (Sx — purple dotted boxes). The collector voltage can be set to 0 V using an additional transistor controlled by 1.2 V digital signals. This effectively turns off the dc current through the respective PA, turning off that path of the VM. This operation principle was introduced in [58]. MMIC 2 & 3 (see Fig. 2) facilitate analog tuning via the reference path of the current mirror. Two resistors of identical size are used, with the control voltage applied in between to adjust the PA's gain (V_x — green dashed-dotted boxes). This allows for tuning the dc current density in the PA and, consequently, for modifying the amplitude of the I or Q signal. As the VM combines two vectors, this adjustment affects both the amplitude and phase at the output.

B. Mixer Design

The circuit diagram of the mixer is depicted in Fig. 4. The left side comprises the Gilbert cell core, including the RF matching networks and current mirror circuit. The right side displays the bias networks for both the RF and LO inputs. The LO input is connected to one of the two Wilkinson dividers' output ports, as shown in Fig. 2(b), while the RF port is connected to the output of the VM. Due to our aim to generate high-speed IF signals using binary sequences, we have opted for a load resistor value of 50 Ω. This choice ensures a favorable match between the mixer's IF output and the connected RF measurement equipment, which utilizes both 50 Ω cables and input impedance. We simulated a peak voltage gain of -7 dB using 1 GHz IF signals. The whole circuit consumes a dc current of 13.8 mA at a supply voltage of 5 V.

III. MEASUREMENT RESULTS

The VM is measured with a Keysight VNA (PNA-X N5247B), VDI *D*-band extenders, and Cascade probes, which were calibrated with a SOLT substrate. The extender at the input side is equipped with an attenuator set to 25 dB to ensure linear operation. All results are deembedded such that the reference plane is in front of the BLC and behind the VM. We achieved this with a pad and balun back-to-back structure (presented in [59]). First, we measured the S-parameters of the back-to-back structure. Then, we transform the S-parameters to *ABCD*-parameters, which we use to deembed the pads and baluns using the RF-Toolbox of MATLAB. Since the balun has a simulated input matching of less than < -20 dB and the pads have a measured input matching of less than < -14 dB at 125 GHz, we expect minor deembedding errors [61]. The BLC itself is not deembedded since we consider the BLC and the VM as one unit whose performance is evaluated together.

Sections III-A–III-C provide detailed insights into all three breakout MMICs, with each section emphasizing specific circuit characteristics. The first MMIC [Fig. 1(a)] demonstrates the $|S_{21}|$ (dB) and $\arg\{S_{21}\}$ (°) parameters at 125 GHz using a constellation diagram when 1.2 V digital control signals are applied (see [58]). The second MMIC [Fig. 1(b)] showcases

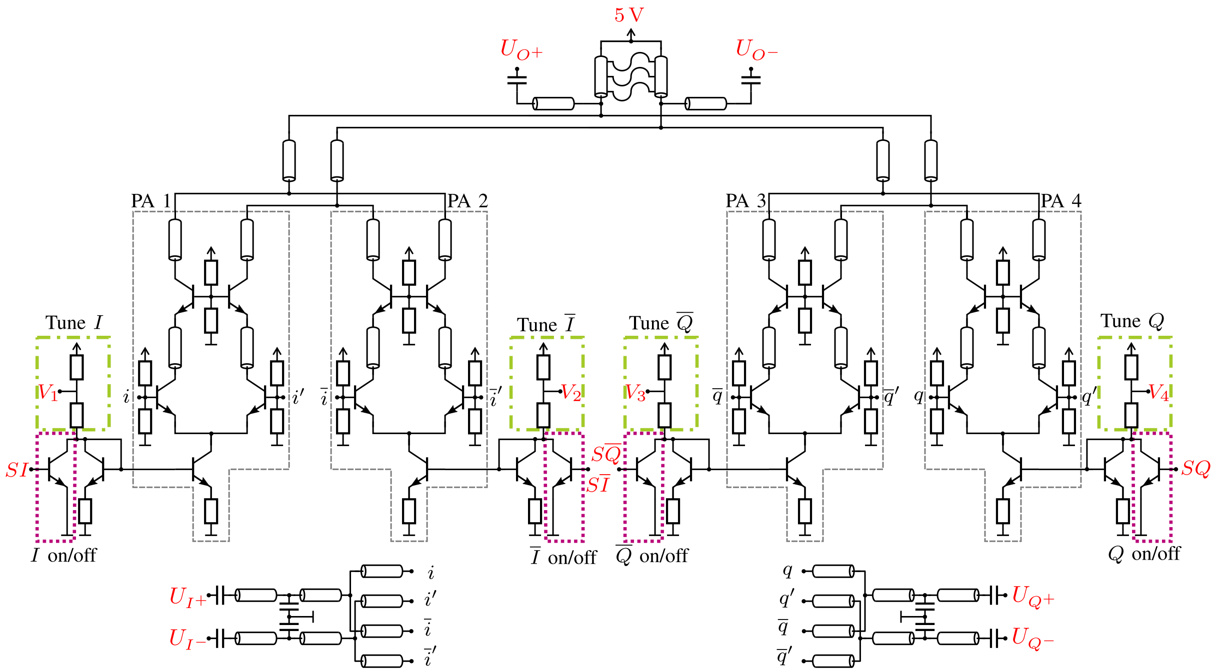


Fig. 3. 125 GHz VM circuit diagram with four switchable PAs, which superimpose, invert, or switch off the I and Q input signals (U_I and U_Q) to the output of the VM (U_O). The first MMIC includes the digital interface (Sx — purple dotted boxes), the second MMIC includes the analog interface enabled by a center tap between the two resistors (V_x — green dashed-dotted boxes), and the third one includes both. The matching networks shown below also serve as power dividers to supply four PAs with two input signals.

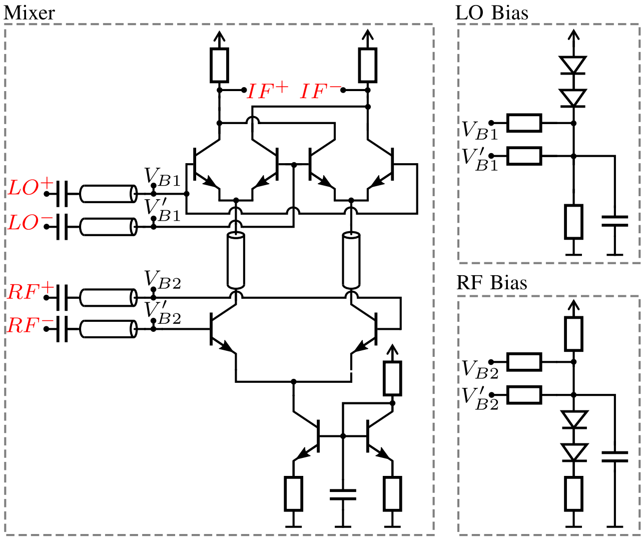


Fig. 4. Schematic of the mixer used on the third MMIC, showing the mixer core on the left and the bias network on the right side.

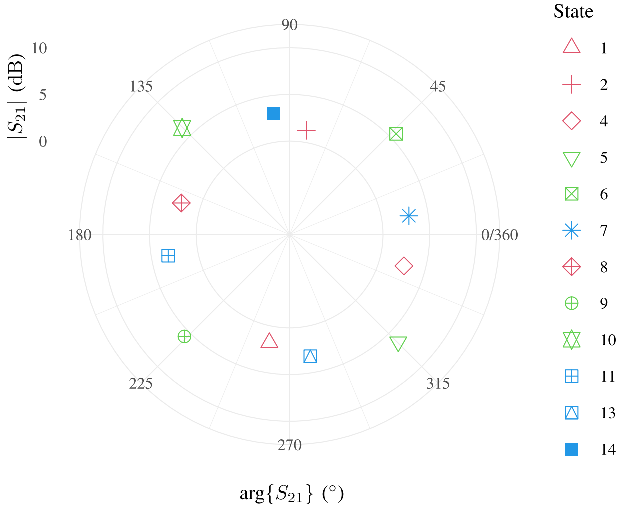


Fig. 5. Measured constellation diagram of the first MMIC at 125 GHz: The radial axis of the polar plot shows the gain ($|S_{21}|$ (dB) — scaling in the top left corner), and the circular axis shows the phase ($\arg\{S_{21}\}$ (°) — scaling at outer circle). States are not shown where both the I and Q path is "quasi-off" or off (similar to [58]).

analog tuning behavior, also based on S-parameter measurements. Furthermore, we conduct an extensive analysis of this analog tuning behavior to elucidate changes in gain and phase. The third MMIC [Fig. 1(c)] serves a distinct purpose: connecting the VM output to a mixer to enable a PMCW measurement, whose result is presented using an eye diagram.

A. First MMIC: Digital Control

The four digital input signals, controlling the four PAs inside the VM, generate up to 16 states. An overview of the different states and their current consumption is shown in Table I. Fig. 5 displays the 125 GHz S-parameter results in a constellation diagram, representing $|S_{21}|$ (dB) and $\arg\{S_{21}\}$ (°) in a polar plot. Depending on the state, an amplification of 6.03 dB (6.51 dB at 123.3 GHz) or attenuation of 39.88 dB are achieved when all PAs are switched off (shown in [58]). The diagram illustrates that the maximum gain is achieved when both $I/\overline{I}$ and $Q/\overline{Q}$ paths are active (states 5, 6, 9, and 10). When either $I/\overline{I}$ (states 7 and 11) or $Q/\overline{Q}$ (states 13 and 14) is employed, the VM amplifies by up to 2.84 dB. States 0 and 15 are omitted from the diagram to maintain its readability; otherwise, the radial axis scaling would be disrupted.

I and $\overline{I}$, as well as Q and $\overline{Q}$, are cross-connected to the inductive load, allowing for a 180° phase inversion. When

TABLE I
OVERVIEW OF THE FIRST MMIC'S 16 DIFFERENT OUTPUT SIGNALS AND THE MEASURED DC CURRENT (mA) AT 5 V [58]

State	I	Q	SI	$S\overline{I}$	$S\overline{Q}$	SQ	I_{dc}
0	q. off	q. off	0 V	0 V	0 V	0 V	59.9
1	q. off	on	0 V	0 V	0 V	1.2 V	47.8
2	q. off	inv.	0 V	0 V	1.2 V	0 V	47.6
3	q. off	off	0 V	0 V	1.2 V	1.2 V	36.0
4	on	q. off	0 V	1.2 V	0 V	0 V	47.2
5	on	on	0 V	1.2 V	0 V	1.2 V	35.7
6	on	inv.	0 V	1.2 V	1.2 V	0 V	34.5
7	on	off	0 V	1.2 V	1.2 V	1.2 V	23.6
8	inv.	q. off.	1.2 V	0 V	0 V	0 V	47.3
9	inv.	on	1.2 V	0 V	0 V	1.2 V	35.7
10	inv.	inv.	1.2 V	0 V	1.2 V	0 V	35.6
11	inv.	off	1.2 V	0 V	1.2 V	1.2 V	23.6
12	off	q. off	1.2 V	1.2 V	0 V	0 V	35.0
13	off	on	1.2 V	1.2 V	0 V	1.2 V	23.2
14	off	inv.	1.2 V	1.2 V	1.2 V	0 V	23.1
15	off	off	1.2 V	1.2 V	1.2 V	1.2 V	10.9

enabling both I and $\overline{I}$ (Q and $\overline{Q}$), the currents through the inductive load interfere destructively, resulting in "quasi-off" behavior. When one of the I or Q paths is in a "quasi-off" state (see Table I) while the other path is active (states 1, 2, 4, and 8, marked in red), a gain of up to 2.35 dB can be achieved. However, these "quasi-off" states exhibit slightly reduced gain, higher current consumption, and significant deviation from a linear phase (arg$\{S_{21}\}$ (°) — not shown here), indicating the effects of group delay [62].

The four digital control signals, resulting in eight ≈ 45° steps, limit the use inside a phased-array system. As seen later in the article, the primary purpose of the digital interface is the high-speed digital switching required for PMCW applications. Nevertheless, VNA results show that the VM allows for time-division multiplexing (TDM) FMCW MIMO radar applications, as the output of the VM can be switched off completely.

The phase relationships of the states are evenly distributed due to the generated IQ outputs (≈ 90°) of the BLC. Nonetheless, states 5, 6, 9, and 10 (where both $I/\overline{I}$ and $Q/\overline{Q}$ are active, marked in green) do not have a phase difference of ≈ 45° from states 7, 11, 13, and 14 (where either $I/\overline{I}$ or $Q/\overline{Q}$ is active, marked in blue). This phenomenon is also observed in simulations and is attributed to parasitic influences within the layout, namely the PA's nonisolated collector nodes at the inductive load.

B. Second MMIC: Analog Control

In the previous subsection, we explored the digital control of the first MMIC, presenting 12 different states. Now, we investigate the second MMIC, where we employ analog control using the two resistors and their center tap (see Fig. 3). Instead of numbering the states after the measurements, we name the states after the used PAs since we analyze 676 different measurements using the second MMIC.

First, we apply only two different voltages to the four different tuning inputs, either switching the PA off (0 V) or operating the PA with the optimal current density to achieve maximum gain (3 V). These signals are labeled as $I/\overline{I}$ and $\overline{Q}/Q$ in the plots depending on the PAs used. Consequently, we have eight unique VM configurations because none/one PA in the I path and/or none/one PA in the Q path is used.

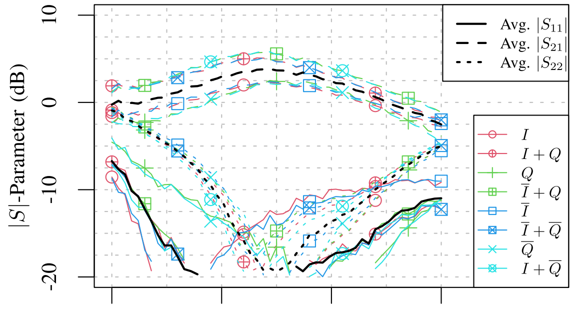


Fig. 6. Measured and deembedded S-parameters (dB) of the second MMIC at 125 GHz with one or two active PAs. The solid lines show S_{11}, the dashed lines show S_{21}, and the dotted lines show S_{22}. The averaged curves are shown with thick black lines without any marker.

Fig. 6 illustrates the deembedded measurement curves for S_{11}, S_{21}, and S_{22}. With two PAs active, we achieve a gain of up to 5.57 dB at 125 GHz or a maximum gain of 5.89 dB at 123.8 GHz. When using only one PA, we obtain gains of 2.41 and 2.36 dB, respectively. In comparison to the first MMIC, the maximum values deviate by less than 1 dB, which indicates a good measurement credibility since different MMICs with independently calibrated measurement setups were used.

While the VM's output matching remains independent of the PAs used, the input matching depends on the tuning voltages. This effect is attributed to the HBT's diffusion capacitance C_{BE}, which varies with collector current [63, p. 520]. Since we use a common-emitter topology, the input impedance and, therefore, the input matching of the VM are affected by the tuning voltages.

The averaged curves for all eight different configurations are also displayed in Fig. 6. The VM achieves an averaged maximum gain of 4.21 dB at 125.18 GHz and an averaged 3/6 dB bandwidth of 17.04/28.74 GHz (13.6%/22.9%).

The S_{21} phase curves are presented in Fig. 7, revealing relatively uniform spacing, which is nearly identical to the first MMIC (see Fig. 5). This uniformity is primarily determined by the accuracy of the BLC [59]. While the desired 45° spacing is mostly achieved at both ends of the frequency spectrum, it starts to diverge due to BLC limitations.

1) Compression Behavior: In addition to the measured S-parameters that encompass gain and matching, compression behavior is a crucial performance indicator in radar systems. Unlike the measured S-parameter data, we illustrate the compression behavior through simulations. Fig. 8 illustrates the compression behavior when one or two PAs are fully active. These curves can be categorized into two groups: those with either one PA active or two. Both groups exhibit a similar trend but are vertically shifted relative to each other due to power combining.

For $I/\overline{I}$, the 1 dB input compression point is −1.37 dBm, whereas for $Q/\overline{Q}$, it is −1.86 dBm. When both I and Q are active in the same way ($I+Q$ and $\overline{I}+\overline{Q}$), the compression point is −1.58 dBm. When one of them is inverted, the

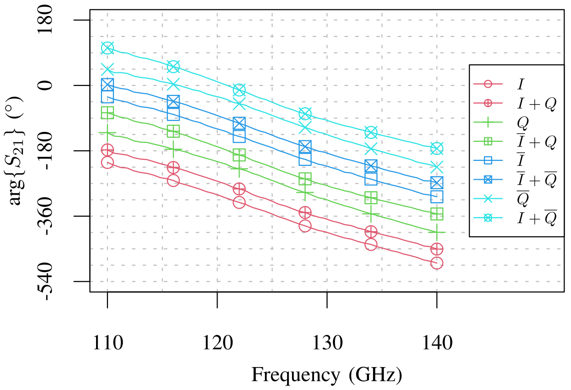


Fig. 7. Measured and deembedded S_{21}-parameter (°) of the second MMIC at 125 GHz with one or two active PAs.

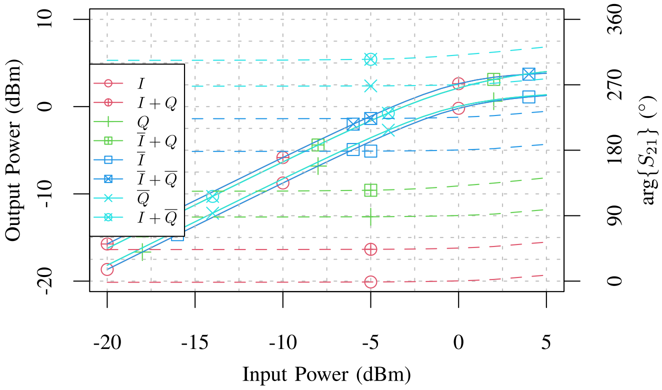


Fig. 8. Simulated compression behavior of the VM for eight different configurations using *RC* parasitics, EM simulation results of the BLC, differential ports, and 80 °C device temperature. The solid lines show the output power, and the dashed lines show the $\arg\{S_{21}\}$ (°) parameter.

compression point is -1.71 dBm. Minor differences in layout result in different curves for I and Q. When splitting the IQ input signals or connecting the collector nodes of the common-base stage to the inductive load, we had to change the layers and cross TRLs using vias. These differences lead to minor variations in the compression curves. When using the VM inside a radar system, it is preferable to incorporate an additional amplifier before the antenna, boasting a higher saturated output power.

Furthermore, Fig. 8 depicts the behavior of $\arg\{S_{21}\}$ (°), where almost every state behaves equally for increasing input power except for $\overline{I}+Q$ and $I+\overline{Q}$. Those states also show a slightly higher gain (see Fig. 9), resulting in a slightly earlier onset of compression.

2) Constellation Diagram: Fig. 9 presents the constellation diagram for the second MMIC. We chose the voltages 0, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500, 2000, 2500, and 3000 mV. With the four different quadrants (combinations of $I/\overline{I}$ and $Q/\overline{Q}$), there are $4 \cdot (13^2) = 676$ different measurements. To manage the quadratic increase, we employed larger steps from 1500 mV upward to maintain a reasonable number of measurements. We plotted each of the 676 different VNA measurements at 125 GHz in a polar plot but omitted points with less than -20 dB.

The markers differ in color and shape based on the employed PAs, with shapes consisting of circles for I (PA 1), squares for $\overline{I}$ (PA 2), crosses for $\overline{Q}$ (PA 3), or plus signs for Q (PA 4). Intensity varies according to the control voltage (0 V $\widehat{=}$ invisible; 3 V $\widehat{=}$ full intensity). In the first quadrant (Q1 $\widehat{=}$ red), the circle and plus sign are more prominent at $\approx 0°$ and $\approx 90°$, respectively. Similar schemes are employed in other quadrants, each with different colors and marker styles highlighting distinct PA combinations. A different style of displaying the control voltage is used later in Fig. 11.

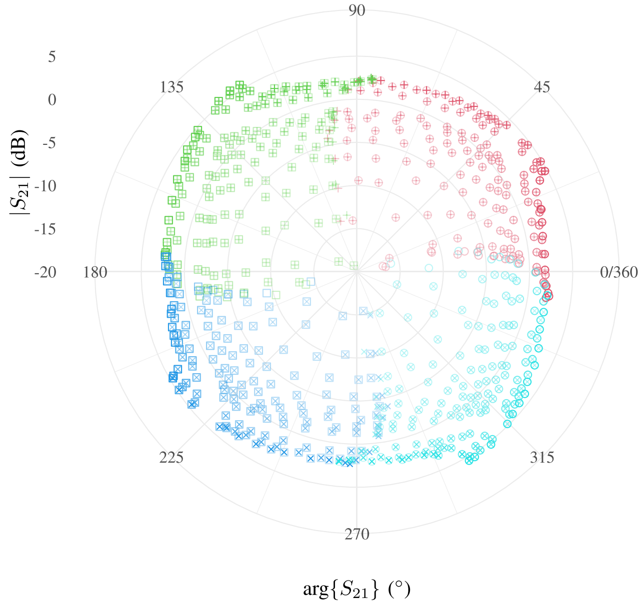


Fig. 9. Measured constellation diagram of the second MMIC at 125 GHz: The radial axis of the polar plot shows the gain ($|S_{21}|$ (dB) — scaling in the top left corner), and the circular axis shows the phase ($\arg\{S_{21}\}$ (°) — scaling at outer circle). Each color and marker style shows a specific combination of PAs, thus a quadrant in the constellation diagram. The circles/squares show the $I/\overline{I}$ component and the plus signs/crosses show the $Q/\overline{Q}$ components. The intensity of the marker indicates the amplitude of the used tuning voltages.

Due to the vector superposition of I and Q, the points at $\approx 45°$, $\approx 135°$, $\approx 225°$, and $\approx 315°$ have a larger amplitude, i.e., a larger radius (see Fig. 5). Also, in radial direction a gap exists since the voltage step from 1500 to 2000 mV results in a notable increase in gain. When using finer resolved steps, the gap would disappear. In summary, the constellation diagram appears symmetrical, just showing minor differences between the quadrants, which emphasizes the accuracy of the BLC and the inductive load.

3) Accuracy: This section delves into the detailed analysis of the VM's behavior based on the control voltages employed. Utilizing Fig. 10, we can examine the VM's behavior from a systems designer's perspective. The plot visualizes the maximum gain and the corresponding control voltages used in the VNA measurements, which in turn is a different representation of Fig. 9. The angular range spanning from 0° to 360° has been divided into 5° sections. While many data points fall within a single section, we have highlighted the point with the maximum gain and the respective control voltages for each angular section. Notably, each control voltage spans two adjacent quadrants, allowing for continuous output phase tuning.

Furthermore, it is important to note a significant jump in control voltage values, occurring between 1500 and 2000 mV, as evident from the graph. This jump results in reduced

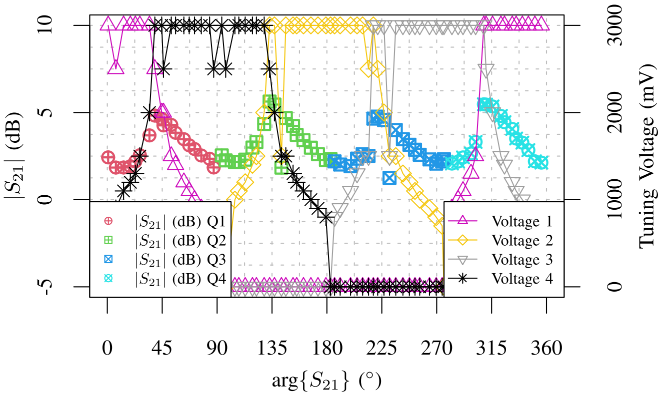


Fig. 10. Analysis of the used analog tuning voltages (MMIC 2) to generate 360° phase shift at 125 GHz. The colors indicate the used quadrant and tuning voltage, respectively. Only the maximum $|S_{21}|$ (dB) values in each 5° section are analyzed.

maximum gain in specific angular ranges, as observed in Fig. 9, leading to spikes, such as at approximately 230°, where voltage 4 transitions from 3000 to 1500 mV as another tuning voltage combination takes over. Therefore, when using the VM inside a system, the control voltage should be at least 100 mV over the whole tuning range, omitting steps that are too large (e.g., 500 mV).

Based on the information provided in Fig. 10, we calculate the rms phase and gain variations across the $N = 72$ angular sections using (1) and (2). We compare the measured phase value $\varphi(n)$ and gain value $A(n)$ to the ideal phase value ($\varphi_{\text{ideal}}(n) = n \cdot 5° + 2.5°$) and the mean gain value ($\overline{A} = 3.14$ dB). Notably, the VM exhibits an rms phase deviation of just 1.32° and an rms gain deviation of 1.1 dB

$$\Delta\varphi = \sqrt{\frac{1}{N} \cdot \sum_{n=0}^{N=71} (\varphi(n) - \varphi_{\text{ideal}}(n))^2} \tag{1}$$

$$\Delta A = \sqrt{\frac{1}{N} \cdot \sum_{n=0}^{N=71} \left(A(n) - \overline{A}\right)^2}. \tag{2}$$

4) Output Analysis: To refine our analysis of the tuning behavior, we chose to interpolate constellation points from the first quadrant (see Fig. 9) [64], which avoids the need to perform thousands of measurements. We interpolate the tuning voltages with a step size of 12.89 mV, which emulates the step size of an 8-bit, low-cost DAC (0–3.3 V). Smaller interpolation steps are feasible but not practical due to relatively coarse measurement steps (≥ 100 mV). Fig. 11(a) presents the interpolated $|S_{21}|$ (dB) data for values above -20 dB, while Fig. 11(b) showcases the interpolated $\arg\{S_{21}\}$ (°) data. Both figures are interconnected via three contour lines shared between them (30°, 60°, and 90°, as well as -3, 0, and 3 dB). Fig. 11(a) illustrates a rapid gain increase as the tuning voltages exceed approximately 700 mV. Additionally, the asymmetry of the I and Q paths of the VM becomes evident, as the 2 dB contour line behaves differently in the right and upper regions of the plot. This discrepancy arises from small layout differences in the VM and a minor IQ imbalance of the BLC. When extracting the possible output phases in Fig. 11(b), we observe that the VM can produce more than 90° when superimposing the I and Q input signals. This is because of the HBT's behavior (capacitance) and, therefore, the VM's output phase changes regarding the dc current. However, when voltages 1 and 4 increase, the possible output angle narrows, as illustrated in Fig. 11(b). In summary, the VM achieves a continuous gain of ≈ 1.5 dB across the entire 90° angular span.

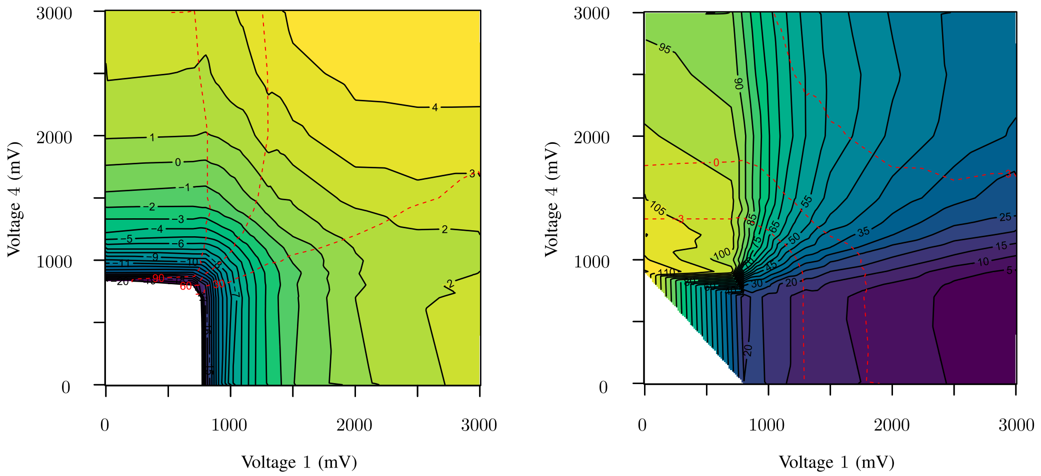
C. Third MMIC: Binary Phase Modulation

Research on PMCW radar has seen a surge in recent years, driven by its attractive attributes with regard to mitigating interference [22], [65], [66], [67]. However, PMCW radar introduces novel challenges in the digital domain [23], [68]. One critical factor in PMCW radar is the speed of phase shift keying (B_c), as it directly impacts the system's range resolution [23]. This resolution, denoted as Δr, is related to B_c by the equation $\Delta r = c/(2 \cdot B_c)$, where c represents the speed of light. Notably, this range resolution is analogous to the bandwidth of an FMCW system [23].

In the first MMIC version, which was presented in [58], no mixer was included in the MMIC design, resulting in the necessity of simulating the switching speed. Using the states $I + Q$ and $\overline{I} + \overline{Q}$, we achieved 10 GHz of modulation speed. In the third MMIC version, explicitly designed for validating the PMCW principle, a mixer is positioned at the VM's output, replacing the balun. This mixer is driven by two essential signals: a monofrequent LO signal generated by the VNA and the VDI extender, which feeds both the mixer and the VM, and the binary-modulated output from the VM. To facilitate this setup, the digital control ports of the VM are connected to a two-channel M8190A 12 GSa/s (5 GHz) Keysight arbitrary waveform generator (AWG) via a differential probe and SMA cables. In this context, we manipulate the I and $\overline{I}$ states using a pseudorandom bit sequence (PRBS), effecting a 180° signal inversion.

As a result of the mixing process, the mixer's IF signal includes the same binary sequence that we initially applied to the VM. This enables examining both the modulation principle and the mixer itself. The mixer's output is connected to a Keysight N9041B UXA signal analyzer using SMA cables and a dc block filter. But, the UXA's analysis bandwidth of 1 GHz limits the usable bandwidth of the AWG significantly. The measured eye diagram is shown in Fig. 12, recorded with the signal vector analyzer functionality of the Keysight UXA. It can be seen that the eye is still clearly open. To what extent the flat transitions are produced by the mixer/modulator or by the measurement setup (e.g., the bandwidth of the UXA) cannot be conclusively clarified. However, the simulations show that the VM can reach a significantly higher modulation frequency [58], which suggests that the analysis bandwidth causes flat transitions.

Given that the third MMIC integrates both digital and analog interfaces, we utilized laser fuses within the MMIC to disengage the mixer from both the VM and the pads while establishing a connection between the VM's output and the pads, as elaborated in Section II. Consequently, we conducted a total of 676 analog and 16 digital measurements using this third MMIC. Our observations revealed similar tuning behavior compared to MMIC 1 and 2, except for a minor gain offset



(a) (b)

Fig. 11. Contour plot with linear interpolated (a) $|S_{21}|$ (dB) and (b) $\arg\{S_{21}\}$ (°) data from the first quadrant of the constellation diagram using MMIC 2. Important S_{21} (°) (a) and $|S_{21}|$ (dB) (b) contours are highlighted with red dashed lines, respectively. The plots depict the tuning behavior of the VM, showcasing the range of possible output phases and amplitudes.

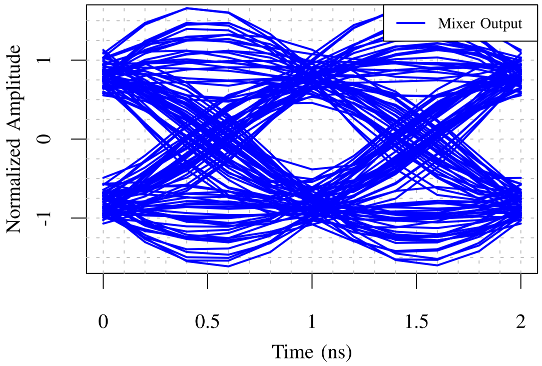


Fig. 12. Measured eye diagram using the third MMIC and a PRBS with a switching frequency of $B_c = 1$ GHz. The UXA normalizes the amplitude.

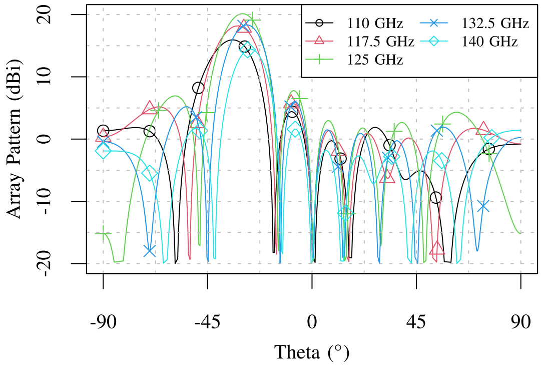


Fig. 13. Beam squint analysis of the VM using eight antennas with a $\lambda_0/2$ spacing and the measured S-parameter data. The phase difference of each antenna is ≈ 90°, so the steering angle is ≈ 30°. The frequency was tuned from 110 to 140 GHz.

due to the inability to compensate for the WK power divider, the laser fuses, and the output pads. If these components could be compensated accordingly, all measurements in this article could have been conducted with MMIC 3.

IV. PHASED-ARRAY ANALYSIS

In this section, we delve into the system characteristics of the VM. To accomplish this, we leverage the measured S-parameter data obtained from the second MMIC, which incorporates analog control. Our objective is to estimate the properties of a uniform linear array (ULA) comprising eight antennas, with an antenna spacing set to $\lambda_0/2$, equivalent to $c_0/(2 \cdot 125\,\text{GHz})$. Equation (3) is used to calculate the array factor [26, p. 293]. In addition, the eight antennas are operated with different control voltages, i.e., with a phase difference of 90°. In addition, the frequency is swept in 7.5 GHz steps. The control voltages are the same for each frequency point

$$F_{\text{dB}}(\theta) = 20 \cdot \log_{10}\Bigg[\sum_{m=1}^{M} A(m) \cdot e^{j\psi(m)} \cdot e^{j \cdot k_0 \vec{r}(m) \cdot sin(\theta) \cdot cos(\varphi_0)}\Bigg]. \tag{3}$$

$A(m)$ is the $|S_{21}|$ (dB) parameter in linear representation, ψ is the $\arg\{S_{21}\}$ (°) parameter, $k_0 = 2\pi/\lambda_0$ is the wavenumber, θ is the spatial angle at which the beam is steered, and φ_0 is a constant angle.

The array factor is shown in Fig. 13. Depending on the selected phase difference between the antennas, the beam can be steered over the complete angular range. Due to the fact that the VM generates only a phase shift and no true time delay, a minor beam squint can be seen. Furthermore, a variation of the amplitude of the array factor can be seen due to the nonconstant S_{21} value (see Fig. 6).

Managing the eight input signals the VM requires for both analog and digital operations can be space-intensive. However, using all eight pads can provide a notable advantage. The VM's analog interface enables an angle selection for the array's beam, while the digital pads facilitate binary phase modulation. Given that the beam's direction is solely defined by the phase difference [as per (3)], applying a uniform phase shift of 180° to all channels does not alter the beam's angle. In summary, using all eight signals enables steerable PMCW signals without using high-speed DACs since only high-speed IO signals are needed, which, to the author's best knowledge, has not been reported yet.

TABLE II

STATE OF THE ART SIGE BICMOS-BASED 360° VMS AT FREQUENCIES ABOVE 100 GHZ

Ref.	**Frequency (GHz)**	**Tech.**	**Area** (mm^2)	**Peak Gain (dB)**	P_{DC} **(mW)**	$P_{1\,dB}$ **(dBm)**	**Control**	**RMS Amplitude (dB)**	**RMS Phase** (°)
[44]	140 – 200	130 nm	$0.26^{\ddagger}$	$10^{\spadesuit}$ ($3.5^{\spadesuit c}$)	28	—	analog	< 3	< 10
[43]	115	130 nm	2.11	$0.5^{\clubsuit}$	$33^{\clubsuit}$	-22 (IP)$^{\clubsuit}$	analog	< 1.6	< 5.5
[47]	92 – 100	130 nm	$0.853^{\ddagger}$	$9.5^{\spadesuit a}$:	50	-26 (IP)	analog	< 1.8	< 5
[27]	113 – 127	130 nm	$0.05^{\ddagger}$	$18.7^{\spadesuit}$	225	0.7 (OP)	analog	—	—
[31]	110 – 130	250 nm	—	$-10^{\spadesuit}$	148	-9 (OP)	analog	—	—
[33]	220 – 250	130 nm	—	$-8^{\clubsuit}$	106	-5 (IP)$^{\clubsuit}$	analog	—	—
[37]	140 – 160	55 nm	$0.05^{\ddagger}$	-4.5	50	2 (IP)	analog	< 1.4	< 7.5
[38]	162 – 190	130 nm	$0.07^{\ddagger}$	-6.2	12.4	-13.5 (IP)$^{\clubsuit}$	analog	< 1	< 8
[42]	160 – 200	130 nm	$0.075^{\ddagger}$	-9.5	8.6	—	analog	< 0.9	< 15
[69]	75 – 100	130 nm	—	$-5^{\clubsuit}$	—	-2 (IP)$^{\clubsuit}$	on-chip DAC	< 1	< 7.5
[70]	146 – 156	130 nm	0.45	-13^{a}	148	—	analog	< 2.8	< 6.9
[71]	200 – 250	130 nm	$0.09^{\ddagger}$	-10.3	55	$-4^{\clubsuit}$	analog	< 1.25	< 10
[50]	110 – 145	90 nm	0.81	1.5	20.3^{a}	-9	analog	< 1.2	< 8.5
[72]	270 – 330	130 nm	$0.023^{\ddagger}$	-10	65	$1^{\clubsuit}$	on-chip DAC	–	< 0.98
[55]	110 – 145	90 nm	0.572	-5.5	21	-4.8	analog	< 1.25	–
[73]	210 – 230	130 nm	$0.046^{\ddagger}$	$-11^{\clubsuit}$	$27^{\clubsuit}$	–	analog	< 1.1	< 2.22
[74]	86 – 106	–	$0.027^{\ddagger}$	2.3^{a}	49	$0.6^{\clubsuit}$	on-chip DAC	< 1	< 6.6
[59]	110 – 140	130 nm	$0.086^{\ddagger}$	6.55 (4.13^{a})	60 – 225	-0.63 (IP)$^{\diamondsuit}$	digital	2.57	16.91
This$^{\sharp}$	110 – 140	130 nm	$0.086^{\ddagger}$	5.57 (3.13^{a})	173	-1.86 (IP)$^{\clubsuit}$	analog	< 1.11	< 1.32

Note: ‡ core area, $^{\spadesuit}$: with additional amplifiers, ^{c} : contentious 360° gain, ^{a} : average, $^{\clubsuit}$: simulated, $^{\diamondsuit}$: at 110 GHz, $^{\sharp}$: Second MMIC.

V. COMPARISON

The comparison of SiGe-based VMs above 100 GHz is shown in Table II and highlights different criteria. The three most important are the gain and the rms errors for amplitude and phase. Considering that the majority of other VMs in the table employ an analog interface for tuning, we incorporate the second MMIC. Here, we achieve excellent values with 5.57/3.13 dB peak/average gain. Moreover, when comparing the presented with other VMs that do not use additional PAs, it shows the second-highest gain since the architecture is based on a PA topology and not on a Gilbert-cell. Also, it shows rms amplitude and phase errors of just 1.11 dB and $< 1.32°$. Particularly, the rms phase error has to be emphasized since it is the second-best value, even though we use a minimum step size of 100 mV (≤ 5 bits). Furthermore, both the compression point and the area consumption are competitive. While other VMs consume less energy, they often need additional PAs to compensate for the VM's losses, which increases the MMIC's size and power consumption.

VI. CONCLUSION

In this article, we presented a 125 GHz VM that enables fast-switching digital modulation and precise analog control while providing a high gain. With a minimum step size of 100 mV (≤ 5 bits), we altered the phase with 5° steps and achieved rms variations of only 1.11 dB and 1.32°. Moreover, we investigated the phased-array behavior using a synthetic ULA and the measured *S*-parameter data. With a frequency ramp of 30 GHz and constant tuning voltages, only a slight beam squint occurs, which should be targeted in future research. Furthermore, the VM amplifies the input signal with an average gain of 3.13 dB and a maximum gain of 5.89 dB. At lastly, with a measured attenuation of ≈ 40 dB, the VM can also be used in time-division MIMO applications.

In addition to its analog tuning capabilities, the VM offers fast BPSK modulation. A switching speed of up to 10 GHz was simulated, and 1 GHz was measured, constrained solely by the signal analyzer's bandwidth. Therefore, the VM supports not only phased-array and time-division MIMO functionality but also high-speed BPSK modulation, essential for PMCW radar. Also, the combination of BPSK modulation and analog phase control presents a notable advancement, enabling the realization of steerable PMCW beams without necessitating high-speed DACs. To summarize, the VM's adaptability enables its seamless integration into various applications without requiring any circuit design or layout modifications.

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