A 360 GHz Fully Integrated Differential Signal Source With 106.7 GHz Continuous Tuning Range in 90 nm SiGe:C BiCMOS

David Starke, *Graduate Student Member, IEEE*, Florian Vogelsang, *Graduate Student Member, IEEE*, Jonathan Bott, *Graduate Student Member, IEEE*, Jan Schöpfel, *Graduate Student Member, IEEE*, Christian Bredendiek, *Member, IEEE*, Klaus Aufinger, *Member, IEEE*, and Nils Pohl, *Senior Member, IEEE*

***Abstract*— Commercial frequency-modulated continuous-wave (FMCW) radar systems are well-established in the frequency range up to 100 GHz, with some exceptions operating in the D-band and above. There are multiple advantages of operating at higher frequencies, such as the use of ON-chip antennas and, therefore, the omission of high-frequency substrates for frontend designs, which enables the fabrication of low-cost FR4 radar frontends. This work features a 360 GHz fully integrated signal source and breakout circuits at 90 and 180 GHz, manufactured in the 90 nm B12HFC SiGe:C BiCMOS technology. We present a 90-GHz wideband Colpitts–Clapp VCO combined with a static frequency divider for stabilization purposes, achieving a tuning range (TR) of 24.1 GHz and an output power of up to 6.43 dBm. Adding a frequency-doubling and amplification stage expands this circuit, achieving 51.7-GHz TR and up to 3.8-dBm output power. The 360 GHz signal source adds another frequency-doubling stage consisting of a wideband differential hybrid coupler for quadrature signal generation, amplifier chains, and two push–push frequency doublers, generating a pseudodifferential output signal with up to −1.8 dBm output power and a frequency TR of 106.7 GHz (29.9%).**

Manuscript received 30 September 2023; revised 14 December 2023; accepted 15 January 2024. Date of publication 6 February 2024; date of current version 7 August 2024. The research work presented in this paper was funded in part by the German Research Foundation ("Deutsche Forschungsgemeinschaft") (DFG) under Project-ID 287022738 TRR 196 for Project C02 and C03, by the German Federal Ministry of Education and Research (BMBF) in the course of the 6GEM research hub under grant number 16KISK037 and by the German Ministry for Economic Affairs and Climate Action (BMWK) in the project URBANSens (no.: 20D2106B) within the research program LuFo VI-2. Furthermore, this project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 876019. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Germany, Netherlands, Austria, Romania, France, Sweden, Cyprus, Greece, Lithuania, Portugal, Italy, Finland, Turkey. This article is an extended version from the International Workshop on Mobile THz Systems, Bonn, Germany, July 3–5, 2023 [DOI: 10.1109/IWMTS58186.2023.10207849]. *(Corresponding author: David Starke.)*

David Starke, Florian Vogelsang, Jonathan Bott, and Jan Schöpfel are with the Institute of Integrated Systems, Ruhr University Bochum, 44801 Bochum, Germany (e-mail: david.starke@rub.de).

Christian Bredendiek is with Fraunhofer Institute for High Frequency Physics and Radar Techniques FHR, 53343 Wachtberg, Germany.

Klaus Aufinger is with Infineon Technologies AG, 85579 Neubiberg, Germany.

Nils Pohl is with the Institute of Integrated Systems, Ruhr University Bochum, 44801 Bochum, Germany, and also with Fraunhofer Institute for High Frequency Physics and Radar Techniques FHR, 53343 Wachtberg, Germany.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2024.3356610.

Digital Object Identifier 10.1109/TMTT.2024.3356610

***Index Terms*— B12HFC, Colpitts–Clapp, frequency doubler, frequency multiplier, frequency-modulated continuous-wave (FMCW) radar, integrated microwave circuits and systems, Lange couplers, millimeter-wave (mmWave) and terahertz components, power amplifier (PA) circuits, semiconductor sources for terahertz, SiGe heterojunction bipolar transistors (SiGe HBTs) circuits, signal generation, signal sources, silicon germanium (SiGe) BiCMOS, static frequency divider, voltage-controlled oscillator (VCO), wideband circuits.**

I. Introduction

CIRCUIT and system designers have increasingly focused on the terahertz (THz) frequency range in the past few years. Recent developments in semiconductor technologies [1], [2], [3] enable circuits and systems beyond the millimeter-wave (mmWave) band ($30-300$ GHz) and deep into the THz frequency band between 0.3 and 3 THz [4], [5], [6], [7], [8]. The THz band has multiple advantages for applications like sensing and communication, such as the large available bandwidth or the small wavelength enabling massive MIMO arrays for small-scale systems. On the other hand, this frequency band is challenging for sensing or communication system designs, because of the increased path loss at these frequencies and the limited output power of these systems because of the operation close to the used semiconductors' maximum frequency $f_{\max}$ [9]. In the last years, complex systems in the THz frequency range, such as THz transceivers and radar systems, have been presented [10], [11]. Even highly integrated frequency-modulated continuous-wave (FMCW) radar transceivers with operation frequencies of nearly 0.5 THz have been demonstrated in the latest research [12], [13].

The main advantage of pushing FMCW radar transceiver designs into the THz frequency range is the large achievable bandwidth. The minimum range resolution Δr of an FMCW radar system is directly linked to the bandwidth, or frequency tuning range (TR) of the radar sensor [14]

$$\Delta r = \frac{c_0}{2 \cdot \mathrm{TR}}. \tag{1}$$

As the relative frequency TR (rTR) of voltage-controlled oscillators (VCOs) in the high mmWave frequency band is limited to around 40% [15] and tends to decrease for higher center frequencies, more complicated signal generation approaches have to be used to achieve higher bandwidths.

For example, the signal generation can be done at lower center frequencies but considerably higher relative TRs [16] and then frequency multiplication is applied to achieve the targeted output frequency. One challenge of this approach is the higher complexity compared with a single VCO and the degradation of phase noise due to the frequency translation of the frequency multipliers. Another solution to extend the frequency TR at a given output frequency is the combination of the frequency TRs of several VCOs [17], [18], which has the disadvantage of considerably more complex circuit and system design compared with a single VCO.

For realizing even higher bandwidth sensors, the center frequency of the radar system is often increased to the low THz frequency region. One of the challenges in these circuits is the generation of high-quality signal sources for these THz systems. A common approach to this problem is the utilization of external signal sources and frequency multiplication [5], [12], [19], [20], [21], [22], [23]. This concept is also used for fully integrated signal sources, which often use an approach of fundamental signal generation and frequency multiplication for a compromise between output power and phase noise [24], [25], [26].

In [27], we introduced and demonstrated two wideband, differential, integrated signal sources at 90 and 180 GHz, with TRs of 24.1 and 51.7 GHz, respectively. In this article, we expand the published findings by detailing the implemented wideband power amplifier (PA) chain at a frequency of 180 GHz and by complementing the published signal sources with an additional frequency-doubling stage achieving differential signal generation at a center frequency of 360 GHz over a TR of 106.7 GHz. This work demonstrates the capabilities of novel SiGe technologies and the possibility of designing transceiver systems well into the THz frequency region, maintaining a high level of integration complexity.

In this article, we begin by introducing the state of the art in THz signal sources, giving an overview of different realizations of THz sources, and focusing on a comparison of integrated silicon germanium (SiGe) sources in the low THz region in Section II. The circuit designs of the three presented signal sources are explained in Section III, including an introduction of the used 90 nm B12HFC semiconductor technology by Infineon Technologies AG. In Section IV, the experimental results of the implemented circuits are detailed and the measurement results are compared with the state-of-the-art signal sources in silicon technologies. The article ends with a conclusion in Section V.

II. State-of-the-Art SiGe THz Sources

Terahertz sources can be broadly classified into two categories by their respective principle of generating the THz signals. The first category of THz sources is photonic THz sources. In these systems, an optical approach is used to generate the THz signals, either by downconverting pulsed or CW laser beams or by directly emitting THz radiation using quantum cascade lasers, photodiodes, or photoconductors [42]. The second realization method of THz signal generation is electronic THz sources. The main advantage of these THz sources is the small size, reliability, and

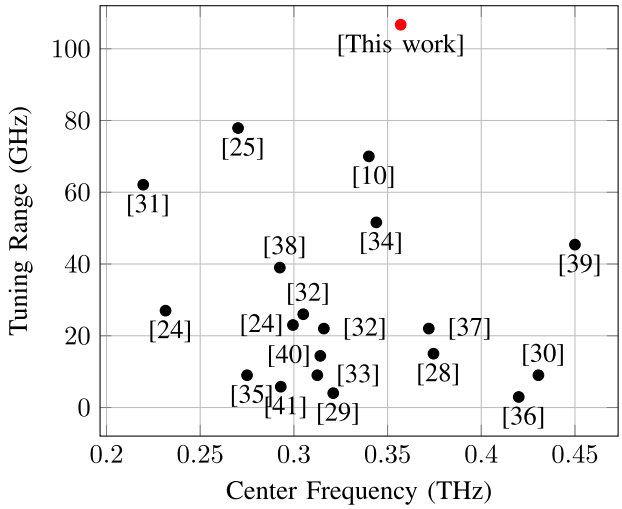

Fig. 1. Comparison of the state-of-the-art fully integrated SiGe sources in the frequency range between 0.2 and 0.5 THz.

the possibility to integrate additional functionality into the source, not only realizing a THz signal source but also implementing complex systems into electronic measurement or communication devices in the THz band. Electronic THz sources relying on highly integrated circuits are limited by the available performance of the used semiconductor technologies. In recent years, THz sources using CMOS, SiGe heterojunction bipolar transistors (SiGe HBTs), and III–V semiconductor technologies, such as indium phosphide (InP), have been demonstrated successfully. These technologies have distinctive advantages and disadvantages and must be carefully chosen for the intended application. Modern CMOS technologies offer a very high level of integration and compatibility with digital logic, so highly complex systems can be integrated into a THz device. Usually, THz sources using III–V technologies exhibit a low level of integration but show higher output powers compared with CMOS or SiGe HBT signal sources. Output frequencies above 1 THz can be achieved when using resonant tunneling diodes, which can be used as an oscillator and have been demonstrated to reach output frequencies of almost 2 THz [43], or Schottky barrier diodes, which have been implemented in THz sources based on cascaded frequency multiplication reaching up to 2.75 THz [44], [45], [46]. Modern SiGe BiCMOS technologies offer good THz performance while still using a high level of integration. Even complex THz systems, such as fully integrated FMCW radar frontends [13] or massive THz radiator arrays [36], can be integrated into a single chip using SiGe technologies.

In SiGe HBT technologies, the development is driven to achieve higher output frequencies and greater frequency TRs of the sources. For sources with a small bandwidth, radiation at 1 THz has been demonstrated in a 130-nm SiGe BiCMOS technology [47]. When looking at high bandwidth signal sources in the low THz frequency range, between 200 and 500 GHz, frequency TRs of more than 70 GHz have been demonstrated in SiGe technologies [10], [25]. A comparison of the state-of-the-art fully integrated SiGe sources up to 500 GHz can be seen in Fig. 1. In this figure, the TR of

the recently published fully integrated SiGe THz sources is plotted over the respective output center frequency.

This work demonstrates a fully integrated 360 GHz source with a continuous frequency TR of 106.7 GHz in a 90 nm SiGe BiCMOS technology. To the authors' knowledge, this is the highest achieved TR for fully integrated, silicon-based THz sources to date [48].

III. Circuit Design

The integrated signal sources presented in this section of this article were designed for a wideband, fully integrated monostatic radar sensor at THz frequencies with more than 100-GHz bandwidth. As interfacing MMICs at this frequency range and high bandwidth is challenging [49], [50], a fully integrated approach was chosen where only low-frequency signals (<10 GHz) are fed from the MMIC to a frontend printed circuit board (PCB). This, in return, means that the radar signal at a center frequency of 360 GHz and a TR of more than 100 GHz has to be radiated from the MMIC using an integrated wideband antenna. A differential antenna concept based on [51] was chosen for this application, which means the signal generation of this radar system also has to generate differential output signals at 360 GHz to avoid a potential bandwidth-limiting balun at the input of the antenna.

An integrated frequency divider is used to divide the center frequency of 90 GHz down to ≈6 GHz to enable the use of commercial phase-locked-loop (PLL) components for frequency stabilization and chirp generation [52]. This low frequency also enables the use of low-cost FR4 PCB material to implement the frontend, which makes the design of low-cost THz transceivers feasible. This material is considerably cheaper than dedicated high-frequency substrates which often drives the price of mmWave and THz components and sensors. The design decision to reduce the frequency of external signals and include the complete high-frequency componentry on the designed MMIC enables the development of low-cost, small form-factor radar sensors in the frequency range between 200 and 500 GHz and above [53]. Combining the complete radar MMIC, which consists of the signal generation presented in this article, a subharmonic receiver, and an efficient differential antenna with high bandwidth, with an FR4 frontend and dielectric lens [54], a complete FMCW radar sensor, roughly the size of a matchbox, can be designed with frequency TRs exceeding 100 GHz for various applications. The high TR leads to high range resolution, enabling the determination of targets close to each other or very high-resolution imaging applications and measurement accuracies in the scale of microns [55], [56]. The center frequency of this system was chosen to be 360 GHz, as this is close to the minimum frequency needed to generate more than 100 GHz of TR with an integrated oscillator operating in the mmWave frequency band. With a higher frequency multiplication factor than 4, as in the presented circuit, a TR of 100 GHz could be achieved at lower center frequencies at the expense of increased physical size and higher phase noise due to the higher frequency conversion factor and, therefore, decreased range accuracy. Preliminary simulations showed that a oscillator at a frequency of approximately 90 GHz and a frequency multiplication factor of four are a good compromise to reach the intended output frequency range for the targeted form-factor and intended applications.

All the circuits detailed in this article were developed and manufactured in the preproduction 90 nm SiGe:C BiCMOS technology B12HFC from Infineon Technologies AG [1], [2], [3]. In addition to some of the fastest bipolar transistors in SiGe with a transit frequency f_T of 300 GHz and a maximum oscillation frequency $f_{max} \geq 500$ GHz, this technology provides p-n junction varactors, RF-MIM capacitors, and RF-TAN resistors. The metal stack of this technology consists of seven copper layers with an additional aluminum layer for bond pads or laser fuses. Four copper layers at the bottom of the metal stack are fine-pitch metal layers for general signal routing on the MMIC. In contrast, the top three layers, with thicknesses between 800 and 2000 μm, can be used to implement high quality factor (Q) passive microwave and THz circuit elements such as coupling structures or microstrip transmission lines [57].

The circuits presented in this section were designed close to the optimal current density of the transistors for maximum f_T and f_{max}. Therefore, the simulations should have been verified using an HICUM model, which more accurately models the high-current effect of the bipolar transistors as operation above the optimum current degrades quickly for higher currents [57]. Due to the early stage of development of the used semiconductor technology, HICUM models were not available during the design of the circuits, so Gummel–Poon models were used which do not sufficiently model high-current effects [58]. Therefore, the circuits' operation point was ensured to stay slightly below the optimum current for all the operation circumstances.

Due to the high signal frequencies and large bandwidths of the developed circuits, they are very susceptible to degradation by circuit parasitics. Therefore, the parasitic elements of all the described circuit cores, consisting of the transistors, vias, capacitors, and the surrounding metal structures, were extracted and considered in the circuit simulations. Furthermore, passive structures such as couplers or transmission lines were EM-simulated using the simulation environment Sonnet 18.52, and the results of these simulations were used while designing the circuits.

The circuits presented in this article were designed to be used in conjunction with each other. Therefore, the inputs and outputs of individual circuit blocks are not necessarily matched to 50- or 100-Ω interfaces but are matched to the other circuit stages. An exception is the 180–360 GHz frequency doubler, as this circuit is designed to drive a differential coupler and a differential antenna, both optimized for 100-Ω interfaces. All the other circuits are optimized for each other in simulations. Input and output impedances of the individual circuit stages were implemented in the simulation environments of preceding and subsequent circuit blocks to optimize the complete chain for the best possible performance.

A. 90-GHz Signal Source

The 90-GHz signal source discussed in this article is realized with a voltage-controlled oscillator (VCO) in a

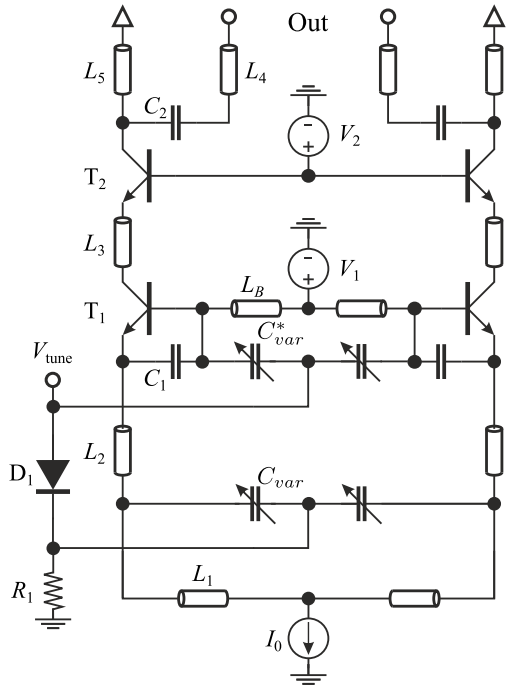

Fig. 2. Schematic of the implemented Colpitts–Clapp VCO. From [27].

TABLE I
DIMENSIONS AND COMPONENT VALUES OF THE IMPLEMENTED VCO CIRCUIT

Comp.	Dimensions; Value; Description
T_1	w_{eff} = 120 nm; l = 7 μm; 2x CBEBC
T_2	w_{eff} = 120 nm; l = 10 μm; 3x CBEBC
D_1	w_{eff} = 120 nm; l = 1 μm; 2x BEBCBEB
C_1	40 fF
C_2	100 fF
C_{var}	w = 1 μm; l = 10 μm; 6 Fingers
C^*_{var}	w = 1 μm; l = 10 μm; 6 Fingers
L_1	w = 2.5 μm; l = 183.4 μm
L_2	w = 6.5 μm; l = 22.35 μm
L_3	w = 6.5 μm; l = 57 μm
L_4	w = 6.5 μm; l = 201.6 μm
L_5	w = 6.5 μm; l = 94 μm
L_B	w = 12.8 μm; l = 95.7 μm
R_1	3 kΩ

Colpitts–Clapp architecture. This topology combines the well-known Colpitts and Clapp oscillator architectures, extending the frequency TR of the circuit. This combination is performed using two simultaneously tunable varactors in the core of the oscillator, one at the emitters of the core transistors T_1, as in the Colpitts architecture, and one at the base of the core transistors, in parallel to the resonator inductance L_B, as in the Clapp architecture [59], [60]. The combination of these two varactors extends the frequency TR compared with a traditional Colpitts or Clapp oscillator. A common base output amplifier is connected to the oscillator core to decouple the core from load influences, such as frequency pulling, and improve the oscillator's output power. A schematic of the designed Colpitts–Clapp VCO is depicted in Fig. 2. The values for the components used to implement the oscillator are given in Table I.

One single external tuning voltage is needed to tune both varactor diodes C_{var} and C^*_{var}. To compensate for the dc voltage drop of the base–emitter diode of the VCO core transistor T_1, the diode D_1, implemented with a transistor with a shorted collector–emitter diode, is implemented in the tuning path. The external tuning voltage V_{tune} can be varied between 1 and 8.7 V.

Inductive elements of this circuit are implemented using microstrip transmission lines, whose length can be tuned after manufacturing to compensate for technology variance and parasitic effects, which may not be included in the simulations performed for this circuit. These fuses can be cut using a laser to vary the length of the transmission lines to tune the resonant frequency of the oscillator by tuning the length of the line L_B or to tune the resonant frequency of the load lines L_5.

The dc power for this circuit is supplied by the integrated current source I_0, which can also be adjusted to tune the circuit's performance. This current source also ensures the rejection of any common-mode oscillation so that only a differential signal is generated at the output nodes of the circuit. This common-mode rejection is further improved by the low resistivity voltage sources V_1 and V_2 at the virtual common-mode ground nodes at the symmetry plane of the circuit [61].

For circuit characterization purposes, 50-Ω load resistors were implemented at the output nodes of the oscillator, next to the output bond pads, which can be removed by destruction of the laser fuses. These resistors emulate the oscillator's loading by single-ended measurement equipment commonly used in this frequency band. Furthermore, the current source, implemented with a current mirror, can be tuned by applying an external voltage to the reference path of the current mirror. This external adjustment can be used to tune the oscillator's performance and, additionally, to turn off the oscillator temporarily.

To implement the possibility of using commercial PLL components for frequency stabilization of the oscillator and chirp generation, a divide-by-16 prescaler complements the VCO, which converts the 90-GHz center frequency (f_c) of the VCO down to a signal with a center frequency of $\approx$5.6 GHz. A static frequency divider architecture in emitter-coupled logic (ECL) is chosen for its reliability and robustness. Inductive shunt peaking is used in the first stage of this prescaler to improve the maximum operating frequency of this frequency divider circuit [62]. Capacitive coupling between the oscillator and frequency divider and asymmetric biasing of the first divider stage is used to prevent oscillation of the divider. The circuit diagram of one stage of this divider circuit is depicted in Fig. 3. The biasing and capacitive coupling of the first stage is not shown in the schematic for reasons of better readability. Also not shown is the generation of the external voltage V_{I0}, which is generated by a voltage divider to create a common control signal for all the current sources T_1–T_6 of the frequency divider. Stages three to four are biased by the output emitter–follower of the preceding divider stage. As the first

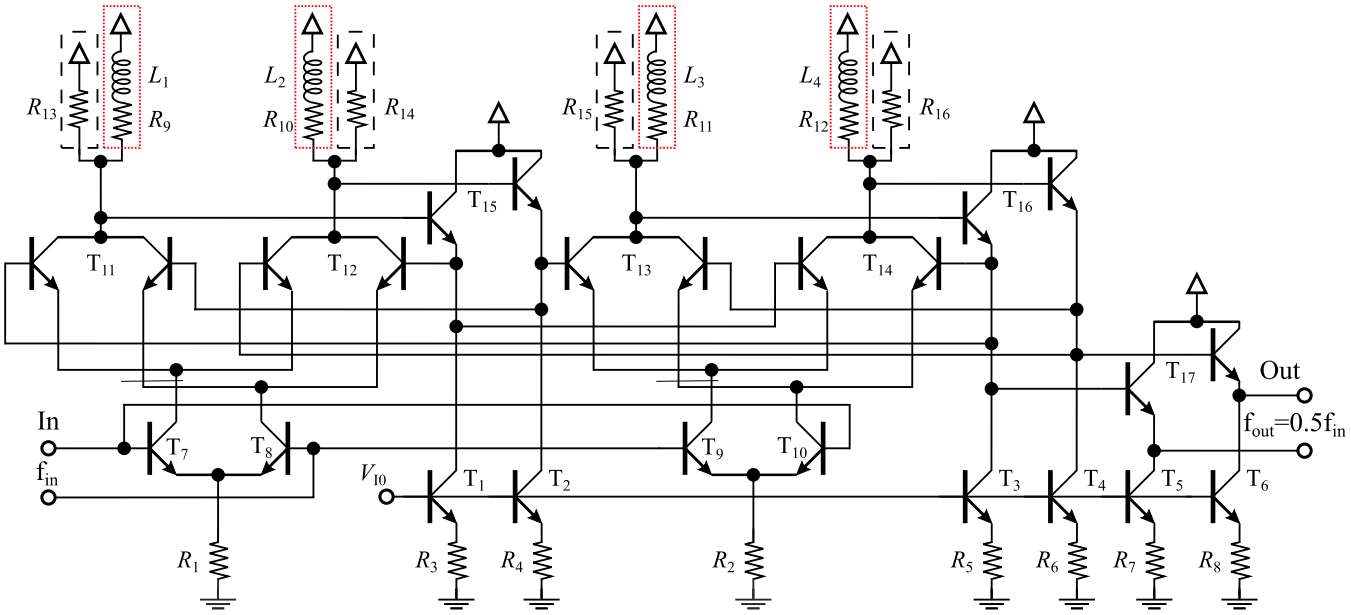

Fig. 3. Schematic of the divider stages of the implemented frequency divider in ECL logic. Apart from the load components, depicted in the dashed and dotted boxes, circuits use a similar schematic with scaled components, detailed in Table II. Inductive shunt peaking (red dotted boxes) is only used in the first stage of the frequency divider. The second to fourth stages of the divider use resistive loads (black dashed boxes).

TABLE II
COMPONENT DIMENSIONS AND VALUES OF THE IMPLEMENTED DIVIDE-BY-16 FREQUENCY DIVIDER CHAIN

Comp.	Dimensions; Value; Description
Stage 1: $T_1 - T_6$	w_{eff} = 120 nm; l = 1.5 μm; BEBC
Stage 1: $T_7 - T_{10}$	w_{eff} = 120 nm; l = 1.3 μm; BEC
Stage 1: $T_{11} - T_{17}$	w_{eff} = 120 nm; l = 1.3 μm; BECEB
Stage 2: $T_1 - T_6$	w_{eff} = 120 nm; l = 1.2 μm; BEBC
Stage 2: $T_7 - T_{10}$	w_{eff} = 120 nm; l = 1.0 μm; BEC
Stage 2: $T_{11} - T_{17}$	w_{eff} = 120 nm; l = 1.0 μm; BECEB
Stage 3: $T_1 - T_6$	w_{eff} = 120 nm; l = 1.0 μm; BEBC
Stage 3: $T_7 - T_{10}$	w_{eff} = 120 nm; l = 1.0 μm; BEC
Stage 3: $T_{11} - T_{17}$	w_{eff} = 120 nm; l = 1.0 μm; BECEB
Stage 4: $T_1 - T_6$	w_{eff} = 120 nm; l = 900 nm; BEBC
Stage 4: $T_7 - T_{10}$	w_{eff} = 120 nm; l = 700 nm; BEC
Stage 4: $T_{11} - T_{17}$	w_{eff} = 120 nm; l = 700 nm; BECEB
$L_1 + L_2$; $L_3 + L_4$	375 pH (diff); Q = 10.3 (diff)
$R_9 - R_{12}$	75 Ω
Stage 1: $R_1 - R_2$	145 Ω
Stage 1: $R_3 - R_8$	170 Ω
Stage 2: $R_1 - R_2$	317 Ω
Stage 2: $R_3 - R_8$	221 Ω
Stage 2: $R_{13} - R_{16}$	125 Ω
Stage 3: $R_1 - R_2$	539 Ω
Stage 3: $R_3 - R_8$	375 Ω
Stage 3: $R_{13} - R_{16}$	161 Ω
Stage 4: $R_1 - R_2$	700 Ω
Stage 4: $R_3 - R_8$	536 Ω
Stage 4: $R_{13} - R_{16}$	255 Ω

stage of the frequency divider uses inductive shunt peaking, the components given in the red dotted box are only used in the first stage. Stages two to four use only resistive loads,

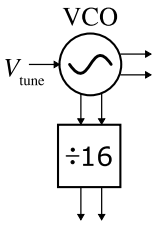

Fig. 4. Functional block diagram of the integrated 90-GHz signal source consisting of a wideband Colpitts–Clapp VCO and a static divide-by-16 prescaler.

as displayed in the black dashed boxes in this figure. The component values of the components used in this circuit are given in Table II. A functional block diagram of the complete presented 90-GHz signal source is depicted in Fig. 4.

These circuits were fabricated on a breakout chip for circuit characterization with GSGSG output pads for the oscillator and GSSG pads for the output of the differential frequency divider. A photograph of this fabricated breakout MMIC can be seen in Fig. 5. The chip size, including the pad frame, is 815 × 565 μm. The total area of the implemented circuits without the pad frame is 0.12 mm^2.

B. 180-GHz Signal Source

The 180-GHz signal source described in this section is a combination of the 90-GHz VCO, described in Section III-A, and a frequency doubler, followed by a PA.

A block diagram of the implemented fully differential signal source is depicted in Fig. 6.

1) Frequency Doubler: The output signal of the VCO, with a center frequency of 90 GHz, is frequency-doubled by a frequency doubler based on a bootstrapped Gilbert-cell topology [63], [64]. In contrast to a regular Gilbert-cell frequency doubler that needs quadrature input signals to eliminate the

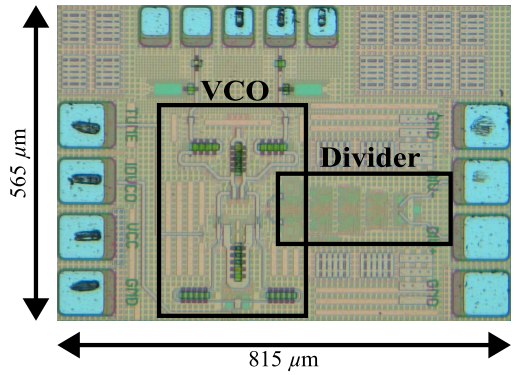

Fig. 5. Photograph of the implemented Colpitts–Clapp VCO. From [27].

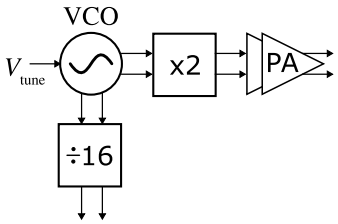

Fig. 6. Functional block diagram of the integrated 180-GHz signal source consisting of a VCO, a static frequency divider, frequency doubler, and PA stage.

dc voltage offset at the output of the mixer quad [65], this topology introduces the phase shift of the signals by a coupling network consisting of the coupling capacitor C_1 and the delay line L_2. Using this circuit architecture, a fully differential frequency doubler with high bandwidth and low amplitude and phase imbalance was designed and manufactured. A schematic of the designed frequency doubler can be seen in Fig. 7. The component dimensions and values used in this circuit are given in Table III.

2) Power Amplifier: The PA used at 180 GHz consists of two consecutive amplifier stages. Each stage is realized as a differential cascode amplifier with transmission lines between the differential pair and the common-base amplifier for internal matching. To improve the bandwidth of the PA chain, both the output networks of the consecutive amplifiers have slightly different resonance frequencies. This well-known circuit topology was used as this circuit architecture was successfully implemented and tested in another novel SiGe preproduction technology in a similar frequency range [39]. Although the PA chain is not optimized for stand-alone operation, as it was optimized to be matched to the output impedance of the first frequency doubler and the input impedance of the push–push frequency doubler, a breakout MMIC was manufactured to characterize the PAs. This breakout MMIC consists of the PA chain with rat-race baluns and GSG probe pads at the input and output of the circuit to enable the use of single-ended measurement equipment. This breakout MMIC is depicted in Fig. 8. The dimensions of this MMIC, including the pad frame, are 940 $\times$ 580 μm, while the PA chain itself has the dimensions of 320 $\times$ 160 μm.

A photograph of the realized 180-GHz signal source MMIC, consisting of the VCO, frequency divider, frequency doubler,

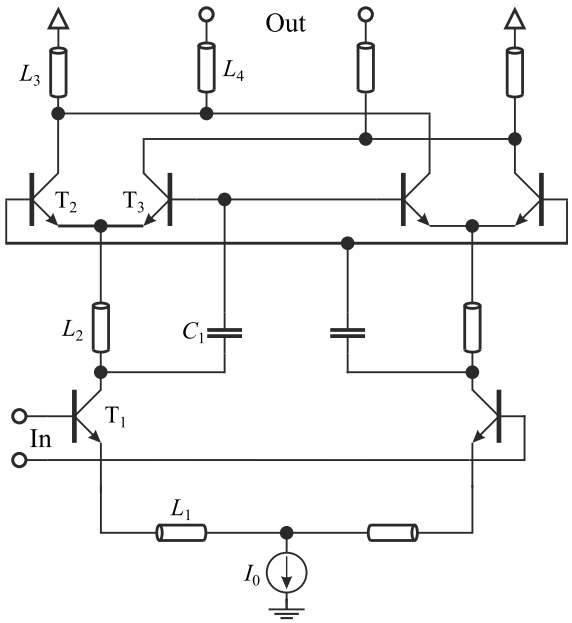

Fig. 7. Schematic of the implemented frequency doubler. From [27].

TABLE III
COMPONENT DIMENSIONS AND VALUES OF THE IMPLEMENTED 90–180-GHz BOOTSTRAPPED GILBERT-CELL FREQUENCY DOUBLER CIRCUIT

Comp.	Dimensions; Value; Description
T_1	w_{eff} = 120 nm; l = 10 μm; CBEBBEBC
T_2	w_{eff} = 120 nm; l = 8 μm; BEBC
T_3	w_{eff} = 120 nm; l = 8 μm; BEBC
C_1	100 fF
L_1	w = 6.5 μm; l = 205 μm
L_2	w = 5.5 μm; l = 140 μm
L_3	w = 12 μm; l = 113.8 μm
L_4	w = 6.5 μm; l = 145 μm

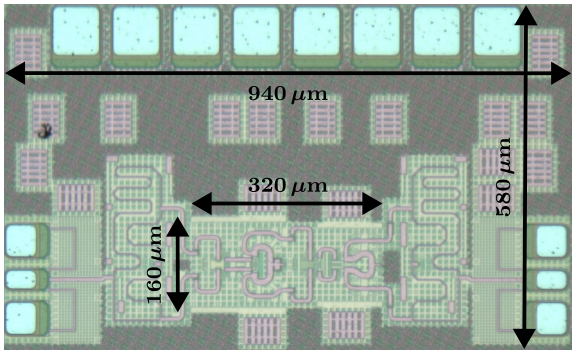

Fig. 8. Micrograph of the breakout MMIC for PA characterization.

and PAs, can be seen in Fig. 9. The dimensions of this MMIC including the pad frame are 1270 $\times$ 840 μm.

C. 360 GHz Signal Source

To generate an output signal at frequencies above the transit frequency of the used semiconductor technology, push–push frequency doublers are commonly used [12], [19], [39]. This architecture of frequency doubler can generate output

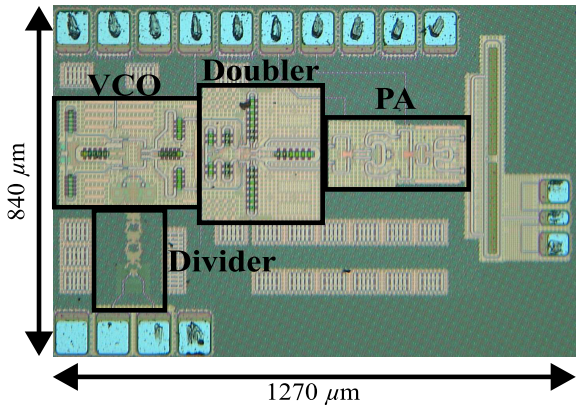

Fig. 9. Micrograph of the developed 180-GHz signal source MMIC. From [27].

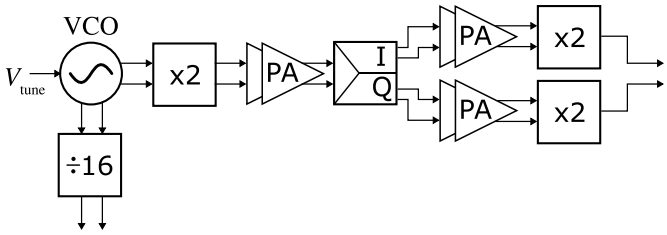

Fig. 10. Functional block diagram of the implemented 360 GHz signal source.

signals above the respective transit frequency while still providing high output power. One disadvantage of this circuit architecture is the loss of one signal phase at the output of the frequency doubler related to the input signal. Driven by a differential input signal at a frequency f_0, push–push doublers will convert this signal to a single-ended signal at the doubled frequency $2f_0$ [65].

As specified at the beginning of Section III, this signal source is designed to be part of a fully differential FMCW THz radar transceiver with a frequency TR of more than 100 GHz. Therefore, a method was implemented to generate this differential output signal. Because of the frequency range of more than 100 GHz, a passive balun, like a rat-race coupler, would have significant losses because of the limited bandwidth of these coupler structures. We used two frequency doublers fed with quadrature signals to generate a differential output signal [66], [67], [68]. These quadrature signals are generated by integrated hybrid couplers described in Section III-C1. The design of the 180–360 GHz frequency doublers is detailed in Section III-C2. A functional block diagram of the implemented 360 GHz signal source is depicted in Fig. 10.

Due to limited available space on the reticle of the development run of the B12HFC technology, no separate breakout MMIC was manufactured for the characterization of this 360 GHz signal source, but it was implemented with a receiver circuit to form a complete radar MMIC with bond pads at the output of the signal source and the input of the receiver. This MMIC was manufactured solely for circuit characterization purposes. A photograph of this MMIC is depicted in Fig. 11. To maximize the usage of the available space on the chip, the 180-GHz source is rotated 90° with regard to the rest of the 360 GHz source. The output signal of the 180-GHz source is split using a power divider for the transmit and

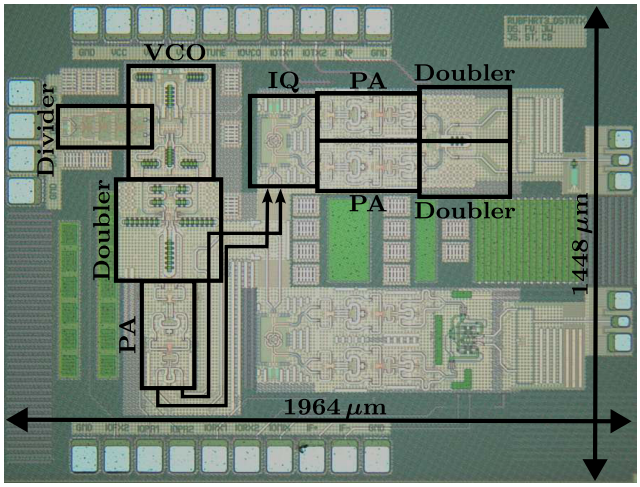

Fig. 11. Micrograph of the developed 360 GHz signal source MMIC. The circuit blocks forming the signal sources described in this article are highlighted. The area of the circuit blocks forming the 360 GHz source is 0.43 mm^2.

receive path of the system, with the transmit path forming the presented 360 GHz signal source. The size of this complete radar transceiver MMIC is 2.84 mm^2.

1) 180-GHz Hybrid Coupler: The quadrature signals needed for the final frequency-doubling path are generated using an integrated differential Lange coupler based on a design presented in [69]. Lange couplers have multiple advantages, such as a small footprint and higher bandwidth compared with other realizations of quadrature couplers, i.e., branchline couplers. Traditional Lange couplers use laterally coupled lines connected with bond wires to implement a four-port quadrature coupler. In our approach, the coupling is done vertically between windings implemented on metal layers M5 and M6 of the MMIC, with bridges between the windings on metal layers M4 and M7.

The center frequency of this coupler is dependent on the loop length of the coupler, with smaller coupler dimensions leading to a higher center frequency. For the targeted frequency range around 180 GHz, a coupler diameter of 55 μm was determined. For the least possible amplitude and phase mismatch between the in-phase and the quadrature output of the coupler, the metal layers of the loops are switched, ensuring the circuit layout's symmetry. The fourth port of the coupler is terminated with two integrated 50-Ω resistors, preventing any reflections of this port and providing a dc potential for the long transmission lines between the 180-GHz signal source and the final frequency-doubling stage. The realized circuit layout of the coupler is depicted in Fig. 12.

The simulation results of the realized Lange coupler are depicted in Fig. 13. For a frequency range between 50 and 220 GHz, the input reflection coefficient S_{11} is below −13.8 dB, and for frequencies between 103.2 and 207.1 GHz, the amplitude error between S_{21} and S_{31} is below 3 dB with a phase error between 1.61° and 6.71°.

2) Frequency Doubler: The second frequency doubler in this THz source is also driven by the PAs discussed in Section III-B2. The quadrature signals must be amplified to drive the differential push–push frequency doubler. Therefore, two PA chains are implemented in the 360 GHz source, one for

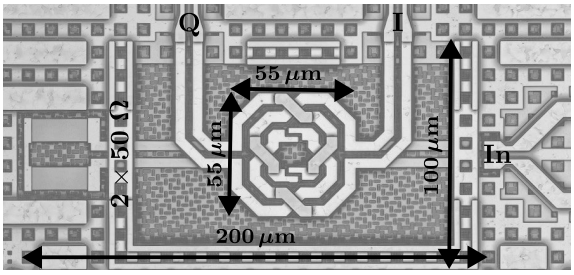

Fig. 12. Manufactured layout of the proposed quadrature coupler. The size of the coupler is 200 × 100 μm including 50 Ω termination resistors. The size of the coupling structure is 55 × 55 μm.

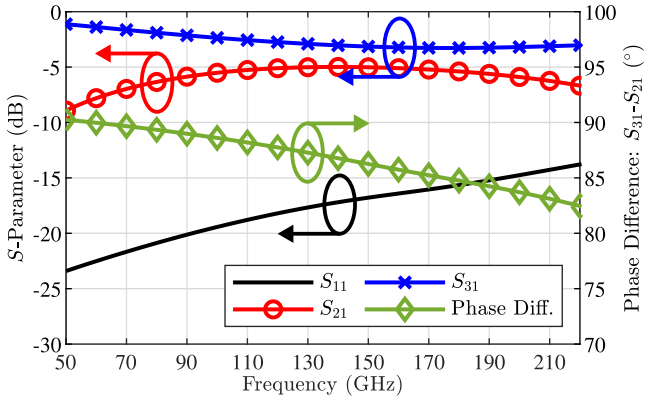

Fig. 13. Simulated S-parameters and phase difference of the implemented hybrid coupler for frequencies between 50 and 220 GHz. Simulations were performed in Sonnet 18.52.

the in-phase path and another for the quadrature-phase path. The frequency-doubling stage is implemented by two independent push–push frequency doublers. The frequency doublers' circuit layout was optimized to form a pseudodifferential frequency doubler using two symmetry cells of one frequency doubler mirrored at one axis. Especially the layout of the doublers load, implemented by the microstrip transmission lines L_7 and L_8, whose length can be adjusted by cutting the laser fuses F_1, was optimized for the best matching of the two pseudodifferential output signals. A circuit schematic of this pseudodifferential push–push frequency doubler is depicted in Fig. 14. The component dimensions and values used in this frequency doubler are given in Table IV.

The pseudodifferential frequency-doubling stage enables the possibility to generate differential output signals with high bandwidths without the use of a potentially bandwidth-limiting balun. Compared with a single push–push doubler and subsequent balun, a higher output power can be achieved as well, as the losses of the balun can be avoided with this topology.

A micrograph of the manufactured circuit layout of the frequency-doubling cell is depicted in Fig. 15.

IV. Experimental Results

In this section, the measured results of the three described wideband signal sources are given and discussed. In Section IV-A, the 90-GHz signal source measurement results are presented. The measurement results of the repeatedly used PA are discussed in Section IV-B, while in

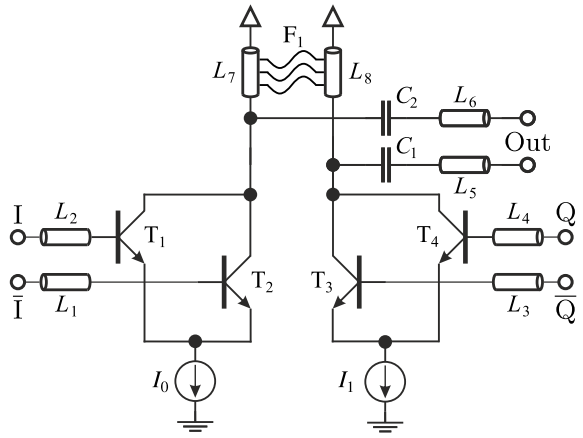

Fig. 14. Schematic of the pseudodifferential 180–360 GHz push–push frequency doubler.

TABLE IV
Component Dimensions and Values of the Implemented 180–360 GHz Push–Push Frequency Doubler Circuit

Comp.	Dimensions; Value; Description
T_1	w_{eff} = 120 nm; l = 5 μm; BEBCBEB
T_2	w_{eff} = 120 nm; l = 5 μm; BEBCBEB
T_3	w_{eff} = 120 nm; l = 5 μm; BEBCBEB
T_4	w_{eff} = 120 nm; l = 5 μm; BEBCBEB
C_1	75 fF
C_1	75 fF
L_1	w = 1.8 μm; l = 88 μm
L_2	w = 1.8 μm; l = 88 μm
L_3	w = 1.8 μm; l = 88 μm
L_4	w = 1.8 μm; l = 88 μm
L_5	w = 6.5 μm; l = 50 μm
L_6	w = 6.5 μm; l = 50 μm
L_7	w = 12 μm; l = 64.2 μm
L_8	w = 12 μm; l = 64.2 μm

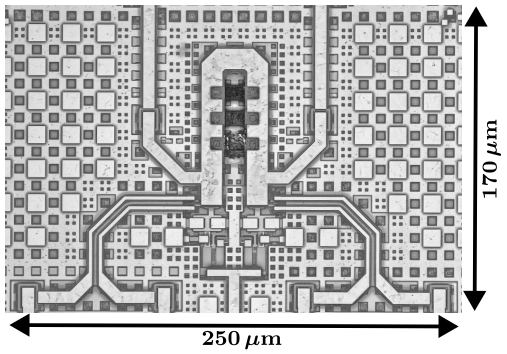

Fig. 15. Manufactured circuit layout of the pseudodifferential 180–360 GHz push–push frequency doubler.

Section IV-C, the results of the 180-GHz signal source are elaborated in detail. Section IV-D introduces the experimental results of the 360 GHz signal source. All these measurements were performed at room temperature. To conclude this section, the measurement results of the three presented signal sources are compared with the state of the art in mmWave and THz

wideband signal sources, with an emphasis on the performance of the THz source at 360 GHz.

A. 90-GHz Signal Source

The output frequency and phase noise of the 90-GHz signal source were measured indirectly at the output of the frequency divider with a Rohde & Schwarz FSWP phase noise analyzer. Because of the frequency translation of the divide-by-16 prescaler with the frequency division factor N, the measured phase noise $\mathrm{PN_{DIV}}$ had to be corrected to calculate the phase noise $\mathrm{PN_{VCO}}$ at the output of the VCO [70]

$$\mathrm{PN_{VCO}} = \mathrm{PN_{DIV}} + 20 \cdot \log_{10}(N). \tag{2}$$

The output power of the VCO was measured using a Keysight 8489A power sensor. The power sensor was connected to one set of GSG output pads on the chip, while the other output of the differential pair was matched using the integrated 50-Ω termination resistor to prevent an unbalanced load from influencing the circuit negatively. At the measured output, the integrated termination resistor was removed by cutting the laser fuse to match the circuit at this port.

While characterizing the tuning behavior of the VCO, the tuning curves of the oscillator were measured for different lengths of the resonator transmission line L_B, which was lengthened in subsequent measurements by cutting the laser fuses connected to L_B. With this variation, the center frequency of the VCO was adjusted from the highest frequency of 104.5 GHz, at the shortest setting of L_B, to the targeted frequency of 90.7 GHz by the destruction of three laser fuses. For verification of the performance of the divide-by-16 prescaler, the VCO was set to the highest frequency at the shortest resonator configuration. Here, the operation of the frequency divider up to 119.2 GHz could be verified. The prescaler was also tested for every other fuse configuration and applied tuning voltage, so an operation frequency range of 78.7–119.2 GHz was verified in measurement.

When set to the targeted center frequency f_c of around 90 GHz, a frequency TR between 78.7 and 102.8 GHz, resulting in a relative TR (rTR) of 26.55%, was measured. A peak output power of 6.43 dBm was determined for a frequency of 85.2 GHz, with a total variation of 2.9 dB over the whole TR of 24.1 GHz. The output power and phase noise, measured at an offset frequency Δf of 1 MHz, for the VCO in this fuse configuration, can be seen in Fig. 16.

The current consumption of the 90-GHz signal source breakout MMIC is 87 mA from a 3.3-V supply voltage, resulting in a power consumption of 287.1 mW. When the VCO was temporarily shut down by turning off its current source, it could be determined that 58 mA was consumed just by the frequency divider, which leaves a current consumption of 29 mA for the oscillator. A power consumption of 95.7 mW for the VCO alone can be calculated, translating into a peak dc-to-RF efficiency of 4.59%.

B. 180-GHz PA

The measurement results of the implemented PA chain were obtained using a Keysight PNAX vector network analyzer

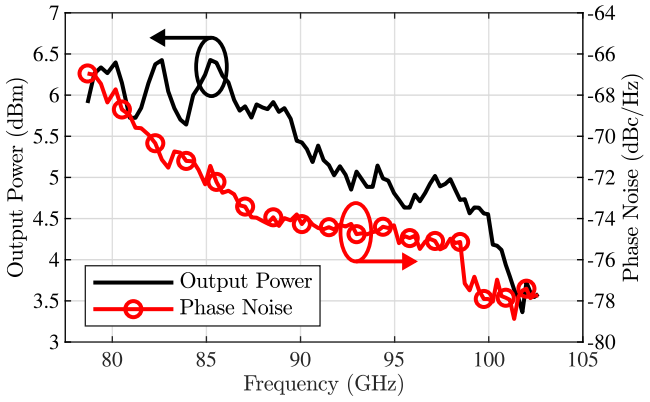

Fig. 16. Measurement results of the implemented Colpitts–Clapp VCO. The phase noise is evaluated for an offset frequency Δf of 1 MHz. From [27].

with VDI WR5.1-VNAX frequency extension modules and the corresponding Formfactor T220 T-Wave probes. The measurement setup was calibrated using a calibration substrate. The current consumption of the amplifier using this measurement setup is 75 mA from a 3.3-V power supply, leading to a power consumption of 247.5 mW per amplifier chain. As the PA is implemented as a differential circuit, baluns at the circuit's input and output were used. The losses of these baluns were removed from the actual measurement results using the results of EM simulations of the structures used with Sonnet 18.52.

The first experiment investigates the behavior of the implemented PA chain over the targeted frequency range. Therefore, the input frequency of the amplifier was swept over the whole WR-5.1 waveguide band, from 140 to 220 GHz. Using this setup, the S-parameters S_{11}, S_{22}, S_{12}, and S_{21} were characterized using a small input power $\mathrm{P_{in}}$, ensuring small-signal behavior of the circuit. These measurements can be seen in Fig. 17 compared with the simulation results of the S-parameters of this circuit. A good match between the measured and simulated results can be seen in these plots. After this measurement, the input power was modulated for each frequency point to determine the saturated output power $\mathrm{P_{sat}}$ and power-added efficiency (PAE). The results of these measurements are depicted in Fig. 18. The output power and PAE measured over the targeted frequency range also agree with the presented simulation results.

The linear gain G, given by the S-parameter S_{21}, shows a maximum of 14.56 dB at a frequency of 192.4 GHz with a 3-dB bandwidth of 45.6 GHz. The reverse isolation of the amplifier chain is better than 40.7 dB for the whole frequency band. When comparing the measured reverse voltage gain S_{12} to the simulated one, one can see that it is considerably worse than the simulated result. However, this was to be expected as the simulation omits parasitic coupling of the measurement setup and between the individual amplifiers, degrading the reverse isolation. The input and output reflection coefficients, S_{11} and S_{22}, show a matching of min. −4 dB over most of the measured frequency range. This is due to the fact that the amplifiers were optimized for operation within the frequency-doubling chain rather than for breakout measurements. This results in nonideal matching when probed at a 100-Ω interface. Further investigations of the circuit

TABLE V
COMPARISON OF STATE-OF-THE-ART PAS AROUND 180 GHZ

Ref.	[71]	[72]	[73]	[74]	[75]	[76]	[77]	[78]	[79]	[80]	This work
Tech.	GaAs	SiGe	InP	GaN	SiGe	SiGe	FD-SOI	InGaAs	InP	CMOS	SiGe
Node (nm)	100	130	250	50	130	130	28	35	250	65	90
f_c (GHz)	135	173	173	175	180	183	184	191*	200	201	180
BW (GHz)	50	8.2	23.8	37	80	8.5	20	158*	20.5	5	45.6
P_{sat} (dBm)	10	0.9	21.43	14.1	15	-2.8	-3.7	14.9	18.5	-1.2	12.2
PAE_{max} (%)	n/a	n/a	9.5	1.2	3.5	n/a	4.2	6.6	8.5	2.1	5.4
OP_{1dB} (dBm)	8*	n/a	18.5	10	13	n/a	-8	7*	17.4	-3.3	7.84
Gain (dB)	16	18.5	23.6	12	19	9.5	7.6	28*	23.1	23.6	14.56

* extracted from published measurement plots

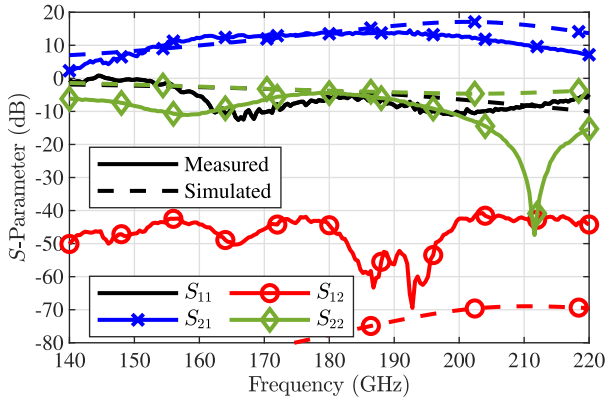

Fig. 17. Measured and simulated S-parameters of the implemented PA. Measured curves are depicted in solid lines and simulated curves are depicted in dashed lines. Simulated reverse voltage gain S_{12} for frequencies below 175 GHz is below −80 db.

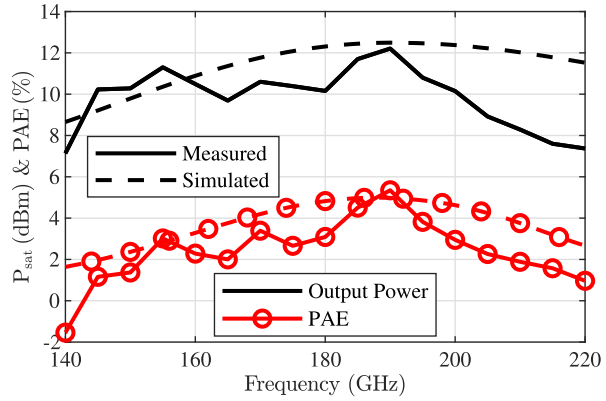

Fig. 18. Measured and simulated saturated output power and PAE of the implemented PA depicted over the operation frequency. Measured curves are depicted in solid lines and simulated curves are depicted in dashed lines.

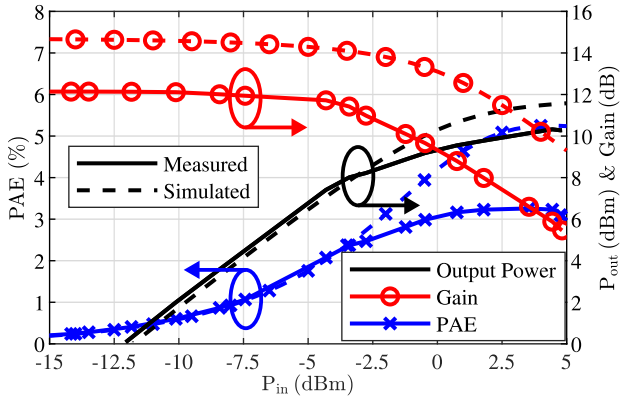

Fig. 19. Measured and simulated gain, output power, and PAE of the wideband PA chain for a input frequency of 170 GHz. Measured curves are depicted in solid lines and simulated results are depicted in dashed lines.

implemented in the 180- and 360 GHz signal source, described in Sections IV-C and IV-D, show a good performance over the targeted frequency range. The following large-signal analysis of the circuit also shows good performance over the targeted frequency band.

The saturated output power of this PA reaches 12.2 dBm at a frequency of 190 GHz and a PAE of 5.4%. This circuit can supply more than 10 dBm of power for frequencies between 145 and 200 GHz.

For the investigation of the circuits' behavior for different input powers P_{in}, the input power of the network analyzer was varied for a fixed frequency of 170 GHz while the output power P_{out} of the circuit was measured. From these data, the gain and PAE of the circuit were calculated for each operating point. The experimental results of this measurement are depicted in Fig. 19.

Here, a small-signal gain of 12.1 dB was measured with a drop-off down to 5.5 dB for input powers of 5 dBm. The maximum output power was measured with an input power of 4.4 dBm, resulting in an output power of 10.32 dBm. The peak PAE of 3.26% for this frequency was measured at an input power of 3.5 dBm, resulting in an output power of 10.14 dBm. Furthermore, an output-referred compression point OP_{1dB} of 7.84 dBm was determined. A comparison of the presented PA chain with the state of the art in amplifier design at a frequency of 180 GHz is given in Table V.

C. 180-GHz Signal Source

The output power of the 180-GHz signal source breakout MMIC was characterized using a T220 T-Wave Probe by Formfactor connected to the GSG bond pads at the output of the circuit. The waveguide probe was connected to an Erickson PM5B calorimeter-style power meter using the corresponding waveguide tapers. The output frequency of the VCO was measured at the output of the frequency divider, like in Section IV-A, to link the measured output power with the output frequency correctly.

Due to the reduced load of the frequency doubler compared with the 50-Ω interfaces of the integrated termination resistor

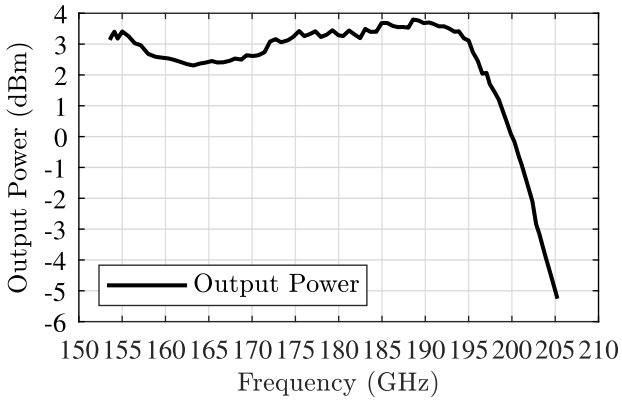

Fig. 20. Measured output power of the 180-GHz signal source. Losses of the balun used for measurement are removed from the results. From [27].

at one output port of the VCO and the powermeter, connected to the other output port, a higher bandwidth can be achieved from the VCO. The usable frequency range is extended to 51.7 GHz, with a frequency TR between 153.6 and 205.3 GHz. This results in a relative TR of 28.8% for the presented 180-GHz signal source.

The used rat-race balun, converting the differential output signal to a single-ended signal suitable for measurement using single-ended equipment such as waveguide probes, was simulated in Sonnet 18.52. The results of this simulation were used to evaluate the performance of the circuit, as the losses of the balun were subtracted from the measurement results, determining the output power of the 180-GHz signal source.

The implemented rat-race balun has a center frequency of ≈203 GHz and an input and output matching of at least −10 dB for a frequency range between 150 and 210 GHz. The amplitude and phase differences of the differential ports are between −3.5 and 0.5 dB and between −204.9° and −175.4°, respectively.

The measured output power of the 180-GHz signal source is presented in Fig. 20. For most of the achievable TR, the signal source's output power is more than 2.3 dBm, with a peak output power of 3.8 dBm. A roll-off in output power was determined for frequencies above 195 GHz. The 3-dB bandwidth of this circuit is 45.4 GHz.

The total current consumption of the 180-GHz source is 190.5 mA from a 3.3-V source, resulting in a total power consumption of 628.7 mW. With the correction of 58 mA for the frequency divider, as described in the previous measurement results of the 90-GHz signal source, the 180-GHz signal generation has a power consumption of 437.3 mW, resulting in a peak dc-to-RF efficiency of 0.55% for the 180-GHz signal source.

D. 360 GHz Signal Source

The measurement results of the developed 360 GHz signal source were obtained in two steps. The first measurement was conducted to verify the output harmonics of the developed circuit. In this investigation, the output harmonics of the signal source were measured using a Keysight N9041B signal analyzer in combination with VDI signal analyzer extension modules. Due to the 50-μm pitch of the output pads, a Formfactor T-Wave waveguide probe with a WR-2.2, also called WM-570, waveguide was used. This waveguide dimension has a lower cutoff frequency of ≈263 GHz, which prevented an investigation of the fundamental frequency generated by the 180-GHz source [88]. When measuring the output frequency of the 360 GHz signal source, at the second harmonic of the 180-GHz input signal, an output frequency between 303.4 and 410.1 GHz could be detected on the signal analyzer when modulating the tuning voltage between 1.3 and 8.7 V. No additional spurious signals could be detected while conducting this measurement.

For the determination of the output power of the developed 360 GHz signal source, the output signal was measured using an Erickson PM5B powermeter, while the output frequency of the VCO was measured through the integrated frequency divider simultaneously to ensure the measurement at the correct output frequency. The output pads of the measured circuit were de-embedded using the measurement results of a back-to-back structure of the pads. The losses of the implemented balun, used to convert the differential output signal of the signal source to a single-ended signal for measurement, were removed from the measurement results using the simulation results. Once again, the balun, implemented using the rat-race topology, was simulated in Sonnet 18.52, and the simulation results were subtracted from the measured output power. In the range from 310 to 500 GHz, the ports are still matched better than −13 dB. The best matching is achieved at the center frequency of this balun at 414 GHz. The amplitude difference and phase difference of the differential ports in this frequency range are between −2.32 and 0.1 dB and between −201.4° and −159.0°, respectively. The losses of this balun lie between 1.46 and 3.05 dB. Although the frequency range of the implemented balun does not perfectly fit the intended frequency range of the signal source, it does not deteriorate the performance of the signal source, as it is still well-matched at the operating frequencies of the source. As the source is intended to drive a differential antenna in an FMCW radar system, the balun is only used for measurement purposes and is not implemented in the developed radar transceiver. Therefore, the losses of the balun can be removed from the measurement results of the source to represent the actual performance of the developed circuits.

Fig. 21 details the simulation and corrected measurement results at the fourth harmonic, showing an output power deviation of just 1.65 dB at 370 GHz and a maximum deviation of 4.31 dB at 304 GHz.

A continuous TR of 106.7 GHz can be observed with a center frequency of 357.1 GHz, achieving a relative TR of 29.9%. The measured output power ranges between −11.25 and −1.85 dBm, with the peak value achieved at a frequency of 370.5 GHz. When evaluating the 3-dB bandwidth of this circuit, a value of 48.7 GHz was achieved.

The power consumption of the measured circuit was 915.8 mW. Here, the power consumption of the receive path, consisting of two PA chains and a subharmonic mixer, is removed from the measurement of the whole MMIC. The

TABLE VI
COMPARISON OF STATE-OF-THE-ART SIGNAL SOURCES IN SILICON TECHNOLOGIES. THE COMPARISON IS DIVIDED INTO SIGNAL SOURCES WITH OUTPUT FREQUENCIES AROUND 90, 180, AND 360 GHz

Ref.	Technology	Type	f_c (GHz)	Tuning Range (GHz)	rTR (%)	P_{dc} (mW)	P_{OUT} (dBm)	PN [$\Delta f = 1$ MHz] (dBc/Hz)
[60]	350 nm SiGe	Colpitts-Clapp VCO	81.0	68.8 – 93.3	30.0	240.0	12.0	−97.0
[81]	130 nm SiGe	Colpitts VCO	90.5	78.0 – 91.0	11.6	60.0	4.3	−112.0*
[15]	130 nm SiGe	Colpitts-Clapp VCO	91.8	74.0 – 109.5	38.6	215.0	7.0	−93.0
This work	90 nm SiGe	Colpitts-Clapp VCO	90.8	78.7 – 102.8	26.6	95.7	6.4	−78.8
[82]	130 nm SiGe	Colpitts-Clapp VCO	160.0	154.2 – 164.0	6.2	117.0	−0.9	−78.0
[83]	28 nm CMOS	Push-Push Osc.	170.0	151.2 – 188.0	21.7	95.0	−9.2	−109.3*
[84]	130 nm SiGe	Injection Locked Osc.	175.0	148.0 – 200.0	28.6	30.0	2.5	−108.0
[85]	200 nm SiGe	Push-Push Osc.	180.0	178.3 – 179.3	0.6	120.0	−12.0	−90.0
[86]	55 nm SiGe	Self-Ref. Freq. Stabilized VCO	216.0	194.0 – 238.0	20.4	103.0	10.2§	−60.0
This work	90 nm SiGe	VCO + Doubler + PA	180.0	153.6 – 205.3	28.8	437.3	3.8	−72.8
[25]	130 nm SiGe	VCO + Quadrupler	270.2	231.2 – 309.1	28.8	700.0	−2.8	−75.0
[38]	130 nm SiGe	VCO + Doubler + Doubler	292.8	273.5 – 312.0	13.2	435.0	2.3	−88.5
[41]	55 nm CMOS	VCO + 3rd Harmonic Extraction	293.0	284.0 – 301.0	5.8	19.0	−2.7	−93.0*
[32]	130 nm SiGe	Push-Push VCO	305.0	292.0 – 318.0	8.5	142.0	0.6	−108.0*
[33]	130 nm SiGe	Injection Locked Harmonic Osc.	312.5	308.0 – 317.0	2.9	1180.0	6.6	−80.1
[40]	130 nm SiGe	VCO + Quadrupler	314.1	306.9 – 321.3	4.4	372.0	−3.3	−90.3
[32]	130 nm SiGe	Push-Push VCO	316.0	305.0 – 327.0	7.0	112.0	0.2	−105.0*
[24]	120 nm SiGe	Push-Push VCO	319.5	309.0 – 330.0	6.6	63.0	−13.3	−78.0*
[29]	130 nm SiGe	Injection Locked Harmonic Osc.	321.0	319.0 – 323.0	1.2	433.0	3.0	−66.8
[37]	130 nm SiGe	Push-Push VCO	330.0	321.0 – 339.0	5.4	40.0	−7.9	−110.0*
[10]	130 nm SiGe	Push-Push VCO + Doubler	340.0	305.0 – 375.0	20.6	568.0†	0.1	−79.0
[34]	130 nm SiGe	Standing Wave Osc.	344.0	318.2 – 369.8	15.1	640.0	−6.8	−93.1*
[87]	55 nm CMOS	Voltage-Controlled Ring Osc.	366.9	338.4 – 395.4	15.5	152.0	6.2§	n/a
[37]	130 nm SiGe	VCO + Doubler	372.0	361.0 – 383.0	5.9	34.0	−6.7	−80.0
[28]	130 nm SiGe	VCO + Quadrupler	374.5	367.0 – 382.0	4.0	380.0	−11.0§	−112.5*
[36]	130 nm SiGe	VCO + Doubler	420.0	418.5 – 421.5	0.7	70.0	−3.5	n/a
[30]	130 nm SiGe	VCO + Doubler	430.5	426.0 – 437.0	2.1	165.0	−6.3	−89.3*
[27]	130 nm SiGe	VCO + Doubler + PA + Doubler	450.0	427.4 – 472.8	10.1	640.0	−12.6	−68.0
This work	90 nm SiGe	VCO + Doubler + PA + Doubler	356.8	303.4 – 410.1	29.9	915.8	−1.85	−69.4

* at 10 MHz offset frequency § EIRP † complete transceiver

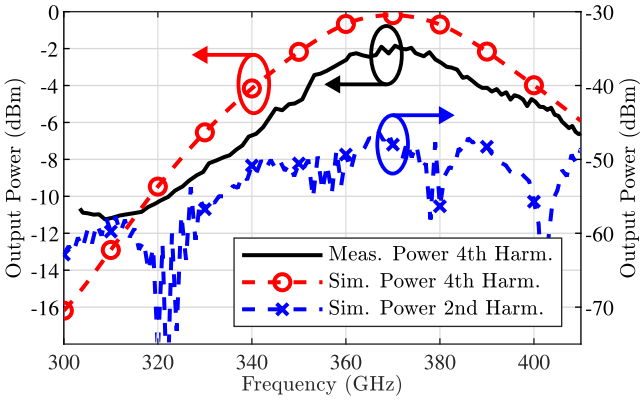

Fig. 21. Measured and simulated output power of the 360 GHz signal source at the fourth harmonic of the oscillator and the simulated power of the second harmonic at the output of the doubler. Losses of the balun used for characterization are removed from the measurement results.

power consumption of the subharmonic mixer was determined by measurement on a separate breakout chip. A peak dc-to-RF efficiency of 0.07% can be calculated for this circuit. Although this efficiency seems to be low, it is right in line with the efficiencies of the other wideband (>10% rTR) silicon-based signal sources referenced in Table VI, with the stated efficiencies ranging from 0.004% to 0.39%.

For the characterization of the phase noise of the 360 GHz signal source, the phase noise was measured at the output of the circuit. As the output frequency exceeds the input frequency range of the used Rohde & Schwarz FSWP phase noise analyzer, a VDI WR2.2 VNAX network analyzer extension module was used to downconvert the 360 GHz signal to a signal frequency the phase noise analyzer can measure. The used network analyzer extension module features an integrated ×36 frequency multiplier, which multiplies an external local oscillator signal (LO) provided by a Keysight PSG E8257D signal generator and uses the multiplied signal to downconvert the output signal of the device under test (DUT) by mixing both the signals. The phase noise of the DUTs' output signal remains unaffected in this process as long as the phase noise of the LO does not dominate the measurement. As the specified

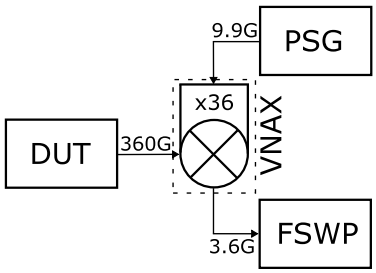

Fig. 22. Block diagram of the downconversion measurement setup to measure the phase noise at the output of the 360 GHz signal source. The mixer and frequency multiplier are integrated in a vector network frequency extender module VNAX by VDI.

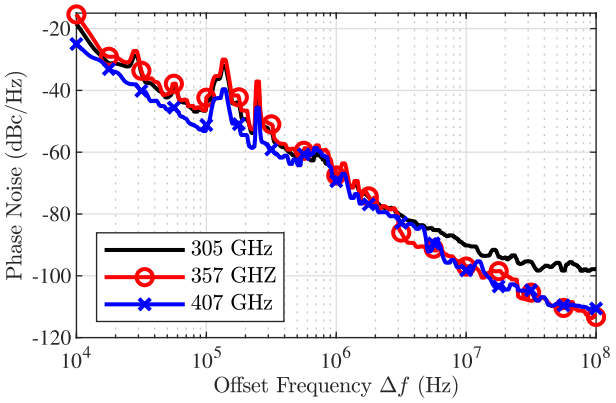

Fig. 23. Measured phase noise at the output of the 360 GHz signal source. At an offset frequency Δf of 1 MHz, the measured phase noise is between -67.5 and -69.4 dBc/Hz.

phase noise of the signal generator is around -145 dBc/Hz for an output frequency of 10 GHz and an offset frequency Δf of 1 MHz, the phase noise of around -113.8 dBc/Hz ($\Delta f = 1$ MHz) when converted to 360 GHz does not dominate the measurement. Because of this, the phase noise of the output signal of the VNAX directly represents the phase noise of the output signal of the 360 GHz signal source. A block diagram of this measurement setup is depicted in Fig. 22. The measurement results obtained with this setup are depicted in Fig. 23. In this measurement plot, three separate measurement curves of the phase noise curves are shown for offset frequencies Δf from 10 kHz to 100 MHz. These phase noise curves were taken for operation at the lowest tunable frequency, around 305 GHz, for the center frequency at 357 GHz, and for the highest achievable frequency at 407 GHz. Evaluating these three measurement curves at an offset frequency Δf of 1 MHz, a phase noise between -67.5 and -69.4 dBc/Hz can be determined, with the lowest value present at a frequency of 407 GHz. A summary of the detailed measurement results is depicted in Table VI.

V. Conclusion

This article demonstrates three fully integrated, wideband signal sources at 90, 180, and 360 GHz, manufactured in the 90 nm B12HFC SiGe BiCMOS technology with an f_T of 300 GHz and an f_{max} of >500 GHz.

The 90-GHz signal source has an rTR of 26.6% while providing up to 6.43-dBm output power.

The 180-GHz signal source, comprising a 90-GHz VCO, a frequency doubler, and a wideband PA, achieves a frequency TR of 51.7 GHz and an output power of up to 3.8 dBm. The wideband PAs in this source achieve a 3-dB bandwidth of 45.6 GHz with a peak saturated power output P_{sat} of 12.2 dBm at a frequency of 190 GHz and a peak PAE of 5.4%.

These circuits are complemented by another frequency-doubling stage, consisting of an integrated, wideband hybrid coupler for quadrature signal generation and push–push doublers to double the frequency to 360 GHz with a pseudodifferential output signal. Simulations of the wideband coupler show a good matching of the coupler and low amplitude and phase imbalance. Measurements of the complete 360 GHz signal source demonstrate a frequency TR of 106.7 GHz with an output power between -11.25 and -1.85 dBm over the whole TR, making it suitable for use in a hyper-wideband FMCW radar system.

To the best of the authors' knowledge, this is the highest frequency TR achieved for any silicon-based, fully integrated signal source published.

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David Starke (Graduate Student Member, IEEE) was born in Herne, Germany, in 1992. He received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from Ruhr University Bochum, Bochum, Germany, in 2015 and 2017, respectively.

Since 2017, he has been a Research Assistant with the Institute of Integrated Systems, Ruhr University Bochum. His current research interests include mmWave to THz radars and monolithic microwave integrated circuit (MMIC) design using silicon–germanium technologies.

Florian Vogelsang (Graduate Student Member, IEEE) was born in Hattingen, Germany, in 1993. He received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from Ruhr University Bochum, Bochum, Germany, in 2015 and 2017, respectively.

Since 2018, he has been a Research Assistant with the Institute of Integrated Systems, Ruhr University Bochum. His current research interests include wideband radar systems in the mmWave and THz range, realized as monolithic microwave integrated circuits (MMICs) in silicon–germanium technologies.

Jonathan Bott (Graduate Student Member, IEEE) was born in Lünen, Germany. He received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from TU Dortmund University, Dortmund, Germany, in 2014 and 2016, respectively.

From 2016 to 2017, he worked in the automotive industry as a Software Developer. Since 2017, he has been a Research Assistant at the Institute of Integrated Systems, Ruhr University Bochum, Bochum, Germany. His current research interests include mmWave radar system design, circuit and MMIC design using silicon–germanium, and MIMO DoA and imaging algorithms.

Jan Schöpfel (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from Ruhr University Bochum, Bochum, Germany, in 2014 and 2016, respectively.

Since 2017, he has been with the Institute for Integrated Systems, Ruhr University Bochum. His current research interests include concepts and integrated circuits for radar sensors for fully autonomous driving.

Mr. Schöpfel was a co-recipient of the EuMIC 2021 Best Student Paper Award.

Christian Bredendiek (Member, IEEE) was born in Gelsenkirchen, Germany, in 1981. He received the Dipl.Ing. and Dr.Ing. degrees in electrical engineering from Ruhr University Bochum, Bochum, Germany, in 2008 and 2014, respectively.

From 2008 to 2014, he was a Research Assistant with the Institute of Integrated Systems, Ruhr University Bochum. Since 2015, he has been with the Department of Integrated Circuits and Sensor Systems, Fraunhofer Institute for High Frequency Physics and Radar Techniques FHR, Wachtberg, Germany. His current research interests include frequency synthesis, working on system concepts and integrated circuits for various mmWave applications.

Klaus Aufinger (Member, IEEE) received the Diploma and Ph.D. degrees in physics from the University of Innsbruck, Innsbruck, Austria, in 1990 and 2001, respectively.

From 1990 to 1991, he was a Teaching Assistant with the Institute of Theoretical Physics, University of Innsbruck. In 1991, he joined the Corporate Research and Development of Siemens AG, Munich, Germany, where he investigated noise in submicrometer bipolar transistors. He is currently with Infineon Technologies AG, Neubiberg, Germany, the former Semiconductor Group of Siemens, Munich, working in the field of device physics, technology development, and modeling of advanced SiGe technologies for high-speed digital and analog circuits. He also gives lectures on analog bipolar technology at the Technical University of Munich, Munich. He has coauthered more than 200 publications in scientific journals and conferences.

Dr. Aufinger was a member of the Technical Program Committee of the IEEE International Electron Devices Meeting (IEDM). He serves as a reviewer for several journals and the *European Microwave Week* (EUMW).

Nils Pohl (Senior Member, IEEE) received the Dipl.-Ing. and Dr.Ing. degrees in electrical engineering from Ruhr University Bochum, Bochum, Germany, in 2005 and 2010, respectively.

From 2006 to 2011, he was a Research Assistant with Ruhr University Bochum, where he was involved in integrated circuits for mmWave radar applications. In 2011, he became an Assistant Professor with Ruhr University Bochum. In 2013, he became the Head of the Department of mmWave radar and high-frequency sensors with the Fraunhofer Institute for High Frequency Physics and Radar Techniques, Wachtberg, Germany. In 2016, he became a Full Professor of integrated systems with Ruhr University Bochum. He has authored or coauthored more than 200 scientific papers and has issued several patents. His current research interests include ultrawideband mmWave radar, design, and optimization of mmWave integrated SiGe circuits and system concepts with frequencies up to 300 GHz and above, and frequency synthesis and antennas.

Prof. Pohl is a member of VDE, ITG, EUMA, and URSI. He has received the Karl-Arnold Award of the North Rhine-Westphalian Academy of Sciences, Humanities and the Arts in 2013, and the IEEE MTT Outstanding Young Engineer Award in 2018. He was a co-recipient of the 2009 EEEfCom Innovation Award, the 2012 EuMIC Prize, the 2015 Best Demo Award of the IEEE Radio Wireless Week, the Best Paper Award at EUMIC 2012, the Best Demo Award at RWW 2015, and the Best Student Paper Awards at RadarConf 2020, RWW 2021, and EuMIC 2022.