Design and Phase Noise Measurements of an Ultrafast Dual-Modulus Prescaler in 130 nm SiGe:C BiCMOS

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***Abstract*— The design complexity of high-speed and power-efficient circuits increases to higher operation frequencies. Therefore, this manuscript gives an overview of how to design and optimize fully differential emitter-coupled logic (ECL) gates using two dual-modulus prescalers with switchable division ratios of 4 and 5. The first prescaler is optimized to the highest operation frequencies, up to 142 GHz and even 166 GHz for the division ratios of 5 and 4, respectively. Furthermore, another prescaler has been optimized for the widely used 80 GHz band, which has been heavily promoted by the automotive industry and has a high number of components in that domain. Both prescalers can be utilized in a fully programmable frequency divider with a wide division ratio range. As the measurement of the additive phase noise for frequency-converting devices with excellent noise performance is quite challenging, this is discussed theoretically and carried out practically. The measured jitter is between 500 as and 1.9 fs within integration limits of 100 Hz up to 1 MHz offset frequency.**

***Index Terms*— Automotive radar, dual-modulus divider, emitter-coupled logic (ECL), frequency divider, mmWave radar, phase-locked loop (PLL), SiGe heterojunction bipolar transistor (HBT).**

I. Introduction

MODERN measurement systems necessitate the generation and acquisition of signals with high precision. Specifically, millimeter-wave (mm-wave) and terahertz measurement systems are capitalizing on advancements in signal synthesis techniques. On the one hand, this fosters traditional applications such as radar [1], [2], device characterization [3], [4], and security [5], [6]. On the other hand, these advancements are paving the way for the exploration of novel emerging applications, such as biomedical sensing [7], [8], plasma diagnostics [9], [10], and material characterization [11], [12], further expanding the potential of these measurement systems.

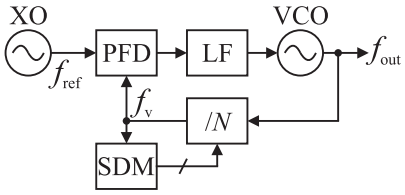

Fig. 1. Generic block diagram of a fractional-N phase-locked loop.

Frequency synthesis techniques are pivotal in scientific research, and recent advancements aim to achieve more efficient and precise operations. One notable approach is the direct synthesis of signals within the desired frequency band, reducing or even eliminating the need for frequency multipliers. This not only reduces the complexity of measurement systems, provides more flexibility, and omits subharmonic spurs, but also greatly increases the demands on the components.

Phase-locked loops (PLLs) are commonly used to generate precise and adjustable signals with modulated output frequencies. A PLL system, shown in Fig. 1, employs high-frequency broadband voltage-controlled oscillators (VCOs), utilizing various technologies such as LC tank resonators [13] or yttrium iron garnet (YIG) resonators [14].

A stable reference source, typically crystal oscillators (XOs), is essential for system stability and accuracy. The reference and output signal phases and frequencies are compared using a phase-frequency detector (PFD), while a frequency divider scales the output frequency by a factor of N to match the reference frequency. In steady state and integer-N mode, the PLL's output frequency f_{out} equals N times the reference frequency f_{ref}. For enhanced frequency resolution and modulation, a sigma-delta modulator (SDM) is applied [15], which modulates the frequency divider factor N in each output cycle. The PLL's output frequency corresponds to the mean of the alternating integer division factors multiplied by the reference frequency, with the SDM reducing noise contribution [15]. Regarding high-performance, high-frequency PLLs, the utilized frequency divider has three main requirements. First, it should be fully programmable with a wide range of division ratios. This gives maximum flexibility in the modulation of

Manuscript received 26 June 2023; revised 1 September 2023 and 26 October 2023; accepted 27 October 2023. Date of publication 14 November 2023; date of current version 10 January 2024. This work was supported in part by the German Research Foundation ("Deutsche Forschungsgemeinschaft") (DFG) under Project-ID 287022738 TRR 196 and in part by the German Federal Ministry of Education and Research (BMBF) in the course of the 6GEM Research Hub under Grant 16KISK037. This paper is an expanded version from the International Microwave Symposium, San Diego, CA, USA, June 10–16, 2023 [DOI: 10.1109/LMWT.2023.3265861]. *(Corresponding author: Lukas Polzin.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2023.3329699.

Digital Object Identifier 10.1109/TMTT.2023.3329699

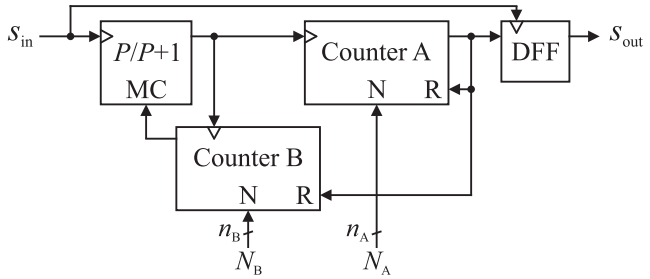

Fig. 2. Block diagram of the dual-modulus concept for fully programmable frequency dividers utilizing one $P/P+1$ prescaler, two counters, and one DFF.

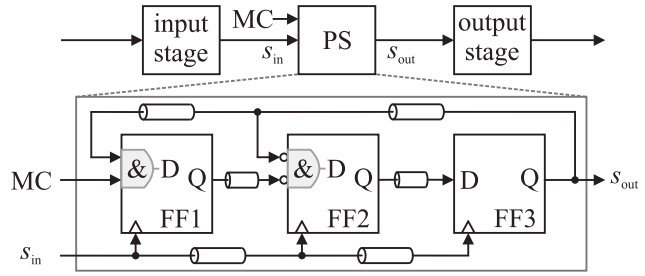

Fig. 3. Block diagram of the realized circuit with a detailed view of the 4/5 prescaler. The prescaler is realized as a Johnson ring counter with three DFFs and two merged AND-gates. Additionally, the modeled delays are depicted as transmission lines.

the output frequency. Secondly, the divider must operate with high input frequencies. Thus, there is no need for an additional prescaler with a fixed division ratio in the feedback path, which would impair the PLL's noise performance and frequency modulation [1], [16]. Omitting the fixed prescaler reduces the frequency swing at the frequency divider's output caused by the SDM, which lowers the requirements on the PFD and increases the PLL's locking range. Thirdly, the additive phase noise of the frequency divider has to be very low, as it occurs multiplied by N^2 at the output of the PLL. The loop filter (LF) can be optimized to minimize the noise of the PLL or to decrease settling time.

The dual-modulus divider concept meets the mentioned requirements for a frequency divider utilized in a high-performance synthesizer. The block diagram is depicted in Fig. 2. Utilizing one dual-modulus prescaler, which can divide by P and $P+1$, as well as two counters (Counter A and B) a fully programmable frequency divider is realized [17]. An additional data flip-flop (DFF) at the output synchronizes the output signal to the input signal in order to reduce the additive phase noise [18]. The divider is synchronously programmable and the division ratio range is as follows:

$$N = P \cdot (P-1), \ldots, 2^{n_A+n_B} + (P-1). \tag{1}$$

The prescaler divides the frequency f_{in} of the signal s_{in} by P or $P+1$ with $P \in \mathbb{N}$ depending on its modulus control input (MC). Counter B provides this MC signal, and for a $P/P+1$ prescaler, the bit width of Counter B has to be $n_B = \lceil \log_2 P \rceil$. The frequency of the output signal of Counter A is the input frequency f_{in} divided by

$$N = P \cdot N_A + N_B. \tag{2}$$

Hence, the output signal of Counter A is used as the output of the overall frequency divider. Additionally, it is used to reset both counters and synchronously load the applied division ratio N. The bit width n_A can be adapted to the required maximum division factor. Advantageously, Counter A and B both operate at the output frequency of the prescaler, which has a maximum of f_{in} divided by P. Hence, the requirements on both counters decrease significantly regarding speed and timing constraints. Due to this fact, the prescaler is the frequency-limiting component of the device and requires special optimization. Therefore, it is necessary to manufacture a stand-alone prescaler and characterize it. So, this work presents two stand-alone prescalers. The first prescaler is optimized to operate with maximum input frequencies and thus has higher power consumption. The second prescaler is optimized to operate in the emerging frequency band for automotive between 76 and 81 GHz. Both realized prescalers can toggle between the division ratios $P = 4$ and $P+1 = 5$. This reduces the requirements on the subsequent counters of the dual-modulus concept significantly but still obtains a low minimum division ratio of $N = 12$.

The dual-modulus prescalers used for the dual-modulus divider concept are usually static frequency dividers. The circuits are truly digital. Other divider techniques such as dynamic regenerative frequency dividers and injection-locked frequency dividers (ILFDs) are discussed in Section VI.

In Section II, the architecture of a 4/5 prescaler is presented. Furthermore, the circuit design and the optimization procedure are discussed. For the realized prescalers, the simulated and measured sensitivity are presented in Section III. In Section IV, the technique for high-performance additive phase noise measurements of frequency-converting devices is elaborated. Thereafter, the resulting measurements of the realized prescalers are presented and compared to simulations. In Section V, the transient behavior of the prescalers is analyzed by means of the eye pattern. Finally, Section VI provides and discusses a comparison with state-of-the-art prescalers.

II. Architecture and Circuit Design

A. Architecture

The prescaler is realized following the principle of a Johnson ring counter as depicted in Fig. 3 [19]. Utilizing three DFFs and two AND-gates, the prescaler provides an output signal s_{out} with a frequency of the input signal s_{in} divided by four or five. The MC input gives the possibility to change between the two division ratios. For a logic low signal at the MC input, flip-flop (FF) FF1 is deactivated. In this case, the FFs FF2 and FF3 operate as a feedback system with s_{in} as clock. Due to the inversion, the output signal toggles with a quarter of the input frequency. In contrast, a logic high MC activates FF1, which delays the toggling of FF2 by one input cycle period. Hence, the division factor is 5. Furthermore, Fig. 3 shows the transmission lines modeling the delay due to the physical dimensions of the prescaler. This will be discussed in Section II-G in more detail.

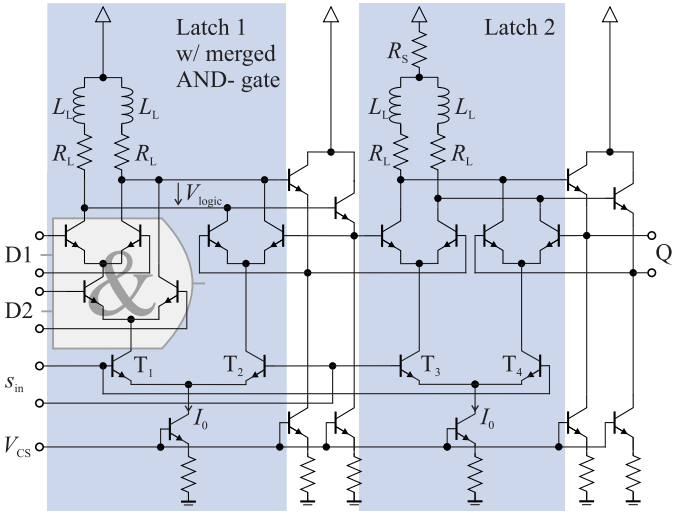

Fig. 4. Schematic of a DFF with merged AND-gate in ECL with inductive shunt peaking.

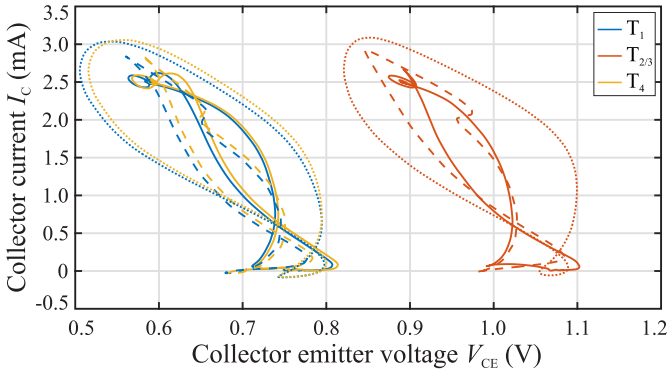

Fig. 5. Collector current I_C as a function of the collector–emitter voltage V_{CE} for input frequencies of 10 GHz (solid), 50 GHz (dashed), and 100 GHz (dotted). The transistors are denominated according to Fig. 4.

B. Circuit Design

The circuit is realized in a fully differential emitter-coupled logic (ECL), as it is the fastest approach for digital components [20], [21]. In Fig. 4, an exemplary schematic of a realized DFF with merged AND-gate is depicted. The differential transistor pairs operate as current switches, guiding the constant core current I_0 through one of the differential loads on top of the circuit. This results in a logic voltage drop V_{logic}, which is the input signal for the next stage. To speed up the toggling of the differential transistor pairs, emitter followers provide the current to rapidly charge the following stages. Moreover, the merged AND-gate is depicted and highlighted in Fig. 4. This offers at least three enhancements. Firstly, the additional gate delays due to the AND-gate is minimized, which increases the maximum operation frequency significantly. Secondly, the layout becomes more compact, which reduces the physical distance between the gates. This becomes crucial toward higher frequencies and will also increase the maximum operation frequency of the prescaler. Thirdly, the total power consumption of the prescaler is reduced, as the merged AND-gates do not require an additional current source. Nevertheless, it should not be neglected that the effort in circuit design increases with the merging of the logic gates into the FFs. It is crucial that the collector–emitter voltage of the transistors is always sufficient to ensure proper operation. Otherwise, saturation of the transistors is limiting the performance of the circuit.

The common-mode voltage of the output acts as bias voltage at the bases of the following transistors to ensure proper operation. To adjust the bias voltage and ensure sufficient collector–emitter voltage V_{CE}, a common-mode resistor R_S in series to the differential load provides a constant voltage drop. This is especially required for merging AND-gates into FFs. As the current I_0 through the resistor R_S is approximately constant, the dynamic behavior of the circuit is barely affected.

Transient simulations are crucial to ensure sufficient collector–emitter voltage V_{CE} in operation. Hence, collector currents I_C as a function of V_{CE} for different input frequencies and transistors are shown in Fig. 5. The dynamic load lines are simulated for three transistors labeled in Fig. 4 which operate at the highest frequencies. T_2 and T_3 show the highest V_{CE}. The merged AND-gate reduces V_{CE} of T_1 considerably. The necessary series resistor R_s reduces V_{CE} of T_4. However, all always remain above 0.5 V.The loops that the line shows are due to overshoots of the rectangular waveforms.

With this topology, three parameters remain for optimization. Firstly, the core current I_0 is determined by the used technology. Secondly, with a given current, the load provides the logic voltage swing V_{logic} and thus must be optimized. Additionally, in series to the load resistor R_L an inductance for inductive shunt peaking is utilized and has to be optimized as a last parameter.

C. Technology

The divider is manufactured by IHP-Leibniz Institute for High Performance Microelectronics in their 130 nm BiCMOS:C technology SG13G3 [22]. It provides heterojunction bipolar transistors (HBTs) with a maximum transit frequency $f_T = 470$ GHz and a maximum oscillation frequency $f_{max} = 650$ GHz. The emitter window size of the minimum transistor is $0.11 \times 1\ \mu m^2$. To scale the emitter sizes, multiple emitters can be parallelized. For the realized logic gates in ECL, the transit frequency f_T matters more than the maximum oscillation frequency f_{max}. Thus, the current has to be optimized to achieve minimum gate delay. The core current I_0 is provided by a current mirror, which is not shown in the schematic in Fig. 4 for the sake of clarity. A tuning voltage allows an external manipulation of the current mirror and by that a defined change of V_{CS}. Hence, the current I_0 can be adjusted slightly even after manufacturing the circuit. The optimum current for the minimum transistor is 2.5 mA regarding the collector–emitter voltage between 0.4 and 0.8 V [22]. This results in a current density of $j_c \approx 22.7\ \text{mA}/\mu\text{m}^2$. The minimum transistor size is utilized to minimize the design and maximize the power efficiency.

Additionally, a design with less power consumption was designed. Here, the core current I_0 was set to 1.35 mA, which corresponds to a current density of $j_c = 12.3\ \text{mA}/\mu\text{m}^2$. Since no smaller emitter size was available, the current density is below the optimum, resulting in a transit frequency of about 340 GHz.

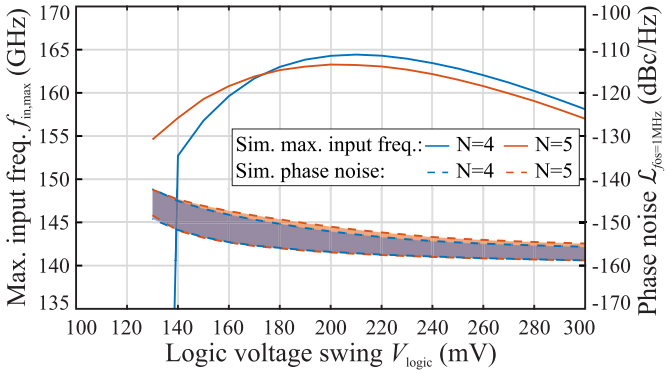

Fig. 6. Simulated maximum input frequency for a constant input power and the noise floor level of the additive phase noise as a function of the logic voltage swing.

For the schematic simulations in Cadence Virtuoso a Vertical Bipolar Intercompany (VBIC) model for the HBTs is provided [23].

D. Logic Voltage Swing

The logic voltage swing V_{logic} of the ECL gates has to be optimized regarding the speed and phase noise of the prescaler. As shown in Fig. 4, the core current and the load determine the voltage swing. With the current already specified by the technology as aforementioned, the load resistance is the remaining parameter to optimize.

The simulations are performed without inductive shunt peaking, as for every load a different individual inductor has to be designed, simulated, and optimized. This would impact the validity of the simulations. Fig. 6 shows the simulated maximum input frequency for an input power of 0 dBm as well as the additive phase noise at an offset frequency to the carrier of 1 MHz. Both results are simulated with the prescaler optimized for the highest operation speed and for both division ratios 4 and 5.

The highest maximum operating frequency is achieved at a logic voltage swing of around 200 mV. For lower voltage swings, the maximum operating frequency decreases rapidly, as the differential transistor pairs are not operating as current switches. Instead, the current is divided between the two differential loads, which further reduces the voltage swing for the next stage. Toward high logic voltage swings, the maximum operation frequency decreases as well, but only slightly. Since the load resistance R_L increases with increasing logic voltage swing, the current I_0 remains constant, the time constant to charge the parasitic capacitances increases.

In Fig. 6, the red-colored area represents the simulated additive phase noise at an offset frequency to the carrier of 1 MHz for input frequencies in the range of 20 to 100 GHz. This corresponds to the noise floor of the spectral density of the additive phase noise. All phase noise results are referred to the output frequency of the divider. The additive phase noise is higher for small logic voltage swings V_{logic} but gets better toward higher ones. Simulations with a division ratio of 5 show a lower additive phase noise because the noise is referred to the output and the jitter is approximately equal for both division ratios.

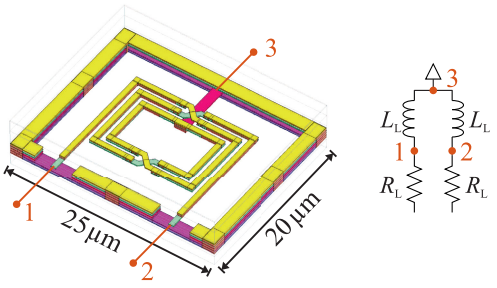

Fig. 7. Layout of the used spiral inductance with center-tap (left) and the corresponding schematic (right) with highlighted pins.

Hence, a trade-off between maximum operation frequency and low phase noise is required. In this design, V_{logic} is set to 200 mV. Decreasing it would degrade the phase noise performance unacceptably and decrease the guard interval to the rapid decay toward low voltage swings. In case V_{logic} is shifted due to inaccurate simulation models or tolerances in production, sufficient functionality is still guaranteed. For higher V_{logic}, the improvement of the phase noise performance is marginal, but the decrease in speed is significant.

It is important to note that these results are generally valid in qualitative respects. However, the quantitative values have to be evaluated for each technology and logic individually.

E. Inductive Shunt Peaking

Due to parasitic capacitances, the effective load of the circuit decreases toward higher frequencies. Thereby, the logic voltage level V_{logic} also decreases and the circuit is not operating at its optimum anymore up to the point of complete dysfunctionality. To compensate for this effect, an inductance is added in series to the load resistor. Designed properly, it improves the frequency response of the effective load impedance, including the transistors' input and output impedance and parasitics of connections and resistors. This ensures adequate signal levels of the prescaler's gates even for higher frequencies without increasing the current and power consumption of the circuit. As shown in [24] and [25], the necessary inductance can be estimated. However, this is only valid for small signals. In contrast, if the transistors are operated as current switches and the influence of the base-transit time gets considerable, transient simulations are crucial. Additionally, the self-resonant frequency must be reasonably higher than the desired operation frequencies. Schematic simulations can be performed either with the scattering parameters or with an electrical equivalent circuit, both obtained from EM simulations of the realized inductance. We used a broadband electrical equivalent circuit based on lumped elements [26], as it properly considers harmonics and offers better convergence in transient simulations.

The inductance is realized as a differential spiral inductor with a center tap, as shown in Fig. 7. Besides the advantage of low susceptibility to manufacturing tolerances, the spiral inductor also occupies less area than other realizations. However, in other cases, it can be useful to realize the inductance as adjustable transmission lines [27].

The differential inductance L_{diff} and quality factor Q_{diff} obtained by 2.5-D EM simulations with Sonnet are depicted in

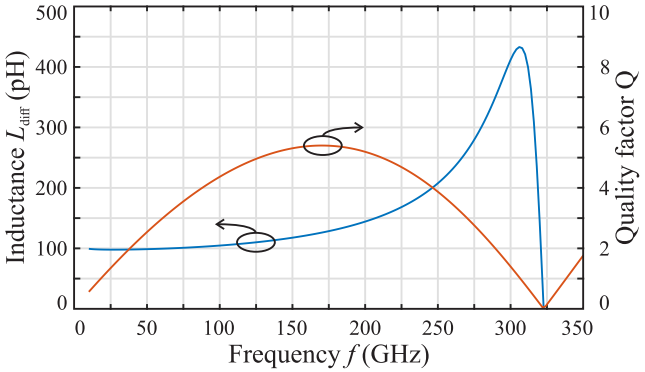

Fig. 8. Differential inductance and quality factor of the differential spiral inductor with center tap obtained by 2.5-D EM simulations.

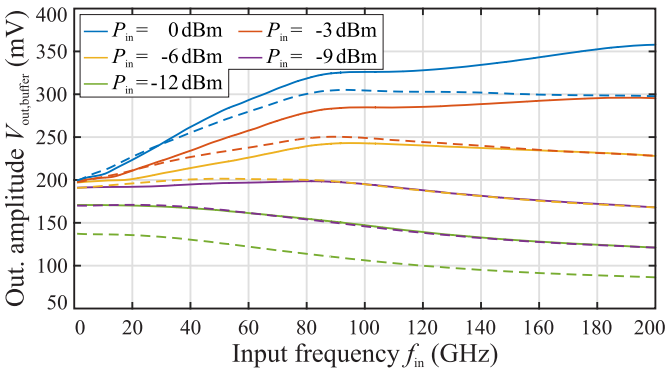

Fig. 10. Simulated output voltage swing of the input buffer for different input powers with differential (solid) and single-ended (dashed) excitation.

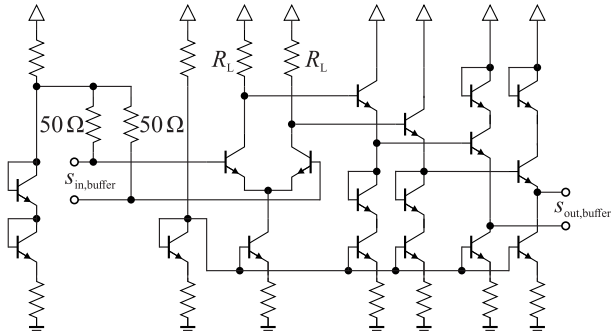

Fig. 9. Schematic of the broadband input stage.

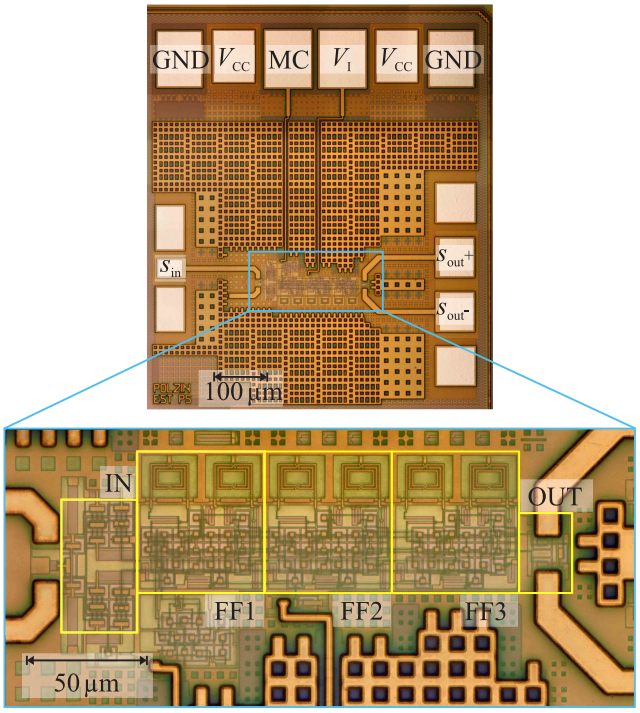

Fig. 11. Micrograph of the speed optimized realized dual-modulus prescaler MMIC (top). In the magnification (bottom), the input buffer (IN), the output buffer (OUT), and the three FFs are highlighted. The spiral inductors are clearly recognizable.

Fig. 8. An inductance of around $L_{diff} = 110$ pH is simulated to be the optimum for the realized gates and resulting prescaler. The self-resonant frequency of the realized inductor is around 325 GHz. This is more than twice the simulated maximum operation frequency. As high self-resonant frequency and small size of the inductor are required, the windings of the inductor are realized in the thin metal layers with a small feature size. Hence, the quality factor is less than 6. Nevertheless, a low quality factor is not disadvantageous, as the load resistor in series can be easily adapted to maintain the desired effective load resistance.

F. Input Stage

An input stage is required to provide the voltage swing and bias voltage for the prescaler's FFs as can be seen in Fig. 3. According to Section II-D, the optimal logical voltage swing is 200 mV to optimize the speed and noise performance of the divider. Other requirements for the input stage include extreme broadband capability and the ability to use both single-ended and differential excitation. Hence, a relatively simple circuit design was selected as shown in Fig. 9. The main part of the circuit is a differential amplifier with a core current of 7.5 mA and two subsequent emitter followers. The emitter sizes are chosen according to the maximum transit frequency. The current sources are realized by current mirrors. Differential input matching is realized by two 50 Ω resistors. The bias voltage for the differential amplifier is provided at the symmetry point of the differential input signal. In contrast to the use within the system, no differential input signal is available for the measurement. Furthermore, for the highest frequencies, it was necessary to measure with single-ended waveguide probes. The used input stage still operates adequately with single-ended excitation, even if the efficiency is reduced. This is shown in Fig. 10. Therefore, only one input pad can be seen on the micrograph in Fig. 11. As expected, in order to achieve comparable behavior, the input power for single-ended excitation is about 3 dB higher than for differential excitation. Fortunately, this has no influence on the frequency behavior and the measured sensitivity of the prescaler. Only an offset in the minimum required input power would be observed. Depending on the application, it makes sense to adapt the input stage to the required operating frequency and input level to provide a constant output swing of 200 mV. For characterizing the divider, this would be disadvantageous, though.

G. Realization

A micrograph of the realized monolithic microwave integrated circuit (MMIC) is depicted in Fig. 11. While the top shows the entire MMIC including pads, the bottom shows a magnification of the prescaler itself. The prescaler optimized to operate up to the highest input frequencies has a power consumption of 144 mW using a 3.3 V voltage supply. Each FF consumes around 48 mW. In contrast, the second prescaler optimized for an operation frequency range of around 80 GHz requires 71 mW. This results in a power consumption of around 24 mW per single FF. As the difference between the two realizations is the current density, only the resistances in the circuit have to be adapted. Thus, the circuit can be adapted to the needed operation frequencies without major effort and does not require a complete redesign and optimization.

The MC pad allows for switching between the two division ratios 4 and 5. To tune the core current I_0 of the FFs [28], a tuning voltage can be provided on the V_I pad as explained in Section II-B. The signal input pads are in a single-ended GSG configuration for proper on-chip probing. The subsequent input stage ensures a proper input voltage swing and provides the bias voltage for the prescaler. This input stage has a power consumption of 135 mW. To drive a load and ensure an adequate voltage swing at the output, a differential output stage is utilized, which consumes a power of around 43 mW. If the prescaler is utilized in an integrated system, both the input and output stages can be adapted and realized with less power consumption.

In the magnification of the prescaler in Fig. 11, the input and output stages are highlighted. Additionally, the three FFs with two spiral inductors each are highlighted. The occupied area of the prescaler is around 200 × 50 μm^2. Each FF has a dimension of around 50 × 35 μm^2. This results in additional delays of the various signals between the FFs due to the physical length of the interconnections. Even if they are only a few micrometers in the range of 10 to 80 μm long, they impair the performance of the prescaler at higher frequencies. These delays are represented by transmission lines, as depicted in Fig. 3.

III. Sensitivity

A common way to characterize frequency dividers is their sensitivity. This shows the minimum required power of a sinusoidal input signal as a function of its frequency at which the divider operates correctly. It has a characteristic minimum at the self-resonant frequency of the frequency divider, as it is a feedback system.

A. Measurement Setup

To cover the entire range of operation frequencies, two frequency synthesizers are used to measure the sensitivity. For input frequencies from 10 to 125 GHz, a Keysight N5291 Network Analyzer System PNA-X with an extended frequency range operates as a frequency synthesizer. It is connected via a FormFactor Infinity Probe with a 1 mm coaxial connector to the MMIC. For input frequencies from 110 to 170 GHz, the PNA-X in combination with the vector network analyzer (VNA) millimeter-wave converter Virginia Diodes (VDIs) WR6.5-VNAX provides the input signal. The MMIC was connected via a corresponding FormFactor Infinity Waveguide Probe. In both cases, the spectrum of the output signal with divided frequency was measured by means of an R&S FSWP. The output was connected via a differential GGB Industries INC. Picoprobe MODEL 67A. The complementary output was terminated with a 50-Ω match.

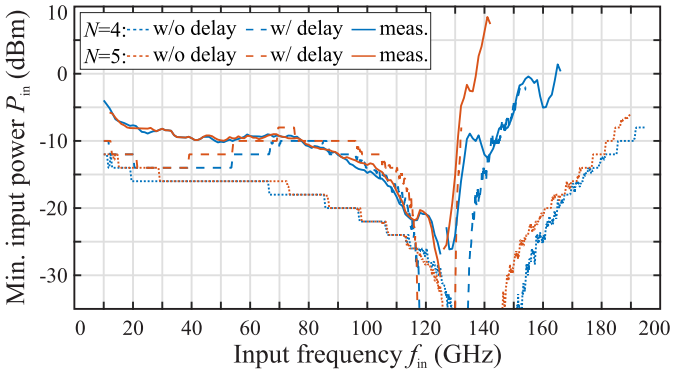

Fig. 12. Sensitivity of the prescaler optimized for highest operation frequencies, simulated with (dotted) and without (dashed) transmission lines as well as measured (solid).

B. Results

The simulated and measured sensitivity of the high-speed prescaler is depicted in Fig. 12 [28]. The current density of this prescaler was optimized to achieve maximum operation frequency. Simulations without the transmission lines exhibit a self-resonant frequency of around 140 GHz. In this case, the maximum input frequencies are 194 and 190 GHz for the division ratios 4 and 5, respectively. The impact of the delay becomes evident in the simulation results including the additional delay. Therefore, the self-resonant frequency is shifted down by 15 GHz, and the achieved maximum input frequency decreases to 132 and 154 GHz for the division ratios 4 and 5, respectively. In contrast to the simulations without delay lines, the achieved maximum input frequencies of both division ratios differ by 22 GHz. This is caused by the additional delay of FF FF1. The measured sensitivity is in good agreement with the simulated sensitivity including the additional delay. However, with high input powers, the measurements achieve higher maximum input frequencies compared to the simulations. The measured maximum input frequency is as high as 142 and 166 GHz for the division ratios 4 and 5, respectively. The reasons for the slight deviation between measurements and simulations are due to the VBIC model of the HBTs used in the simulations. The simulations' accuracy is limited in high current region with transistors switching on and off [23].

The second prescaler is optimized to operate at a frequency range of around 80 GHz and thus has a lower power consumption. The corresponding simulated and measured sensitivities are depicted in Fig. 13. Concerning the simulations without additional delay, this prescaler exhibits a self-resonant frequency around 90 GHz and achieves a maximum input frequency of 140 and 143 GHz for the division

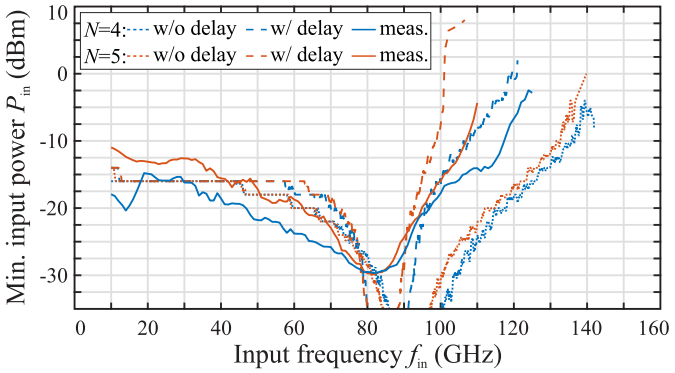

Fig. 13. Sensitivity of the prescaler optimized to operate for frequencies around 80 GHz, simulated with (dotted) and without (dashed) transmission lines as well as measured (solid).

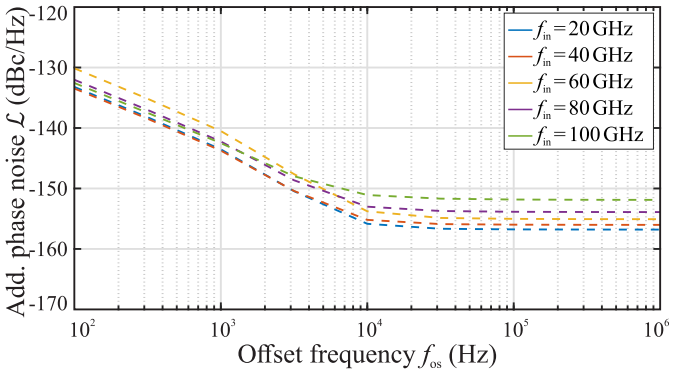

Fig. 14. Simulated spectral additive phase noise density of the speed-optimized prescaler for input frequencies from 20 to 100 GHz.

ratios 4 and 5, respectively. As previously observed, the self-resonant frequency decreases by 10 GHz if the delays are added to the simulation. Also, the maximum achieved maximum input frequency decreases to 107 and 121 GHz for division ratios 5 and 4, respectively. Again, the measurements are in good agreement with the simulations. In this case, the measured maximum input frequencies are 110 and 125 GHz for division ratios 4 and 5, respectively. For the emerging frequency band from 76 to 81 GHz, which is pushed by automotive radar, the required input power of a sinusoidal signal is even below −27.7 dBm.

IV. Noise Performance

A. Simulated Additive Phase Noise

The additive phase noise determines the noise that is added by a device and is typically referred to the output. The simulations of the additive phase noise are performed with Cadence Virtuoso applying the periodic steady-state (PSS) analysis. In Fig. 14, the simulated noise spectral density of the additive phase noise is depicted for input frequencies from 20 to 100 GHz as a function of the offset frequency to the carrier. It is simulated for offset frequencies f_{os} from 100 Hz to 1 MHz, which are reasonable frequencies concerning common PLL design. The simulations are performed for the prescaler optimized for highest operation frequencies. As expected, the additive phase noise increases slightly toward higher frequencies from a noise floor of −157 to −152 dBc/Hz. The flicker noise corner frequency f_c is around 10 kHz, which meets the expectations for HBTs.

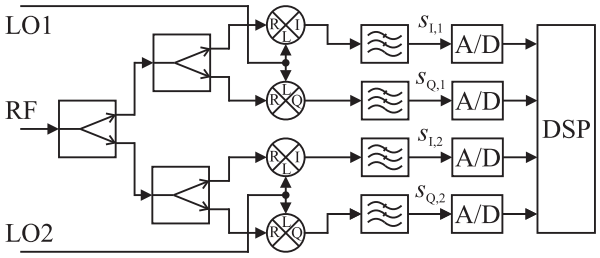

Fig. 15. Block diagram of the I/Q measurement path of the R&S FSWP. The analyzed signal (RF) is down-converted by two uncorrelated LOs and analyzed in DSP.

B. Measurement Principle

The basic principle to measure additive phase noise is applying a sinusoidal signal to the device under test (DUT) and measuring the phase noise of the output signal. By canceling the noise contribution of the input signal source and the ones of the measurement system itself, the remaining noise must be the additive phase noise. In principle, the subsequently presented methods can be realized with dedicated components. Therefore, the methods are discussed in a generic and detailed way. However, to minimize calibration and hardware demands, we utilized the phase noise analyzer system R&S FSWP to exemplify and perform the measurements. The R&S FSWP uses two independent local oscillators (LOs), which are loosely coupled to ensure the same frequency and phase but uncorrelated noise contribution for offset frequencies above 0.1 Hz. The signal under test is split and down-converted to an intermediate frequency (IF) with the help of two in-phase and quadrature (I/Q) mixers. The IF signal is digitized, which allows a direct and flexible analysis of the signals. As the noise contributions of the two LO signals are uncorrelated, they are canceled out by cross correlation in the digital signal processing (DSP). In Fig. 15, a simplified block diagram of the I/Q measurement path is depicted. More details on the measurement principle of the R&S FSWP are given in [29].

To measure the additive phase noise of frequency-converting devices, the measurement setup for the FSWP is more complex. As the analyzed frequency and the LO frequency must be the same, multiple frequency converters are needed. Moreover, this is required to cancel the phase noise of the input signal as discussed in the subsequent sections. In this case, two different measurement methods exist, the two-converter method and the three-converter method [30].

C. Three-Converter Method

For the three-converter method, three DUTs are required. Both an external signal source and the FSWP's signal source can be used to generate the input signals of the DUTs. Using power dividers, this reference signal is the input signal for all three DUTs. While the output signals of two DUTs are used as the two different LOs, the output signal of the third DUT is the signal under test. A block diagram of the measurement

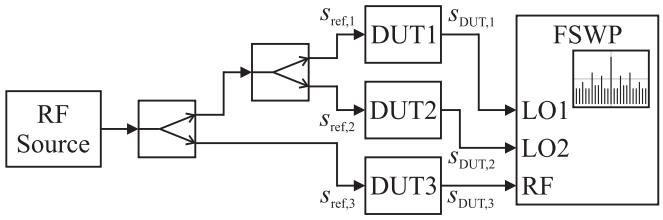

Fig. 16. Block diagram of the three-converter method to measure the additive phase noise of frequency-converting DUTs with the R&S FSWP.

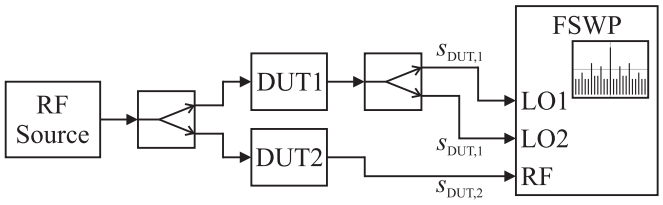

Fig. 17. Block diagram of the two-converter method to measure the additive phase noise of frequency-converting DUTs with the R&S FSWP.

setup is shown in Fig. 16. Each input signal $s_{\mathrm{ref},i}$ for the three DUTs is given as follows:

$$s_{\mathrm{ref},i} = A_{\mathrm{ref},i} \cdot \sin(\omega_{\mathrm{ref}} \cdot t + \phi_{\mathrm{ref},i} + \phi_{\mathrm{ref},n}(t)). \tag{3}$$

$A_{\mathrm{ref},i}$ is the amplitude, $\phi_{\mathrm{ref},i}$ is a constant phase shift due to the signal power divider, and $\phi_{\mathrm{ref},n}$ is the phase noise of the reference source. As the frequency dividers divide the signals $s_{\mathrm{ref},i}$ by the division ratio N, their outputs $s_{\mathrm{DUT},i}$ are as follows:

$$s_{\mathrm{DUT},i} = A_{\mathrm{DUT},i} \cdot \sin\left(\frac{\omega_{\mathrm{ref}} \cdot t}{N} + \frac{\phi_{\mathrm{ref},i}}{N} + \frac{\phi_{\mathrm{ref},n}(t)}{N} + \phi_{\mathrm{DUT},i,n}(t)\right). \tag{4}$$

Here, it is crucial to note that the additive phase noise contributions $\phi_{\mathrm{DUT},i,n}(t)$ of the three DUTs are uncorrelated. Additionally, the amplitude changes to $A_{\mathrm{DUT},i}$, as it is determined by the DUT. These three signals $s_{\mathrm{DUT},i}$ are used as input signals for the FSWP as shown in Fig. 15. The signals $s_{\mathrm{DUT},1/2}$ serve as the LO signals LO1 and LO2, respectively. In contrast, $s_{\mathrm{DUT},3}$ is the signal under test. According to Fig. 15, the signal under test is I/Q down-converted using the two LO signals. By low-pass filtering the signals, only the baseband signal component remains in $s_{\mathrm{I},1/2}$ and $s_{\mathrm{Q},1/2}$. For the in-phase path, the resulting digitized signals are as follows:

$$s_{\mathrm{I},1/2} = \frac{A_{\mathrm{DUT},1/2} \cdot A_{\mathrm{DUT},3}}{2} \cdot \cos\left(\frac{\phi_{\mathrm{ref},1/2} - \phi_{\mathrm{ref},3}}{N} + \phi_{\mathrm{DUT},1/2,n}(t) - \phi_{\mathrm{DUT},3,n}(t)\right). \tag{5}$$

Due to the 90° phase shift, the resulting digitized signals of the quadrature path are as follows:

$$s_{\mathrm{Q},1/2} = \frac{A_{\mathrm{DUT},1/2} \cdot A_{\mathrm{DUT},3}}{2} \cdot \sin\left(\frac{\phi_{\mathrm{ref},1/2} - \phi_{\mathrm{ref},3}}{N} + \phi_{\mathrm{DUT},1/2,n}(t) - \phi_{\mathrm{DUT},3,n}(t)\right). \tag{6}$$

In the DSP, the phases of the signals are calculated by

$$\phi(t) = \arctan\left(\frac{s_{\mathrm{Q},1/2}}{s_{\mathrm{I},1/2}}\right). \tag{7}$$

Hence, the two resulting phases are as follows:

$$\phi_1 = \frac{\phi_{\mathrm{ref},1} - \phi_{\mathrm{ref},3}}{N} + \phi_{\mathrm{DUT},1,n}(t) - \phi_{\mathrm{DUT},3,n}(t) \tag{8}$$

$$\phi_2 = \frac{\phi_{\mathrm{ref},2} - \phi_{\mathrm{ref},3}}{N} + \phi_{\mathrm{DUT},2,n}(t) - \phi_{\mathrm{DUT},3,n}(t). \tag{9}$$

As the constant phase terms only contribute to the dc value, they have no influence on the additive phase noise and can be ignored. The same holds true for other constant phase shifts that are introduced by the measurement setup, for example, cables. They are not included in the equations above for clarity, as the calculation is alike. Both phases (8) and (9) exhibit two noise contributions: On the one hand $\phi_{\mathrm{DUT},1/2,n}(t)$, which are uncorrelated, and on the other hand $\phi_{\mathrm{DUT},3,n}(t)$, which is the same in both equations and thus perfectly correlated. Hence, by cross-correlating the two phases ϕ_1 and ϕ_2, the additive phase noise $\phi_{\mathrm{DUT},3,n}(t)$ can be extracted. Moreover, noise added by the FSWP itself is canceled by this cross correlation, as the noise of the two internal analysis paths is uncorrelated.

D. Two-Converter Method

Another method to measure the additive phase noise of frequency-converting signals with the R&S FSWP is the two-converter method as shown in Fig. 17. The main advantage is the less complex setup. Only two DUTs and one high-frequency power divider are needed. However, both LOs are provided by the same DUT, so the calculated phases are identical as follows:

$$\phi_{1/2}(t) = \frac{\phi_{\mathrm{ref},1} - \phi_{\mathrm{ref},2}}{N} + \phi_{\mathrm{DUT},1,n}(t) + \phi_{\mathrm{DUT},2,n}(t). \tag{10}$$

Hence, cross correlation cannot extract the phase noise of one DUT but is still essential to cancel the noise added by the FSWP itself as aforementioned. So, the result is the accumulated noise of both DUTs. If both DUTs exhibit the same spectral density of the phase noise, simply 3 dB need to be subtracted from the measurement result. If the spectral density of the phase noise of both DUTs differs, the DUT with higher phase noise will dominate the measured additive phase noise. Since all fabricated components have a slightly different noise performance, it can never be assumed with certainty which of the two cases applies. Hence, the measurement exhibits a 3 dB uncertainty. This can be counteracted by measuring all permutations of three DUTs. Then a linear system of equations has to be solved, but the measurement effort also increases significantly.

E. Measurement Setup

The measurements in this work are performed with the R&S FSWP and the three-converter method. A photograph of the measurement setup is shown in Fig. 18. The three required prescalers are mounted on a printed circuit board (PCB) using an RO4350B substrate. The inputs of the three

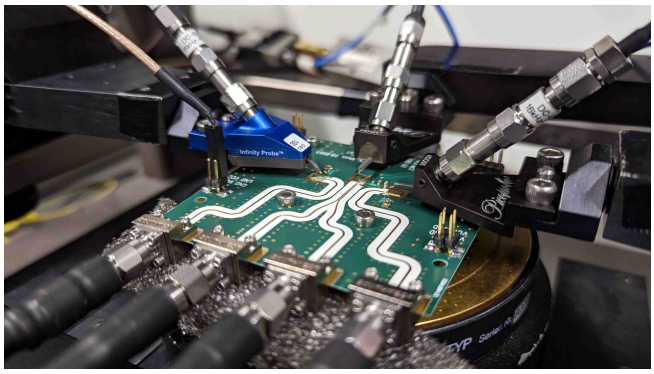

Fig. 18. Photograph of the measurement setup to measure the additive phase noise of the prescaler with help of the three-converter method.

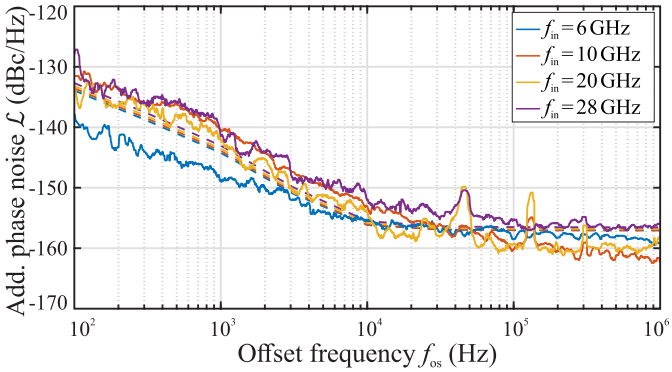

Fig. 19. Measured (solid) and simulated (dashed) noise spectral density of the additive phase noise of the speed-optimized prescaler for input frequencies from 6 to 28 GHz.

prescalers are each contacted via an individual probe, two using a GGB Industries INC. Picoprobe MODEL 67A and one using a Cascade Infinity Probe-Coaxial GSG 100. The outputs are all wire-bonded to the PCB and connected via 2.92 mm coaxial cables to the FSWP. One output can be accessed differentially to measure the transient signal. The supply voltage and the MC signal are also bonded to the PCB. Two HP 87304C power dividers are used to provide the three input signals. The input signal was generated by a Keysight PSG Signal Generator. Because the frequency response of the power dividers limits the maximum input frequency up to 28 GHz, the measurements are also bound to these limits. As both the high-speed prescaler and the one optimized for 80 GHz are realized on the same MMIC, only the high-speed prescaler was bondable. Thus, all noise measurements are realized utilizing this prescaler.

F. Measurement Results

Fig. 19 shows the measured noise spectral density of the additive phase noise for input frequencies from 6 to 28 GHz referred to the output frequency. While the noise floor is between −162 and −157 dBc/Hz, the flicker noise corner is just around 13 kHz. Integrating from an offset frequency of 100 Hz to 1 MHz results in a jitter between 0.5 fs and 1.9 fs depending on the input frequency. The integration limits refer to common PLL designs and measurement systems. On the one hand, the LF and the resulting PLL's loop bandwidth

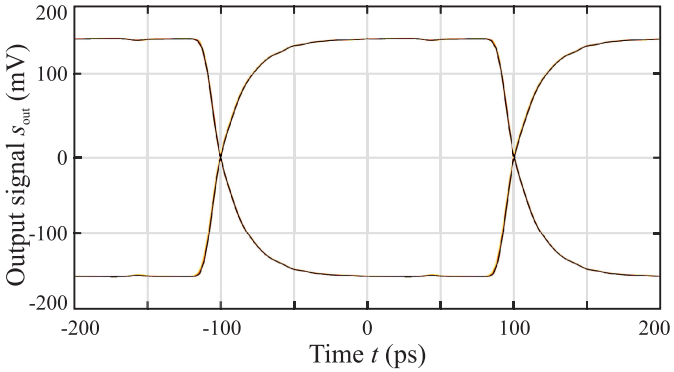

Fig. 20. Simulated eye pattern of the speed-optimized prescaler at an input frequency of 10 GHz and a division ratio of 4, with a simulated input impedance matching the specifications of the oscilloscope.

determine the reasonable upper integration limit. For offset frequencies higher than the PLL's loop bandwidth, the contribution of the divider's phase noise to the PLL's output is reduced by the low-pass characteristics of the PLL's closed-loop transfer function. On the other hand, the measurement time of a prospective measurement system determines the reasonable lower integration limit. For comparison, the corresponding simulated noise spectral densities of the additive phase noise are depicted in Fig. 19 as well. All in all, the simulations and measurements are in good agreement. However, the measured flicker noise for an input frequency of 6 GHz is slightly better than the simulated one.

V. Transient Behavior

The output stage of the divider offers a common mode logic output with an output current of 5 mA and an on-chip resistive load of 100 Ω. To make simulations and measurements comparable, the input stage of the oscilloscope was considered in the simulations. The 50 Ω input impedance in parallel to the 100 Ω on-chip resistor results in a signal amplitude of 160 mV. The 30 GHz bandwidth of the oscilloscope as well as the parasitic inductances and capacitance of the bond wires and connections reduces the output bandwidth additionally. The simulated transient output signal is shown in Fig. 20 as an eye pattern for an input frequency of 10 GHz and a division ratio of 4. It shows almost no jitter, as the only noise source in the simulations is the very low additive phase noise of the prescaler. The signal source and oscilloscope are modeled ideally without noise.

The output signal was measured fully differentially by means of a Teledyne LeCroy SDA 830ZI-B Oscilloscope offering 30 GHz bandwidth and 80 GS/s sample rate. For the input signal, again a Keysight PSG Signal Generator was utilized and connected to the MMIC via a GGB Industries INC. Picoprobe MODEL 67A. The measured transient behavior in Fig. 21 and the simulated behavior in Fig. 20 of the prescaler are in pretty good agreement. However, the measurement in Fig. 21 exhibits a visible jitter, which is dominated by the synthesizer and the oscilloscope. Additionally, the relatively low sampling rate in contrast to the high signal frequency results in uncertainties in the reconstruction of the signal. As the measured additive phase noise of the prescaler results

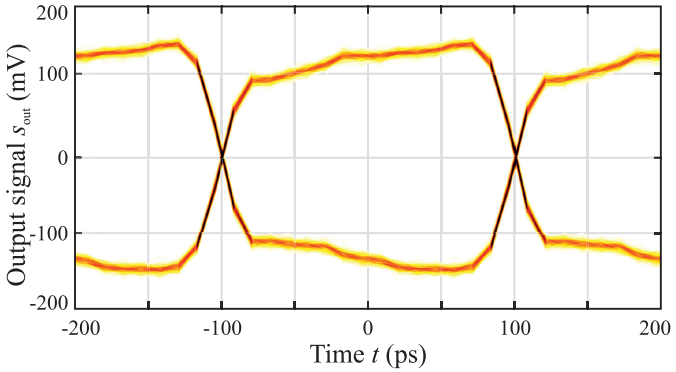

Fig. 21. Eye pattern of the speed-optimized prescaler's output signal measured with 80 GS/s and 30 GHz bandwidth at an input frequency of 10 GHz and a division ratio of 4.

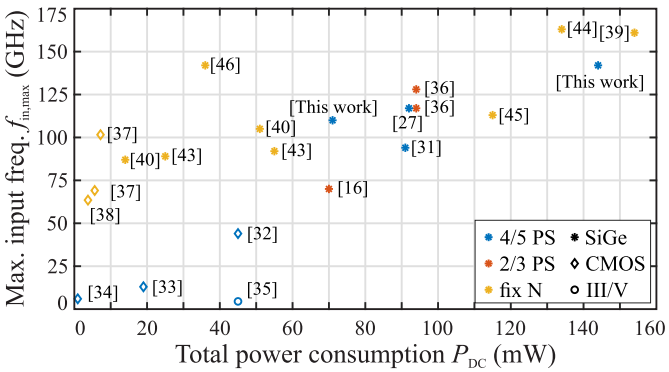

Fig. 22. Achieved maximum operation frequency and total power consumption of state-of-the-art prescalers.

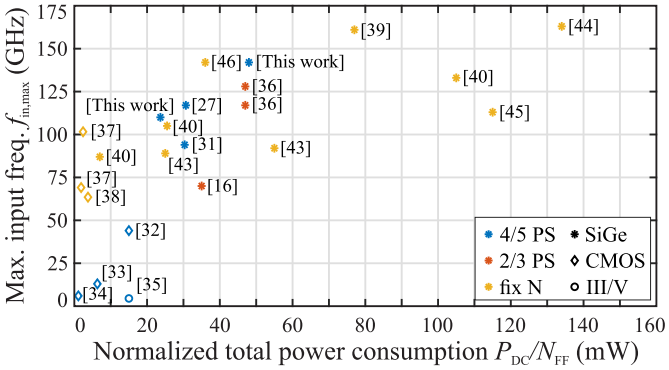

Fig. 23. Achieved maximum operation frequency and total power consumption normalized to amount of FFs of state-of-the-art prescalers.

in a jitter as low as 1.46 fs at an input frequency of 10 GHz, this is not recognizable in Fig. 21. Printed in US letter size, 1 fs time resolution in the eye pattern corresponds to 125 nm resolution on the printed manuscript in the figure.

VI. State-of-the-Art Comparison

Prescalers are excellent benchmarks for comparing different technologies and implementations. There are various comparison criteria involved. Of particular interest are the maximum achievable input frequency and the power consumption of the prescalers. Table I gives an overview of various published prescalers realized in different technologies and different circuit design techniques. It includes not only 4/5 prescalers but also 2/3 prescalers and prescalers with a fixed division ratio of 2 or 4. Not every prescaler operates in the baseband and thus, the operation bandwidth (BW) can be smaller than the achieved maximum input frequency $f_{\text{in,max}}$. For asynchronous concepts similar to those in [44], only the first stage is considered. These static frequency dividers are realized with FFs using ECL or current mode logic (CML). Dynamic regenerative dividers such as in [41], [46] are mentioned for completeness, although they are hard to compare. They feature good power efficiency and outstanding high operation frequencies. Nevertheless, there is no possibility to realize programmable frequency dividers based on regenerative dividers. Another approach to realizing high-performance frequency divider is ILFDs. They are oscillators that oscillate at a fraction of the input frequency by super-harmonic injection-locking [47]. These are particularly interesting because they have low energy consumption. LC-oscillator-based ILFDs (LC-ILFD) offer a better noise performance but are limited by a narrow bandwidth [38]. Ring-oscillator-based ILFDs (RO-ILFD) feature a higher bandwidth but in return a higher phase noise [37]. Since ILFDs are narrow-band and mostly not programmable, their application range is strongly limited. The approaches to realize dual-modulus ILFDs do not yet reach frequencies above 6 GHz [34]. Additionally, to realize a fully programmable frequency divider with a dual-modulus ILFD, a mixed-signal approach has to be realized.

Fig. 22 shows the achieved maximum input frequency $f_{\text{in,max}}$, and the total power consumption P_{DC} of the prescalers from Table I. The colors indicate the division ratios of the prescalers and the symbols indicate the technology of the realizations. The realized high-speed prescaler achieves the highest operating frequency among all dual-modulus prescalers. Nevertheless, there are prescalers with a fixed division ratio, which achieve higher operation frequencies. The realization for an optimum operation frequency of around 80 GHz seems to have an average power efficiency.

In order to evaluate the power efficiency of the listed prescalers, it is reasonable to consider the power consumption of one single FF. By normalizing the total power consumption P_{DC} to the amount N_{FF} of utilized FFs, the different realizations get comparable. In Fig. 23, the achieved maximum input frequency $f_{\text{in,max}}$ and the power consumption of one single FF $P_{\text{DC}}/N_{\text{FF}}$ are depicted. Both realizations feature excellent energy efficiency regarding prescalers at the highest frequencies. Higher operation frequencies can only be achieved through a massive increase in power consumption.

As aforementioned, the additive phase noise of the frequency divider is essential in PLL design. Therefore, the additive phase noise (PN) of the state-of-the-art prescalers is listed in Table I as well. The phase noise is specified at an offset frequency of 1 MHz. Furthermore, the output frequency $f_{\text{out,PN}}$ of the divider at which the phase noise was measured is given. To compare the additive phase noise of different frequency dividers, the phase noise can be normalized to a common output frequency $f_{\text{out,norm}}$ by subtracting $20 \cdot \log_{10}(f_{\text{out,PN}}/f_{\text{out,norm}})$. Therefore, Table I also lists the phase noise PN_{norm} normalized to $f_{\text{out,norm}} = 1$ GHz. If utilized

TABLE I
COMPARISON OF STATE-OF-THE-ART PRESCALERS

Ref	Year	Technology	Div. ratio	Max. inp. frequency (GHz)	BW (GHz)	Power con. (mW)	Technique	PN @1 MHz (dbc/Hz)	$f_{out,PN}$ (GHz)	PN_{norm} @1 MHz (dbc/Hz)
This work	2023	130 nm SiGe BiCMOS	4/5	142 110	142 110	144 71	ECL inductive peaking ECL inductive peak.	−157	4	−169
[27]	2020	90 nm SiGe BiCMOS	4/5	117	117	92	ECL inductive peaking			
[31]	2017	130 nm SiGe BiCMOS	4/5	94	94	91	ECL inductive peaking			
[32]	2006	90 nm Bulk CMOS	4/5	44	44	45	CML inductive peaking	−96.6*	8.31	−115
[33]	2017	130 nm CMOS	4/5	13	13	19	Modified CML			
[34]	2008	180 nm CMOS	4/5	6	4.2	0.22	RO-ILFD			
[35]	2005	GaAs pHEMT	4/5	4.5	4.5	45	Src. Coup. FET Logic			
[36]	2022	130 nm SiGe BiCMOS	2/3	117 128	117 48	94 94	ECL inductive peaking ECL inductive peaking	−145*	2.6	−153.3
[16]	2015	130 nm SiGe BiCMOS	2/3	70	70	66	ECL inductive peaking			
[37]	2022	28 nm CMOS	5	69.1 101.6	24.7 2.6	5.6 7.2	RO-ILFD RO-ILFD	−139	10	−159
[38]	2011	90 nm CMOS	5	63.5	4.1	3.75	LC-ILFD	−134*	12.5	−156
[39]	2015	130 nm SiGe BiCMOS	4	161	161	154	ECL			
[40]	2010	SiGe HBT	4	133 105 87	133 105 87	210 51 14	ECL ECL CML			
[41]	2020	90 nm SiGe BiCMOS	2	242	122	155	regenerative			
[42]	2021	0.8 µm InP DHBT	2	65 55	65 55	225 380	ECL CML	−131* −127*	10 10	−151 −147
[43]	2017	130 nm SiGe BiCMOS	2	92 89	90 75	55 25	CML CML			
[44]	2022	130 nm SiGe BiCMOS	2	163	52	134	ECL			
[45]	2009	180 nm SiGe BiCMOS	2	113	48	115	ECL			
[46]	2023	90 nm SiGe BiCMOS	2	142	22	36	dyn. CML ind. peaking	−117*	64.2	−153

* The phase noise of the input signal reduced by $20 \cdot \log_{10}(N)$ was measured. Thus, the additive phase noise will be lower.

in a PLL, as shown in Fig. 1, the comparison is valid for the contribution of the divider's additive phase noise to the PLL's output phase noise. However, this comparison must be treated with caution. The additive phase noise of a given frequency divider does not simply scale with the output frequency, as the phase noise floor is often determined by thermal noise. Unfortunately, most of the publications listed in Table I provide insufficient or no information on the additive phase noise. Some works, which are marked with *, only measure the phase noise of the divider's input signal reduced by $20 \cdot \log_{10}(N)$. Hence, they only demonstrate that the additive phase noise of the frequency divider is lower than this.

VII. CONCLUSION

We have presented two prescalers designed for use in a dual-modulus divider. Both prescalers are realized in IHP's 130 nm SiGe BiCMOS:C technology. The first prescaler has been optimized to achieve the highest operating frequencies. With a total power consumption of 144 mW and operation frequencies of up to 142 GHz for a division ratio of 5 and even 166 GHz for a division ratio of 4, the power efficiency is very good. The design was optimized regarding the circuit design, the core currents, the logic voltage swing, and the inductive shunt peaking.

The second prescaler was not designed for maximum speed but rather optimized for optimal performance in the frequency range of around 80 GHz. Nevertheless, it still achieves input frequencies of 110 and 125 GHz for the two division ratios of 5 and 4, respectively. Therefore, it has excellent power efficiency as the prescaler's power consumption is 71 mW. For the emerging automotive radar band from 76 to 81 GHz, the minimum required input power is only −27.7 dBm.

Moreover, we elaborated the three-converter method to measure the additive phase noise of frequency-converting DUTs. By applying this, the additive phase noise of the presented prescaler was measured for input frequencies up to 28 GHz. It achieves a low phase noise floor in the range of −162 to −157 dBc/Hz corresponding to a jitter in the range of 0.5 to 1.9 fs depending on the input frequency.

ACKNOWLEDGMENT

The authors would like to thank Leibniz Institute for High Performance Microelectronics for manufacturing the chips.

REFERENCES

[1] G. Hasenaecker, M. van Delden, T. Jaeschke, N. Pohl, K. Aufinger, and T. Musch, "A SiGe fractional-*N* frequency synthesizer for mm-wave wideband FMCW radar transceivers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 847–858, Mar. 2016.

[2] M. Hitzler et al., "Ultracompact 160-GHz FMCW radar MMIC with fully integrated offset synthesizer," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1682–1691, May 2017.

[3] T. Jaeschke, S. Kueppers, N. Pohl, and J. Barowski, "Calibrated and frequency traceable D-band FMCW radar for VNA-like S-parameter measurements," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2022, pp. 64–67.

[4] J. Nehring, M. Dietz, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "A 4–32-GHz chipset for a highly integrated heterodyne two-port vector network analyzer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 892–905, Mar. 2016.

[5] W. Zhang and J. A. Martinez-Lorenzo, "Toward 4-D imaging of on-the-move object at 2500 volumetric frames per second by software-defined millimeter-wave MIMO with compressive reflector antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 3, pp. 1337–1347, Mar. 2023.

[6] K. B. Cooper, R. J. Dengler, N. Llombart, B. Thomas, G. Chattopadhyay, and P. H. Siegel, "Thz imaging radar for standoff personnel screening," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 169–182, Sep. 2011.

[7] D. Kissinger, M. Kaynak, and A. Mai, "Integrated millimeter-wave and terahertz analyzers for biomedical applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 11, pp. 5141–5158, Nov. 2022.

[8] J. Chen, D. Zhang, Z. Wu, F. Zhou, Q. Sun, and Y. Chen, "Contactless electrocardiogram monitoring with millimeter wave radar," *IEEE Trans. Mobile Comput.*, early access, Oct. 14, 2022, doi: 10.1109/TMC.2022.3214721.

[9] M. Mallach, M. Oberberg, P. Awakowicz, and T. Musch, "Fast broadband reflectometer for diagnostics of plasma processes based on spatially distributed multipole resonance probes," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1022–1025.

[10] F. Schenkel, C. Schulz, C. Baer, and I. Rolfes, "Plasma state supervision utilizing 140 GHz radar measurements," in *Proc. 18th Eur. Radar Conf. (EuRAD)*, Apr. 2022, pp. 25–28.

[11] J. Barowski, M. Zimmermanns, and I. Rolfes, "Millimeter-wave characterization of dielectric materials using calibrated FMCW transceivers," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 8, pp. 3683–3689, Aug. 2018.

[12] N. Palka, M. Szala, and E. Czerwinska, "Characterization of prospective explosive materials using terahertz time-domain spectroscopy," *Appl. Opt.*, vol. 55, no. 17, p. 4575, 2016.

[13] M. van Delden, N. Pohl, and T. Musch, "An ultra-wideband fast frequency ramp synthesizer at 60 GHz with low noise using a new loop gain compensation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 9, pp. 3937–3946, Sep. 2018.

[14] M. van Delden, N. Pohl, K. Aufinger, C. Baer, and T. Musch, "A low-noise transmission-type yttrium iron garnet tuned oscillator based on a SiGe MMIC and bond-coupling operating up to 48 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 10, pp. 3973–3982, Oct. 2019.

[15] R. Best, *Phase-Locked Loops*, 6th ed. New York, NY, USA: McGraw-Hill Education, 2007.

[16] A. Ergintav, J. Borngräber, B. Heinemann, H. Rücker, F. Herzel, and D. Kissinger, "A 70 GHz static dual-modulus frequency divider in SiGe BiCMOS technology," in *Proc. 10th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2015, pp. 65–68.

[17] M. van Delden, G. Hasenaecker, N. Pohl, K. Aufinger, and T. Musch, "An 80 GHz programmable frequency divider for wideband mm-wave frequency ramp synthesis," in *Proc. IEEE Int. Symp. Radio-Frequency Integr. Technol. (RFIT)*, Aug. 2015, pp. 181–183.

[18] S. Levantino, L. Romano, S. Pellerano, C. Samori, and A. L. Lacaita, "Phase noise in digital frequency dividers," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 775–784, May 2004.

[19] R. R. Johnson, "Electronic counter," U.S. Patent 3 030 581, Apr. 17, 1962.

[20] U. Tietze and C. Schenk, *Electronic Circuits*, 2nd ed. Heidelberg, Germany: Springer, 2008.

[21] H.-M. Rein and M. Moller, "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1076–1090, Aug. 1996.

[22] H. Rücker and B. Heinemann, "Device architectures for high-speed SiGe HBTs," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, pp. 1–7.

[23] C. C. McAndrew et al., "VBIC95, the vertical bipolar inter-company model," *IEEE J. Solid-State Circuits*, vol. 31, no. 10, pp. 1476–1483, Oct. 1996.

[24] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[25] S. Voinigescu, *High-Speed Integrated Circuits*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 2013.

[26] Sonnet Software. (2018). *Sonnet User's Guide*. Syracuse, NY, USA. [Online]. Available: https://www.sonnetsoftware.com/support/downloads/manuals/st_users.pdf

[27] L. Polzin, M. van Delden, N. Pohl, K. Aufinger, and T. Musch, "A 117 GHz dual-modulus prescaler with inductive peaking for a programmable frequency divider," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4.

[28] L. Polzin, M. van Delden, N. Pohl, H. Rücker, and T. Musch, "A 142-GHz 4/5 dual-modulus prescaler for wideband and low noise frequency synthesizers in 130-nm SiGe:C BiCMOS," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 6, pp. 867–870, Jun. 2023.

[29] G. Feldhaus and A. Roth, "A 1 MHz to 50 GHz direct down-conversion phase noise analyzer with cross-correlation," in *Proc. Eur. Freq. Time Forum (EFTF)*, Apr. 2016, pp. 1–4.

[30] Rohde & Schwarz. (Oct. 2017). *2-Port Residual Noise Measurements*. Accessed: Jun. 11, 2023. [Online]. Available: http://www.rohde-schwarz.com/appnote/1EF100

[31] M. van Delden, N. Pohl, K. Aufinger, and T. Musch, "A 94 GHz programmable frequency divider with inductive peaking for wideband and highly stable frequency synthesizers," in *Proc. 12th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2017, pp. 9–12.

[32] C. Lee, L.-C. Cho, and S.-I. Liu, "A 44 GHz dual-modulus divide-by-4/5 prescaler in 90 nm CMOS technology," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2006, pp. 397–400.

[33] V. Issakov and S. Trotta, "Low-power dual-modulus frequency divider by 4/5 up to 13-GHz in 0.13 μm CMOS," in *Proc. IEEE Int. Conf. Microw., Antennas, Commun. Electron. Syst. (COMCAS)*, Nov. 2017, pp. 1–4.

[34] X. Yu, J. Zhou, X. Yan, W. M. Lim, M. A. Do, and K. S. Yeo, "Sub-mW multi-GHz CMOS dual-modulus prescalers based on programmable injection-locked frequency dividers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 431–434.

[35] M. Detratti, J. Cabo, J. P. Pascual, and A. Herrera, "A 4.5 GHz 3–4 dual-modulus frequency divider IC in GaAs technology," in *Proc. Eur. Microw. Conf.*, vol. 2, Oct. 2005, p. 994.

[36] A. Ergintav, F. Herzel, F. Korndorfer, T. Mausolf, D. Kissinger, and G. Fischer, "A dual-modulus frequency divider up to 128 GHz in SiGe BiCMOS technology," in *Proc.17th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2022, pp. 48–51.

[37] A. Garghetti, A. L. Lacaita, D. Seebacher, M. Bassi, and S. Levantino, "Analysis and design of 8-to-101.6-GHz injection-locked frequency divider by five with concurrent dual-path multi-injection topology," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1788–1799, Jun. 2022.

[38] M.-W. Li, H.-C. Kuo, T.-H. Huang, and H.-R. Chuang, "60 GHz CMOS divide-by-5 injection-locked frequency divider with an open-stub-loaded floating-source injector," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2011, pp. 1–4.

[39] A. Fox et al., "Advanced heterojunction bipolar transistor for half-THz SiGe BiCMOS technology," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 642–644, Jul. 2015.

[40] H. Knapp et al., "Static frequency dividers up to 133 GHz in SiGe:C bipolar technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Oct. 2010, pp. 29–32.

[41] B. Sene, H. Knapp, D. Reiter, and N. Pohl, "A 122–242 GHz dynamic frequency divider in an advanced BiCMOS technology," in *Proc. 15th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Jan. 2021, pp. 296–299.

[42] W. Zhen, S. Cao, Y. Su, S. Li, and Z. Jin, "A novel design method of SOF for InP DHBT ECL and CML static frequency dividers," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 583–586, Jun. 2021.

[43] V. Issakov, S. Trotta, and H. Knapp, "Low-voltage flip-flop-based frequency divider up to 92 GHz in 130 nm SiGe BiCMOS technology," in *Proc. Integr. Nonlinear Microw. Millimetre-Wave Circuits Workshop (INMMiC)*, Apr. 2017, pp. 1–3.

[44] F. Vogelsang, C. Bredendiek, J. Schöpfel, H. Rücker, and N. Pohl, "A static frequency divider up to 163 GHz in SiGe-BiCMOS technology," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Oct. 2022, pp. 49–52.

[45] S. Trotta, H. Li, V. P. Trivedi, and J. John, "A tunable flipflop-based frequency divider up to 113 GHz and a fully differential 77 GHz push-push VCO in SiGe BiCMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 47–50.

[46] Z. Hu, T.-C. Hsueh, and G. M. Rebeiz, "A low-power 130-GHz tuned frequency divider in 90-nm SiGe BiCMOS," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 6, pp. 735–738, Jun. 2023.

[47] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

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