Novel High-Performance SIW Cavity-Based Switching Structures

Kareem H. El-Gendy, *Graduate Student Member, IEEE*, Mohammad Abu Khater, *Senior Member, IEEE*, Islam H. Abdelaziem, *Graduate Student Member, IEEE*, Mahmoud A. Abdalla, *Senior Member, IEEE*, Dimitrios Peroulis, *Fellow, IEEE*, and Mohamed F. Hagag, *Senior Member, IEEE*

***Abstract*— In this article, novel architectures for high-speed substrate integrated waveguide (SIW) filtering switches with high-power handling are presented. A four-port filtering double-pole, double-throw (DPDT) switch and a three-port filtering routing switch are demonstrated as a proof-of-concept. For both switches, the structure consists of a main switching circular cavity with concentric posts. These posts enable the excitation of multiple resonant modes. The resonant modes are aligned in frequency using loading capacitances. p-i-n-diodes are used to short loading posts. Consequently, the generated fields interfere constructively and destructively at the output ports. Concept-proving structures are designed, implemented, and measured. For the SIW-DPDT switch, a measured insertion loss and isolation of 2.95 and 26 dB are achieved, respectively, at 7.4 GHz. Furthermore, a 2.98 and 30 dB measured insertion loss and isolation are obtained for the SIW-routing switch, respectively, at 7.7 GHz. The measured insertion losses include the losses of the filtering cavities. The proposed structures share the same switching technique. As a result, the power handling measurements are performed only for the routing switch, which is measured to handle 40 dBm of input power. Also, the employed switching technique is demonstrated to exhibit a switching speed of less than 80 ns.**

***Index Terms*— Double-pole double-throw (DPDT), evanescent-mode cavity, filtering, high-power switch, high-speed switch, substrate integrated waveguide (SIW).**

I. Introduction

SWITCHES are crucial building blocks in an extensive range of microwave devices and radio frequency (RF) applications. They control the energy flow of RF signals among multiple devices, independently. Switches are generally defined by their numbers of poles and throws, exhibiting different operational states. There are many aspects that cover the switch performance, such as switching speed, isolation, power handling, and linearity. In nowadays applications, high switching speed is a critical feature to avoid information loss, especially in high-frequency applications. In the switch design, the utilized active devices (diodes and transistors) play an essential role in determining the switch design features. Although micro-electromechanical systems (MEMSs) switches have high levels of isolation and linearity, their speed is relatively low, as they operate in the range of microseconds. On the other side, solid-state switches (e.g., p-i-n-diodes) have a relatively high switching speed as they switch in nanoseconds [1], [2], [3], [4].

High-power handling is another main attribute of switch design. A compromise often exists between switching speed and power handling capability, as they both depend on the active switching devices. High-power handling switches have a relatively low switching speed and vice-versa [5], [6], [7], [8]. For example, in [9], a dielectric cavity resonator is used to implement an SPDT switch using a p-i-n-diode [6]. Although the switching structure handles a high input power, it has a low switching speed and is bulky in size. In [10], a high-power SPQT switch is presented using coaxial cavity resonators. The switch suffers from low switching speed as well as integration difficulty.

Substrate integrated waveguide (SIW) technology paved the way for implementing easily-integrable compact-size microwave devices with high unloaded quality factor and high-power handling capability [11], [12], [13]. Moreover, a wide variety of SIW switching topologies have been studied and implemented, such as single-pole, single-throw (SPST) [14], [15], [16], single-pole, double-throw (SPDT) [16], [17], [18], and single-pole, multiple-throw (SPMT) switches [19]. Despite the state-of-the-art performance of the previously-stated switching topologies, they all have low switching speeds. To the authors' best knowledge, a double-pole, double-throw (DPDT) switching topology using SIW technology has not been proposed yet. Moreover, a three-port device with the capability of routing the energy flow between any arbitrary ports while maintaining the third port isolated is designed and implemented, for the first time.

Novel high-speed, high-power SIW cavity-based filtering switching structures are proposed in this article. A DPDT switch and a three-port routing switch are demonstrated. Both structures share the same switching technique based on multimode SIW cavities. Circular evanescent-mode SIW

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Kareem H. El-Gendy, Mahmoud A. Abdalla, and Mohamed F. Hagag are with the Department of Electronic Engineering, Military Technical College, Cairo 11766, Egypt (e-mail: kareemhossam@ieee.org; maaabdalla@ieee.org; m.a.fouadhagag@ieee.org).

Mohammad Abu Khater was with the School of Electrical and Computer Engineering, Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA. He is now with Normal Computing, New York City, NY 10007 USA (e-mail: mabukhater@ieee.org).

Islam H. Abdelaziem and Dimitrios Peroulis are with the School of Electrical and Computer Engineering, Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: iabdelaz@purdue.edu; dperouli@purdue.edu).

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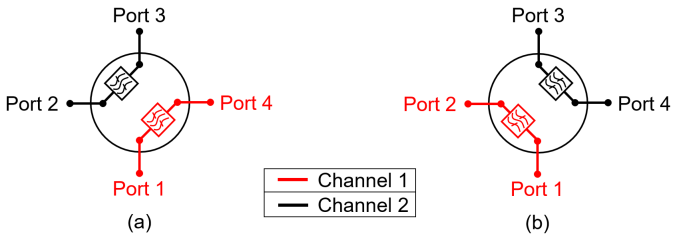


Fig. 1. Architecture of a filtering DPDT switching structure. (a) State 1. (b) State 2.

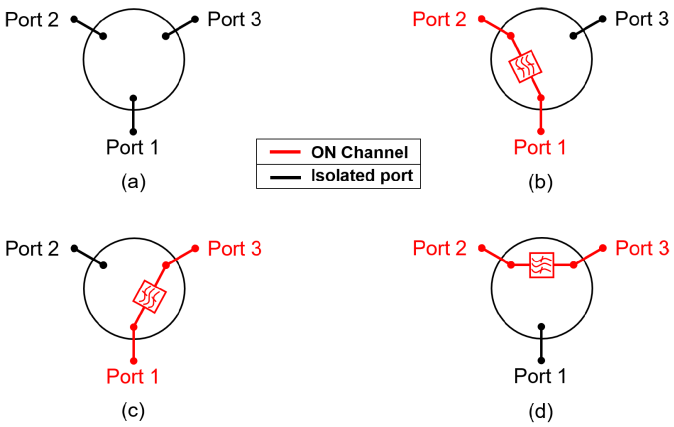
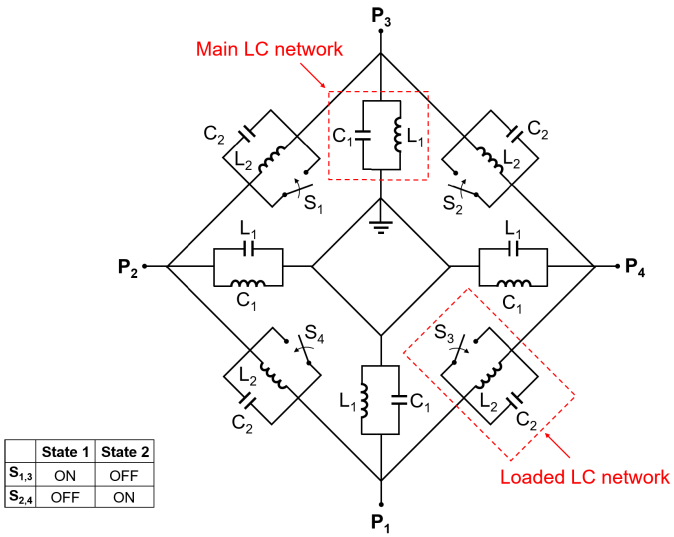


Fig. 2. Architecture of a filtering routing switch. (a) State zero. (b) State 1. (c) State 2. (d) State 3.



	State 1	State 2
$S_{1,3}$	ON	OFF
$S_{2,4}$	OFF	ON

Fig. 3. Equivalent circuit of the proposed DPDT switching structure.

cavity resonators are employed. Both switches consist of a main SIW cavity resonator for switching purposes as well as SIW cavity resonators for additional filtering functions at each port. In the main switching SIW cavity of both switches, two different evanescent-modes (modes I and II) are excited and aligned in resonant frequencies. High switching speed p-i-n-diodes [8] are connected between adjacent posts. Switching the ON/OFF states of the p-i-n-diodes, manipulate the positions in which the two modes add constructively and destructively. Thus, different operational states are generated. Compared to our work (SPDT switch) in [20], the switching structures here (DPDT and routing switches) have a much-improved filtering response and a higher isolation between channels. The proposed SIW cavities have a size of $0.5\lambda_g \times 0.5\lambda_g$. For both states of the SIW-DPDT switch, a 2.95 dB insertion loss and a 26 dB isolation are measured at 7.4 GHz. Furthermore, the SIW-routing switch has a measured insertion loss and isolation of 2.98 and 30 dB at 7.7 GHz, respectively. For both switches, the measured insertion loss includes the losses of the filtering cavities. Although the p-i-n-diode switches deployed in the proposed switching structures have a low power handling capability of only 24 dBm, the proposed switching structures increase the measured power handling capability to reach 40 dBm in the routing switch.

First, the equivalent circuits of the proposed switching structures are presented in Section II, explaining the used switching methodology and the isolation-bandwidth tuning. The switches are then designed and realized in Section III, clarifying the isolation between channels through full-wave simulations. The fabricated switches are shown in Section V including the measured S-parameters and power handling results.

II. Theoretical Analysis

The presented switching structures can be utilized in a number of RF circuits. In this work, a filtering DPDT switch and a filtering routing structure are designed accordingly as shown in Figs. 1 and 2, respectively. This section discusses the basic design and analysis of those two switching circuits. The schematic of the filtering DPDT switching structure is shown in Fig. 1. Considering any two opposite ports (e.g., ports 1 and 3) as the input ports, the output ports are switched between the other orthogonal ports (ports 2 and 4) creating two switchable filtering isolated channels, as shown in Fig. 1(a) and (b). In addition, the schematic of the filtering routing switch is shown in Fig. 2. The switch consists of three ports with four operational states including an OFF-state and three ON-states. Fig. 2(a) defines the zero state (OFF-state) in which all ports are isolated and there is no transmission among them. The ON-states are shown in Fig. 2(b)–(d), where a channel could be created between any two ports with the third port remaining isolated.

A. DPDT Switching Circuit

The equivalent circuit of the proposed DPDT switching structure is shown in Fig. 3. It consists of four main parallel LC networks with an inductor (L_1) and a capacitor (C_1). Each LC network is coupled to a port. An additional parallel LC network is loaded between each two adjacent main LC networks. The loaded network consists of a parallel capacitor (C_2), an inductor (L_2) and a switch (S_n) where $n = 1, 2, 3, 4$. By controlling the states of the switches (ON and OFF), the states of the DPDT switching structure are defined. The first operational state occurs when switches ($S_{1,3}$) are ON and ($S_{2,4}$) are OFF. Two isolated channels are created between ports 1 and 4 (channel 1), and between ports 2 and 3 (channel 2) as shown in Fig. 1(a). Conversely, switching ($S_{2,4}$) are ON and ($S_{1,3}$) are OFF, defines state 2 with two channels

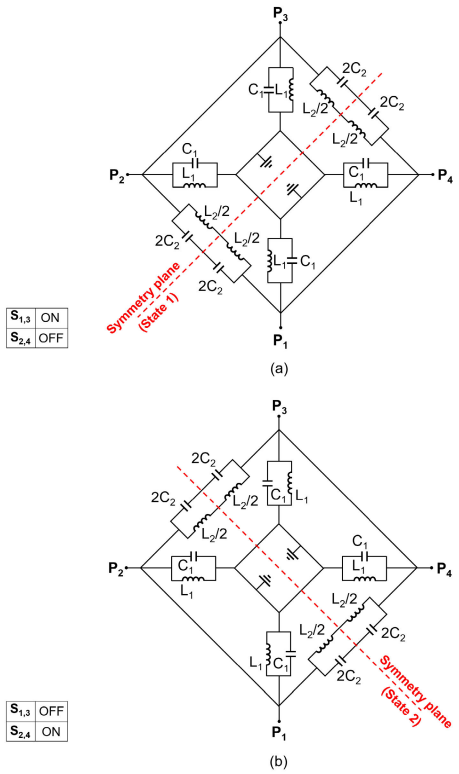


Fig. 4. DPDT switch equivalent circuit with different symmetry planes. (a) State 1. (b) State 2.

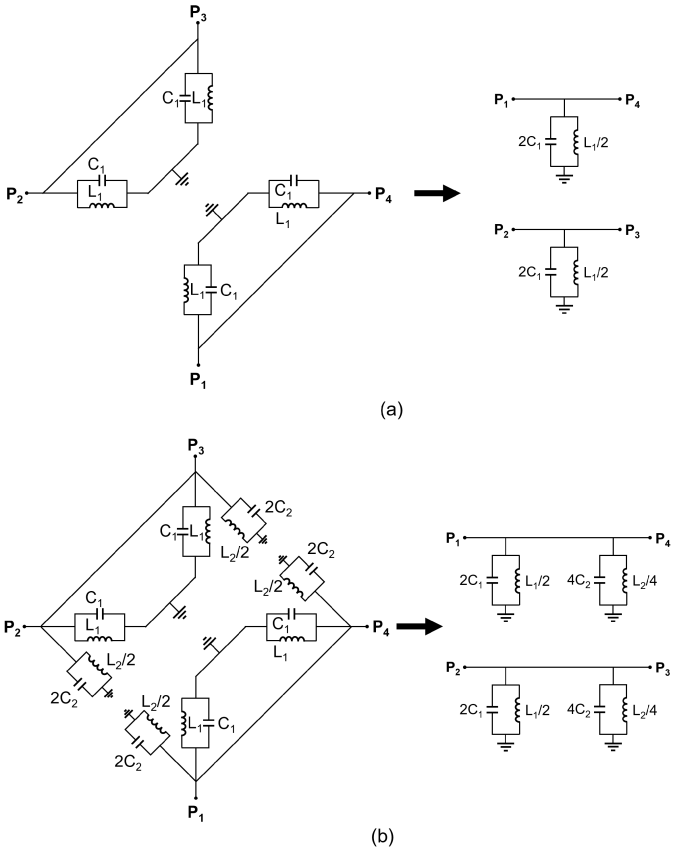


Fig. 5. Equivalent circuit of the first state of the proposed DPDT switch. (a) Even mode circuit. (b) Odd mode circuit.

between ports 1 and 2 (channel 1) and between ports 3 and 4 (channel 2) as shown in Fig. 1(b).

The symmetric forms of the DPDT equivalent circuit are shown in Fig. 4(a) and (b) for states 1 and 2, respectively. Due to the symmetry of the equivalent circuit, even-odd mode analysis can be used.

State 1 is analyzed below, with the results applying to state 2 due to the circuit symmetry. The boundary conditions for the even and odd modes analysis, of the symmetrical circuit in Fig. 4(a), are applied. The reduced circuit of the even mode analysis (magnetic wall) is shown in Fig. 5(a). In addition, Fig. 5(b) shows the odd mode analysis (electric wall) reduced circuit. The even and odd admittances at each port are

$$Y_e = 2j\left(\omega C_1 - \frac{1}{\omega L_1}\right) \tag{1}$$

$$Y_o = 2j\left(\omega(C_1 + 2C_2) - \frac{1}{\omega}\left(\frac{1}{L_1} + \frac{2}{L_2}\right)\right). \tag{2}$$

Given the shunt connection of each LC resonator, the input–output ABCD matrix can be found as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{e,o} = \begin{bmatrix} 1 & 0 \\ Y_{e,o} & 1 \end{bmatrix}. \tag{3}$$

From the ABCD matrix and by the principle of superposition, the S-parameters of the first operational state of the DPDT switching circuit are obtained as follows [21], where (Z_0) is the port impedance

$$S_{11} = -Z_0\left(\frac{Y_e + Y_o + Z_0 Y_e Y_o}{Z_0^2 Y_e Y_o + 2Z_0 Y_e + 2Z_0 Y_o + 4}\right) \tag{4}$$

$$S_{21} = S_{43} = Z_0\left(\frac{Y_o - Y_e}{Z_0^2 Y_e Y_o + 2Z_0 Y_e + 2Z_0 Y_o + 4}\right) \tag{5}$$

$$S_{31} = S_{42} = Z_0\left(\frac{Y_o - Y_e}{Z_0^2 Y_e Y_o + 2Z_0 Y_e + 2Z_0 Y_o + 4}\right) \tag{6}$$

$$S_{41} = S_{32} = \left(\frac{Z_0 Y_e + Z_0 Y_o + 4}{Z_0^2 Y_e Y_o + 2Z_0 Y_e + 2Z_0 Y_o + 4}\right). \tag{7}$$

To achieve the isolation between channels, the admittances of the even and odd mode circuits should be equal $(Y_e = Y_o)$ at the resonant frequency (f_0) as one can conclude from (5) and (6). So, the transmission coefficients become

$$|S_{21}| = |S_{43}| = |S_{31}| = |S_{42}| = 0, \quad (\omega = \omega_0) \tag{8}$$

$$|S_{41}| = |S_{32}| = 1, \quad (\omega = \omega_0). \tag{9}$$

As a result, power flow exists only between ports [1, 4] exhibiting channel 1, and between ports [2, 3] for channel 2, creating the isolation.

For the even and the odd admittances to be equal, the loaded LC networks should be tuned to resonate at the same frequency as the main LC networks. This can be achieved by choosing the values of the lumped elements of the loaded LC networks to be scaled values of the main LC networks, namely,

$$C_2 = nC_1, \quad L_2 = \frac{L_1}{n}. \tag{10}$$

If (10) is satisfied, the even and odd mode admittances are both zeros at the resonant frequency (ω_0), as shown

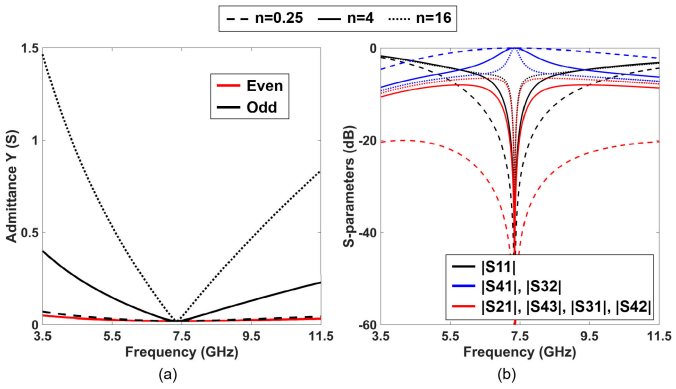


Fig. 6. Impact of the scaling factor (n) on the DPDT switching circuit with ($C_1 = 0.296$ pF, $L_1 = 1.583$ nH and by considering an infinite external coupling at each port). (a) Even and odd mode admittances. (b) Simulated S-parameters of the first operational state.

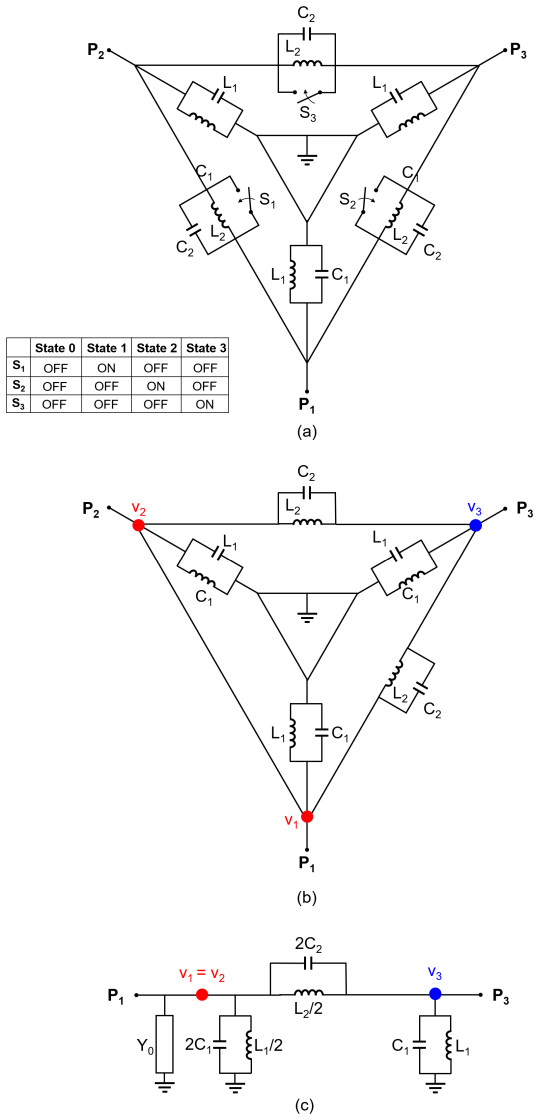
in Fig. 6(a). At further frequencies from the resonance, the odd mode admittance gradually diverges from the even mode one, decreasing the isolation. This divergence rate is directly proportional to the ratio (n). In other words, the isolation bandwidth can be controlled by the ratio (n). Fig. 6(b) shows the S-parameters of the first operational state of the DPDT switching circuit, simulated at different values of (n). It can be observed from Fig. 6 and by considering an infinite external coupling at each port, increasing (n) exhibits a faster diversion rate of change and a narrower isolation bandwidth is obtained.

B. Routing Switch Circuit

A similar transfer function control can also be implemented in a three-port routing switch. The equivalent circuit of the routing switch is shown in Fig. 7(a). It consists of three main and three loaded LC networks. Each loaded LC network is connected in series between each two adjacent main LC networks. Similar to the DPDT switching circuit, the switches define the operational states of the routing switch. When turning OFF all the switches, no channels are created and all ports are isolated from each other, as shown in Fig. 2(a). The ON-states of the routing switch are shown in Fig. 2(b)–(d), in which the power flow could be routed between any two ports while the third port is isolated. A channel is created by turning ON the switch between its ports while the other switches are turned OFF as shown in Fig. 7(a).

Turning ON the switch (S_1) while keeping ($S_{2,3}$) OFF, reduces the equivalent circuit of the routing switch to the one shown in Fig. 7(b). These conditions define the first operational state of the routing switch shown in Fig. 2(b), in which a channel is created between ports 1 and 2 while port 3 is kept isolated. As seen in Fig. 7(b), the power flows between ports 1 and 2 directly achieving the desired channel. To define the isolation between the channel's ports and the isolated port, the equivalent circuit in Fig. 7(b) is reduced to the two-port circuit shown in Fig. 7(c) as the node voltages (v_1) and (v_2) are equal, expressing the isolation between ports 1 and 3, while port 2 is matched.

Considering the reduced circuit in Fig. 7(c) as a two-port π-equivalent circuit, the admittance parameters can be



	State 0	State 1	State 2	State 3
S_1	OFF	ON	OFF	OFF
S_2	OFF	OFF	ON	OFF
S_3	OFF	OFF	OFF	ON

Fig. 7. (a) Equivalent circuit of the proposed routing switch. (b) Equivalent circuit of state 1. (c) Reduced two-port equivalent circuit of state 1 with port 2 is connected to a matched load with an admittance (Y_0).

obtained as follows [21]:

$$Y_{11} = 2j\left(\omega(C_1 + C_2) - \frac{1}{\omega}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)\right) + Y_0 \tag{11}$$

$$Y_{33} = j\left(\omega(C_1 + 2C_2) - \frac{1}{\omega}\left(\frac{1}{L_1} + \frac{2}{L_2}\right)\right) \tag{12}$$

$$Y_{13} = 2j\left(\frac{1}{\omega L_2} - \omega C_2\right). \tag{13}$$

From the admittance parameters, the S-parameters can be found as in (14) and (15), where (Y_0) is the port admittance

$$S_{11} = S_{33} = \frac{(Y_0 - Y_{11})(Y_0 + Y_{33}) + Y_{13}^2}{(Y_0 + Y_{11})(Y_0 + Y_{33}) - Y_{13}^2} \tag{14}$$

$$S_{13} = S_{31} = \frac{-2Y_0Y_{13}}{(Y_0 + Y_{11})(Y_0 + Y_{33}) - Y_{13}^2}. \tag{15}$$

For good isolation, (15) has to be minimized. This can be achieved by minimizing the admittance parameter (Y_{13}). Thus,

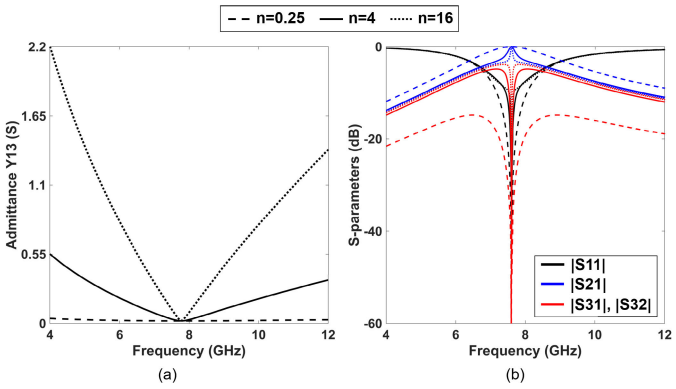


Fig. 8. Behavior of the routing switch with multiple values of (n), at ($C_1 = 0.988$ pF, $L_1 = 0.424$ nH and by considering an infinite external coupling at each port). (a) Admittance parameter (Y_{13}) of the reduced two-port network. (b) Simulated S-parameters of state 1.

at resonant frequency ($Y_{13} = 0$), the series branch acts as an open circuit, exhibiting a band-stop response. Away from the resonant frequency, the admittance value (Y_{13}) gradually increases and a lower level of isolation is obtained.

By symmetry, any two ports can have energy flow between them, with the third one being isolated as discussed above.

The value of the admittance parameter (Y_{13}) is controlled by tuning the value of the scaling factor (n), as discussed in (10). Fig. 8(a) shows that with a greater value of (n), the admittance (Y_{13}) exhibits a higher increasing rate and a narrower isolation bandwidth is obtained. So, the isolation bandwidth of the routing switch is designed by tuning the scaling factor (n), as shown in Fig. 8(a) and (b), respectively.

III. Switching Structures Realization

The concepts presented in Section II are designed in this section using SIW evanescent-mode cavity resonators. The main LC networks are realized by the capacitive posts and the walls of the SIW cavity resonator. The isolation is achieved between the channels by realizing the loaded LC networks with conductive areas (A_2). The switching process between different operational states is achieved using p-i-n-diodes. In Section III-A, the DPDT switching circuit shown in Fig. 3 is realized. Two switchable channels are created with two operational states. The isolation between channels is demonstrated based on the field analysis of the generated evanescent modes. Similarly and in Section III-B, the three-ports routing switch circuit shown in Fig. 7(a) is realized. The proposed SIW cavity can route the RF signal path between any two arbitrary ports. The SIW cavity exhibits three ON-states and an OFF-state with the same isolation technique as in the SIW-DPDT switching cavity.

A. DPDT Switching Structure

The topology of the proposed SIW-DPDT filtering switch is shown in Fig. 9(a). It consists of four LC networks, as previously shown in Fig. 3, connected to two outer resonators for filtering purposes using transmission lines. A 3-D structure of the proposed SIW-DPDT switch is shown in Fig. 9(b). The design includes two substrates and three copper layers. It consists of three evanescent-mode circular SIW cavity resonators, and a main switching cavity is sandwiched between two cavities for additional filtering purposes. The switching cavity is loaded with four capacitive posts, while each filtering cavity resonator is loaded with one capacitive post. Each filtering cavity has a simulated insertion loss of 1 dB as shown in the inset of Fig. 9(b).

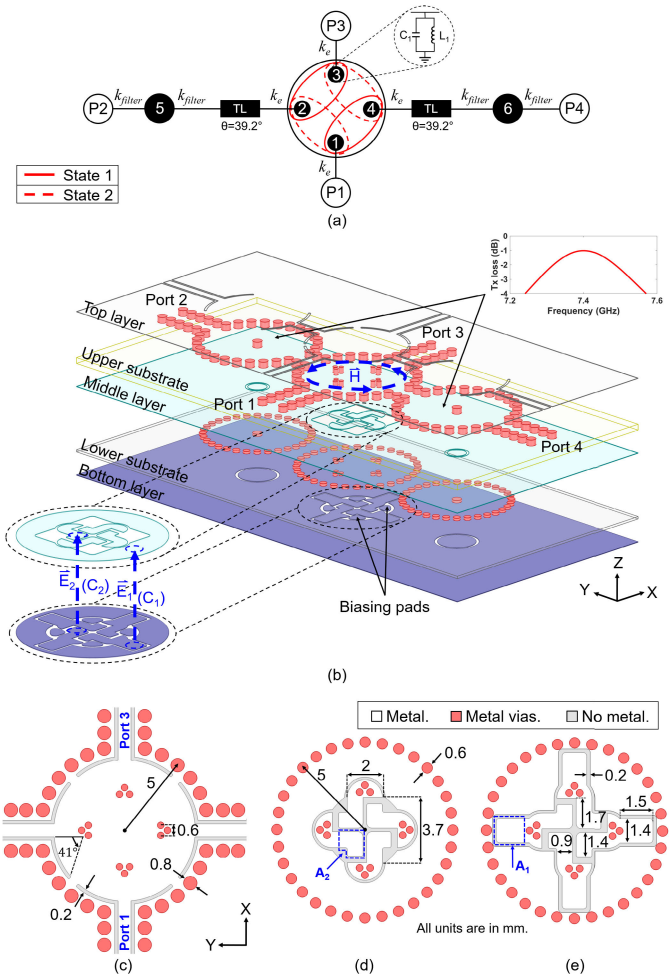


Fig. 9. (a) Coupling diagram of the proposed SIW-DPDT filtering switch. (b) Three-dimensional view of the presented SIW-DPDT filtering switch (the directions of the electric/magnetic fields of the switching cavity are clarified). A top view of the center switching cavity. (c) Top layer. (d) Middle layer. (e) Bottom layer (all units are in mm).

The three copper layers of the proposed SIW-DPDT switch are shown in Fig. 9(c)–(e). The three circular SIW cavity resonators are hosted in the upper substrate, shown in Fig. 9(b), between the top and the middle copper layers. The external coupling is controlled using an arc-shaped structure in the top copper layer shown in Fig. 9(c). The bottom layer contains a controllable loading capacitance for each resonator to properly align different resonating modes in frequency. Namely, the metalized area (A_1), as shown in Fig. 9(e), creates a parallel plate loading (C_1). Another parallel plate (C_2) is created between areas (A_2) of each two adjacent posts in different copper layers. This capacitance controls the resonant frequency of mode II as will be discussed later in this section. The electric field of the cavity is confined in the lower substrate through the aforementioned capacitances while most of the magnetic field is found in the upper substrate.

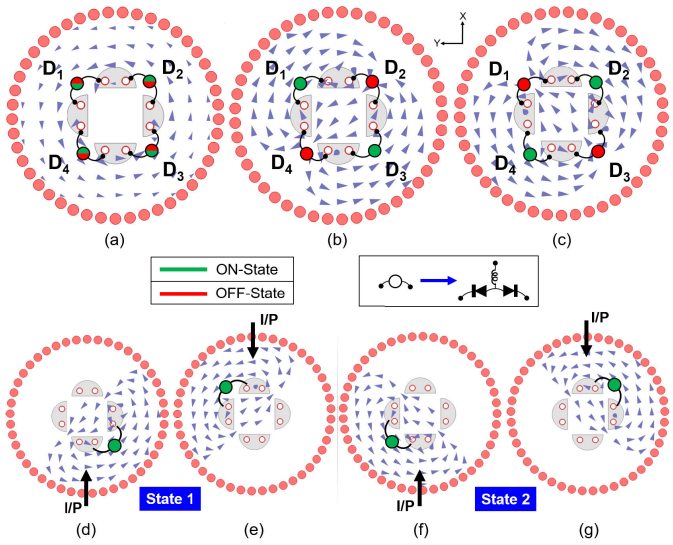


Fig. 10. For the SIW switching cavity resonator in the upper substrate and by taking port 1 as the input port. (a) Magnetic field distribution of mode I. (b) Magnetic field distribution of mode II ($D_{1,3}$ ON and $D_{2,4}$ OFF). (c) Magnetic field distribution of mode II ($D_{2,4}$ ON and $D_{1,3}$ OFF). (d)–(g) Behavior of the resultant magnetic field for different channels (each circle symbol stands for two back-to-back connected p-i-n-diodes).

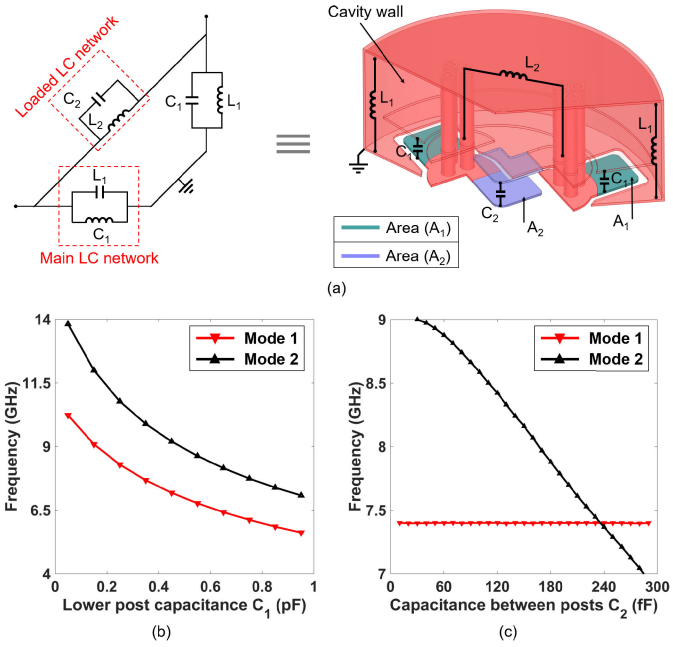


Fig. 11. (a) Magnified 3-D view of a cross section of the proposed DPDT cavity resonator is compared with its equivalent circuit shown in Fig. 3, defining the equivalent lumped elements (L_1, L_2, C_1, and C_2) and showing the designed areas (A_1 and A_2). (b) Impact of the capacitance (C_1) on the resonant frequencies of the excited evanescent modes. (c) Impact of the capacitance (C_2) on the resonant frequencies of the excited evanescent modes.

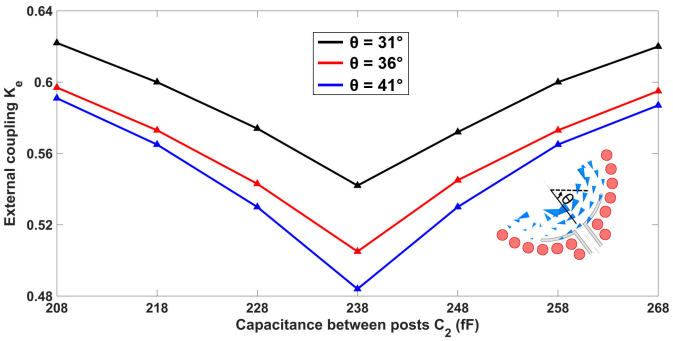


Fig. 12. In the DPDT main switching cavity and by using the single-port model, the behavior of the external coupling (K_e), of the resultant mode, with various angles of the two-sided coupling arc-shaped structure (showing the asymmetrical distribution of the field of the resultant mode with the coupling slots).

In the main switching cavity, two different evanescent modes are generated (modes I and II) as shown in Fig. 10. Four pairs of p-i-n-diodes are used, each pair is placed between each two adjacent capacitive posts. The magnetic field distribution of mode I, the main mode, is shown in Fig. 10(a). It can be noticed that it is located only in the area outside the posts and circulates in a single direction. Switching the p-i-n-diodes has no effect on the distribution of mode I. On the other hand, mode II is a differential higher-order evanescent mode. Fig. 10(b) shows the magnetic field behavior of mode II when p-i-n-diodes ($D_{1,3}$ ON) and ($D_{2,4}$ OFF). As shown in Fig. 10(c), by swapping the p-i-n-diodes states, ($D_{2,4}$ ON) and ($D_{1,3}$ OFF), mode II is rotated by 90°. The resultant magnetic fields for channels 1 and 2 are shown, respectively, in Fig. 10(d) and (e) for state 1, and in Fig. 10(f) and (g) for state 2 of the DPDT switch. The values of (C_1) and (C_2), along with the structure of the resonator, create constructive and destructive interference between modes I and II such that the proper DPDT switching occurs

$$C = \frac{\epsilon A}{d}. \tag{16}$$

As shown in Fig. 11(a), the realized structure of the proposed DPDT cavity resonator is compared with its equivalent circuit shown in Fig. 3, defining the equivalent lumped element (L_1, L_2, C_1, and C_2). For the main LC network, the inductance (L_1) is represented by the side walls of the cavity, while the capacitance (C_1) is represented by the area (A_1). In addition and for the loaded LC network, the inductance (L_2) is represented by the metalized connection between each two adjacent posts through the ground, while the capacitance (C_2) is represented by the areas (A_2) between adjacent posts. Each capacitance can be approximated as a parallel plate structure as in (16), in which (ϵ) and (d) are the permittivity and the thickness of the lower substrate, respectively. The capacitance (C_1) controls the resonant frequency of both modes, but the capacitance (C_2) can only control the resonant frequency of mode II. So, by controlling the value of (C_1) through adjusting (A_1), the operating frequency of the switching structure is set as shown in Fig. 11(b). Then, the tuning of (C_2), through adjusting (A_2), is used to align the resonant frequency of mode II to that of mode I as shown in Fig. 11(c).

Using the single-port model, the behavior of the external coupling coefficient (K_e) of the resultant mode, in the main switching cavity, is shown in Fig. 12. A two-sided coupling arc-shaped structure is used for the proposed DPDT cavity to keep the symmetry across its four ports, which is necessary for the switching process. The external coupling is designed around the value of the capacitance (C_2) in which mode II is aligned with mode I in resonant frequency. As shown in Fig. 12, the external coupling coefficient changes with

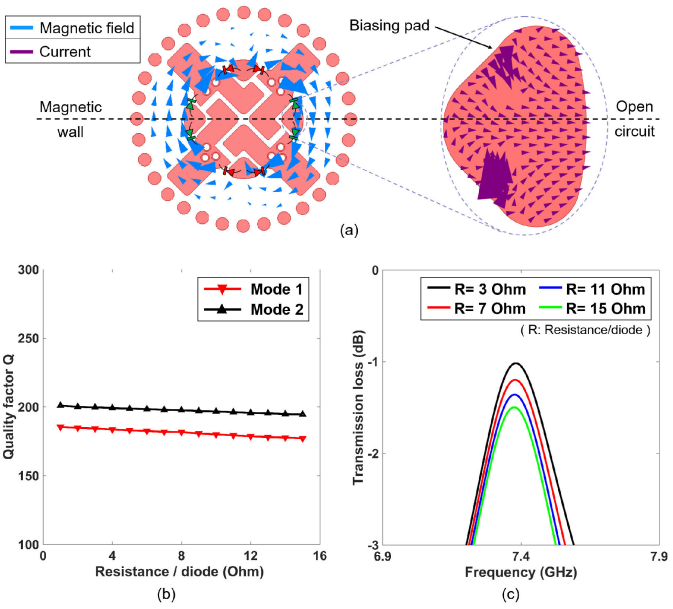


Fig. 13. For any switching operational state. (a) Resultant magnetic field of the SIW cavity, along with the distribution of the current on the surface of a biasing pad with ON-stated p-i-n-diodes. (b) Variation of the simulated unloaded quality factor (Q), extracted by using the HFSS Eigen-mode solver, with the changing value of the p-i-n-diode's resistance. (c) Simulated transmission loss of a DPDT channel with different values of p-i-n-diode's resistance.

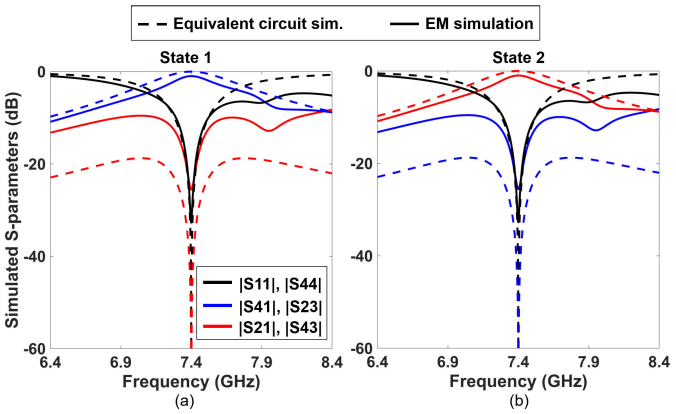


Fig. 14. For the DPDT main switching SIW cavity resonator, a comparison between the simulated S-parameters of its equivalent circuit shown in Fig. 3 ($C_1 = 0.793$ pF, $L_1 = 0.588$ nH, $n = 0.3$ and by considering an external coupling of 0.48 at each port) and its EM simulation results. (a) State 1. (b) State 2.

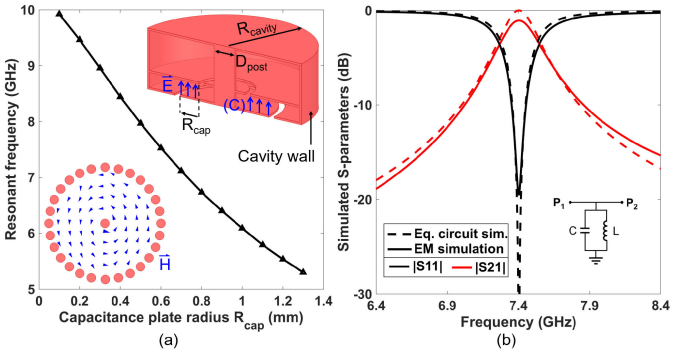


Fig. 15. For the additional SIW evanescent cavity resonator. (a) Impact of varying the radius of the capacitance plate on the resonant frequency of the cavity, with a cavity radius (R_{cavity}) of 5 mm and a post diameter (D_{post}) of 1.6 mm. (b) Comparison between the simulated S-parameters of the cavity's equivalent circuit ($C = 0.79$ pF, $L = 0.585$ nH and an external coupling of 0.185 at each port) and its EM simulation results ($R_{\text{cap}} = 0.58$ mm).

the variation of the capacitance between posts (C_2). The operational point of the switch is defined as the capacitance value at which the two modes are aligned. At this capacitance, the external coupling is minimal. The bandwidth of the DPDT switch is designed by adjusting the angle (θ) of the arc-shaped structure of the switching cavity. Increasing the angle (θ) exhibits a lower external coupling coefficient, as the field of the resultant mode has an asymmetrical distribution across the two sides of the arc-shaped structure.

For any DPDT operational state, the resultant magnetic field of its two channels is shown in Fig. 13(a). Also, a magnified view of the biasing pad between any channel's output ports, clarifying the current distribution, is shown in Fig. 13(a). Following the orientations of both, the current and the resultant magnetic field, the switching cavity exhibits a magnetic wall (open-circuit) boundary condition that bisects the two channels as shown in Fig. 13(a). So, a minimum current will flow to the pad and the p-i-n-diodes soldered on it. This explains the high unloaded quality factor (Q) of the DPDT switching cavity as shown in Fig. 13(b). Using p-i-n-diodes with very high resistance slightly degrades the quality factor of the modes of the switching cavity. As a result, a low simulated insertion loss of the switching cavity is obtained as shown in Fig. 13(c).

By setting the p-i-n-diodes at the state [($D_{1,3}$ ON) and ($D_{2,4}$ OFF)], mode II will have the distribution shown in Fig. 10(b). Considering ports 1 and 3 as the input ports, the summations of modes I and II are shown in Fig. 10(d) and (e). For the input signal at port 1, the two modes add up constructively at port 4 while they add up constructively at port 2 for the input power at port 3, defining the first operational state of the proposed DPDT switch shown in Fig. 1(a). The EM simulated S-parameters of this state are shown in Fig. 14(a). It can be seen that the results coincide with the simulated S-parameters of its equivalent circuit shown in Fig. 4(a). The isolation between the two channels is achieved because the summations of the two modes (modes I and II) excited from two opposite input ports are out of phase. This can be shown in Fig. 10(d) and (e) where the summations (magnetic field vectors) have opposite directions. As shown in Fig. 10(f) and (g), switching the diodes to the second state [($D_{1,3}$ OFF) and ($D_{2,4}$ ON)], the summations are rotated by 90° changing the path of the channels as discussed before. Fig. 14(b) shows a comparison between the EM simulated S-parameters of state 2 with the simulated S-parameters of its equivalent circuit shown previously in Fig. 4(b).

As mentioned, an additional SIW evanescent cavity resonator is placed at the output ports of the DPDT main switching cavity. A parallel LC network represents the equivalent circuit of each additional SIW cavity resonator. Each resonator is loaded with a capacitive post, exciting one evanescent mode (the fundamental evanescent mode) [22]. The magnetic field distribution of this mode is shown in Fig. 15(a). The capacitive post represents the equivalent circuit capacitance (C), while the equivalent circuit inductance (L) is represented by the

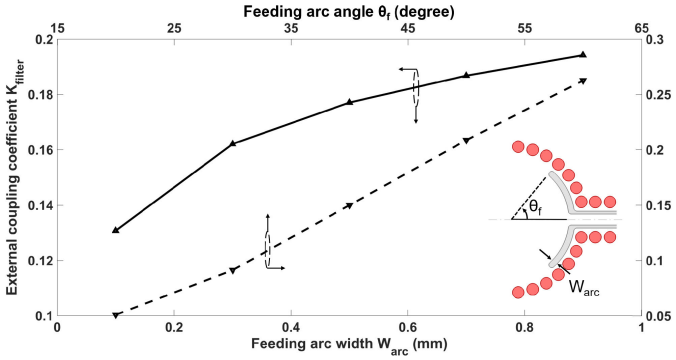


Fig. 16. Behavior of the external coupling coefficient (K_{filter}) of the additional SIW cavity resonator with the feeding arc width (W_{arc}) simulated at a feeding arc angle (θ_f) of 40°, and with (θ_f) simulated at (W_{arc}) of 0.2 mm.

walls of the cavity. The resonant frequency of the cavity is tuned by adjusting the capacitance plate radius (R_{cap}). As shown in Fig. 15(a), the resonant frequency decreases by maximizing the capacitance (C) through increasing (R_{cap}). A comparison between the equivalent circuit simulation ($C = 0.79$ pF and $L = 0.585$ nH and an external coupling of 0.185 at each port) of each additional cavity resonator and its EM simulation is shown in Fig. 15(b). By tuning the resonant frequency of the additional cavity resonators to coincide with the resonant frequency of the main switching cavity, the filtering response of the DPDT switching structure is enhanced. The behavior of the external coupling coefficient (K_{filter}) of the cascaded filtering cavities is shown in Fig. 16. As can be seen, (K_{filter}) rises with the increase of both, the feeding arc width (W_{arc}) and the angle (θ_f).

B. Routing Switch Structure

The topology of the proposed SIW routing switch cavity is shown in Fig. 17(a). It consists of three LC networks, as previously shown in Fig. 7, in which the signal's path can be routed between any two adjacent ones. A detailed view of the proposed SIW routing switch cavity is shown in Fig. 17(b). Two substrates are aligned vertically with a circular SIW cavity in the upper substrate. The cavity is loaded with three capacitive posts. Three grounded coplanar waveguide (CPWG) feeding ports are attached to the SIW cavity. The three ports have the same orientation as the capacitive posts. The top, middle, and bottom conductive layers of the proposed routing switch are, respectively, shown in Fig. 17(c)–(e). Similar to the DPDT switching cavity, each post is attached with two different metalized areas, area (A_1) and area (A_2). The area (A_1) in the bottom layer, with the middle conductive layer, represents the two parallel plates of the capacitance (C_1). This capacitance is used to tune the resonant frequency of both, modes I and II. In the same way, the capacitance (C_2) represented with the metalized areas (A_2) in both, the middle and the bottom layers, is used to adjust the resonant frequency of mode II. The impact of the capacitances (C_1) and (C_2) on both modes is the same as in the DPDT switching cavity.

The routing cavity excites two evanescent modes, modes I and II. Three pairs of p-i-n-diodes are utilized in the cavity. Each pair is attached to a biasing pad, connecting two adjacent posts. Mode I exists in the area outside the

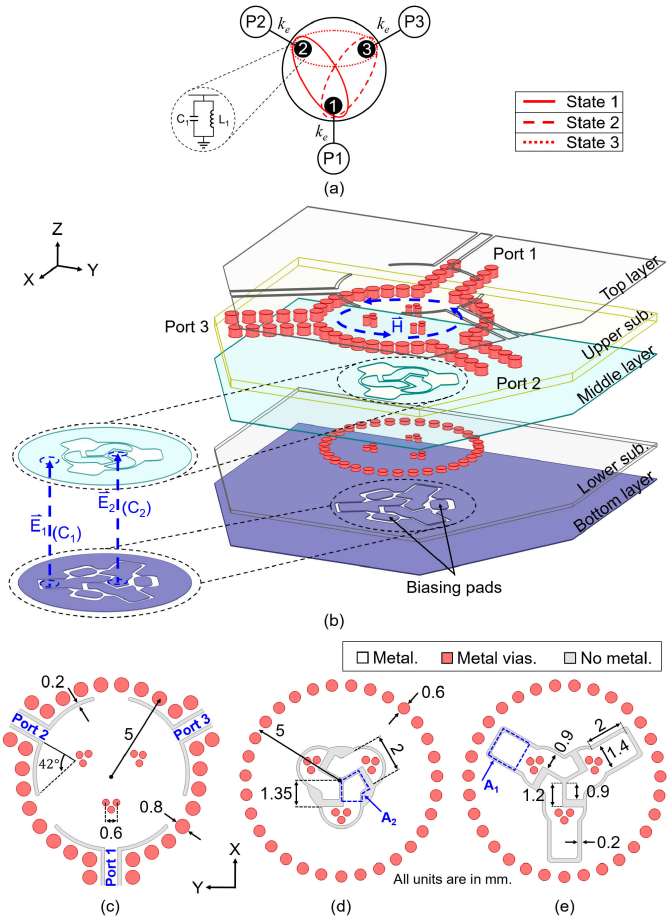


Fig. 17. (a) Coupling diagram of the proposed SIW routing switch cavity. (b) Detailed view of the proposed SIW routing switch cavity (the directions of electric/magnetic fields of the switching cavity are clarified). A Top view of the routing switch cavity. (c) Top layer. (d) Middle layer. (e) Bottom layer (all units are in mm).

posts and its magnetic field is oriented around the posts in the same direction as shown in Fig. 18(a). Mode I exists in the cavity whether the p-i-n-diodes states are ON or OFF. The magnetic field distribution of mode II is shown in Fig. 18(b)–(d) for the first, second and third ON-operational states, respectively. It can be seen that mode II is similar to a differential mode that rotates around the two connected posts, with the ON-state p-i-n-diodes in between, and the third post. For the first operational state, the p-i-n-diode (D_1) is ON while ($D_{2,3}$) are OFF. So, mode II will rotate around the two posts connected with (D_1) and the third post as shown in Fig. 18(b). The resultant magnetic field for this state is shown in Fig. 18(e). Furthermore, when p-i-n-diodes (D_1 ON and $D_{2,3}$OFF), the magnetic field of mode II is rotated by 120° as shown in Fig. 18(c) and the resultant magnetic field of the cavity, representing state 2, is shown in Fig. 18(f). Moreover, Fig. 18(d) and (g) shows the magnetic field distribution of mode II and the resultant magnetic field of the third operational state, respectively.

The behavior of the external coupling (K_e) of the resultant mode of the routing cavity switch is shown in Fig. 19. The two modes are aligned in resonant frequency at a capacitance (C_2) value of (188 fF). As previously explained, by varying the angle (θ) of the arc-shaped structure, the external coupling is

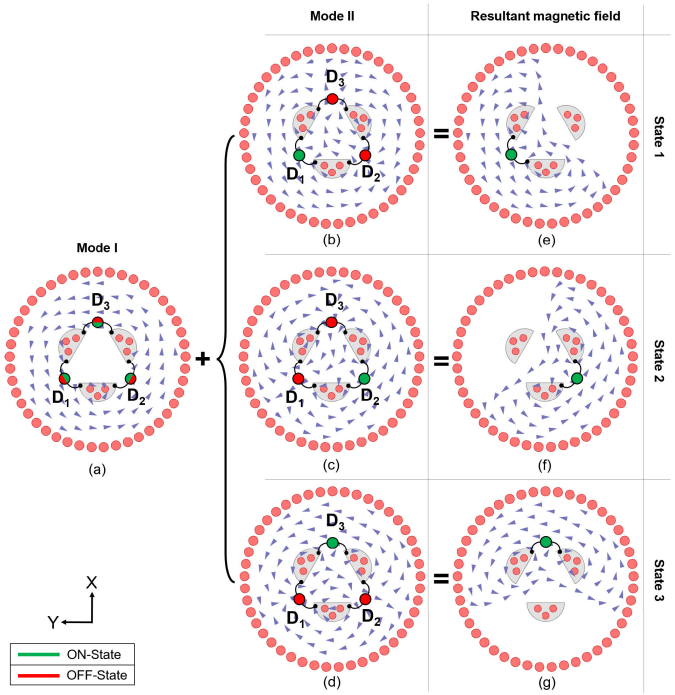


Fig. 18. For the SIW routing switch cavity resonator in the upper substrate. (a) Magnetic field distribution of mode I. (b) Magnetic field distribution of mode II (D_1 ON and $D_{2,3}$ OFF). (c) Magnetic field distribution of mode II (D_2 ON and $D_{1,3}$ OFF). (d) Magnetic field distribution of mode II (D_3 ON and $D_{1,2}$ OFF). (e)–(g) Resultant magnetic field of the cavity for different states (each circle symbol stands for two back-to-back connected p-i-n-diodes).

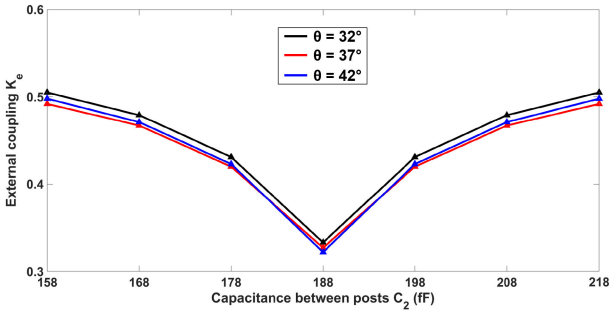


Fig. 19. For the routing cavity switch and by using the single-port model, the behavior of the external coupling (K_e), of the resultant mode, with various angles of the coupling arc-shaped structure.

tuned and the bandwidth of the switch is designed. As shown in Fig. 19, increasing the angle (θ) exhibits a lower external coupling coefficient.

For any ON-operational state, the routing cavity exhibits a magnetic wall boundary condition as previously explained in the DPDT switching cavity. So, a minimum current flows to the ON-state p-i-n-diodes and a high unloaded quality factor (Q) is obtained as shown in Fig. 20(a). For both modes (modes I and II), the unloaded quality factor is nearly unchanged despite using high-resistance p-i-n-diodes. Accordingly, the proposed routing SIW cavity achieves a low simulated insertion loss even with high-resistance p-i-n-diodes. As shown in Fig. 20(b), the routing cavity exhibits a low insertion loss with p-i-n-diodes resistances up to 15 Ω.

By turning the p-i-n-diodes [(D_1 ON) and ($D_{2,3}$ OFF)], the routing cavity exhibits the first operational state shown in

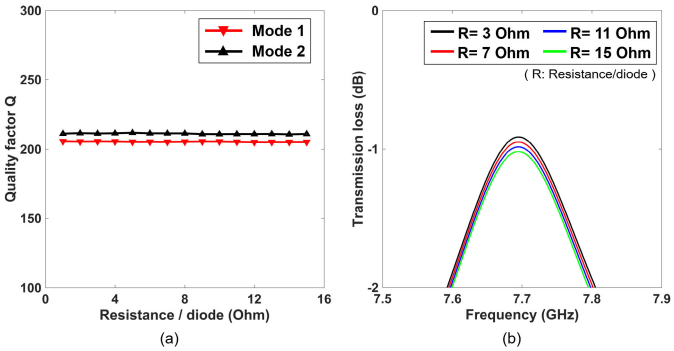


Fig. 20. (a) Impact of varying the resistance of the p-i-n-diodes on the simulated unloaded quality factor (Q), extracted by using the HFSS Eigen-mode solver, of the routing switch cavity. (b) Simulated transmission loss of the routing cavity with different values of the diode's resistance.

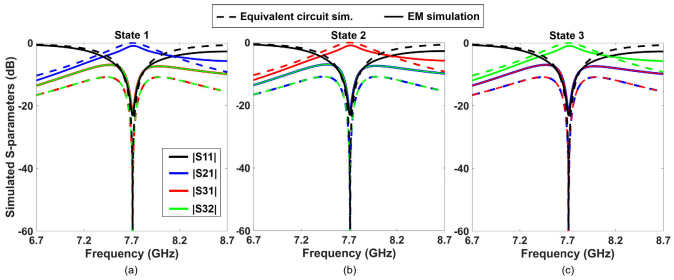


Fig. 21. For the routing main switching SIW cavity resonator, a comparison between its EM simulated S-parameters and the simulated S-parameters of its equivalent circuit shown in Fig. 7(a), at $C_1 = 0.376$ pF, $L_1 = 1.133$ nH, $n = 0.5$ and by considering an external coupling of 0.322 at each port. (a) State 1. (b) State 2. (c) State 3.

Fig. 2(b) where the behavior of mode II will be as shown in Fig. 18(b). So, modes I and II will add up constructively at ports 1 and 2 and destructively at port 3 as shown in Fig. 18(e). Thus, a channel is created between ports 1 and 2 while port 3 remains isolated. Furthermore, switching the states of the p-i-n-diodes [(D_2 ON) and ($D_{1,3}$ OFF)], the summation of the modes is rotated by 120° as shown in Fig. 18(f) exhibiting the second operational state shown in Fig. 2(c) and the path of the input signal at port 1 is routed to port 3 while port 2 will be isolated. Moreover, state 3 shown in Fig. 2(d) is occurred when the p-i-n-diodes [(D_3 ON) and ($D_{1,2}$ OFF)]. As a result, the resultant magnetic field of the SIW cavity will be as shown in Fig. 18(g), and the channel is created between ports 2 and 3 while port 1 will be isolated. Conversely, Switching all the p-i-n-diodes OFF, the routing cavity exhibits an OFF-operational state. So, there will be no power flow among ports and all ports become isolated from each other. For the different operational ON-states of the routing cavity switch, Fig. 21 shows a comparison between the simulated S-parameters of its equivalent circuit, shows in Fig. 7(a), and its EM simulation results.

IV. Experiment Results and Discussion

Both switching structures are fabricated with the measurements being demonstrated in this section. Rogers RO4003C substrates, with 20 and 8 mils thicknesses for the upper and lower substrates, respectively, are utilized in the fabrication process. Four and three pairs of high switching speed

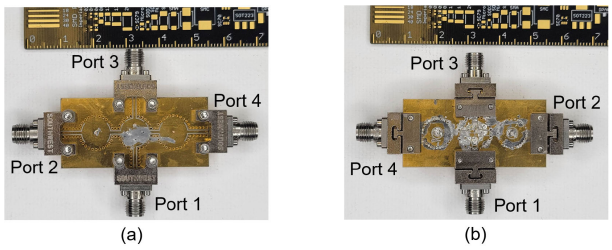


Fig. 22. Photograph of the fabricated filtering SIW-DPDT switching structure. (a) Top view. (b) Bottom view (bias details are removed for clarity).

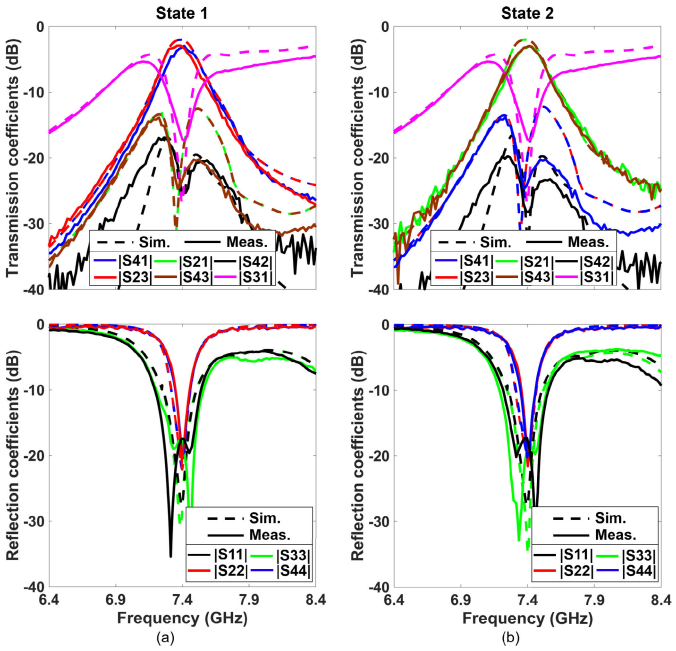


Fig. 23. Simulated and measured S-parameters of the fabricated filtering SIW-DPDT switching structure. (a) State 1. (b) State 2 (10 mA/−10 V are used to bias the p-i-n-diodes ON/OFF states).

p-i-n-diodes (DSM8100-000 Skyworks Mesa Beam-Lead) are used for the DPDT and the routing switches, respectively. The measured S-parameters of both fabricated switches are demonstrated. The DPDT is discussed first, followed by the routing switch. The power handling measurements are applied for only the routing switch to prevent redundancy. The proposed switches have the same switching technique as in our previous work [20]. This technique is demonstrated to have a high switching speed of less than 80 ns.

A. DPDT Switch

Photographs of the fabricated SIW-DPDT filtering switch are shown in Fig. 22. The main switching cavity has a size of 11 × 11 mm^2 without the feeding lines. Four pairs of high-switching speed p-i-n-diodes are deployed. Each pair is positioned between two adjacent posts using the biasing pad in between.

For the proposed filtering DPDT switch, the simulated and measurement results of the first and second operational states are shown in Fig. 23(a) and (b), respectively. A measured 2.95 dB insertion loss is obtained for both states at 7.4 GHz. Also, input and output ports have measured reflection coefficients of 18 and 20 dB, respectively. Isolation of 26 dB is

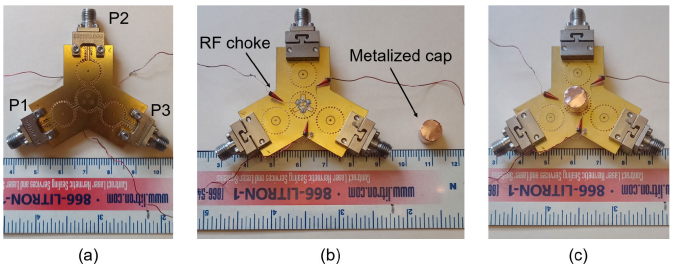


Fig. 24. Photograph of the fabricated filtering routing switch with the bias details. (a) Top view. (b) Bottom view. (c) Bottom view with the metalized cap.

measured between channels of the same state. A bandwidth of 160 MHz is measured at an isolation level of 15 dB. Due to a little misalignment or a slight rotation of one of the two substrates in the lamination process. Mode II is a little shifted from mode I in resonant frequency. As a result, a slight shift exists in the measured frequency responses between both states. Also, the measured reflection coefficients of the main switching cavity ports $|S_{11}|$ and $|S_{33}|$ exhibit a small shift in the resonant frequency of mode II. This shift has a minor effect on the operation of the proposed DPDT switch. As can be seen and compared to our work (SPDT switch) in [20], the filtering response of the DPDT switching structure is enhanced by using the additional SIW cavity resonators.

B. Routing Switch

The top and bottom views of the fabricated filtering SIW-routing switch are shown in Fig. 24(a) and (b), respectively. A metalized cap is utilized as shown in Fig. 24(c) to minimize the radiation loss of the switching cavity and enhance the insertion loss measurements. A 11 × 11 mm^2 routing cavity is surrounded by three filtering cavities. Three pairs of the previously mentioned p-i-n-diodes are soldered in the routing cavity for the switching process between different operational states.

The simulated and measured S-parameters of the fabricated filtering SIW-routing switch are shown in Fig. 25 for different operational states. For an ON-state, state 1 is discussed in Fig. 25(a). A channel is created between ports 1 and 2 with a resonant frequency of 7.7 GHz. An insertion loss of 2.98 dB is measured (including the losses of the two filtering cavities of the channel). Furthermore, the created channel is isolated from the third port (port 3) with a 30 dB measured ON-state isolation level. Moreover, the measured reflection coefficients of the channel's ports are 26.6 dB, while the isolated port has a measured reflection coefficient of 8.4 dB (unmatched). In addition, the zero state (OFF-state) is shown in Fig. 25(b). The SIW-routing switch has a measured OFF-state isolation of 31 dB. Also, all ports have unmatched measured reflection coefficients of 4 dB. A slight frequency shift between ON and OFF states is realized due to the added ON-state capacitance of the p-i-n-diodes. This frequency shift has a minor effect on the operation of the fabricated SIW-routing switch.

The power handling capability of the fabricated SIW-routing cavity is evaluated using the setup shown in Fig. 26(a). The channel between ports 1 and 2 is examined (state 1), while a 25-W load is connected to port 3. A circulator with an 18 dB isolation is employed for protection purposes. As the level of

TABLE I
COMPARISON WITH STATE-OF-THE-ART SWITCHING TOPOLOGIES AND PRODUCTS

[Ref.]	Topology	Technology	f_0 (GHz)	ON-state active devices / channel	Iso. / IL (dB)	Switching speed (ns)	P_{max} (dBm)	Size
[20]°	SPDT	SIW Eva-cavity resonators	8	2 PIN-Diodes	18 / 1.6	T_{on}=39 T_{off}=76	N.A.	$0.5\lambda_g \times 0.5\lambda_g$
[19]	SPDT	SIW Eva-cavity resonators	1.953 - 2.782	6 Varactors - 4 Piezo	47 / 3.1-2.7	>1000	N.A.	N.A.
[23]	SPDT	Stub-loaded resonators	0.9 /1.9	3 PIN-Diodes	34.1 / 1.98	>100	N.A.	$0.45\lambda_g \times 0.22\lambda_g$
[24]	SP4T	Coaxial cavity resonators	2.37	2 PIN-Diodes	25.8 / 0.93	>100	N.A.	$0.52\lambda_g \times 0.2\lambda_g \times 0.51\lambda_g$
[9]	SPDT	Dielectric cavity resonators	1.861	2 PIN-Diodes	40 / 0.5	>700	> 49⋆	$0.61\lambda_g \times 0.46\lambda_g$
[25]	SPDT	Dielectric cavity resonators	1.831	2 PIN-Diodes	45 / 0.4	>700	> 49⋆	$0.79\lambda_g \times 0.7\lambda_g$
[26]	SPDT	Printed circuit board	1	2 PIN-Diodes	40 / 0.97	>100	> 40	$0.54\lambda_g \times 0.5\lambda_g$
[5]	SP4T	MEMS	0-13	N.A.	19-27 / 0.45-0.63	7.5×10^4	32	N.A.
[6]	SPST	Solid state	0-6	1 PIN-diode	37 / 0.42	> 700	51.46	N.A.
[7]	SP4T	MEMS	0-18	N.A.	13-26 / 0.34-1.7	2×10^5	33	N.A.
[8]	SPST	Solid state	0-18	N.A.	N.A. / 0.25-0.3	> 25	24	N.A.
This work-I	**DPDT**	**SIW Eva-cavity resonators**	**7.4**	**2 PIN-Diodes**	**26 / 2.95***	**T_{on}=39 T_{off}=76**	**40**	**$(0.5\lambda_g \times 0.5\lambda_g)$‡**
This work-II	**Routing**	**SIW Eva-cavity resonators**	**7.7**	**2 PIN-Diodes**	**30 / 2.98***	**T_{on}=39 T_{off}=76**	**40**	**$(0.5\lambda_g \times 0.5\lambda_g)$‡**

- Iso.: Isolation, IL: Insertion loss, TL: Transmission line, EVA: Evanescent, N.A.: Not available.
- ○ Our previous work.
- ⋆ Using high-power PIN-diodes.
- * Including losses of the filtering cavities.
- ‡ The size of the main switching cavities.
- For references with no measured switching speed, minimum switching speed has been mentioned based on the carrier lifetime of the used PIN-diodes.

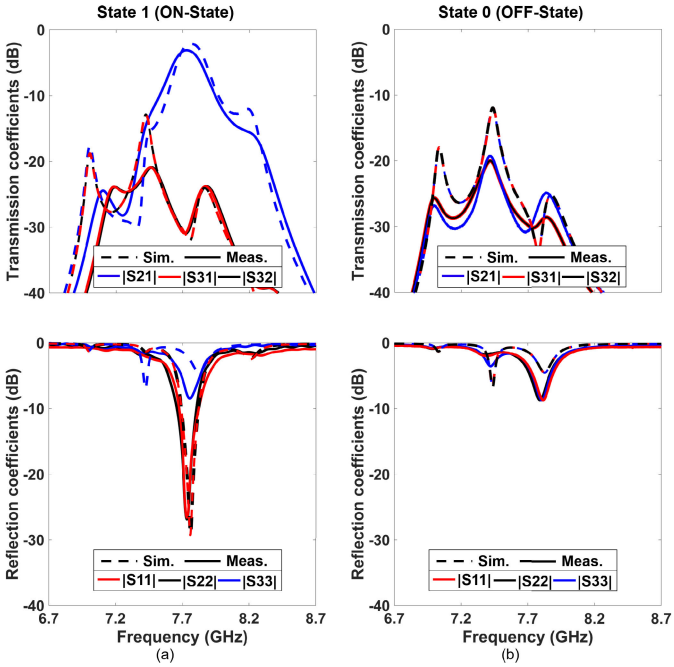


Fig. 25. Simulated and measured S-parameters of the fabricated filtering SIW-routing switch. (a) State 1 (ON-state). (b) State zero (OFF-state) (10 mA/−10 V are used to bias the p-i-n-diodes ON/OFF states).

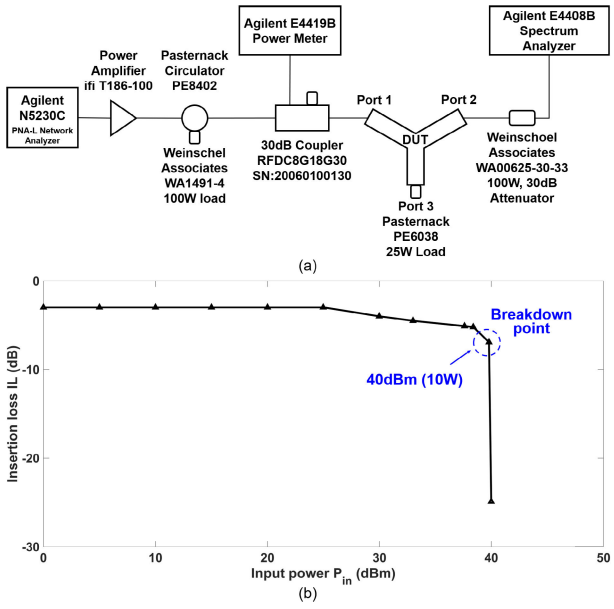


Fig. 26. Power handling measurements of the filtering SIW-routing switch. (a) Measurement setup. (b) Measurement result.

the input power to the tested device rises, the insertion loss increases until the device falls down at a certain point known as the breakdown point. As shown in Fig. 26(b), the fabricated SIW-routing switch can handle a measured high input power up to 40 dBm (10 W).

Table I shows a comparison between the proposed SIW switches with other state-of-the-art switching topologies and products. Our switching architectures have the highest measured switching speed compared to all other related works as demonstrated in [20]. The proposed work has a relatively high insertion loss because of the losses added by the filtering cavities. Although the switch products [5], [6], [7] have high levels of isolation and low levels of insertion loss along their frequency band, they have low switching speeds. The proposed switches have a low number of used ON diodes per channel and a reasonable circuit size. The high-power handling levels of the switches stated in [9] and [25] are the highest, as they use dielectric cavity resonators with high-power p-i-n-diodes. A moderate level of input power is handled by the proposed switches. Moreover, compared to other switching structures, the introduced work shows the most challenging switching

topologies. For the first time, a DPDT switch is implemented by using the SIW technology. Also, the proposed switching topology of the routing switch is implemented for the first time. As a proof-of-concept, the SPST switch [8], which is deployed in the proposed switches, has a high switching speed ($>$ 25 ns), but a low power handling of only 24 dBm.

V. Conclusion

Novel high-power filtering SIW switches with high switching speeds are presented. The first switching structure is a four-port DPDT switch with two operational states, each with two isolated channels. Also, a three-port routing switch with four operational states is introduced. An OFF-state, in which all ports are isolated from each other. Also, three ON-states where a channel is created between any two ports while the third one remains isolated. Circular SIW cavity resonators are used, a main switching cavity and filtering cavities at output ports. Switching between channels is realized in the main cavity by exciting two modes with the same resonant frequencies to achieve isolation. p-i-n-diodes are used to connect different capacitive posts in the main cavity of both SIW switches. Swapping the ON/OFF states of the p-i-n-diodes, variate the orientation of mode II, changing the positions of constructive and destructive summations of modes I and II. This creates the operational states of each presented SIW switch. The introduced switching cavities have a size of $0.5\lambda_g \times 0.5\lambda_g$ at the resonant frequency. For the SIW-DPDT switch, a 2.95 dB insertion loss is measured for all channels with a measured isolation level of 26 dB between them. Also, the channels of the SIW-routing switch exhibit a measured insertion loss of 2.98 dB and a measured isolation of 30 dB. A high-power handling of 40 dBm is measured for the routing cavity. Furthermore, this type of switching technique has a fast switching speed ($<$80 ns) as demonstrated in our previous work [20].

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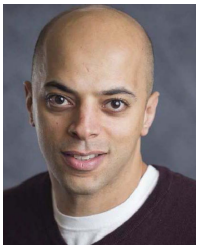
Kareem H. El-Gendy (Graduate Student Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the Electrical Engineering Department, Military Technical College, Cairo, Egypt, in 2019, where he is currently pursuing the M.Sc. degree.

His research interests include reconfigurable radio frequency (RF) front-end components based on high-Q cavity resonators.



Mohammad Abu Khater (Senior Member, IEEE) received the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2015.

He held several academic and industrial positions, including Senior Research Scientist at Purdue University. He is currently a Staff at Normal Computing, New York City, NY, USA. His research interests include adaptive and reconfigurable radio frequency (RF)/microwave/mmWave frontends, filters, impedance tuners, PAs, and interference detectors.

Dr. Abu Khater's research work received multiple recognitions including the WAMICON-2022 Best Paper Award and the MWCL's Most Significant Contribution in 2019. He is a Fulbright Alumnus and received the Excellence in Teaching Award from the College of Engineering, Purdue University.

Islam H. Abdelaziem (Graduate Student Member, IEEE) was born in 1993. He received the B.Sc. degree (Hons.) in electronics and communication engineering from the Electrical Engineering Department, Faculty of Engineering, Sohag University, Sohag, Egypt, in 2016, and the M.Sc. degree in electronics and communication engineering from the Electronics and Communication Engineering Department, Minia University, El-Minia, Egypt, in 2021. He is currently pursuing the Ph.D. degree at Purdue University, West Lafayette, IN, USA.

He has been with the Faculty of Engineering, Sohag University, since 2017, where he serves as an Assistant Lecturer with the Electrical Engineering Department. His research interests include metasurface-based antennas, dual-band, and multiband antennas, frequency reconfigurable antennas, polarization reconfigurable antennas, high gain antennas, gain enhancement techniques, microwave engineering, microwave filters and switches, and future 5G applications.

Mahmoud A. Abdalla (Senior Member, IEEE) was born in 1973. He received the B.Sc. degree (Hons.) in electrical engineering from the Electrical Engineering Department, Military Technical College, Cairo, Egypt, in 1995, the M.Sc. degree in electrical engineering from the Military Technical College in 2000, and the Ph.D. degree from the Microwave and Communication Group, School of Electrical Engineering, The University of Manchester, U.K., in 2009.

He has been with the Military Technical College since 1996, where he is now a Professor. He was the Head of the Electromagnetic Waves/Microwave Group, Electronic Engineering Department, the Electronic Engineering Department and the Council Committee Department, and the Electrical Engineering School. He has been a Visiting Professor with the Department of Computer and Electrical Engineering, University of Waterloo, Waterloo, ON, Canada, since 2017. He has published more than 250 peer-reviewed journals and conference papers. His research interests include miniaturized multiband antennas/wideband microwave/millimeter components, antennas with great attention to employing metamaterial/electromagnetic band gap (EBG), structures, electromagnetic multiple input multiple output (MIMO) antennas, energy harvesting systems, smart antennas, frequency selective surfaces, radar absorbers, and electromagnetic launchers.

Prof. Abdalla has been a Senior Member of Union Radio Scientifique Internationale / International Union of Radio Science (URSI) since 2020 and the European Microwave Association EuMA since 2011. He is a recognized International Authority at the Society of Electromagnetics. He served on the technical committee of many international conferences in the areas of electromagnetic/electronic and communication. He was a recipient of the Egyptian Encouragement State Prize Award for engineering sciences in 2014. In 2019, he was the recipient of the Egyptian El-Sherouq Innovation Award in electronic engineering. He was awarded the Top 1% Publon Worldwide Reviewer Award in 2018 and 2019. In 2020 and 2021, he was named in the Top 2% of Scientists in "A Standardized Citation Metrics Author Database Annotated For Scientific Field/Updated Science-Wide Author Databases of Standardized Citation Indicators." He is currently an Editor and a reviewer in many electromagnetic journals such as IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, IEEE TRANSACTIONS ON MAGNETICS, *IET Microwaves, Antenna and Propagation*, *IET Electronics Letters*, *IET Communications*, *Microwave and Optical Technology Letters*, *International Journal of Microwave and Wireless Technologies*, *Scientific Reports*, *AEU-International Journal of Electronics and Communications*, *Wireless Personal Communications*, and *Applied Physics*.

Dimitrios Peroulis (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2003.

From 2019 to 2023, he served as the Michael and Katherine Birck Head of ECE and a Special Adviser to the Dean of Engineering in online learning. He is the Senior Vice President (Online) at Purdue University, West Lafayette, IN, USA, where he is also the Reilly Professor of the Elmore Family School of Electrical and Computer Engineering. He has coauthored over 450 journals and conference papers. His research interests include reconfigurable systems, plasma radio frequency (RF) electronics, and RF-assisted lyophilization. He has been a key contributor to developing high-quality widely tunable filters and novel filter architectures based on miniaturized high-Q cavity-based resonators.

Dr. Peroulis received the National Science Foundation CAREER Award in 2008. He received the "Tatsuo Itoh" Award in 2019 and the Outstanding Young Engineer Award in 2014 from the IEEE Microwave Theory and Techniques Society (MTT-S). In 2012, he received the Outstanding Paper Award from the IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society (Ferroelectrics Section). His students have received numerous student paper awards and other student research-based scholarships. He has been a Purdue University Faculty Scholar and has also received 11 teaching awards including the 2010 HKN C. Holmes MacDonald Outstanding Teaching Award and the 2010 Charles B. Murphy Award, which is Purdue University's highest undergraduate teaching honor.

Mohamed F. Hagag (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and computer engineering from the Military Technical College, Cairo, Egypt, in 2007 and 2013, respectively, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2018.

From 2009 to 2014, he was a Research and Teaching Assistant with the Electronic Engineering Department, Military Technical College. From 2015 to 2018, he was with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, where he was involved in reconfigurable radio frequency (RF) front-end components based on high-Q cavity resonators. He is currently an Assistant Professor of electrical engineering with the Military Technical College.

Dr. Hagag was a recipient of the Egyptian Government Graduate Scholarship, the Best Conference Paper Award from the IEEE 19th Wireless and Microwave Technology Conference (WAMICON), Clearwater, FL, USA, in 2018, and the Third Place Award from the RF Tunable Filter Student Design Competition of the 2018 IEEE Microwave Theory and Techniques Society (MTT-S) International Microwave Symposiums. He is a reviewer in many electro-magnetic journals such as IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.