A *W*-Band Transmitter for Automotive Radar Sensors in 28-nm FD-SOI CMOS

Giuseppe Papotto, Alessandro Parisi, Alessandro Finocchiaro, *Member, IEEE*, Claudio Nocera, Andrea Cavarra, Alessandro Castorina, and Giuseppe Palmisano, *Senior Member, IEEE*

***Abstract*— This article presents a 77-GHz transmitter (TX) in a 28-nm fully depleted silicon-on-insulator CMOS technology for automotive radar applications. The circuit has been designed to simultaneously fulfill both short-/medium-range (S/MR) and long-range (LR) operations. It exploits an LO frequency doubling architecture, which allows preventing voltage-controlled oscillator (VCO) pulling effects for improved phase noise (PN) performance. The proposed TX comprises a 38-GHz VCO driving a frequency doubler and then a current-combining two-path power amplifier. The VCO takes advantage of a novel tank architecture to cope S/MR and LR requirements with an effective and silicon area-saving solution. The proposed TX also features a feedback loop that allows properly setting the power delivered to the output load. It exhibits a 5-GHz bandwidth, ranging from 76 to 81 GHz, with a PN performance as low as −93 dBc/Hz at a 1-MHz offset frequency from a 77-GHz carrier. It is also able to deliver a maximum output power as high as 17.5 dBm with a dynamic control range of around 13 dB. The overall power consumption is 351 mW.**

***Index Terms*— CMOS mm-wave transmitter (TX), electromagnetic (EM) simulations, frequency doubler, integrated transformer, voltage-controlled oscillator (VCO).**

I. Introduction

AUTONOMOUS driving systems may drastically reduce car accidents, preventing injuries and ultimately saving human lives. Typically, such systems exploit different kinds of sensors (e.g., lidar, radar, video, infrared, and acoustic) as shown in Fig. 1, which are aimed at monitoring the environment surrounding the vehicle and hence properly control its motion [1].

The *W*-band radar sensor is an enabling technology for the implementation of effective self-driving systems due to its inherent robustness to environmental interference such as poor light, extreme temperature, and weather condition, which make it irreplaceable. According to the coverage area, radar sensors can be grouped into two categories, namely, short-/medium-range (S/MR) and long-range (LR) sensors.

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Giuseppe Papotto, Alessandro Parisi, Alessandro Finocchiaro, Claudio Nocera, Andrea Cavarra, and Alessandro Castorina are with STMicroelectronics, I-95121 Catania, Italy (e-mail: giuseppe.papotto@st.com; alessandro.parisi@st.com; alessandro.finocchiaro@st.com; claudio.nocera@st.com; andrea.cavarra@st.com; alessandro.castorina@st.com).

Giuseppe Palmisano is with DIEEI, Università di Catania, I-95125 Catania, Italy (e-mail: giuseppe.palmisano@unict.it).

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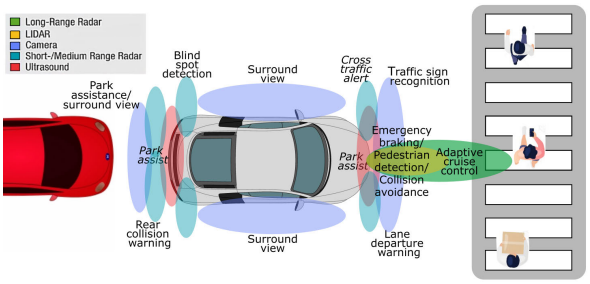


Fig. 1. Typical autonomous driving system configuration.

The former provides a detection range of a few meters but with a resolution of tens of centimeters, whereas the latter must provide a coverage area of more than 250 m but with a less stringent resolution requirement with respect to their S/MR counterpart. Recently, research efforts have been addressed to embed S/MR and LR functionalities into the same device to reduce size and costs. However, this translates into stringent requirements for both the receiver (RX) and transmitter (TX) side of the radar sensor. Specifically, S/MR sensors demand for a local oscillator (LO) with a wide tuning range (TR), besides very high linear RX. Conversely, addressing LR applications calls for both high transmitted power and very low phase noise (PN) [2]. Commercial radars take advantage of advanced SiGe BiCMOS technology platforms that enable the integration on a single chip of radar sensors, including mm-wave radio front end, analog baseband, analog-to-digital converter (ADC), and digital interface [3]. However, nanometer CMOS technologies are now able to provide also high-speed digital processing and nonvolatile memories, thus resulting in the best candidates for the system-on-chip (SoC) implementation of high-performance *W*-band sensors [4], [5], [6]. Nevertheless, most of the recently reported CMOS radar implementations are targeted to S/MR applications and therefore are far from simultaneously addressing LR radar requirements [7], [8].

In this work, a 77-GHz TX in a 28-nm fully depleted silicon-on-insulator (FD-SOI) CMOS technology is presented, which can cope with both S/MR and LR applications. The TX includes a 38-GHz voltage-controlled oscillator (VCO), a frequency doubler, and a 77-GHz two-path power amplifier (PA). It also features a feedback loop that allows setting the power delivered to the output load according to the addressed application. This article is organized as follows. Section II deals with the description of the adopted architecture. A detailed circuit design is presented in Section III and

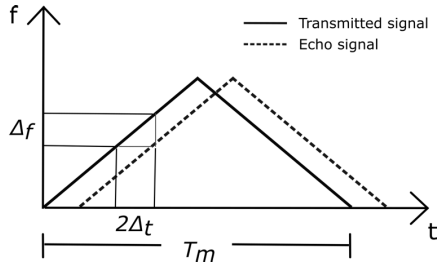


Fig. 2. FMCW radar operating scheme.

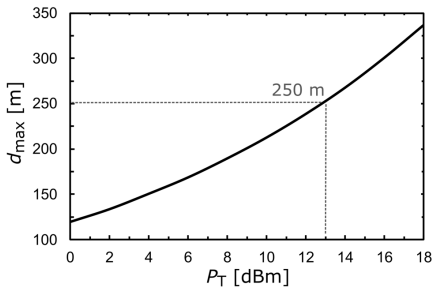


Fig. 3. Operating distance, $d_{\max}$, as a function of the required transmitted power, P_T, according to (2).

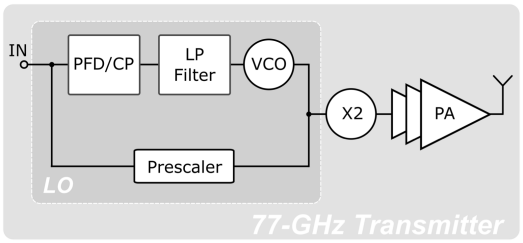


Fig. 4. Simplified block diagram of the proposed 77-GHz TX.

measurements are extensively discussed and compared with the state of the art in Section IV. Finally, conclusions are drawn in Section V.

II. System Description

Automotive radar sensors usually exploit a frequency-modulated continuous-wave (FMCW) operating scheme. Therefore, they continuously transmit a linear frequency-modulated signal, whose detection is performed by receiving the echo reflected by the target.

As shown in Fig. 2, the time of flight of the transmitted signal, Δt (i.e., the time it takes to get the target) and ultimately the distance d between sensor and target, can be drawn by measuring the frequency difference, Δf, between the transmitted and echo signals. Specifically, the distance d can be expressed as

$$d = \frac{cT_m}{4B}\Delta f \tag{1}$$

where B and T_m are the modulation bandwidth and period of the transmitted signal, respectively, and c is the speed of light. As apparent, the radar resolution, namely, the minimum detectable distance $d_{\min}$, is inversely proportional to the bandwidth B. Therefore, improving the radar resolution calls for a higher and higher modulation bandwidth. In modern automotive radar systems, T_m and $\Delta f_{\min}$ (i.e., the minimum detectable frequency difference) are typically set to 10 μs and 100 kHz, respectively. Consequently, the 10-cm resolution targeted by S/MR applications translates into a modulation bandwidth requirement, and ultimately a VCO TR, as high as 4 GHz.

Conversely, LR applications demand for the extension of the maximum detectable distance, $d_{\max}$, which is basically set by the RX sensitivity, S_{RX}, and the transmitted power, P_T. Of course, at a given P_T, the echo signal level at the RX input rapidly drops out, while the distance between the target and the radar sensor increases. Therefore, the lower is P_T, the higher should be the RX sensitivity to extend the radar coverage area. For the next generation of automotive radar sensors, a sensitivity as low as -110 dBm has been targeted, which imposes a stringent requirement for both the RX noise figure (NF) and the VCO PN. Specifically, assuming an RX NF of around 11 dB, the targeted RX sensitivity demands a VCO PN lower than -90 dBc/Hz at a 1-MHz offset frequency from the 77-GHz carrier [1], [9].

As mentioned above, the radar coverage area also depends on the transmitted power. Indeed, as well known from the radar theory [10], $d_{\max}$ can be expressed as follows:

$$d_{\max} = \sqrt[4]{\left(\frac{\sigma G_T G_R \lambda^2}{(4\pi)^3 L_{\text{ATM}}}\frac{P_T}{S_{\text{RX}}}\right)} \tag{2}$$

where G_T and G_R are the gains of the transmitting and receiving antennas, respectively, λ is the signal wavelength, L_{ATM} is the atmosphere propagation loss, and σ is the radar cross section of the target. The atmosphere loss at 77 GHz is around 0.3–0.5 dB/km, and the radar cross section for a mid-size car is assumed to be 30 m^2, whereas the receiving and transmitting antenna gain are typically around 20 dBi [9]. Fig. 3 reports $d_{\max}$ as a function of P_T for S_{RX} set to -110 dBm. As apparent, a transmitted power as high as 13 dBm is required to achieve an operating range higher than 250 m.

Unfortunately, since the PA output power is affected by the package insertion loss besides suffering from process, voltage and temperature (PVT) variations, the power constraint for the PA is much more severe than predicted from (2). Indeed, although radar sensors usually exploit custom advanced flip-chip assembly techniques, a package insertion loss of around 1 dB must be considered in the PA power budget. Furthermore, the output power exhibits a typical 3-dB additional reduction due to PVT variations. Therefore, the output power should be higher than 17 dBm to cope with LR applications. As far as the architecture is concerned, W-band radar sensors usually adopt a direct conversion scheme that guarantees high integration level and low power consumption. However, because of the zero offset between the frequencies of the LO and the transmitted signal, the LO can be affected by the PA output signal. Actually, due to the limited substrate isolation, especially at mm-wave, the PA signal may leak into the VCO, thus corrupting the LO spectrum.

To overcome this limitation, a frequency-doubled architecture is used in this work, as shown in Fig. 4. Therefore, the LO provides a carrier at half of the operating frequency, i.e.,

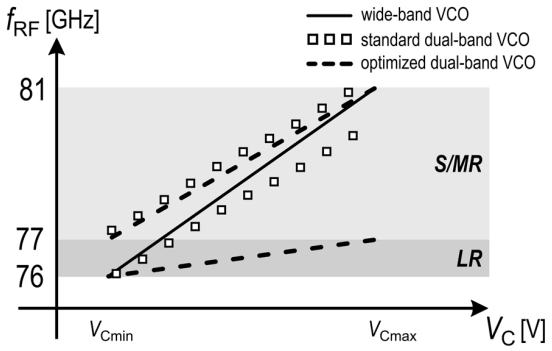


Fig. 5. TR for different tuning approaches.

around 38 GHz, and a frequency doubler is used to drive the PA with the 77-GHz carrier. This avoids the VCO frequency pulling, thus improving the PN performance.

III. Circuit Design

The proposed TX was designed in a 28-nm FD-SOI CMOS technology, which provides 1-V low-V_t transistors and has a low-cost standard back end of line (BEOL) [11]. The lack of dedicated thick-copper metal layers, typically available in mm-wave customized technologies, makes crucial passive component design and layout arrangements (e.g., signal paths, power supply, and ground interconnections), which greatly affects the TX performance. Therefore, extensive electromagnetic (EM) simulations were carried out to drive the design of passive networks while carefully considering undesired parasitic effects.

A. VCO Design

The VCO is the very bottleneck for the implementation of a radar sensor embedding S/MR and LR features. Indeed, simultaneously achieving low PN and wide TR is a nontrivial task, especially at mm-wave frequencies. Nevertheless, designing a VCO able to address both S/MR and LR applications is mandatory to reduce production costs. To this aim, a wideband VCO is typically used [12], [13], [14], which relies on a single varactor to cover both LR and S/MR subbands, as shown in the solid line in Fig 5. Although this approach can guarantee the required TR, it is not suitable to fulfill the PN requirements of LR applications due to the high conversion gain of the varactor (k_{VCO}). Indeed, the higher k_{VCO}, the worse the PN performance due to a higher AM-to-phase modulation (PM) conversion [15]. Actually, wide TR and low PN are not to be simultaneously provided. Indeed, LR applications exploit a small band typically ranging from 76 to 77 GHz (i.e., low TR requirement), where stringent PN performance is to be achieved to guarantee an operating range up to 250 m. Conversely, S/MR applications use a wider band extending from 77 to 81 GHz to get a resolution of a few centimeters, but they have a relaxed PN requirement. Therefore, a dual-band VCO would be the best option to cope with both S/MR and LR applications. The basic idea is to implement a dual-band operation based on a couple of varactors to cover the two targeted subbands, being the size of such varactors as small as possible, as shown in Fig. 5 (dashed lines). Consequently, k_{VCO} in the lower band would be considerably reduced, thus improving PN performance, while a wide TR in the upper band would be simultaneously achieved.

Nevertheless, at the state of the art, dual-band operation is typically achieved by means of *LC* VCOs with switched components, such as switched capacitor (SC) [16], switched inductor (SL) [17], or switched core [18], as schematically shown in Fig. 6(a)–(c), respectively. SC- and SL-based VCOs exploit a shunt switch, SW, to enable/disable either a capacitor or an inductor. This allows the tuning curve to be properly shifted to cover both the lower and upper bands, as shown in Fig. 5 (squared lines), but without a substantial reduction of k_{VCO} between the two configurations. Indeed, such solutions adopt a varactor, C_V, that is sized to cover the wider TR, namely, that one related to the upper band. Consequently, the varactor turns out to be oversized for the operation in the lower band (i.e., the LR band), which results in a high k_{VCO} and hence poor PN performance. Moreover, the switch SW provides a nonnegligible contribution to both resistive losses and parasitic capacitance of the VCO tank, thus affecting PN besides limiting the maximum VCO operating frequency. Conversely, switched-core VCOs take advantage of two different VCOs with optimized *LC* tank. Therefore, the lower and upper bands are merely covered by enabling the related core, which relies on a dedicated properly sized varactor (C_{V1} or C_{V2}). This allows fulfilling PN requirements of the lower band while guaranteeing a wide TR in the upper band, but at the cost of both a large silicon area occupation and higher system complexity.

To overcome these limitations, a novel dual-band VCO is proposed [19]. It consists of a single-core cross-coupled VCO operated at 1-V supply voltage for reduced power consumption. It features an *LC* tank with a couple of varactors, C_{V1} and C_{V2}, which are alternatively enabled by means of switches, SW and $\bar{SW}$, as shown in Fig. 6(d). The basic idea is to use the enabled varactor C_{V1} (C_{V2}) to cover the lower (upper) band, whereas the disabled varactor C_{V2} (C_{V1}) acts as a fixed capacitor, allowing the tuning curve to be properly shifted. For the sake of completeness, varactor and switch configurations for both S/MR and LR mode operation are shown in Fig. 7(a) and (b), respectively. Fig. 7(c) shows the varactor normalized equivalent capacitance as a function of the control voltage, V_C. Note that, according to the selected subband, V_C is applied to the varactor that must be operated as a variable capacitance, namely, C_{V1} for LR mode or C_{V2} for S/MR mode. At the same time, the varactor that must be acted as a fixed capacitance, namely, C_{V2} for LR mode or C_{V1} for S/MR mode, is connected to the dc voltages, V_{B2} or V_{B1}, respectively. Specifically, in the lower band, the fixed contribution, C_{V2}, must provide a large capacitance, and consequently, V_{B2} is set to 150 mV. Conversely, in the upper band, C_{V1} must provide a small capacitance, and hence, V_{B1} is set to 850 mV. Due to this approach, the tuning varactor, i.e., the varactor that sets the TR for each subband and, hence, the related capacitance variation, is as small as possible, as shown in Fig. 7(c). This translates into a substantial reduction of the k_{VCO} in the lower band, which improves the PN performance, while still guaranteeing a

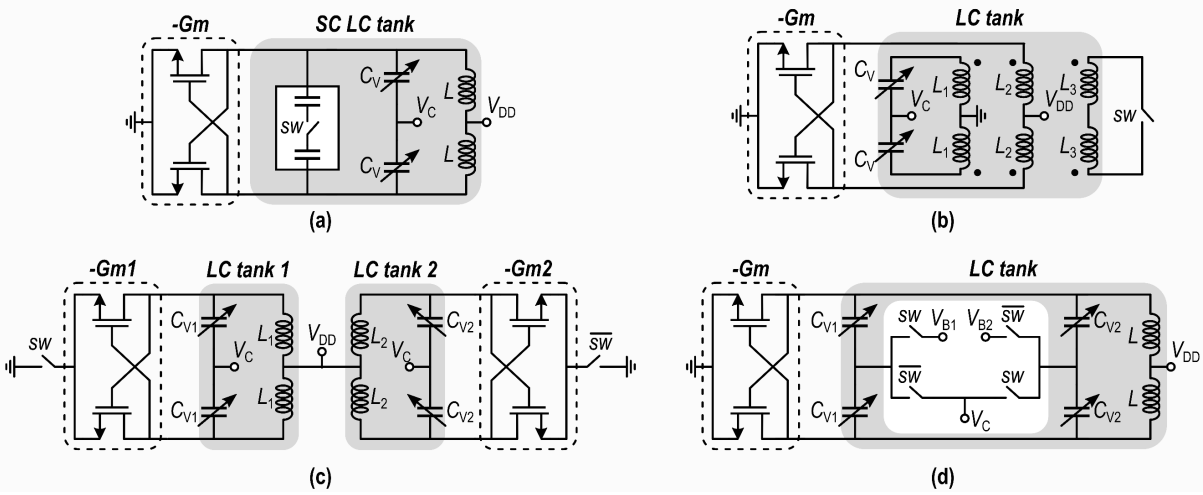


Fig. 6. Simplified schematic of dual-band VCO. (a) Switched-capacitor based. (b) Switched-inductor based. (c) Switched-core based. (d) Proposed.

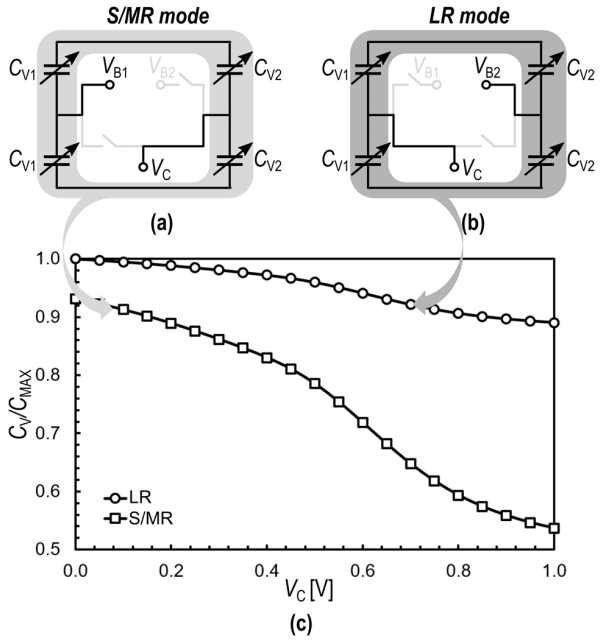


Fig. 7. Switch configuration for (a) S/MR and (b) LR operation, and (c) varactor normalized equivalent capacitance as a function of the control voltage.

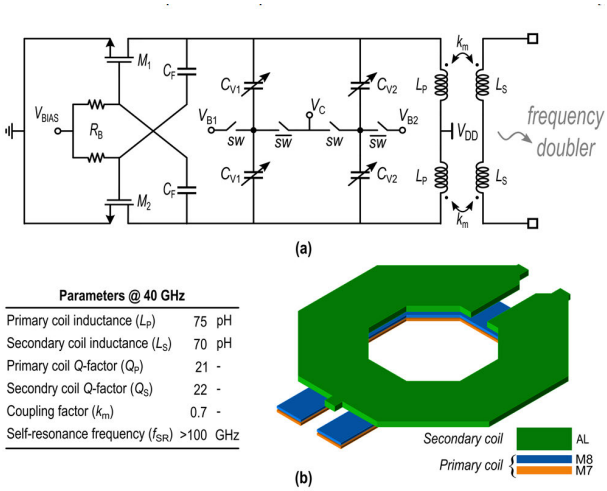


Fig. 8. Proposed dual-band VCO. (a) Completed schematic. (b) 3-D view of the transformer with the adopted metal stack and its main parameters.

wide TR in the upper band. Furthermore, it is worth noting that the band-selection switches are located at the common-mode node of the VCO tank. Therefore, they have negligible impact on the PN performance and no impact on the VCO maximum operating frequency, and this ultimately greatly relaxes the switch design. The full schematic of the proposed VCO is sketched in Fig. 8(a). It is based on an nMOS topology with transformer-coupled tank. The transformer allows increasing the equivalent load provided to the VCO active core, thus reducing the current consumption while simultaneously lowering the parasitic capacitance coming from the secondary side [20]. The VCO active core consists of a cross-coupled differential pair, $M_{1,2}$, which is operated in D-class with the aim of improving PN performance by maximizing oscillation amplitude [21]. Accordingly, transistors $M_{1,2}$ are large to be operated as switches and to reduce the corner of the flicker noise, thus improving VCO PN at low offset frequency. Their channel width and length were set to 28 μm and 45 nm, respectively. AC coupling was preferred to implement the feedback path in the VCO active core since it allows the bias voltage, V_{BIAS}, of transistor $M_{1,2}$ to be set to trade off startup condition and power consumption.

As far as the tank transformer is concerned, a 3-D view along with the adopted metal stack and main electrical parameters is shown in Fig. 8(b). The transformer adopts single-turn octagonal windings with a stacked configuration, whose inner diameter is 46 μm, while the metal width for primary and secondary coils is 16 and 25 μm, respectively. The thicker and outermost metal layers of the BEOL were used to minimize both resistive losses and parasitic capacitances. Extensive EM simulations were carried out to design this transformer also including interconnections and supply/ground paths, with the aim of minimizing undesired parasitic effects.

B. Frequency Doubler Design

Frequency doubling is a core feature of the proposed 77-GHz TX since it allows preventing VCO pulling, thus improving the PN performance of the LO. Fig. 9 shows the

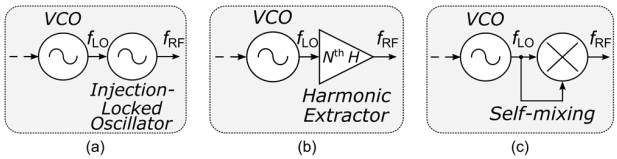


Fig. 9. Frequency doublers based on (a) subharmonic injection locking, (b) harmonic extraction, and (c) self-mixing.

main frequency doubler techniques at the state of the art. The injection-locked frequency doublers (ILFDs) exploit an auxiliary oscillator operating at a frequency, f_{RF}, which is twice the oscillation frequency, f_{LO}, of the main VCO, as shown in Fig. 9(a). Basically, frequency doubling is performed by injecting the main VCO output signal into the auxiliary oscillator to lock its oscillation frequency. Although effective, this technique calls for a very high signal level to be injected into the auxiliary oscillator to guarantee locking, which is a critical requirement, especially at mm-wave frequencies. Indeed, a power-consuming amplification chain is required between the VCO and the ILFD to guarantee robust operation [22]. Similarly, the harmonic-extractor doubler in Fig. 9(b) needs a high-gain amplification chain, tuned at f_{RF}, being $f_{RF} = 2 \times f_{LO}$, to selectively amplify the second harmonic of the VCO output signal. This ultimately allows frequency doubling to be performed but again with a complex and power-hungry solution, especially at mm-wave [23]. Self-mixing-based multipliers allow doubling the VCO oscillation frequency, f_{LO}, by means of a double-balanced Gilbert cell [24], as shown in Fig. 9(c). Specifically, by supplying both the LO and RF input port of the mixer with the f_{LO} signal, a differential doubled output signal is delivered at the IF port, but at the cost of very high silicon area occupation and power consumption. Conversely, the push–push frequency doubler in Fig. 10(a) can deliver a doubled high-level output signal with low power consumption. Therefore, this solution is widely used at mm-wave frequencies [25], [26], [27]. It basically consists of a transistor pair, $M_{1,2}$, in a common-source (CS) configuration, whose drain terminals are connected together. Transistors $M_{1,2}$ are driven by the LO signal and provide a common-mode RF output current, i_{RF}, whose fundamental frequency, f_{RF}, is twice f_{LO}. Finally, a transformer-based resonant load tuned at f_{RF} simultaneously performs current-to-voltage and single-ended-to-differential conversion, thus providing a frequency-doubled output voltage, V_{RF} [28]. Unfortunately, push–push frequency doublers are inherently single-ended circuits, and hence, they suffer from a high sensitivity to the impedance, Z_S, of the supply paths, namely, the routing paths used to locally deliver V_{DD} and GND to the circuit. The simulated amplitude of the output signal of the push–push frequency multiplier is shown in Fig. 10(b) as a function of f_{RF} for different Z_S. As apparent, the output signal is heavily affected by Z_S. Indeed, an equivalent impedance as low as 20 Ω, which is provided by a parasitic inductance of 40 pH, can drastically reduce the output signal amplitude at 77 GHz. Therefore, the supply path impedances should be carefully considered for a correct design of a conventional push–push frequency doubler. Unfortunately, keeping sufficiently low such impedances is a nontrivial task at mm-wave frequency,

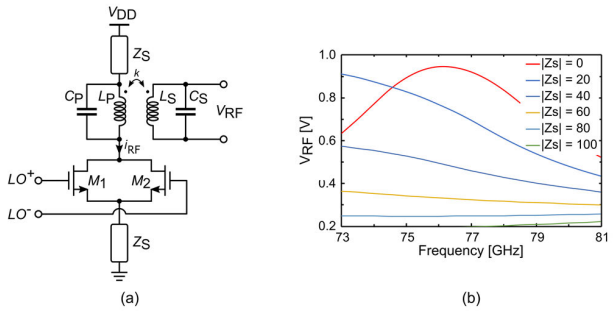


Fig. 10. (a) Simplified schematic of a push–push frequency doubler. (b) Simulated output voltage as a function of fRF for different values of Z_S.

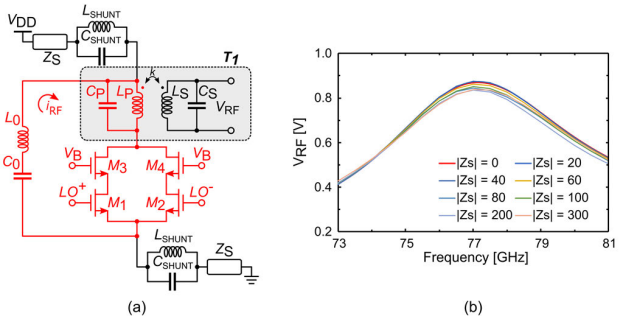


Fig. 11. (a) Simplified schematic of the proposed push–push frequency doubler. (b) Simulated output voltage for different values of Z_S.

and this issue is especially critical for high complex systems such as radar sensors, which typically feature multiple TX and RX on the same die. To overcome this limitation a novel push–push frequency doubler is proposed, which is almost insensitive to the impedance of the supply paths [29]. The simplified schematic of the proposed frequency doubler is reported in Fig. 11(a). It uses a cascode push–push pair M_{1-4} that drives the load resonant transformer. To prevent the output current, i_{RF}, from being affected by the supply paths, shunt resonators, $L_{SHUNT} - C_{SHUNT}$, are effectively used to decouple the inner circuitry from the supply path. Specifically, these resonators operate as dc-feed tuned at f_{RF}. Therefore, they provide the frequency multiplier with the supply voltages (i.e., GND and V_{DD}) while simultaneously offering a relatively high impedance path at f_{RF}. Finally, the series resonant bypass, $L_0 - C_0$, tuned at f_{RF} performs a low-impedance path for i_{RF} between the output load and the local GND, thus avoiding the current to flow through Z_S. This ultimately prevents the output load from being affected by Z_S. The simulated amplitude of the output signal for the proposed frequency multiplier is shown in Fig. 11(b) as a function of f_{RF} for different Z_S. As apparent, despite the inherent single-ended operation, the adopted solution is almost insensitive to Z_S. This greatly improves the circuit robustness, thus ultimately reducing the design effort. Moreover, the adoption of a cascode push–push pair leads to a higher conversion gain besides avoiding Miller amplification of gate–drain capacitances at the input.

Note that, the proposed, frequency doubler is meant to be operated with a supply voltage of 2 V. Therefore, the bias voltage, V_B, of the common-gate (CG) transistors, $M_{3,4}$, is properly set to simultaneously guarantee optimized frequency response and safe operating condition for the cascode pair. This is achieved by equally sharing the supply voltage

TABLE I
INDUCTIVE COMPONENT GEOMETRICAL AND ELECTRICAL PARAMETERS

Parameters	T_1	L_{SHUNT}	L_0	Units
Metal width	5.5	4	4	[μm]
Inner diameters (P/S)	44	34.5	34.5	[μm]
Coil inductance (P/S)	90	103	104	[pH]
Q-factor @ 77 GHz (P/S)	18/26	23	21	-
k @ 77 GHz	0.62	-	-	-

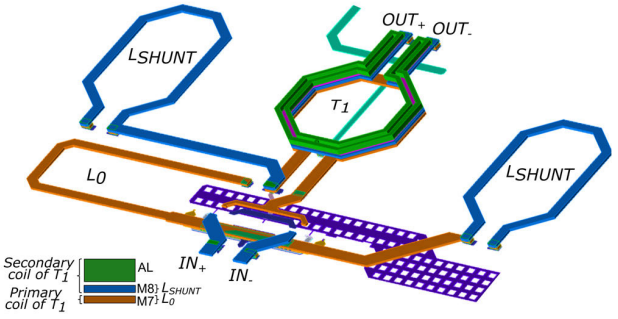


Fig. 12. 3-D view of the passive circuitry of the frequency multiplier.

between the drain and source voltages of the stacked transistors $M_{1,3}$ and $M_{2,4}$. Incidentally, this also maximizes output voltage swing, thus allowing the PA to be properly driven. A minimum channel length was used for the implementation of the cascode pair for optimum frequency response, whereas the channel width was set to 12 μm for a fair tradeoff between conversion gain and power consumption. As far as the load transformer T_1 is concerned, a stacked topology was preferred since it guarantees the highest magnetic coupling coefficient, k, between transformer windings, which provides maximum power transfer and better area occupation with respect to interleaved structures. Finally, the folded configuration was used for the design of the inductors of the shunt, L_{SHUNT}, and series resonators, L_0, to allow circuit floor plan optimization. Indeed, folded inductors are highly area-saving with respect to traditional spiral inductors. For the sake of completeness, Table I summarizes the geometrical and electrical parameters of the adopted inductive components.

Finally, Fig. 12 shows the 3-D-layout view of the passive circuitry of the proposed frequency doubler, which includes inductors, transformers, and interconnections among components. This layout was used as the entry of the EM simulator to accurately account for both layout parasitics and undesired coupling effects.

C. PA Design

The PA is a key building block of the radar sensor since it sets the maximum distance at which a target can be properly detected. As mentioned above, achieving an operating distance as high as 250 m calls for a PA output power as high as 17 dBm. Unfortunately, this power requirement cannot be attained with single-path CMOS PAs, especially in a low-voltage scaled CMOS implementation [30], [31]. To overcome this limitation, a current-combining 2-V PA is used for this design. As shown in Fig. 13(a), it consists of a variable gain amplifier (VGA) that drives the PA presented in [32],

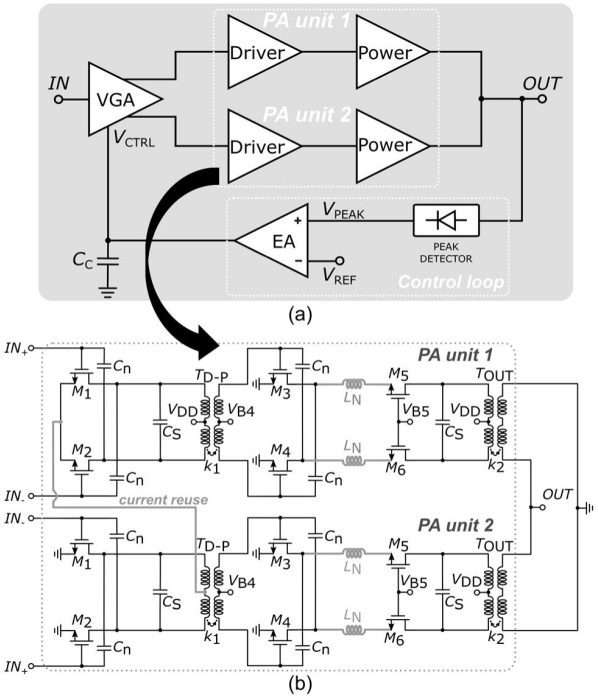


Fig. 13. Proposed two-path PA: (a) simplified block diagram and (b) schematic of the PA units.

which comprises two PA units arranged in a current-combining configuration to boost the power delivered to the output load. A feedback loop is also implemented to properly set the PA output power according to the targeted application.

Each PA unit includes a driver and power stage. As shown in Fig. 13(b), the driver stages, based on transistors $M_{1,2}$, adopt a CS topology and exploit a transformer-coupled current-reuse approach in which they share the same quiescent current, thus saving power and improving PA efficiency. Neutralization capacitors, C_n, are used to compensate for gate–drain capacitances of $M_{1,2}$. This results in a higher input and output isolation, which increases frequency stability and gain performance. The power stage of each PA unit, based on transistors M_{3-6}, adopts an enhanced-cascode topology in which series inductors L_N between the CS and CG stages are used to compensate for the overall parasitic capacitance in the interstage node. Moreover, inductors L_N perform an upward transformation on the real part of the input impedance of the CG transistors $M_{5,6}$, thus improving the output power transfer.

The two PA units are coupled to the external load through stacked transformers, T_{OUT}, which perform a current-combining structure, simultaneously providing impedance matching, power combining, biasing, and differential-to-single-ended conversion.

The two PA units are driven by a 77-GHz VGA, which allows the PA input power to be properly controlled, thus setting the PA output power. The simplified schematic of the designed VGA is shown in Fig. 14. It exploits a cascode differential topology with the CG stage implemented by two pairs of source-coupled transistors $M_{3,4}$ and $M_{5,6}$, whose drain terminals are connected to the supply voltage or to the output load. This allows delivering the output power either to the

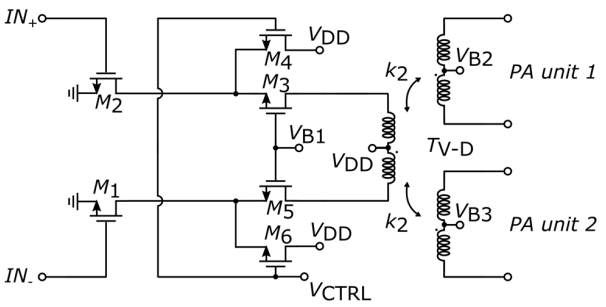


Fig. 14. Simplified schematic of the VGA.

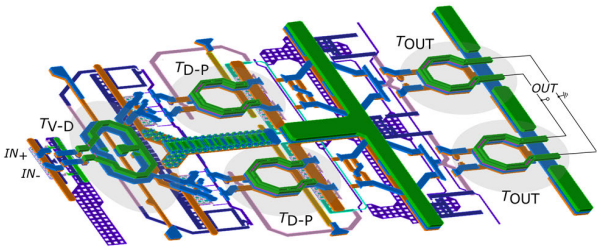


Fig. 15. 3-D view of the passive circuitry of the two-path PA.

two PA units or to the supply voltage according to the control signal, V_{CTRL}, applied to the gate terminals of $M_{4,6}$.

The VGA is loaded by a three-way transformer, T_{V-D}, which allows equally splitting the output power to drive the two PA units with the same input signal level. The VGA control voltage, V_{CTRL}, is properly set by the feedback loop shown in Fig. 13(a). It comprises a peak detector and an error amplifier (EA). The peak detector is made up of an ac-coupled common-drain stage [32], which provides a dc output voltage, V_{PEAK}, proportional to the PA output power. The EA compares V_{PEAK} with a reference voltage, V_{REF}, and sets accordingly the VGA control voltage, V_{CTRL}, which properly tunes the PA input power to deliver the desired power to the output load. Therefore, the PA output power can be set to address the specific S/MR and LR radar requirements by merely changing V_{REF}. Loop stability is guaranteed by capacitance C_C, which performs dominant pole compensation at the output of the EA. The simulated open-loop gain is around 50 dB with a 3-MHz bandwidth and a phase margin of around 70°.

The proposed PA is operated with a 2-V power supply. The bias voltages of the CG stages in the cascode structures of both the VGA and power stages (i.e., V_{B1} and V_{B5}, respectively) are set to equally split the supply voltage between the drain and source voltages of CS and CG stages, as in the frequency doubler.

Finally, extensive EM simulations of the PA passive circuitry from the VGA transformer to the power stages were carried out to accurately account for both layout parasitics and undesired coupling effects. An *s*-parameter model of this circuitry was extracted from the EM simulations and embedded into the main schematic entry to finely tune transistor aspect ratios and matching networks for the optimum PA performance. Fig. 15 shows a 3-D-layout view of this passive circuitry, which includes inductors, transformers, and interconnections among components. The main simulated electrical parameters of the PA transformers are summarized in Table II.

TABLE II
ELECTRICAL PARAMETERS OF TRANSFORMERS AT 77 GHz

	Inductance (pH)		k	Q	
	Primary	Secondary		Primary	Secondary
$T_{\mathrm{V\text{-}D}}$	110	110/110	0.55/0.55	15.5	13/13
$T_{\mathrm{D\text{-}P}}$, T_{OUT}	60	50	0.6	16	24

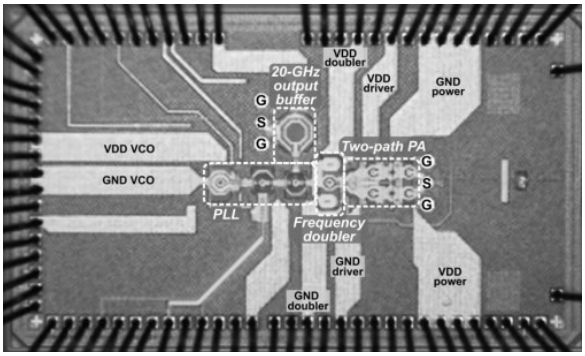
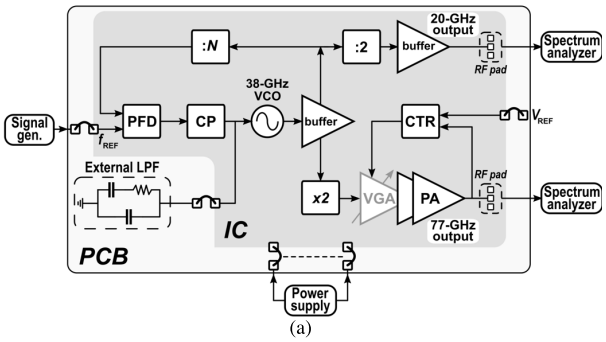
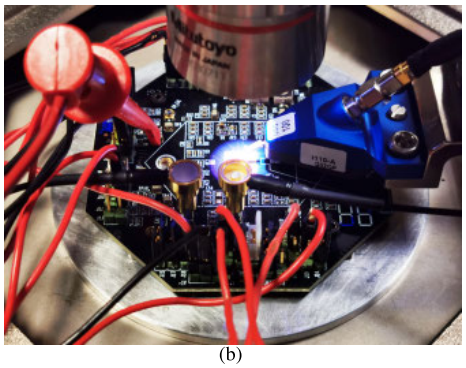


Fig. 16. Chip microphotograph of the TX.



(a)



(b)

Fig. 17. TX testing setup. (a) Simplified block diagram. (b) Photograph.

TABLE III
SUMMARIZED POWER CONSUMPTION AND SUPPLY VOLTAGES

Block	VCO	Doubler + PA	TX
P_{dc} (mW)	15	336	351
V_{DD} (V)	1	2	1/2

IV. EXPERIMENTAL RESULTS

The proposed 77-GHz radar TX was fabricated in a 28-nm FD-SOI CMOS technology by STMicroelectronics, which features a standard low-cost BEOL with eight copper metal layers plus an aluminum top one, and metal–oxide–metal (MOM) capacitors with a 5 fF/μm^2 of specific capacitance. A chip microphotograph is shown in Fig. 16.

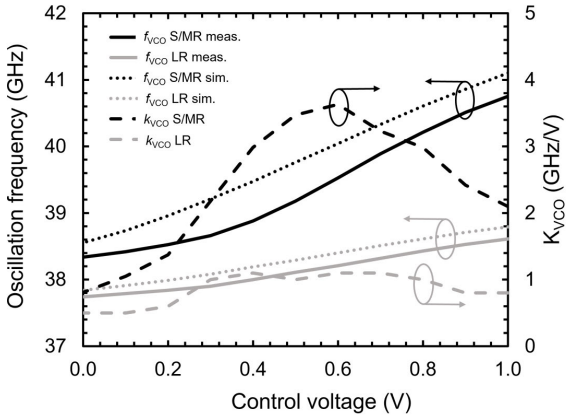


Fig. 18. VCO TR and k_{VCO}.

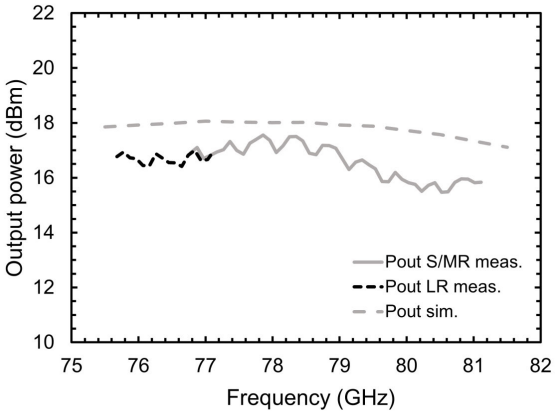


Fig. 20. TX output power as a function of frequency.

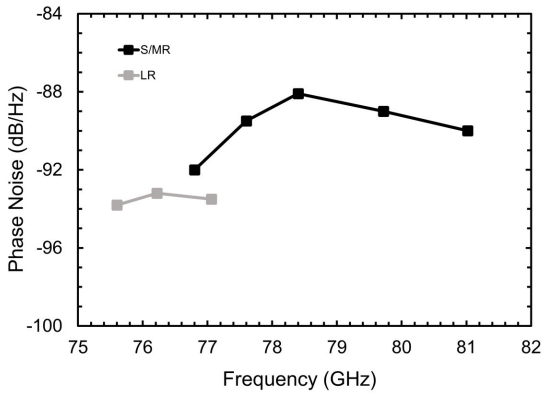


Fig. 19. Measured PN for S/MR and LR band at the 1-MHz offset frequency.

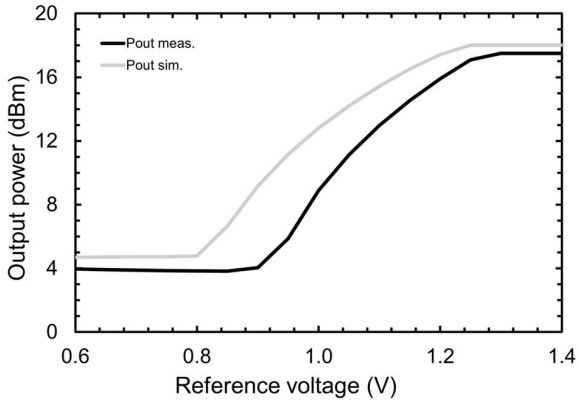


Fig. 21. TX output power as a function of the reference voltage.

The die area is pad limited for exhaustive testing purposes. The total area is 2.9 × 1.7 mm, whereas the core size is 1.1 × 0.3 mm, excluding testing circuitry (i.e., 20-GHz output buffer). A simplified block diagram and a photograph of the adopted measurement setup are shown in Fig. 17(a) and (b), respectively. The chip was assembled on an FR4 printed circuit board using the chip-on-board approach to allow wire bonding of low-frequency signals (i.e., bias terminals and control bits). Conversely, mm-wave signals are directly probed on die by means of a cascade probe station, using dedicated GSG on-chip pads, as shown in Fig. 17. Specifically, the TX provides two mm-wave outputs, namely, the 50-Ω PA output at 77 GHz and a 50-Ω output at 20 GHz, which is used for better VCO characterization. To this aim, the VCO was also embedded within an on-chip phase-locked loop (PLL) designed for testing purpose, which uses an off-chip 2nd-order low-pass filter (LPF). The integrated PLL is operated at 1-V supply voltage and adopts a frequency divider by 384 and a reference frequency of around 100 MHz. The measurement setup includes a spectrum analyzer and a signal generator as a PLL frequency reference. Fig. 18 shows the measured and simulated VCO TR and k_{VCO}. As apparent, a good agreement between measurements and simulations was achieved. The oscillation frequency ranges from 37.7 to 38.6 GHz and from 38.3 to 40.7 GHz in the lower and upper bands, respectively, with the varactor control voltage swept from 0 to 1 V. Due to the adopted VCO tank architecture, the peak value of k_{VCO} in the lower band (i.e., around 1 GHz/V) is about three times lower than that in the upper band (i.e., around 3.5 GHz/V), which means lower AM-to-PM noise conversion and hence better PN performance for LR applications. Moreover, the k_{VCO} variation over the TR is minimized, especially in the lower band, thus allowing constant PN performance. The VCO PN performance was measured by setting the PLL bandwidth as low as 20 kHz to make the VCO noise contribution dominant at the PLL output. Noise measurements were carried out at the 20-GHz output. The measured PN is about −105 and −100 dBc/Hz at the 1-MHz offset frequency for the lower and upper bands, respectively. This translates into a PN performance of −93 and −88 dBc/Hz in the lower and upper band, respectively, at the 1-MHz offset frequency from the 77-GHz carrier, as shown in Fig. 19. Due to the lower k_{VCO} in the lower band, a 5-dB PN improvement is achieved with respect to the one in the upper band.

As discussed, the VCO drives, through the frequency doubler, the two-path PA. The TX output power as a function of frequency is shown in Fig. 20. The TX can deliver a maximum saturated output power, P_{sat}, of 17.5 dBm at 78 GHz. The output power curve is almost flat over a wide frequency range. Specifically, it exhibits a variation of around 2 dB in the band of interest, ranging from 76 to 81 GHz. Moreover, simulations give a reduction of the saturated output power of around 1 dB at 125 °C. The operation of the power control loop is shown in Fig. 21, which shows the TX output power as a function

TABLE IV
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART 77-GHz TXs

Reference	Technology	Features	Frequency [GHz]	Modulation	P_{out} [dBm]	77-GHz PN @1MHz [dBc/Hz]	P_{dc} [mW]	P_{dc} / P_{sat}
[1]	65-nm CMOS	2-TX 3-RX	74.4÷84	FMCW	13.4	-87.4	254[3]	11.6
[5]	40-nm CMOS	3-TX 8-RX	76÷77	FMCW	14.1	-91	-	-
[6]	28-nm CMOS	2-TX 2-RX	78÷87	PMCW	10[1]	-92	410[4]	41
[16]	65-nm CMOS	1-TX	76.8÷77.95	FMCW	8.9	-91.2	117[3]	15.1
[33]	65-nm CMOS	1-TX	75÷81.3	UWB	14.5	-89.2	239[5]	8.5
[34]	65-nm CMOS	1-TX 1-RX	77÷81	FMCW	13	-91	-	-
[35]	65-nm CMOS	1-TX 1-RX	76.9÷78.8	FMCW	13	-81	187[5]	9.4
[36]	65-nm CMOS	2-TX 6-RX	75÷82	FMCW	13.7	n.a.[2]	381[6]	16.3
[37]	45-nm CMOS	3-TX 4-RX	76÷81	FMCW	12.1	-93	-	-
This work	**28-nm CMOS**	**1-TX**	**75.5÷81.5**	**FMCW**	**17.5**	**-93**	**351**	**6.2**

[1] with flip chip and module. [2] external LO source. [3] TX + PLL.
[4] PLL+LO buffer+1 TX. [5] PA+VCO+frequency multiplier. [6] PA+frequency multiplier.

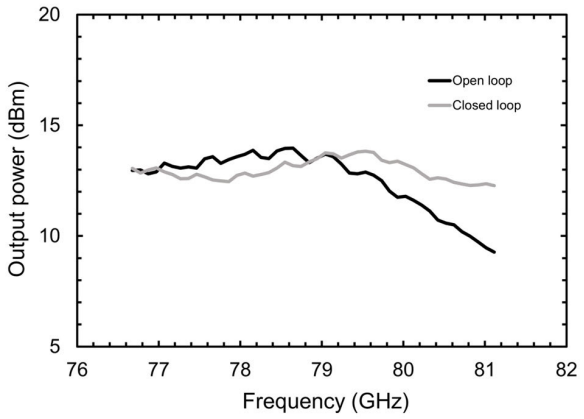


Fig. 22. TX output power in open- and closed-loop conditions.

of the reference voltage, V_{REF}, with the operating frequency of 78 GHz. An extended power range of around 13 dB is achieved, which allows properly addressing with the same device for both S/MR and LR applications that have very different requirements in terms of output power. Importantly, the power control loop is aimed at keeping the output power as flat as possible in the operating band, which is a challenging feature, especially for the S/MR applications. Fig. 22 shows the TX output power for both open- and closed-loop conditions for an output power level of 13 dBm. As apparent, the control loop allows quite flat output power over the operating band to be achieved.

Table III gives supply voltages and power consumptions of main building blocks as well as of the whole TX. The overall TX power consumption is 351 mW. Finally, Table IV summarizes the TX experimental results while comparing them with the state of the art of 77-GHz CMOS works. The proposed TX exhibits the highest saturated output power along with an excellent PN performance. A similar PN performance is reported in [6], which adopts a 16-GHz VCO and, hence, a higher frequency-multiplication factor. This solution increases the TR but at the cost of higher silicon area, due to the higher inductor required by the VCO tank. Moreover, the more complex frequency multiplier to provide the 77-GHz carrier further increases silicon area besides power dissipation. Therefore, the adopted frequency-doubling architecture turns out to be the best solution to trade off TX performance and power/area consumption. As a proof of this, the proposed TX exhibits the best P_{dc}/P_{sat} ratio (i.e., the minimum power consumption per output power) while guaranteeing a 5-GHz bandwidth.

V. CONCLUSION

This article presents a 77-GHz radar TX implemented in a 28-nm FD-SOI CMOS technology. The circuit has been designed to simultaneously fulfill both S/MR and LR applications. Starting from an integrated 38-GHz VCO, a frequency doubler provides the 77-GHz carrier that drives the current combining two-path PA. Despite the standard BEOL of the adopted technology, the proposed TX achieves an excellent saturated output power as high as 17.5 dBm and a PN performance as low as −93 dBc/Hz at the 1-MHz offset frequency from the 77-GHz carrier while covering 5 GHz of operating bandwidth.

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Giuseppe Papotto received the Laurea degree (cum laude) in electronic engineering and the Ph.D. degree in electronic and automation engineering from the University of Catania, Catania, Italy, in 2007 and 2012, respectively.

Since 2007, he has been with the Radio Frequency Advanced Design Center (RF ADC), a joint research center supported by the University of Catania and STMicroelectronics, Catania. In 2012, he joined STMicroelectronics, where he is currently the Design Manager of the RF-ADC with the Research and Development Department of the Automotive Discrete Group. He is involved in the design of mm-wave circuits and systems for automotive radar and 5G applications. He is the coauthor of around 20 papers in international journals and conference proceedings. He also holds several patents in the field of RF/mm-wave circuits. His research interests also include integrated RF energy harvesting systems and low-power transceivers for wireless sensor networks.

Alessandro Parisi received the M.S. degree (cum laude) in electronic engineering and the Ph.D. degree in systems engineering from the University of Catania, Catania, Italy, in 2015 and 2019, respectively.

Since 2014, he has been with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics, Catania, where he has been involved in the design of power and data transfer systems for both isolated sensors and gate driver applications. In 2019, he joined STMicroelectronics, where he is currently focused on the design of integrated RF/mm-wave circuits for automotive radar transceivers and 5G applications. His research activity also included the field of wireless sensor networks with an emphasis on ultralow-power reference circuits.

Alessandro Finocchiaro (Member, IEEE) received the Laurea degree in electronic engineering from the University of Catania, Catania, Italy, in 2006.

In 2006, he joined STMicroelectronics, Catania. He is currently a Senior RF and Analog Integrated Circuit (IC) Designer with the Radio Frequency Advanced Design Center (RF-ADC), a joint research group supported by the University of Catania and STMicroelectronics, Catania. He has been involved in the design and development of RF front ends, RF harvesters, and power management units integrated in different CMOS and BiCMOS technologies. Recently, he is active in the radar design team of the RF-ADC. He holds more than a dozen U.S. and European patents. His current research interests include RF-powered sensor nodes and ultralow-power transceivers for the next generation of wireless applications.

Claudio Nocera received the M.S degree in electronic engineering and the Ph.D. degree in systems engineering from the University of Catania, Catania, Italy, in 2017 and 2021, respectively.

Since February 2021, he joined STMicroelectronics, Catania. He is working with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics, where he has been involved in the design of mm-wave circuits for automotive radar systems with a particular emphasis on power amplifiers (PAs). His current research interests include the design and optimization of analog circuits in GaN technology for 5G applications up to mm-wave frequencies.

Andrea Cavarra received the M.S. degree (cum laude) in electronic engineering and the Ph.D. degree in systems engineering from the University of Catania, Catania, Italy, in 2018 and 2022, respectively.

Since November 2021, he has been with the Power Transistors Division, STMicroelectronics, Catania. He has been involved in the design of voltage-controlled oscillators (VCOs), frequency synthesizers, and building blocks for low-power radio frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs), for radar applications with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics. He is currently involved in the design of GaN RFICs for 5G applications.

Alessandro Castorina was born in Catania, Italy, in 1981. Since 2001, he has been with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania, Catania, and STMicroelectronics, Catania, as Senior Application Engineer. He has been involved in the characterization of silicon-integrated transceivers for cellular, W-LAN, ultrawideband, digital video broadcasting-satellite (DVB-S) applications, as well as mm-wave ICs for radar, harvesting, and organic semiconductor circuits. In the last years, he has also been involved in the characterization of galvanically isolated integrated systems.

Giuseppe Palmisano (Senior Member, IEEE) received the Laurea degree in electronic engineering from the University of Pavia, Pavia, Italy, in 1982.

From 1983 to 1991, he was a Researcher with the Department of Electronics, University of Pavia, where he was involved in CMOS and BiCMOS analog integrated circuit design. In 1992, he was a Visiting Professor with Universidad Autonoma Metropolitana (UAM), Mexico City, Mexico, where he taught microelectronics for Ph.D. students. In 1993 and 2000, he joined the Faculty of Engineering, University of Catania, Catania, Italy, as an Associate Professor and Full Professor, respectively, teaching microelectronics. Since 1999, he has been leading the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics, Catania. He has supervised the design of several innovative analog integrated circuits and systems within the framework of national and European research projects and in collaboration with electronic industries. He is the coauthor of more than 250 papers in international journals and conference proceedings, 60 international patents, and three books. His research interests lie in the area of analog integrated circuit (IC) design with special emphasis on RF applications. Presently, he is involved in integrated galvanic isolation interfaces in both GaN and BCD technologies for switching power converters and in GaN RF power amplifiers for 5G communications.

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