On-Chip Integration of Orthogonal Subsystems Enabled by Broadband Twist at 220–325 GHz

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***Abstract*— In this article, we report for the first time on a low-loss compact platform that enables the integration of H- and E-plane rectangular waveguide subsystems enabled by 90° polarization rotation of rectangular waveguide sections on a silicon-micromachined chip. The proposed platform offers unprecedented design flexibility for a 2.5D fabrication technology such as silicon micromachining, since orthogonal waveguide device sections with full design freedom in H-plane geometries can be cofabricated with sections with full design freedom in E-plane geometries, enabled by novel, integrated waveguide twists optimized for 2.5D fabrication. The platform is developed for use in broadband millimeter- and submillimeter-wave waveguide circuits and prototypes are implemented in the 220–325-GHz band. A prototype chip demonstrating the platform, implemented by bonding three stacked silicon chips, is fabricated. The measured results of the twist prototype exhibit a very low insertion loss of less than 0.2 dB and a return loss of 20 dB or better in most of the 220–325-GHz band. An integrated eighth-degree lowpass waveguide filter with axial ports having a cut-off frequency of 280 GHz is codesigned with the twist transition and fabricated on the platform to demonstrate its application. The filter shows 0.4-dB measured insertion loss and has a measured return loss in the passband of better than 14 dB.**

***Index Terms*— Lowpass filters (LPFs), measurement techniques, millimeter-wave and terahertz (THz) components, multilayer integration, silicon micromachining, underetching, waveguide filters, waveguide transitions, waveguide twists.**

I. Introduction

APPLICATIONS including next-generation high-data-rate communication, high-resolution radars, imaging, and terrestrial and space-borne remote sensing need microwave components in the subterahertz and terahertz (THz) frequency spectrum from 100 GHz to 10 THz [1], [2], [3], [4], [5]. The progress in THz electronics and these upcoming applications requires a fundamental shift from fabrication techniques used for low-volume scientific instrumentation toward volume-manufacturable THz devices and systems. Future THz manufacturing methods must support the cofabrication of THz systems with different orientations enabling the interconnection of subsystems on a single platform.

The highly advanced and robust deep-silicon micromachining processes, based on proven high-volume semiconductor manufacturing methods, enable the fabrication of micrometer-size features with a high-aspect ratio ideal for subterahertz and THz applications. It also enables low insertion loss due to the nanoscale roughness [6], [7], [8], [9].

Air-filled rectangular waveguides are the primary choice for THz circuits since they allow for low-loss signal routing [6]. The integration of silicon micromachined components and devices with conventional waveguide systems, and their characterization is still challenging. Traditional approaches, such as inserting the silicon chip into a CNC-milled test fixture [10], [11], [12] or using coplanar waveguide probes [13], [14], [15], [16], have numerous disadvantages, especially at sub-THz and THz frequencies, including sensitivity to misalignment, complex and expensive fabrication, radiation losses due to gaps between connectors, and parasitic coupling between probes. A silicon micromachined platform with axial waveguide interface, introduced in [17] to address these problems, enabled direct interconnection and characterization of H-plane waveguide circuits (here, H-plane waveguides refers to having the H-plane in-plane with the wafer surface, i.e., orthogonal to the direction of etching) integrated on a single chip, including narrowband bandpass filters with unparalleled fabrication accuracy. For bandpass filters, all the geometries defining their performance, such as cavity and inductive-coupling irises sizes, have the same waveguide heights and thus require a single etching step for their fabrication. However, for lowpass filters (LPFs) traditionally designed using cascaded sections of capacitive irises, their integration in a silicon micromachined H-plane waveguide circuit would require as many different etching steps as there are waveguide sections of various heights in a design, which makes the fabrication extremely complex. Alternatively, the required waveguide sections with various heights can be implemented using a single photomask if the waveguides are rotated by 90°, so their E-plane is normal to the direction of etching. However, the transition between the H- and E-plane waveguide subsystems requires a 90° polarization twist which is also designed for a 2.5D fabrication process and integrated into the silicon micromachined chip

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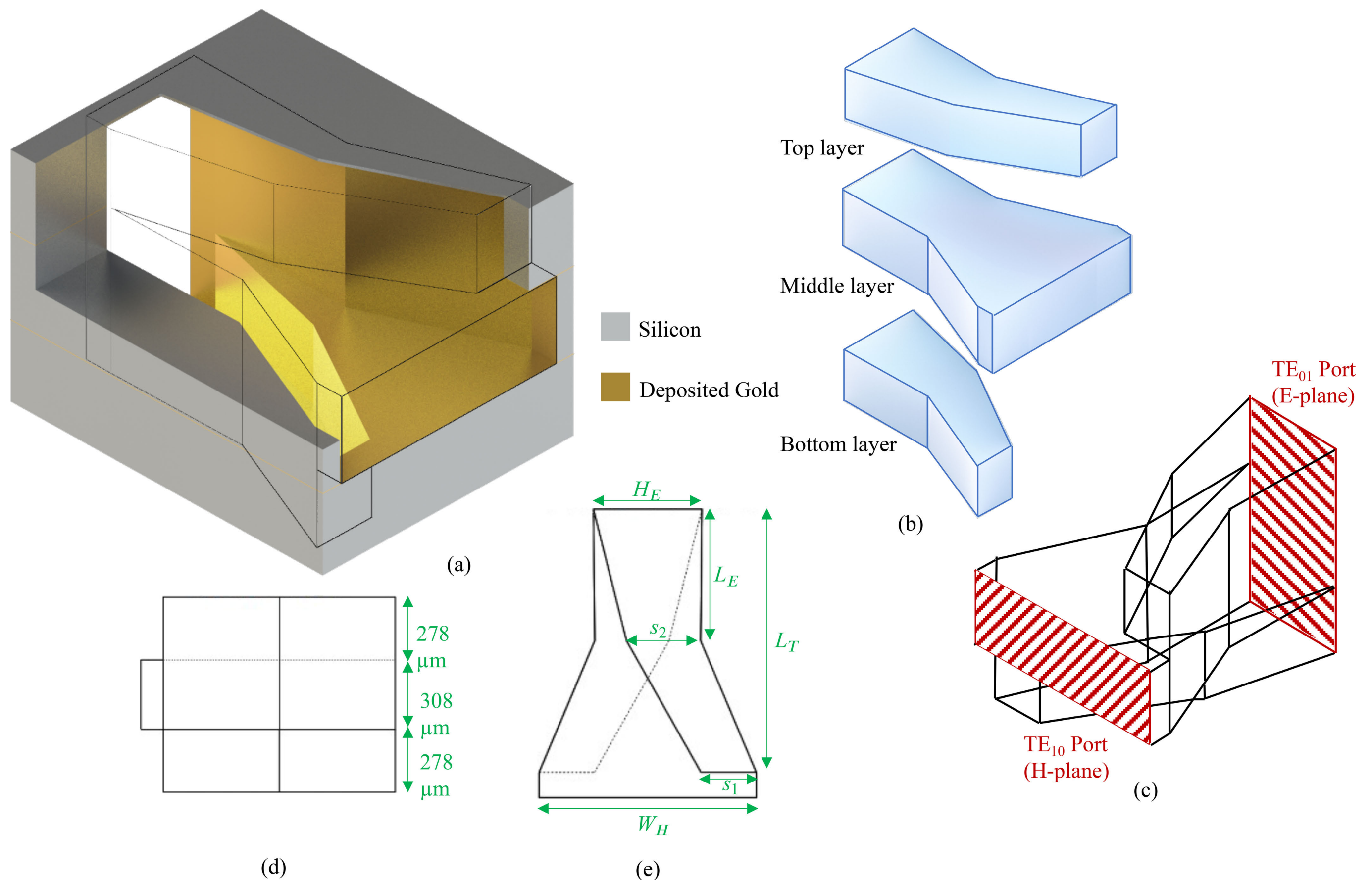


Fig. 1. Views of the proposed 90°-twist transition: (a) 3-D drawing of the twist located in a three-layer silicon-micromachined chip; (b) exploded view; (c) 3-D view with ports; (d) side view; and (e) top view with design variables.

TABLE I
DIMENSIONS OF THE PROPOSED TRANSITION (SEE FIG. 1)

Dimension	Value, µm	Dimension	Value, µm
L_T	1044	W_H	864
L_E	522	$s1$	295
H_E	432	$s1$	220

platform. Important properties of such a twist are wideband operation, low losses, and manufacturability.

Typically, two concepts are followed to design waveguide twists in rectangular waveguides: 1) gradual rotation [18], [19] and 2) a single [20], [21], [22], [23], [24] or multiple waveguide steps [25], [26], [27], [28]. Gradual or multiple-step rotations result in excellent matching, and thus a low return loss of as good as 30 dB can be achieved at the expense of elongated structures and fabrication complexity. A multiple-step waveguide twist can be implemented in one piece [25], [26] or by stacking discrete waveguide sections [27], [28]. The latter is rarely used at THz frequencies due to its stringent alignment requirement, which is critical at these frequencies.

THz frequencies demand precise manufacturing with tight tolerances. The CNC milling technique is still the standard fabrication technique. Recently, a considerable amount of THz CNC-milled waveguide twists has been reported. CNC-milled single-step twists are less bulky than continuous rotation implementations; however, tight tolerances are required [20], [21], [22]. Zeng et al. [25] introduce a CNC-milled twist transition with a return loss of 25 dB. The proposed transition at 220–325 GHz has a length of 1.469 mm and has been implemented using the multistep method. Chattopadhyay et al. [26] present a twist design for the same frequency band, which has also been implemented by CNC milling and has a geometry that would also be compatible with silicon micromachining. The twist is performed in several steps and is quite large, with a total length of 6 mm, which makes it unsuitable for compact on-chip systems.

This article presents a novel on-chip integrated full-band silicon micromachined rectangular waveguide 90° twist operating at subterahertz frequencies. The proposed twist provides on-chip interconnection of H- and E-plane waveguide subsystems in the same platform and allows larger device design freedom for the 2.5D fabrication techniques, including micromachining and computer numerical control (CNC) milling. The coexisting orthogonal waveguide subsystems combined on the same chip enable devices with complex geometries in E-plane and H-plane at a high level of integration, including the example of compact waveguide LPFs with axial chip-to-flange interfaces at sub-THz frequencies, as demonstrated in this article.

II. DESIGN AND TOLERANCE ANALYSIS

A. TE_{10}-to-TE_{01} Transition Design

Fig. 1(a) shows the proposed 90° twist, also referred to as a TE_{10}-to-TE_{01} transition, integrated on a multilayer

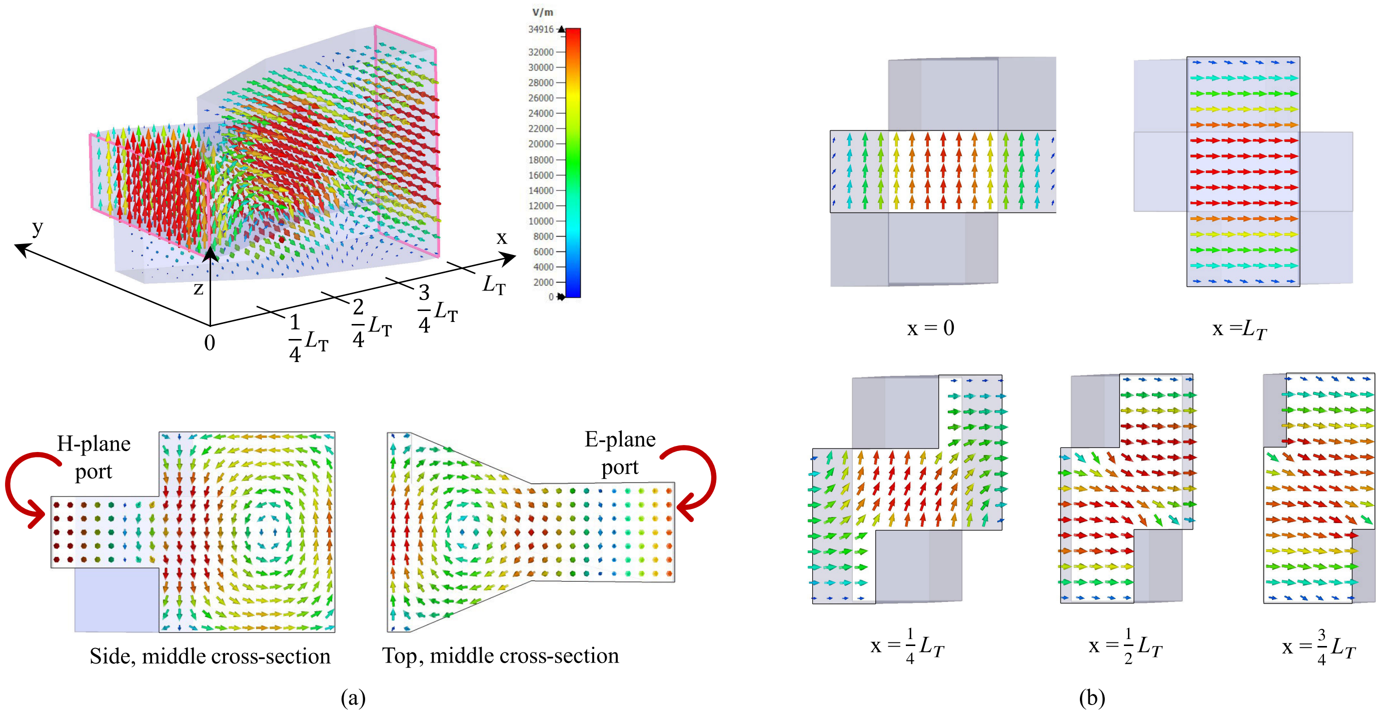


Fig. 2. Electromagnetic field distribution in the proposed transition at 280 GHz: (a) magnetic field distributions for the side and top cross sections in the middle and (b) electric field distribution at various transition's cross sections.

silicon-micromachined platform. The transition is designed by incrementally twisting the H-plane waveguide at the input by 90° to obtain an orthogonal orientation of the waveguide (E-plane waveguide) at the output, and the concept was adopted to be manufacturable by micromachining, taking into account fabrication imperfections such as the effect of underetching [29], while keeping the manufacturing complexity reasonable. The transition between the input and the output is created through a waveguide taper in the middle layer connecting the input and output directly, and by two extensions in the top and the bottom layer connecting to the E-plane waveguide, bent in opposed directions and shorted at the H-plane waveguide's input. The detailed geometrical dimensions of the implemented waveguide transition are shown in Fig. 1. To facilitate the fabrication, the structure uses only three gold-metalized silicon layers, which have been chosen as a tradeoff between the simplicity of manufacturing and the electrical performance of the transition. This three-layer structure consists of an input H-plane waveguide, supporting propagation of the TE_{10} mode in the middle layer, and an output E-plane waveguide that confines the TE_{01} mode in three layers.

The transition was optimized using a full-wave 3-D finite-element electromagnetic solver (CST microwave studio) for its four design parameters [$s1$, $s2$, LE, and LT; see Fig. 1(d)] to achieve more than 20 dB return loss throughout the entire 220–325-GHz frequency band.

Fig. 2 illustrates the distribution of the electric and magnetic fields inside the transition at various cross sections. The TE_{10} mode of the H-plane port twists along the transition and converts to the TE_{01} mode at the E-plane port and vice versa.

The E-plane waveguide port's width and height, and the H-plane waveguide's width are defined by the WM-864 standard (864 × 432 μm), while the H-plane waveguide's height is determined by the wafer thickness (308 μm). This decreased height does not have a major impact on the performance and design implication except for slightly increased losses. The E-plane waveguide port's width is determined by the triple-stack wafer thickness (864 μm). Utilization of a single wafer for manufacturing, the ability to achieve the standard width for the E-plane waveguide, and keeping the fabrication simple determined the H-plane waveguide's height. The dimensions are shown in Table I.

B. Performance and Tolerance Analysis

Underetching is a common fabrication phenomenon in deep reactive ion etching (DRIE) of large cavities, which, if left uncompensated, impacts the device's performance [8], [29]. Fig. 3 shows the return loss of the transition, including the influence of the nonverticality of sidewalls on the performance, for 0-, 10-, and 20-μm underetching. The underetching is avoided in the middle layer since it is manufactured using fall-out structures, resulting in close-to-zero underetching [23], but the extensional features located in the top and the bottom layers are inevitably affected by underetching, due to their large etching area.

Another performance-influencing factor is the misalignment of the stacked layers. Fig. 4 shows the influence of this effect on the return loss, with 20 random sample points for the misalignment between adjacent chip layers in the x- and y-directions, using a normal distribution with a standard deviation of 5 μm, for the three-layer structure. The

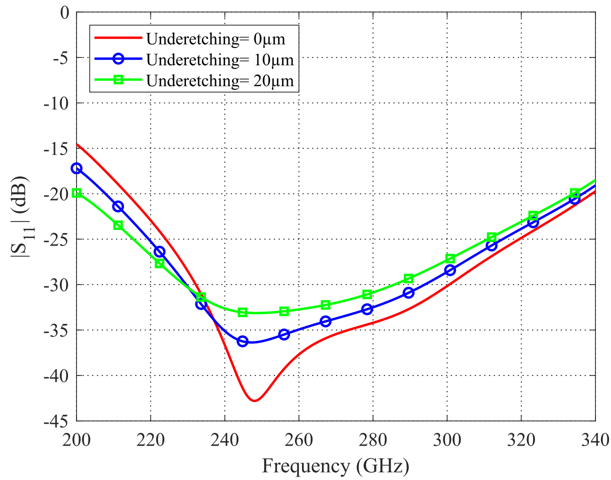


Fig. 3. Simulated return losses of the twist transition with different underetching values.

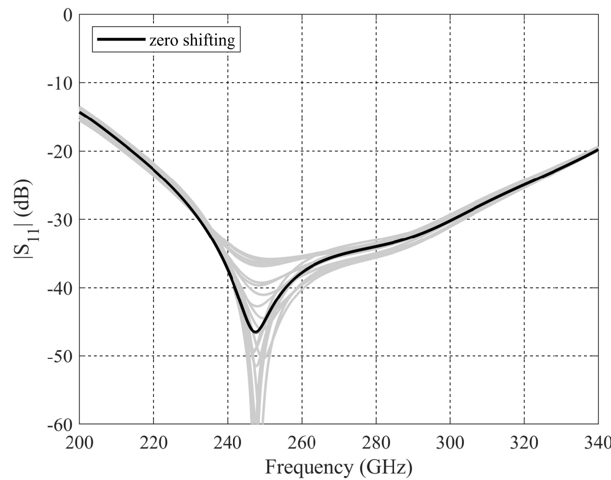


Fig. 4. Sensitivity analysis of the proposed TE_{10}-to-TE_{01} transition for chip misalignment. The gray curves represent the return loss of 20 random (normally distributed with a standard deviation of 5 μm in both directions) shifts between the chips in vertical and horizontal directions.

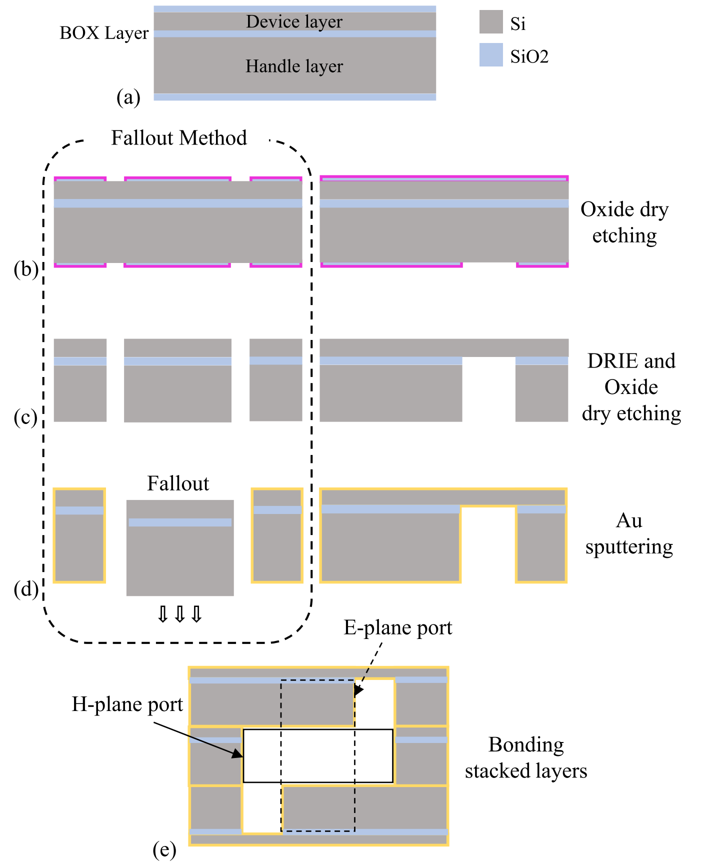


Fig. 5. Schematic fabrication process flow for fall-out and standard fabrication method. (a) SOI wafer coated with 2-μm oxide layers. (b) Hard mask preparation on the SOI wafer. (c) DRIE of device layer and handle layer. (d) Metallization. (e) Thermo-compression bonding.

analyses show that the proposed sandwich design is very robust to the most relevant fabrication-related imperfections for the entire frequency range of interest.

III. Fabrication and Assembly

The proposed transition is fabricated using a silicon-on-insulator (SOI) micromachining process, where both the handle layer and device layer are etched using a deep-reactive-ion-etching (DRIE) based on an advanced BOSCH process to obtain low sidewall roughness. The buried oxide (BOX) isolation layer serves as an etch-stop layer; thus, both top and bottom waveguide faces have a very smooth surface resulting in low losses [8], [30].

As shown in Fig. 5, the SOI wafer (3-μm BOX layer, 275-μm handle layer, and 30-μm device layer) coated with a 2-μm thermal SiO_2 layer on both sides. As the first step, the mask is patterned on both sides of the wafer by means of lithography and oxide dry etching. Afterward, the handle and device layers are etched down to the BOX layer in two steps (first, the top side is etched then the wafer is flipped over, and the bottom side is etched as well). A dry etching process is later used in two steps for the top and bottom sides to remove the oxide hard masks and the BOX layer. Then gold metallization has been performed in a sequence of two-step spurting a 50-nm-thick titanium-tungsten (TiW) adhesion layer and then sputtering 1.5-μm gold. This sequence is carried out on both the top and bottom sides separately to coat all sides of the wafer. The average surface roughness achieved using this method is about 2.14 nm for the top/bottom of the waveguide, and 163.13 nm for the waveguide sidewalls [30]. Finally, the three metalized layers are vertically stacked in the desired order with the aid of predesigned precise Vernier scale alignment marks and vacuum holes on chips. Alignment is carried out manually based on [31] by using the vacuum and the Vernier scale marks placed in the corners of the chips. This method allows misalignment to be tracked and adjusted. The chips are assembled using thermo-compression bonding [32].

IV. Measurements and Analysis

The conventional method of measuring silicon chips containing micromachined waveguides is to insert the silicon chip into a CNC-milled fixture with standard waveguide interfaces [31], [33], [34]. However, for sub-THz/THz frequencies, not matching fabrication tolerances and surface nonuniformities of the metal fixture, as compared to the more accurately

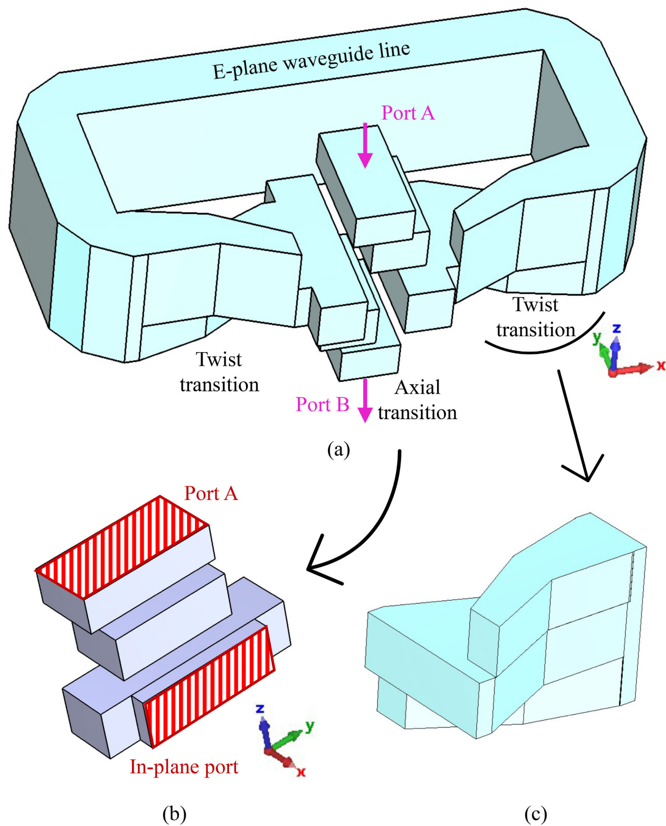
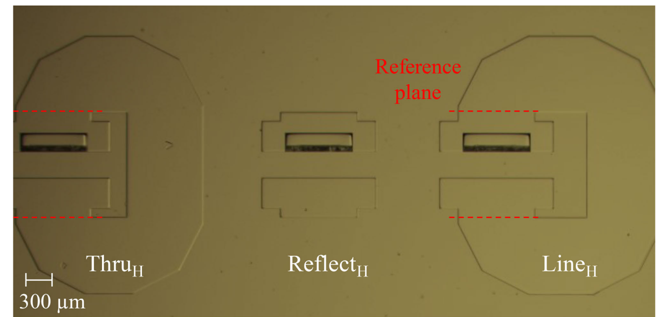
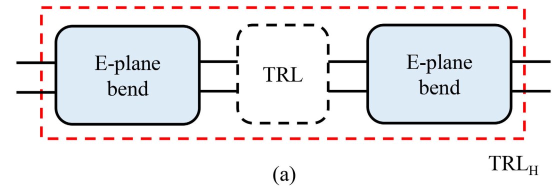
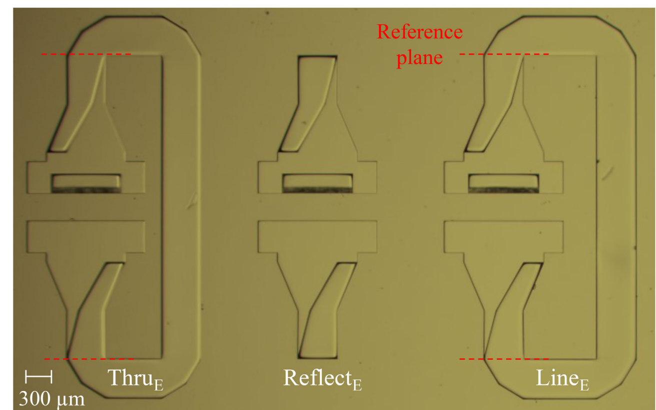


Fig. 6. (a) Configuration of the fabricated waveguide circuit; (b) E-plane multistep bend; and (c) proposed twist.







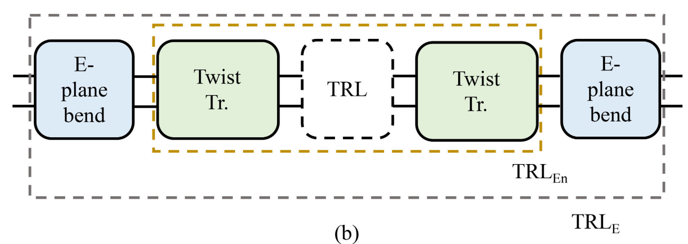


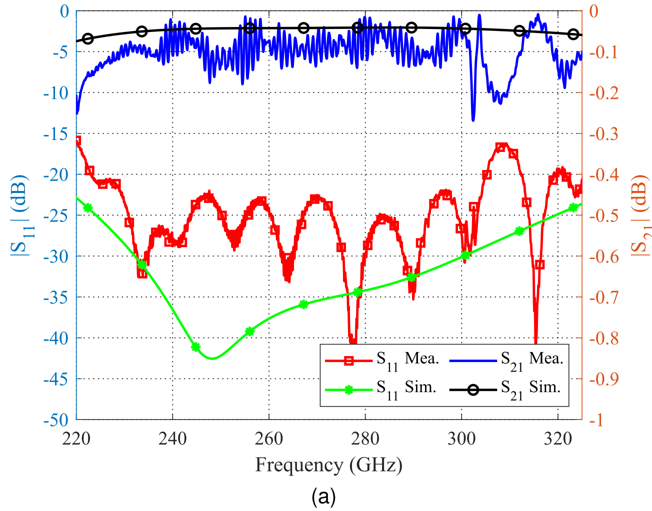
Fig. 7. Microphotographs of the fabricated two sets of calibration kits: (a) TRL$_H$ and (b) TRL$_E$.

manufactured silicon chips, resulting in interface problems. To avoid CNC-milled fixtures or interposers, an on-chip waveguide-flange interface is required to provide axial port configuration for the two device ports which allow the chip to be placed directly between the flanges of two test ports. Two-port S-parameters of the fabricated devices are measured using the ZVA-24 vector network analyzer (VNA) and Rohde & Schwarz ZC330 frequency extenders for 220–330 GHz.

Fig. 6 shows the circuit configuration used to characterize the proposed twist. An on-chip axial transition is employed to guide the wave from the out-of-plane direction to the H-plane waveguide port (TE_{10} port of the 90B:-twist). The axial transitions consist of two E-plane bends established in three layers which transfer the waves from out-of-plane to in-plane while isolating the input and output [17]. Two of the proposed 90°-twist transitions are connected to the H-plane waveguide outputs of the axial transitions with a subsequent E-plane waveguide section between them to close the circuit loop. The closed-loop circuit consists of three E-plane waveguides and four E-plane 90° bends. It should be noted that any designed E-plane waveguide device can be placed on the chip instead of the circuit loop.

The response of the proposed transition needs to be de-embedded from the measured data. A two-tier calibration utilizing two sets of on-chip Thru-Reflect-Line TRL calibration kits [6], [7] is utilized for determining the S-parameters of the twist transition. One calibration kit (TRL$_H$) has its reference plane at the input of the characterized TE_{10}-to-TE_{01} transition, corresponding to the port with the TE_{10} mode, while the other (TRL$_E$) has its reference plane at the output of the transition (port with TE_{01}). Both calibration kits are cofabricated on the same wafer. Fig. 7 shows microphotographs of the silicon-micromachined TRL$_H$ and TRL$_E$ calibration kits during the assembly when the first layer and the second layer have been vertically stacked and aligned.

The first calibration step is to use the TRL$_H$ and do the routine calibration for the T_E, R_E, and L_E standards as DUTs. The first calibration removes the errors caused by the axial transitions from TRL$_E$ and shifts the reference plane to the twist's input. In other words, the results of the performed TRL$_H$ calibration are S-parameters of a new calibration kit TRL$_{En}$ which are a cascade of S-parameters of the proposed transition and S-parameters of the standards. The second step is to calibrate one of the previous step's outcomes as a DUT



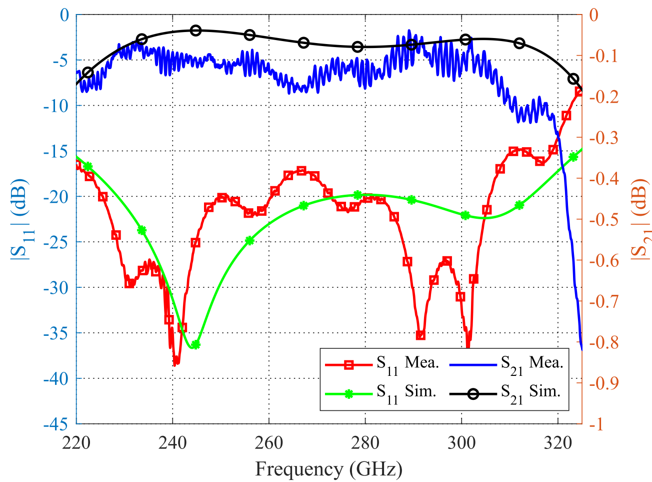


Fig. 8. (a) Measured and simulated S-parameters of the proposed 90B:-twist [see Fig. 1(c)] and (b) measured and simulated S-parameters of the axial transition from port A to the H-plane port [see Fig. 6(b)].

TABLE II
PERFORMANCE COMPARISON OF SUB-THZ WAVEGUIDE 90B:-TWIST TRANSITION

Ref	Frequency (GHz)	Total length (mm)	IL (dB)	RL (dB)	Technique
[26]	220-320	6	0.5	20	CNC
[19]	500-700	2.643	2.5	20	CNC
[20]	140-220	0.66	0.4	20	CNC
[21]	600-750	0.27	0.5	18.8	UV-LIGA
[22]	220-330	0.25	0.4	25	CNC
[25]	220-330	1.469	0.6	25	CNC
This work	220-330	1.044	0.2	20	DRIE

with TRL_{En}; here, we used S-parameters of L_{En}. The error of the second calibration results in the S-parameters of the proposed on-chip twist.

The measured S-parameters of the de-embedded proposed 90°-twist transition are shown in Fig. 8(a). The insertion loss is less than 0.2 dB with a return loss of better than 16 dB in the entire 220–325-GHz band (better than 23 dB in 223–305-GHz

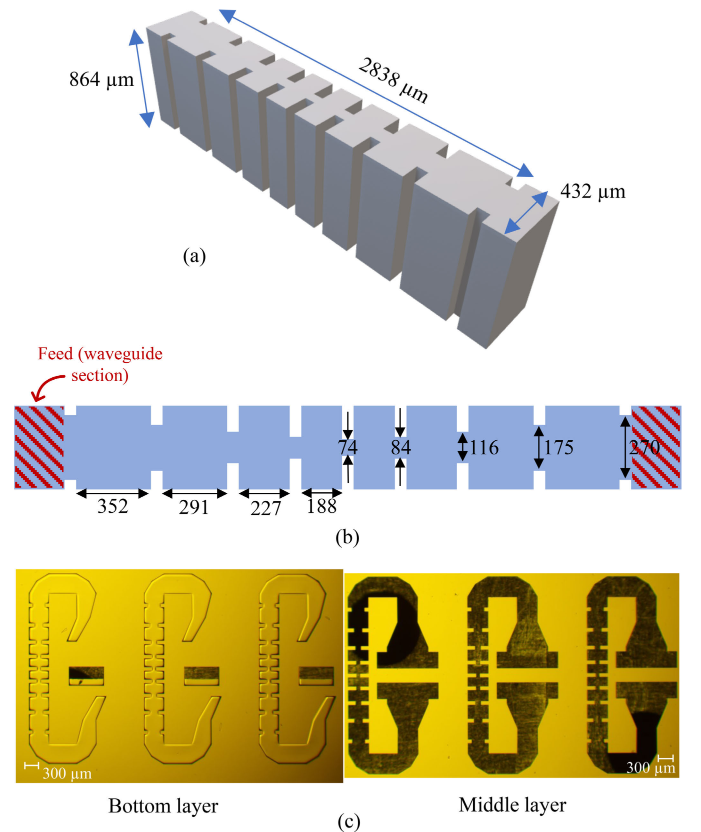


Fig. 9. Proposed LPF: (a) 3-D model; (b) top view of the structure (all dimensions are in μm); and (c) microphotographs of the fabricated LPFs before assembly.

range). There is a good agreement between measurement and simulation results. The visible ripples in the measures S-parameters are a result of TRL calibrations that use a Thru standard with nonzero length instead of ideal Thru [35]. The measured S-parameters of the transition from port A to the H-plane waveguide (input of the twist) are shown in Fig. 8(b); the extracted results are in excellent agreement with the ones reported earlier in [17].

A comparison between the performance of the proposed twist and other recently published transitions in the sub-THz frequency range is summarized in Table II.

V. LOWPASS FILTER

An LPF is designed and integrated with the proposed 90°-twist transition to demonstrate the application of the platform. Traditionally, LPFs are designed through an L-C ladder network, which, in rectangular waveguides, is implemented by capacitive irises and inductive waveguide sections having lengths shorter than a quarter wavelength. The capacitive irises are attached to the top and bottom walls of the waveguide; therefore, their fabrication in silicon micromachining is much simpler using the orthogonal orientation of the waveguide, as etching is carried out vertically. Due to this fact, the proposed orthogonal orientation platform is an enabling technology for silicon micromachined LPFs.

For the demonstrator filter, a cutoff frequency f_{max} of 280 GHz and a return loss RL of 20 dB have been chosen

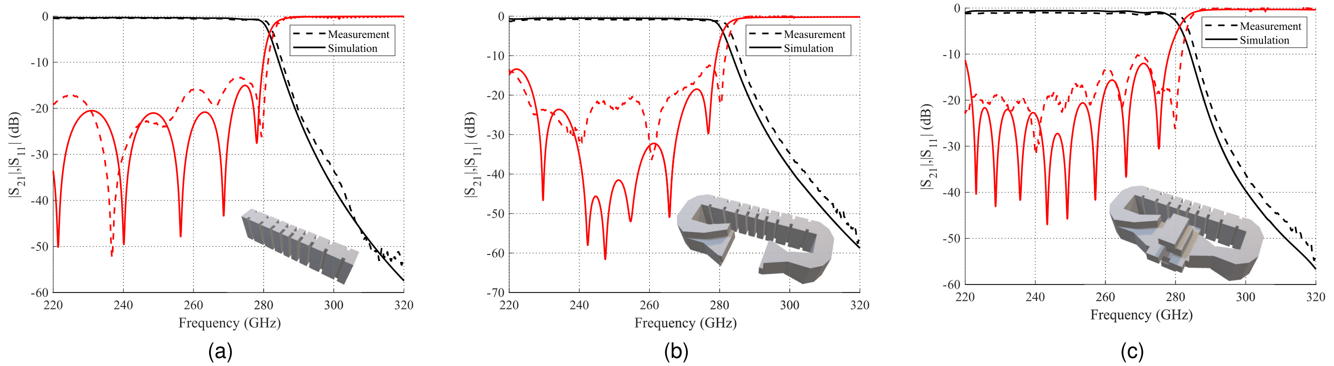


Fig. 10. (a) De-embedded measured and simulated S-parameters of the silicon micromachined LPF; (b) measured and simulated S-parameters of the lowpass filter together with two twists connected to input and output; and (c) measured and simulated S-parameters of the whole device containing axial transition and two twist together with LPF.

as design specifications. The design of the LPF, consisting of ten sections of the three-layer uniform silicon micromachined E-plane waveguide separated by nine capacitive irises, is shown in Figs. 9(a) and (b). The reference planes are located at the input and output irises. Fig. 9(c) shows a microphotograph of the top and the middle layer of the LPF before assembly. The LPF is characterized using an on-chip TRL calibration kit integrated on the same chip as the LPF. The de-embedded measured results are shown in Fig. 10(a), along with the simulated, which are in good agreement. The average insertion loss in the passband is 0.4 dB, and the return loss is better than 14 dB. Fig. 10(b) shows measured and simulated S-parameters of the LPF together with connected input and output twists. Fig. 10(c) shows the measured and simulated S-parameters of the whole structure before de-embedding, containing the axial transition, both twists, and the LPF. In our design, the performance of the LPF (the external and internal couplings) is optimized without considering the twist and axial transition. However, the dimensions can be reoptimized to achieve the desirable performance of the LPF with the twists and axial transitions connected.

VI. Conclusion

We have presented a low-loss compact platform enabling cofabrication and on-chip connection of orthogonal waveguide subsystems using a novel silicon-micromachined 90° rectangular waveguide twist with simple and compact geometry. The structure has been fabricated in three gold-metalized silicon chips bonded together. A sensitivity analysis of the assembly imperfections has been performed, and the effects of underetching have been studied. A good agreement between simulation and measurement results has been achieved. The experimental results have shown a 23-dB return loss in most of the operation bands (223–305 GHz). A two-tier calibration method using two sets of TRL calibration kits has been employed to de-embed the proposed twist's S-parameters. The proposed solution enables on-chip interconnection and simple integration of the H- and E-plane waveguide networks in the subterahertz range, including LPFs. For the first time, a silicon micromachined LPF with a cut-off frequency of 280 GHz has been fabricated and directly measured on a flange with the aid of the proposed platform. The LPF has shown an excellent performance throughout the entire band of operation.

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