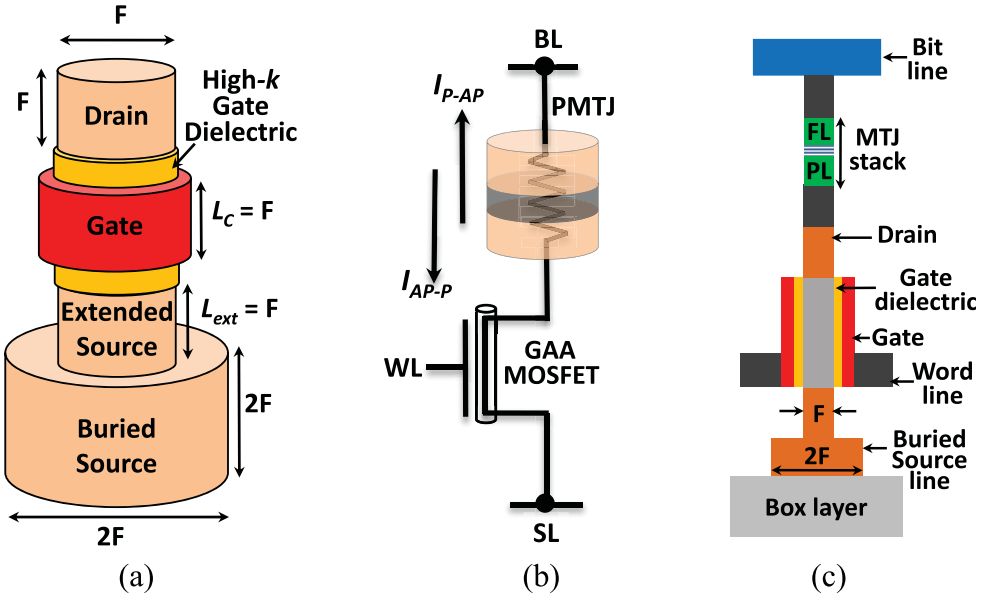
IEEE TRANSACTIONS ON

MAGNETICS

A PUBLICATION OF THE IEEE MAGNETICS SOCIETY

JUNE 2018 VOLUME 54 NUMBER 6 IEMGAQ (ISSN 0018-9464)

PART II OF TWO PARTS



(a) 3-D structure of vertical gate-all-around (GAA) NW transistor with high-k gate dielectric (GD), (b) circuit schematic, and (c) cross-sectional layout of high-k GAA-based single level cell (SLC) STT-MRAM. From the paper, "Parallel Multilevel Cell STT-MRAMs for Optimized Area Energy and Read-Write Operations" by S. Prajapati and B. K. Kaushik *et al.*, Art. no. 4400309.