Reconfigurable Hardware in Postsilicon Microarchitecture

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Computer architects want to design processors that are general purpose yet have the performance of special-purpose hardware tailored to each application. Recently, this goal has led to a proliferation of hardware accelerators for important tasks, including machine learning and cryptography. Despite the benefits of these accelerators, we cannot possibly design and incorporate enough of them to benefit all of the workloads that the processor will run.

In "Post-Silicon Microarchitecture," authors Kumar et al.[1] introduce a new microprocessor design that tightly integrates reconfigurable hardware [for example, a field-programmable gate array (FPGA)] that can be used to accelerate any application.

While reconfigurable hardware itself is not new, its use in postsilicon microarchitecture (PSM) is radically different. Unlike schemes that use the reconfigurable hardware to implement the functionality of software idioms (that is, by configuring it to implement a frequently used function), PSM uses it to implement tailored microprocessor modules that can be used by a general-purpose processor. PSM can, for example, provide branch predictors and data prefetchers that are tailored to specific programs. These customized modules can, by virtue of being designed explicitly for individual programs, far outperform their general-purpose versions.

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The idea of PSM has great potential, and the article[1] further shows how to turn that potential into reality. Implementing PSM requires solving several engineering challenges, the most significant of which is providing an efficient interface between the general-purpose processor and the reconfigurable hardware. The design explicitly distinguishes between the PSM's reconfigurable fabric (PSM-RF) and the PSM agent (PSM-A), which serves as the interface between the PSM-RF and the general-purpose processor (see Figure 1). The PSM-A interfaces to this processor only at clearly defined observation and injection points. At observation points, such as the instruction commit stage, the PSM-A monitors what the processor is doing. At injection points, such as the instruction fetch stage, the PSM-A inserts information, such as a branch prediction or a prefetch instruction, into the general-purpose processor. The PSM-A must also bridge the performance gap between the high-frequency processor and the low-frequency PSM-RF.

The future of computer architecture is expected to rely increasingly upon special-purpose hardware, and it is imperative that the research community continue to innovate how it is used. PSM is an exciting new design paradigm in this space, and it opens up many new opportunities for computer architects.

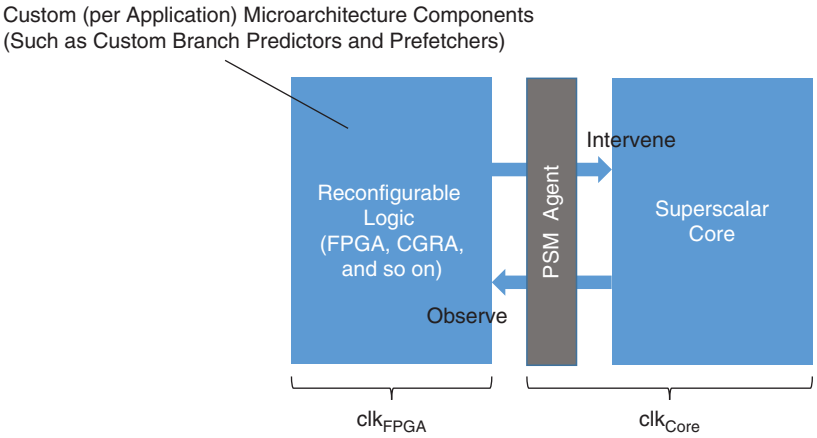

FIGURE 1. The organization of a PSM. CGRA: coarse-grained reconfigurable architecture.

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REFERENCE

1. C. Kumar et al., "Post-silicon microarchitecture," *IEEE Comput. Arch. Lett.*, vol. 19, no. 1, pp. 26–29, 2020. doi: 10.1109/LCA.2020.2978841.

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