

Generalizing Access to Instrumentation Embedded in a Semiconductor Device

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Despite the success of IEEE 1687, it has one significant shortcoming: it's difficult to use on devices without an 1149.1 test access port (TAP) controller. IEEE P1687.1 addresses this problem.

In the 1980s—the early days of circuit boards—most failures were due to poor solder joints on the boards, imperfections among board connections, or problems with the bonds and bond wires from integrated circuit (IC) pads to pin lead frames. The Joint Test Action Group (JTAG) formed in 1985 to provide a pins-out view from one IC pad to another so these faults could be examined. The eventual result was *IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture*, last revised in 2013, which defines the test access port (TAP) controller present in all

IC chips since Intel released JTAG with its 80486 CPU. JTAG designed the standard to assist with device, board, and system testing; diagnosis; and fault isolation. Today, the term JTAG is used to refer to devices that comply with the standard. Such devices are the primary means of accessing subblocks of ICs, making it an essential mechanism for debugging embedded systems without other debug-capable communications channels.

Many years later, another IEEE working group devised the *IEEE Standard 1687-2014 for Access and Control of Instrumentation Embedded within a Semiconductor Device*—also called internal JTAG, or IJTAG—to bring management, optimization, portability, and scalability to the operation of instruments embedded in semiconductor devices. By instrument, we mean an embedded intellectual property (IP) whose interface would adhere to the rules and





descriptions defined in the standard. Although the working group originally aimed to test applications, early in the conceptualization phase they discovered that the idea of an instrument can be expanded far beyond this, including instruments used for debugging, characterization, process monitoring, environment monitoring, functional configuration, establishing operational settings, specification tuning, and other on-chip resources.

Even before IJTAG was officially released in 2014, it enjoyed quick and widespread attention, not only in industry but also in academia.¹ Academia had researched how to make best use of the possibilities IJTAG enables, and industry was composing a standard that solves actual day-to-day problems, automating an error-prone and painful manual process. From there, a project authorization request (PAR) for IEEE P1687 was issued. It found wide and quick adoption, tools were created, design-for-test methodologies were architected based on the standard, and devices were put into silicon—all before the standard was released in 2014.

AN INSURMOUNTABLE OBSTACLE

IEEE 1687-2014 was off to a promising start. So, why the need for an IEEE P1687.1 shortly afterward? To understand this, we must consider how an IJTAG device interfaces with the external world.

IJTAG has two principal ways to bring data over the device pin interfaces: parallel data ports and shifting, chiefly orchestrated by an IEEE 1149.1-compliant TAP and TAP controller. Industry primarily uses the latter method because it allows risk-free adoption of the new standard, using the same well-known and widely used methodology of IEEE 1149.1. In particular, this allows tools to operate

IEEE 1149.1-“compliant” IP as an IJTAG-compliant instrument. In short, those interested in trying IJTAG need only describe their existing JTAG-based design in IJTAG terms. They won’t get all the advantages of 1687, but it’s a good start.

Typically, after this initial “safe” tryout of 1687, many users designed projects from the ground up, harnessing all the advantages of 1687. However, all these 1687-based designs still rely on a TAP controller at the chip’s

boundary. Although this is undoubtedly the right choice for many devices, it’s an insurmountable obstacle for others. For reasons that include severe pin limitation, security concerns, and reuse requirement of legacy, non-1149.1 access methods, a TAP controller at the device’s boundary isn’t available in all devices. These devices often support other interfaces and controllers to access their internal test, debug, configuration, and monitoring resources and instruments—device pin interfaces such as serial peripheral interface bus (SPI), inter-integrated circuit (I2C), universal serial bus (USB), advanced microcontroller bus architecture (AMBA), and many others. Still, these device owners, seeing the advantages of IJTAG, also wanted to use IJTAG.

Toward IEEE P1687.1

1687 anticipated such non-TAP interfaces through a simple 1687 instrument connectivity language (ICL) keyword called AccessLink. AccessLink for 1149.1 is a JTAG Instruction Register

encoding that selects a 1687 network of instruments as the active shift register to be placed between the device pin interface’s scan input and scan output pins while synchronizing the network registers with the device pin interface test clock (TCK) pin. In addition to linking 1687 to 1149.1, AccessLink also includes a generic documentation item to allow other interfaces. However, the 1687 standard provides no details on using

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non-1149.1 interfaces, leaving it up to users to develop these on their own. So, the question remained: Is AccessLink sufficient for all use cases, and is the plug-and-play portable network defined by the 1687 standard capable of being driven by any given pin interface and controller?

To make the new 1687 standard operable under these non-1149.1 interfaces, a study group was created at a Test Technology Standards Committee meeting held at the 2015 IEEE International Test Conference. The concept was presented as an extension of the 1687 use model, to be called 1687.1. The PAR was submitted in May 2016, and in December 2016, the study group became the IEEE P1687.1 Working Group.

The goal of IEEE P1687.1

P1687.1 envisions the investigation and inclusion of any device pin interface. The working group felt that a pragmatic approach was to analyze contemporary, widely used, non-TAP

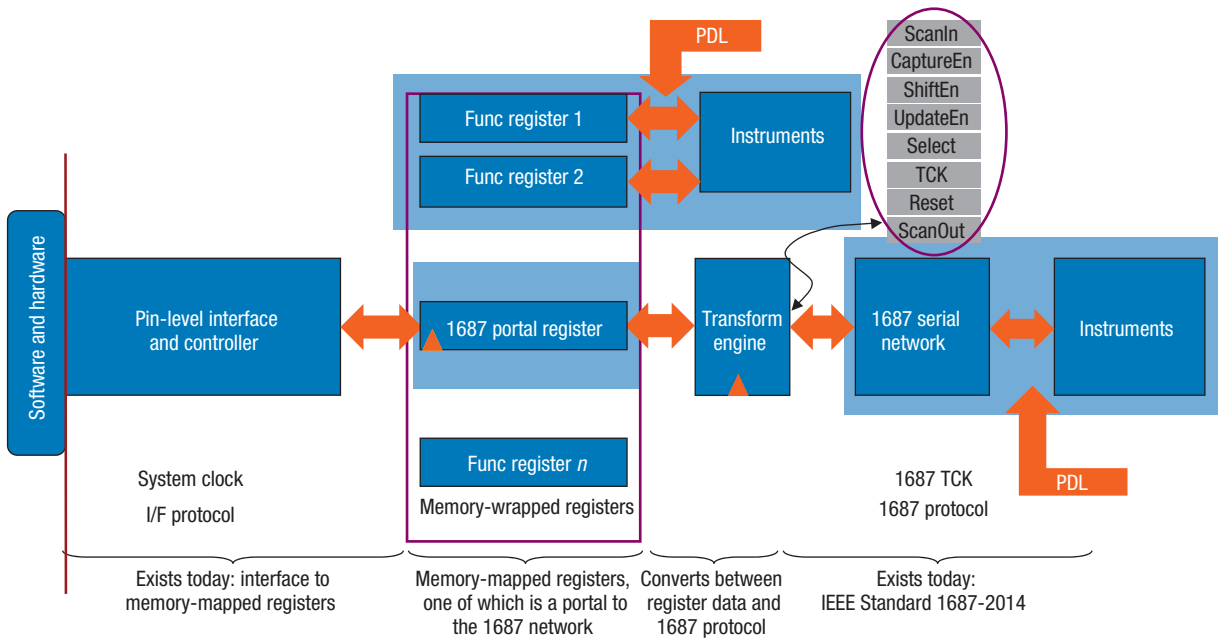


Figure 1. Abstract view of what the IEEE P1687.1 Working Group is currently discussing. At the center is the transformation engine. Objects with a light blue background can be described in 1687 today. I/F: interface; PDL: procedural description language; TCK: test clock.

interfaces and abstract commonalities from them. If 1687.1 is flexible enough to describe today's SPI, I2C, and similar interfaces, it should be able to describe future interfaces without the need to regularly update the standard. One such commonality is that these interfaces communicate through a register with instruments inside the device. If a register could be designated to interface with the IJTAG network, then, for example, an existing SPI implementation could operate natively 1687 instruments.

Figure 1 depicts an abstract view of what the working group is currently discussing, with elements that are describable in today's 1687 standard framed in light blue. On the left is the device's pin interface, unchanged in hardware and protocol. It interfaces, as usual, with memory-mapped registers, one of which is designated to further interface with the IJTAG network.


The tricky part here is transforming data written to and read from this 1687 portal register to generate the common shift/capture/update protocol,

operating the 1687-compliant network on the far right side of the figure. Current ideas for the inner workings of this transformation engine include first-in, first-outs (FIFOs) managing data streams, and an embedded TAP controller as the protocol generator. Questions of full- and half-duplex operation (IJTAG is a full-duplex protocol) and bandwidth matching as well as (TCK) clock generation and compatibility must be addressed. The top center of the figure illustrates that the addressable registers can, already today, operate IJTAG instruments with parallel data port interfaces; no transformation engine is needed there.

Besides the transformation engine hardware and protocol, the group must identify the proper handoff point of 1687.1 to, for instance, the SPI interface and the details behind the electronic design automation (EDA) software. Is it sufficient to describe 1687.1 "patterns" as input/output of the portal register data, or do other parts of the infrastructure—from the device pin interface to the IJTAG

instrument—need to be described as well? Would 1687.1 EDA software users expect the option to generate a top-level Verilog test bench for a given protocol, implementing what was defined by an IJTAG instrument's procedural description language deep inside the device?

Furthermore, at the board level, such non-TAP interfaces are commonly used to communicate between two or more devices. Would 1687.1 need more descriptive power for this? Would this include the ability to precisely trigger events in multiple devices, like initiating a transition on one device that must be received by a second within a precise time window? Figure 2 summarizes some of these questions.

There are many things to investigate, discuss, and eventually define. This young working group has just begun its journey. Contact us if you want to provide input or join the working group. 

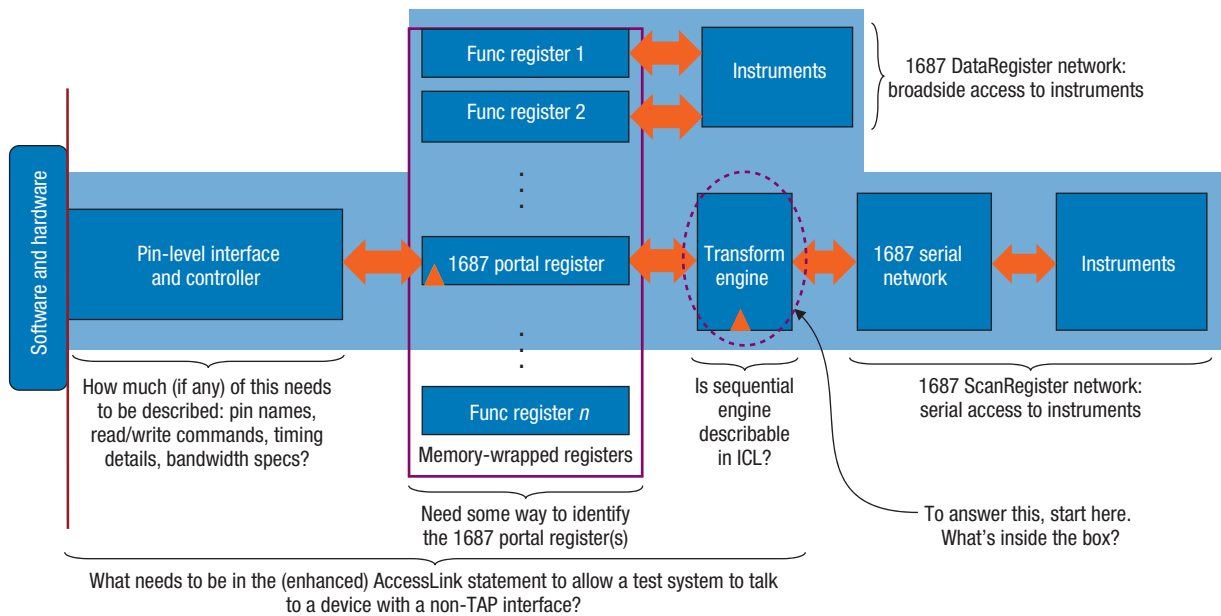


Figure 2. Selected list of questions the IEEE P1687.1 Working Group must address. ICL: instrument connectivity language; TAP: test access portal.

REFERENCE

1. *IEEE Design & Test*, special issue on IEEE's P1687, vol. 30, no. 5, 2013.

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