Binary Sequences for Online Electrochemical Impedance Spectroscopy of Battery Cells

Roberta Ramilli, Francesco Santoni, Alessio De Angelis, *Member, IEEE*, Marco Crescentini, *Member, IEEE*, Paolo Carbone, *Fellow, IEEE*, and Pier Andrea Traverso, *Member, IEEE*

***Abstract*— Online diagnostic of lithium-ion battery (LIB) cells may have significant impact on chemical energy storage systems. Electrochemical impedance spectroscopy (EIS) is widely used for the characterization of LIBs and could be the most appropriate technique for online diagnostic, but its response time should be shortened. This work investigates the usage of multisine excitation to shorten the measurement time and simplify the hardware implementation for EIS of battery cells. Two types of multisine binary sequences are considered: sigma–delta modulated multisine sequences (SDMSs) and maximum length binary sequences (MLBSs). Their applicability to online and *in situ* EIS monitoring is evaluated by designing a measurement architecture also suitable to be implemented in a system-on-chip. The calibrated measurement system is compared with a benchtop reference instrument, reporting an RMSE deviation smaller than 5% in the frequency range of interest 1–200 Hz. The realized system is then used for online monitoring of the discharge process of a commercial 18650 LIB cell. The two proposed sequences are compared in terms of accuracy using a digital battery emulator circuit. Both the sequences demonstrated to be suitable for fast measurement and simple hardware integration, enabling online *in situ* EIS monitoring at cell level.**

***Index Terms*— Batteries, binary sequences, electrochemical impedance spectroscopy (EIS), maximum length binary sequences (MLBSs), sigma–delta.**

I. Introduction

ELECTROCHEMICAL impedance spectroscopy (EIS) is a nondestructive and reliable measurement technique widely used for the characterization of batteries [1]. Several key parameters can be inferred from EIS data, including the state of charge (SoC), the state of health (SoH) [1], [2], [3], [4], rate capacity or power fade, degradation, and temperature dependence. Accurate estimation of the state parameters is fundamental for the diagnosis of the battery behavior, which is at the basis of the efficient and safe operation of numerous applications relying on batteries; from mobility to consumer electronics, as well as energy storage. The implementation of an *in situ* EIS monitor (i.e., directly on the battery cell) and the capability of making an online diagnosis (i.e., while the battery is working in its real environment) would have a huge impact on the widespread usage of electrochemical storage systems [5], [6], [7]. To realize this vision, the EIS measurement system must face the challenges of shortening the measurement time and reducing the dimensions of the system to be integrated into the battery cell [8].

Many authors in the literature respond to these challenges by proposing methodologies and architectures in which EIS excitation is realized by properly controlling the electronic load, like the power converter or the motor controller [9], [10]. These methods are limited to specific systems requiring switching power electronics and have the critical drawback of injecting unavoidable ripples in the output voltage [11], [12]. Other authors describe custom IC optimized to be embedded in the battery management unit [13]. Sensichips has recently developed a microchip for cell management units which includes an electrochemical impedance spectrometer [14]. However, such architectures perform EIS by providing a sine-wave excitation to the battery. The usage of a broadband excitation signal allows for a reduction in the measurement time with respect to conventional narrowband excitation, such as the sine-sweep method [15]. Different broadband excitation sequences have been proposed, such as multisine excitation [16], [17], [18] and pseudorandom sequences [19], [20]. To limit the power consumption and occupation area of the excitation section of an EIS measurement system, its architectural complexity should be as simple as possible. Therefore, an interesting solution is represented by binary sequences, since they can be generated by simple digital circuits, without requiring a complex digital-to-analog converter (DAC) [20]. Thus, VLSI implementation of an impedance measurement system relying on binary sequences can respond to the challenges posed by the *in situ* and online diagnostic of battery cells. In [19], pseudorandom binary and ternary sequences were used to perform EIS on lithium polymer cells using a commercial DAQ system. This article demonstrated the ability of multisine sequences to cut the measurement time in off-line measurements. Nejad and Gladwin [21] combined EIS based on pseudorandom binary sequence (PRBS) with dual extended Kalman filter for online estimation of battery state of power. The PRBS-EIS technique was used only when the battery was in quiescent mode to support the Kalman filter. Binary excitation-based EIS systems can also be easily fitted in motor controllers, as shown in [12] for EIS measurement purposes.

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This article analyzes the applicability of multisine binary sequences to online *in situ* EIS monitoring. The article presents two approaches for designing binary sequences to be used as excitation signals for EIS of battery cells and proposes a simple measurement architecture that takes advantage of binary excitation and is suitable to be implemented as a system-on-chip in VLSI technology. The first approach is based on sigma-delta modulated multisine sequence (SDMS) [22], [23], while the second approach is based on the maximum length binary sequence (MLBS). A prototype of the system is realized with off-the-shelf components on a PCB board. After being calibrated, the prototype is compared with gold standard EIS instrumentation and assessed in online monitoring of the discharge process of a commercial battery. The two proposed multisine binary excitation sequences are compared with the help of a battery emulator, which can be treated as a stable and reliable reference of the battery impedance. The SDMS provides greater flexibility in designing the spectral properties of the sequence. The MLBS, on the other hand, contains all the harmonics of the fundamental frequency.

The remainder of this article is organized as follows. Section II reports the theoretical background of the two investigated binary sequences, while Sections III and IV describe the architecture of the proposed measurement system and the battery emulator, respectively. Detailed descriptions of the prototypes and experimental results are provided in Section V. Finally, conclusions are drawn in Section VI.

II. Binary Sequences for EIS

A. Sigma–Delta Multisine Sequence

A basic requirement for online EIS monitoring of batteries is the short measurement time required to assume the battery behavior to be invariant. To this end, it is necessary to excite a number of frequency points at the same time. This can be easily achieved by digitally creating a broadband excitation signal as a sum of sine waves [24]

$$x(t) = \sum_{i=1}^{M} A_i \sin(\omega_i t + \theta_i) \tag{1}$$

where the maximum flexibility on the choice of the number of sine waves M, the amplitudes A_i, the phases θ_i, and the angular frequencies $\omega_i = 2\pi f_i$ is granted. This flexibility allows the adaptation of the excitation signal to meet the application requirements. When EIS is used for battery monitoring, the frequencies should be selected to better investigate the low-frequency portion of the Cole–Cole plot where the majority of the information about the battery state is placed [4]. The phase of each sine wave should be randomly chosen to limit the crest factor of the resulting waveform $x(t)$ and to not trigger nonlinear responses.

The multisine waveform of (1) is usually represented as a multibit signal; hence, a complex multibit DAC is required to generate the analog excitation with a suitable signal-to-quantization noise ratio (SQNR). To simplify the implementation of DAC, in terms of occupied area and power consumption in a VLSI implementation, we propose the application of single-bit multisine sequences. A possible method to realize this single-bit sequence is to apply the sigma–delta modulation to the original multibit multisine signal. An high-order modulator allows one to achieve rather high SQNR levels using a single-bit sequence as the output [25]. Moreover, the complexity required by high-order modulation is totally demanded to the digital processor while the 1-bit DAC is easy to design and it is inherently linear [26], [27]. Therefore, the SDMS is a good candidate for *in situ* and online monitoring of battery cells.

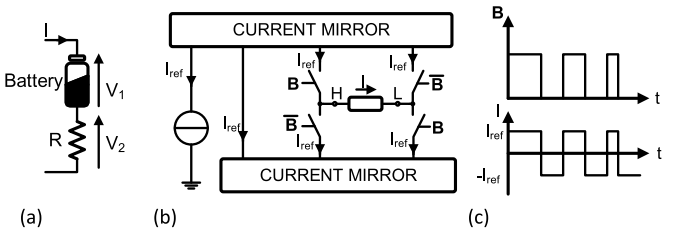

Fig. 1. (a) Representation of the two-voltage method. (b) Scheme of the H-bridge used as a bipolar 1-bit current DAC. (c) Current generated by the H-bridge in relation to the input sequence **B**.

B. Maximum Length Binary Sequence

An alternative method to realize a multisine sequences that still allows to excite many tones concurrently is the MLBS. MLBSs are characterized by a flat spectrum and excellent periodic autocorrelation and cross correlation properties [28]. Therefore, they are widely used for system identification purposes, e.g., to measure the impulse response and frequency response of linear systems [15]. An additional advantage of such sequences is simple generation, which can be achieved using a shift register and elementary logic gates. This simple generation can also be implemented by low-complexity microcontrollers, thus enabling practical applications in numerous fields.

The MLBS is less flexible than the SDMS, because it excites equally all the harmonics. However, it is possible to introduce some level of flexibility by starting from an MLBS and repeating every bit a number of times. This has the effect of shaping the spectrum in a low-pass fashion and providing more energy at low frequencies than at high frequencies, as shown in [23]. The bit-repetition approach is well-suited to battery EIS measurement, because typically the low frequencies provide most of the information, and the high frequencies, roughly above the kilohertz range, are less informative. Furthermore, the low-pass behavior of the signal induced by bit repetition also mitigates the aliasing effects, which may occur in practical scenarios due to the wide bandwidth of the MLBS signal. Therefore, in the following, we use MLBS with bit repetition to perform EIS measurements.

III. Impedance Analyzer With Binary Excitation

The proposed impedance measurement system is based on the two-voltage method shown in Fig. 1(a) [29]. The impedance of the battery is defined as

$$Z_{\text{bat}} = \frac{V_1}{V_2} R \tag{2}$$

where V_1 is the voltage across the battery, V_2 is the voltage across the reference resistor, and R is the reference resistance that should be selected close to the nominal value of the dc resistance of the battery under test. The type of excitation signal does not directly affect the measurement model of (2), but it limits the validity of the model over certain frequency

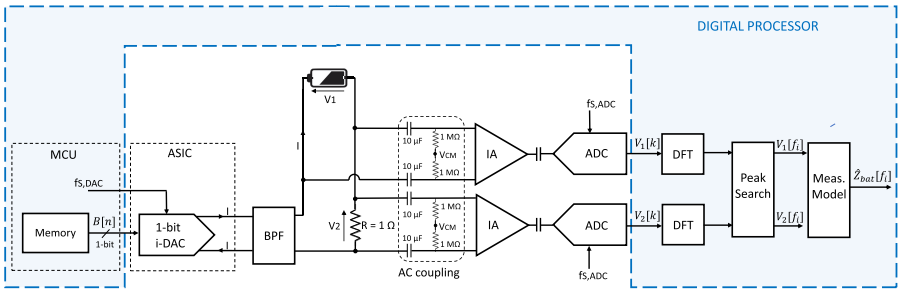

Fig. 2. Architecture of the proposed impedance analyzer for battery EIS monitoring based on binary sequence excitation.

values. The usage of a multisine excitation, by means of either SDMS or MLBS, limits the validity of (2) only to the excited frequency points. Following this measurement definition, the excitation signal could be either a voltage or a current. However, battery cells set specific constraints on the measurement procedure. First, a battery is generally a nonlinear device and can be assumed linear only under small perturbations [30]. Furthermore, the battery is usually characterized by a very small impedance, ranging from 100 $\mu\Omega$ to a few Ω depending on its chemical/physical realization [1]. These two considerations hamper the usage of a voltage excitation while suggest to excite the battery with a current in the mA to A range, easier to control and offering a better signal-to-noise ratio [31].

The usage of binary sequence excitations, such as SDMS and MLBS, simplifies the design of the current generator. An H-bridge circuit [see Fig. 1(b)], as the one described in [26], can be easily used as a bipolar 1-bit current DAC. When the digital word $\mathbf{B} = 1$, the bridge forces a current of value I_{ref} to flow from node H to node L, while $\mathbf{B} = 0$ causes a current of the same value to flow from node L to node H. From the standpoint of the load connected between nodes H and L, this behavior is equal to the generation of a digital current signal toggling between levels $+I_{\text{ref}}$ and $-I_{\text{ref}}$. This H-bridge circuit can be directly driven by the digital 1-bit sequences that are stored in or computed by a digital processor. In this way, the sampling frequency $f_{S,\text{DAC}}$ of DAC is equal to the transmission rate of the binary sequence. The current generator is then ac-coupled to the battery by a bandpass filter (BPF) that has the twofold purpose of avoiding dc currents from the battery to the H-bridge circuit and filtering the high-frequency components of the excitation signal, providing both the anti-aliasing function and the noise reduction required by the MLBS and SDMS, respectively. The proposed architecture for the current generator is simple and suitable to be implemented in silicon technology for future miniaturization.

The overall architecture of the proposed impedance analyzer for battery EIS monitoring based on binary sequence excitation is reported in Fig. 2. Given the limitations on the amplitude of the excitation signal and the low resistance values, the voltages V_1 and V_2 usually range from a few μV to a few mV. Hence, a low-noise amplification stage is required, by means of instrumentation amplifiers (IAs), before analog-to-digital conversion. The two analog-to-digital converters (ADCs) work at the same sampling frequency $f_{S,\text{ADC}}$, which should be higher than $f_{S,\text{DAC}}$ to avoid aliasing. The time skew between the two acquisition channels is of little importance in battery EIS because the frequencies of interest are very low. The output streams $V_1[k]$ and $V_2[k]$ of the two ADCs are then digitally processed. Discrete Fourier transforms (DFTs) with the same parameters are computed on both the streams using a fast Fourier transform (FFT) algorithm, and then a peak search algorithm is applied to detect the amplitude and phase values of the complex coefficients of the DFT outputs only at the excitation frequencies f_i. An elevated zero-padding factor is beneficial to increase the numerical resolution of the DFT and better detect the peaks, coping with the intrinsic low SNR of the acquired voltage signals. To minimize the phase error introduced by digital processing, the peak search algorithm works in a coordinated way on both the streams $V_1[k]$ and $V_2[k]$ to find the same frequency bins corresponding to the excitation frequencies f_i.

IV. Battery Impedance Emulator for Binary Sequences

To comparatively analyze the performances of the binary sequences, an impedance emulator has been used instead of a real battery. Indeed, the characteristics of a battery are not fully reproducible over repeated measurements. The emulator provides a stable impedance reference that, in principle, can be used to test and calibrate any measurement system. The emulator had previously been developed [32].

The core idea is to implement on a microcontroller unit (MCU) a programmable digital filter whose frequency response reproduces the impedance of a battery. The implemented architecture is sketched in Fig. 3. A four-wire impedance analyzer can be generically sketched as a current source and measurement unit injecting the excitation signal into the device under test, and a separate voltage measurement system acquiring the response of the excited device. The emulator is devised to be connected in place of the battery. It is equipped with an ADC to acquire the excitation signal and a DAC that emulates the battery response. Since the current cannot be injected directly into the ADC, a suitable load resistor R_{load} has to be connected in parallel with the emulator as shown in Fig. 3. The ADC measures the voltage V_{in} across R_{load}, and the DAC emulates the corresponding response V_{out}. The impedance analyzer reads the emulated voltage from the DAC, as if it was acquiring the signal of a real battery.

The ADC and DAC sample the signals at $F_s = (1/T_s) = 1$ kSa/s, resulting in the sequences $x[n] = V_{\text{in}}(nT_s)$ and $y[n] = V_{\text{out}}(nT_s)$. The filter response in the time domain can be expressed as

$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k] \tag{3}$$

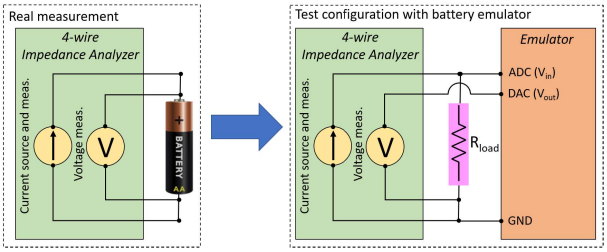

Fig. 3. Simplified scheme of the impedance emulator and its connection to a generic four-wire impedance analyzer.

where $h[k]$ is the impulse response, and N is the total number of samples. The frequency response $H(\omega_k)$ is obtained as the DFT of the impulse response

$$H(\omega_k) = \sum_{n=0}^{N-1} h[n] e^{-i\frac{2\pi kn}{N}} \tag{4}$$

where $\omega_k = (2\pi F_s/N)k$. The frequency response is numerically equal to the ratio $(V_{\text{out}}(\omega))/(V_{\text{in}}(\omega))$; hence, it is independent of the value of R_{load}. Thus, the following relationships hold:

$$H(\omega) = \frac{V_{\text{out}}(\omega)}{V_{\text{in}}(\omega)} = \frac{V_{\text{out}}(\omega)}{R_{\text{load}} I(\omega)} \tag{5}$$

where $I(\omega)$ is the current across the load resistor injected by the impedance analyzer. Hence, the measured emulated impedance is $Z_{\text{emu}}(\omega) = R_{\text{load}} H(\omega)$. The digital filter has been programmed to emulate the impedance of the Samsung ICR18650-26J battery model. As detailed in [32], an analytical model of $Z_{\text{emu}}(\omega)$ has been used. Then, by inverting DFT (4), $h[n]$ was obtained and preloaded on the MCU.

V. Experimental Results

A. Generation of Sequences

For the design of SDMS, the idinput function of MATLAB[1] was used. The generated sequence is 8192 bits long and sampled at 12 593 Sa/s, leading to an excitation time of only 650 ms. A third-order 1-bit sigma–delta modulator with an oversampling ratio of 32 was applied to shape the quantization noise out of the band of interest, resulting in an excitation signal with an SQNR value of 87.2 dB. The SDMS encompasses 25 sine waves specially selected to estimate the low-frequency portion of the impedance spectrum. The frequencies $f_i = [1.5, 3.1, 4.6, 6.2, 7.7, 9.3, 10.8, 12.4, 13.9, 15.4, 17, 20.1, 23.2, 27.8, 32.4, 40.2, 49.4, 55.6, 60.2704, 72.6, 86.5, 100.4, 120.5, 151.4, 196.3]$ Hz are logarithmically distributed in the band 1–200 Hz.

The MLBS was generated using the *mlbs* function of the *fdident* MATLAB[1] toolbox. Each bit of the 1023-bit long MLBS was repeated eight times to achieve a final sequence length of 8184, comparable to SDMS.

B. Impedance Analyzer Prototype

A prototype of the impedance analyzer was realized to carry out the EIS measurement on the battery sample and validate the system in online battery monitoring. The hardware prototype consists of a four-layer PCB board together with benchtop instrumentation.

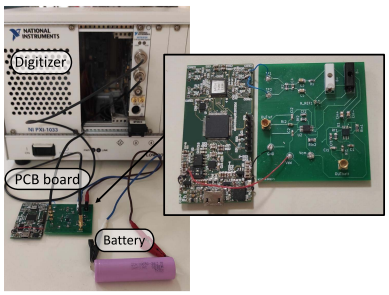

Fig. 4. Measurement setup and realized PCB test board.

The board is divided into two sections. The first section hosts an MCU and a CMOS application-specific integrated circuit (ASIC) that integrates the H-bridge circuit, while the second section is composed of the passive BPF, the coupling circuit, and the IAs (Texas Instruments INA331). The 1-bit sequence is digitally generated in software and stored in a portion of the MCU memory, which sends the sequence to the H-bridge current generator with a transmission rate equal to the sampling frequency of DAC $f_{S,\text{DAC}} = 12\,593$ Hz. Then the 1-bit DAC forces a maximum instantaneous peak current of value $I_{\text{ref}} = 1$ mA to flow into the battery. This limitation on the maximum stimulus current prevented from the usage of the prototype with MLBS. Indeed, MLBS spreads the energy over the whole excitation band resulting to a lower SNR at the single frequency point. Therefore, the prototype is tested using only SDMS.

A 1-Ω high-precision resistor is chosen as the reference resistor, since its value is convenient for subsequent computation. The 25-mHz to 250-Hz BPF placed in between the DAC and the battery removes the high-frequency noise associated with the excitation signal without limiting the frequency range required to estimate the interesting portion of the spectrum of the battery. The ac coupling circuit consists of two 10-μF capacitors to block the dc voltage and two 1-MΩ resistors to set the common-mode dc input voltage of the IAs. The gain factor for each IA is set to a maximum value of 1000. The analog-to-digital conversion is carried out using the 12-bit NI-5124 PXI two-channel digitizer, sampling at $f_{S,\text{ADC}} = 35$ kHz. Since the high-pass cutoff frequency of the ac coupling of the digitizer is 12 Hz, the ADC inputs were set in dc coupling mode with a high-value capacitor in series for each channel. The use of a commercial digitizer allows us to assume the receiver ideal and focus on the generation. The hardware used is based on a VLSI implementation of a 1-bit current DAC, highlighting the possible *in situ* implementation. A photograph of the realized test board together with the measurement setup is reported in Fig. 4.

C. Calibration of the Impedance Analyzer

The realized impedance analyzer prototype is not optimized and suffers from many parasitic elements and nonidealities. Some of those nonidealities are related to the actual implementation: the frequency response of the passive BPF is not perfectly constant throughout the frequency range, adding frequency dispersion of the gain and phase estimates; the

[1]Registered trademark.

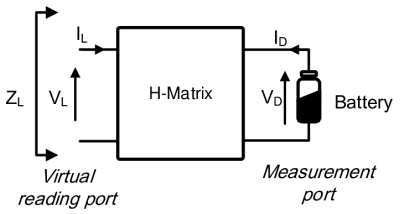

Fig. 5. Two-port representation of the measurement system.

fixture for the battery connection, the ac coupling circuit to the battery, and the general circuital implementation add parasitic elements causing frequency-dependent phase rotation. For instance, the fixture adds inductive and resistive series parasitic elements and parallel capacitive elements. Therefore, a calibration procedure of the impedance analyzer prototype is required. To this end, we followed a behavioral modeling approach that consists of describing the measurement system (up to the ADC) as a two-port network: 1) the measurement port connected to the real battery under test and defined by the voltage $V_D = V_1$ and current $I_D = I = V_2/R$ and 2) the virtual reading port defined by the uncalibrated estimates of the voltage $V_L = \hat{V}_1$ and current $I_L = \hat{V}_2/R$ (see Fig. 5). This system is composed of components that can be assumed linear (at least in their normal operating region): the 1-bit DAC, passive BPF, coupling circuits, and IAs; thus, it is reasonable to model it with the nonhomogeneous H-parameter matrix

$$\begin{bmatrix} I_L \\ V_D \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \cdot \begin{bmatrix} V_L \\ I_D \end{bmatrix} + \begin{bmatrix} I_{\text{os}} \\ V_{\text{os}} \end{bmatrix}. \tag{6}$$

The terms I_{os} and V_{os} would be required to describe the presence of the independent current source (i.e., the H-bridge current DAC) in the two-port network. However, they are neglected in the following calibration procedure to reduce its level of complexity, since such an approximation will not lead to a substantial loss of accuracy while allowing an easy practical implementation of the technique. Solving (6) by applying the load characteristic curve $V_D = -Z_{\text{bat}} \cdot I_D$ leads to the model

$$Z_L = \frac{Z_{\text{bat}} + h_{22}}{h_{11}Z_{\text{bat}} + h_{11}h_{22} - h_{12}h_{21}} = \frac{Z_{\text{bat}} + h_{22}}{h_{11}Z_{\text{bat}} + \gamma} \tag{7}$$

where Z_L is the uncalibrated estimate of the battery impedance defined as

$$Z_L = \frac{V_L}{I_L} = \frac{\hat{V}_1}{\hat{V}_2}R. \tag{8}$$

Equation (7) assumes ideal digital processing of voltages V_1 and V_2. Unfortunately, nonideal ac coupling to the ADC inputs does not perfectly remove the very low-frequency interferences, and a spurious leakage component adding to the low-frequency estimates is still present. This unwanted behavior can be considered in the model by defining the uncalibrated estimate of the battery impedance at frequency f_i, after digital processing, as

$$Z_L^{\text{post}}(f_i) = \frac{V_L(f_i) + A_1(f_i)}{I_L(f_i) + A_2(f_i)} = \frac{Z_L(f_i) + \epsilon_1(f_i)}{1 + \epsilon_2(f_i)} \tag{9}$$

where A_1 and A_2 are the perturbative terms modeling the leakage of the low-frequency components at excitation frequencies f_i. Substituting (7) into (9) gives the final model of

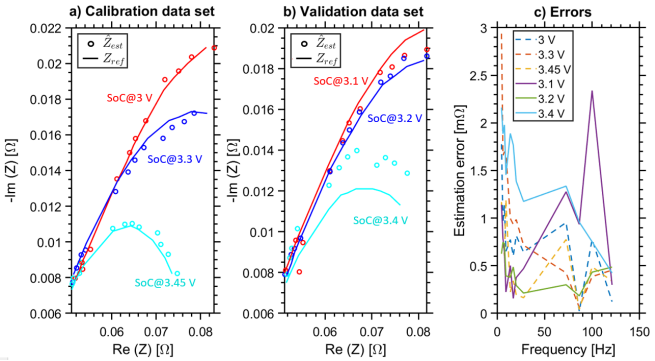

Fig. 6. (a) Estimated Cole–Cole plots compared with the reference ones over the calibration space. (b) Estimated Cole–Cole plots compared with the reference ones over the validation space. (c) Errors of estimated values.

the measurement at each excitation frequency f_i

$$Z_L^{\text{post}}(f_i) = \frac{Z_{\text{bat}} + h_{22}}{h_{11}Z_{\text{bat}} + h_{11}h_{22} - h_{12}h_{21}}[1 - \epsilon_2] + \epsilon_1[1 - \epsilon_2]. \tag{10}$$

The final equation (10) shows a nonlinear model of the measurement with at least five parameters that need to be estimated in the calibration procedure. The calibration was performed on a sample battery (Samsung ICR18650-26J) charged at three different SoC levels representing the entire measurement space of interest (from SoC = 100% to SoC = 10%). The SoC levels were realized following a procedure similar to the one reported in [8]. The battery was first fully charged and then discharged by means of a resistive load. A 2-h-long relaxation time was adopted to allow for the stabilization of the slow dynamic effects. At each SoC level, the impedance of the battery was measured by the uncalibrated impedance analyzer and the reference benchtop impedance analyzer HIOKI IM3590, with a rated accuracy of about 8% of reading for the absolute value and 5° for the phase in the range of interest. The HIOKI impedance analyzer provides the reference value Z_{ref}. The parameters of the model were obtained by minimizing the following cost function at each frequency point f_i:

$$\sum_{n=1}^{N} \left\| Z_{L,n}^{\text{post}}(f_i) - Z_{\text{ref},n}(f_i) \right\|^2 \tag{11}$$

where n refers to a different SoC level used for the calibration procedure. Then, the rough estimates $Z_{L,n}^{\text{post}}$ are corrected by applying the inverted (10) to obtain the final estimates of the battery impedance $\hat{Z}_{\text{bat}}(f_i)$.

Fig. 6(a) shows comparison of the calibrated estimates of the battery impedance $\hat{Z}_{\text{bat}}$ (circles) with the reference values (lines) over the calibration dataset composed of $n = 3$ different SoC values, showing the goodness of the calibration procedure. For a better reading of Fig. 6(a), only 12 of the 25 frequency points of the multisine sequence are shown. To further validate the calibration process, the calibrated impedance analyzer is compared with the reference instrument over a different dataset (different SoC levels) in Fig. 6(b). In both the cases, the error of the estimated impedance is less than 3 mΩ, as shown in Fig. 6(c).

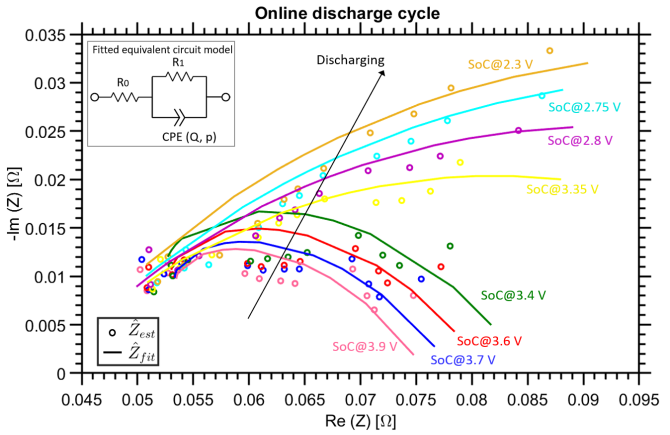

Fig. 7. Online acquisition of the impedance spectra by the calibrated impedance analyzer prototype during the discharge process by a constant dc current.

D. Online Measurements

The calibrated impedance analyzer prototype is tested and validated in the case study of online monitoring of the battery impedance spectrum. To this aim, we reproduce the discharge process of the battery sample (Samsung ICR18650-26J) through an electronic load. The battery is connected to the Keithley 2450 source measurement unit (SMU) that emulates the electronic load with a constant sink current of 400 mA, and the impedance Z_{bat} is constantly monitored by the proposed impedance analyzer. Fig. 7 shows the evolution of the impedance spectrum during the discharge cycle covering the entire SoC space. The calibrated estimates of the battery impedance $\hat{Z}_{\text{est}}$ (circles) are compared with fitted values $\hat{Z}_{\text{fit}}$ (lines) obtained using a simplified Randles model consisting of a resistor in series with a parallel connection between a constant phase element (CPE) and a resistor. This equivalent circuit differs from the standard Randles model by the lack of the series Warburg element, which models the mass transfer phenomena. This is reasonable because mass transport occurs at frequencies lower than the excited ones. The impedance of the fitting model is given by

$$\hat{Z}_{\text{fit}}(f) = R_0 + \frac{R_1}{1 + R_1 Q (j2\pi f)^p} \tag{12}$$

where Q and p are the parameters of the CPE. From Fig. 7 it is possible to infer that even though singular estimated points have a large error, the discharging trend of the battery impedance is correctly identified by the measurement system. That proves the capability of the proposed impedance analyzer to monitor the state parameters of the battery online.

E. Emulator

As introduced in Section IV, the results obtained with the SDMS and MLBS sequences, respectively, are compared by means of the battery impedance emulator. The generation frequency is 1 kSa/s for both the sequences. Consequently, the frequency components of the SDMS sequence are f_i = [0.12, 0.24, 0.37, 0.49, 0.61, 0.73, 0.85, 0.98, 1.10, 1.22, 1.34, 1.59, 1.83, 2.20, 2.56, 3.17, 3.91, 4.39, 4.76, 5.74, 6.84, 7.93, 9.52, 11.96, 15.50] Hz. The emulated impedance curve is represented by the blue reference curve of Figs. 8–10.

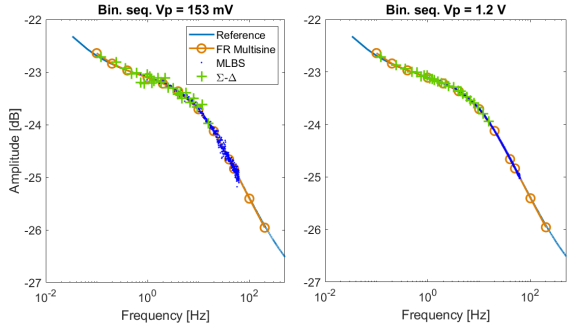

Fig. 8. Amplitude of the emulated impedance measured by means of MLBS and Σ−Δ sequences, for low and high excitation signal amplitude.

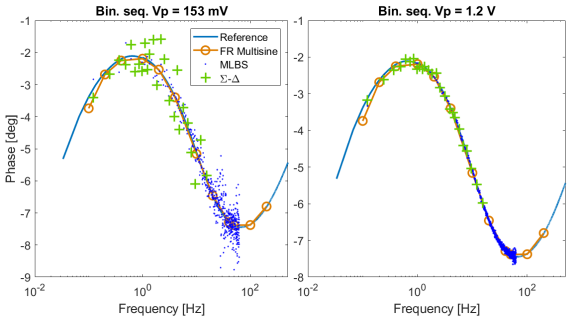

Fig. 9. Phase of the emulated impedance measured by means of MLBS and Σ−Δ sequences, for low and high excitation signal amplitude.

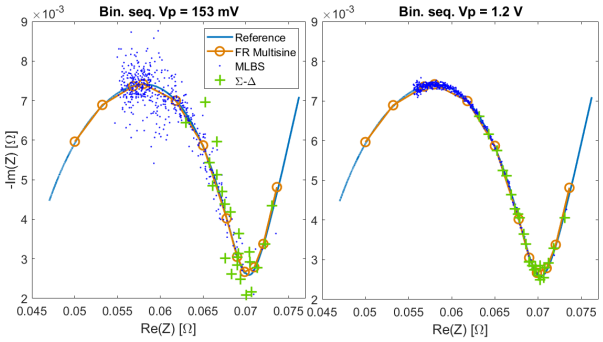

Fig. 10. Cole–Cole plot of the emulated impedance measured by means of MLBS and Σ−Δ sequences, for low and high excitation signal amplitude.

To test the binary sequences, it was not necessary to connect the emulator to the actual impedance analyzer. It has been sufficient to voltage control the emulator input by generating the binary sequences with a bench waveform generator and by acquiring the DAC output with a digital oscilloscope. Since no windowing is applied, the duration of the impulse response $h[k]$ in (3) has been set, for coherent sampling, to be exactly three repetitions of the binary sequences. Also, three sequence repetitions were acquired at each measurement with the oscilloscope.

First, following the calibration procedure illustrated in [32], the emulator has been calibrated by means of a full-resolution (FR) random phase multisine signal obtained by summing sinusoids with frequencies [0.1, 0.2, 0.4, 1, 2, 4, 10, 20, 40, 50, 100, 200] Hz. The rms amplitude of the total signal was V_{rms} = 153 mV, corresponding to a peak-to-peak voltage V_{pp} = 1.2 V for the total signal. The calibrated frequency response for the FR multisine is represented by the orange curve with circles in Figs. 8–10.

The impedance of the calibrated emulator has then been analyzed by means of both the MLBS and SDMS. The main limit of the FR multisine is that V_{pp} increases rapidly as more frequency components are added; hence, both the number of components and V_{rms} have to be kept low to avoid saturation problems. Instead, for binary sequences, V_{rms} is the same as V_{pp}, allowing to inject more power into the system under test before achieving the same peak-to-peak level compliance set to avoid saturation.

To compare the accuracy of the binary sequences with that obtained by means of the FR multisine, $V_{pp} = 153$ mV has been set for the sequences. The resulting response is shown on the left panels of Figs. 8–10. As shown in Fig. 8, the measured impedance amplitude is quite accurate, but the measured impedance phase is very noisy, as shown in Figs. 9 and 10.

Then $V_{pp} = 1.2$ V has been set for both the sequences. As shown on the right panels of Figs. 8–10, the results are quite as accurate as those obtained with the FR multisine, but with the advantage that more frequency components have been excited.

VI. Conclusion

This article investigated the applicability of multisine binary sequences for online and *in situ* monitoring of battery cell impedance. SDMS and MLBS allow for reduced measurement time and effective VLSI implementation of the measuring system, since they excite many frequency points at the same time and rely on binary excitation. The two excitation sequences were compared in the analysis of the impedance of a battery emulator, reporting similar accuracy and dependence on the excitation level. In particular, the analysis on the impedance emulator has shown that binary sequences allow to inject more power into the system and excite a greater number of frequencies with respect to an FR multisine signal. Indeed, the peak voltage of FR multisine increases rapidly as more frequency components are added, while the peak-to-peak voltage of a binary sequence does not depend on the number of components. To demonstrate the applicability to online and *in situ* EIS monitoring of battery cells, an architecture of impedance analyzer exploiting the binary nature of SDMS and MLBS and suitable to be implemented in VLSI technology was presented. A proof of concept was realized using off-the-shelf components. Though the architecture can be used with either SDMS or MLBS, the realized prototype is limited to the former kind of excitation due to the maximum peak excitation current of 1 mA. After calibration, it was compared with a benchtop reference instrument, showing an average deviation of less than 3 mΩ. The prototype was validated in online EIS monitoring of a commercial battery cell during its discharge process.

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