Verification of a Capacitive Voltage Divider With 6-μrad Uncertainty Up To 100 kV

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Abstract—A reference setup for system calibration of industrial transformer loss measurement (TLM) systems consists of three main components, a voltage divider, a current transformer, and a power meter, and their phase displacements should each not be more than 10 μrad to achieve an overall system uncertainty of better than 20 μW/VA. We have extensively verified the uncertainty level of the current-comparator-based capacitive voltage divider (CVD) used in the TLM reference setup of the Van Swinden Laboratorium (VSL), both from the component level and the system as a whole. Different practical conditions relevant for on-site measurements are considered, e.g., measurement cable lengths, cable types, and grounding. The verification measurement results show an agreement of better than $(6 \pm 6) \times 10^{-6}$ in ratio error and (4 ± 6) μrad in phase displacement between the CVD component and system calibrations up to 100 kV. Requirements for achieving this agreement are adequate grounding of the CVD and the use of triax cable between the high-voltage (HV) capacitor and the CVD low-voltage electronics in case large distances have to be covered on-site. The (4 ± 6) μrad agreement in phase displacement is well within the required 10 μrad limit for voltage measurements as part of on-site TLM system calibrations with 20 μW/VA overall uncertainty at low power factors.

Index Terms—Calibration, capacitive voltage divider (CVD), high voltage, loss measurement, power transformer, uncertainty, verification, voltage divider (VD), voltage transformer (VT).

I. INTRODUCTION

POWER transformer losses account for a significant part of the total network losses. These losses not only affect the total cost of ownership but also have a significant environmental impact. Therefore, the European Union has issued a regulation with regard to power transformers, as part of the sustainable energy policies of the so-called "Ecodesign Directive" [1]. Commercial transformer loss measurement (TLM) systems are used by power transformer manufacturers to verify the loss specification of their products during the final factory acceptance tests. These TLM systems need to be calibrated with a much more accurate reference system to guarantee sufficient TLM accuracy and thus reliable TLM test results.

The accuracy of industrial TLM systems can be confirmed by calibrating its individual components or by calibrating the TLM system as a whole [2]. The latter "system calibration" approach has the very significant advantage that lower uncertainties can be achieved, and moreover, this covers all possible systematic errors of the TLM system. The basic approach in the TLM system calibration is to simultaneously apply voltage and current to the TLM system with a stable, adjustable, phase between voltage and current in order to simulate a load with controllable loss to the TLM system. To this end, the Van Swinden Laboratorium (VSL) has developed a reference setup for TLM system calibration, suitable for on-site use at the premises of power transformer manufacturers, which can reach an uncertainty of 0.2% ($k = 2$) at power factor (λ) of 0.01 [3]. This VSL system essentially is a digital implementation of the original analog system of the National Research Council Canada (NRC) [4].

The measurement part of a reference setup for TLM calibration consists of three main components: a voltage divider (VD), a current transformer (CT), and a power meter. The essence of the VSL approach chosen for the test signal generation is a combination of analog current comparator technology with digital sampling techniques to generate test currents with stable and accurate phase angle with respect to the applied high voltage. In load-loss power transformer testing, the current is almost fully orthogonal to the voltage with a typical power factor λ of around 0.01. To reach an uncertainty level of 1% in loss power, a TLM phase uncertainty of 100 μrad must be reached. For the purpose of reaching and proving the best uncertainty levels achievable by the TLM setup, it needs to be calibrated by a reference that is 3–5 times more accurate, i.e., around 20 μW/VA. Therefore, the phase displacements of the individual components of the reference setup for TLM systems should not be more than 10 μrad. Reaching such a low uncertainty is one of the key aims of the European "TrafoLoss" research project [5].

The VD in the reference setup is used to scale the applied high voltages down to the level where they can be measured with a high-accuracy power meter. To achieve the required high accuracy, the VSL reference setup uses one of two available current-comparator-based capacitive voltage dividers (CVDs) suitable for voltages up to 100 and 230 kV, respectively. The CVDs consist of a low-voltage (LV) current-comparator unit (MIL2500A),[1] and high-voltage (HV) and

[1]The manufacturers and instrumentation mentioned in this article do not indicate any preference by the authors nor do they indicate that these are the best available for the application discussed.
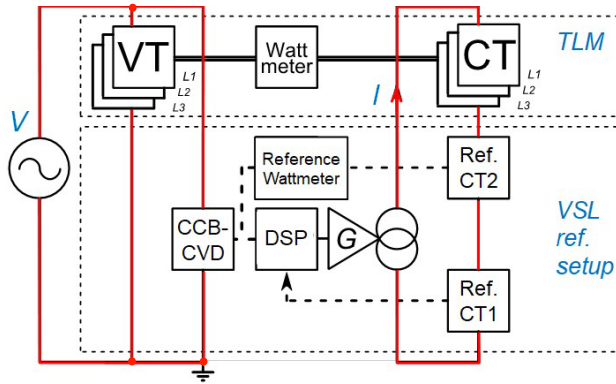
Fig. 1. VSL approach for TLM system calibration with the three-phase TLM system as device under test (DUT; top) and the single-phase reference setup (bottom).

LV capacitors [6]. The advantage of this approach over a conventional voltage transformer (VT) is that it is much less bulky and thus more suitable for on-site measurements and moreover can achieve good phase uncertainties. Although the uncertainties of several reference setups for TLM system calibration were given in [4] and [7]–[10], a detailed evaluation of the VD uncertainty in these setups is not presented so far. Recent work on accurate characterization of VDs focuses on step-up methods for calibration of conventional VTs [11]–[14]. Mohns et al. [25] have recently developed and characterized a CVD; however, this CVD is mainly designed for short-term stability and high linearity to facilitate the step-up characterization of conventional VTs.

In this article, the uncertainty level of the voltage channel used in the VSL reference setup for the TLM system calibration is verified by comparing the results of the CVD calibration as a whole with those of the calibration of the individual CVD components. After a short description of the VSL reference setup for TLM system calibrations, the methodology for verifying the voltage measurement accuracy is presented, and the results from both an LV and HV verification are presented. Furthermore, the impact of different measurement conditions is investigated, such as grounding and long cables required in on-site measurements.

II. TLM SYSTEM CALIBRATION SETUP

Fig. 1 shows the working principle of the reference setup developed at VSL for TLM system calibration. A current-comparator-based CVD provides an LV output of the applied high voltage. A digital signal processing (DSP) unit subsequently generates a driving signal for the transconductance amplifier G that generates the high test current. The actual applied current is measured with an active electronically compensated CT (CT1 in Fig. 1). The DSP unit adjusts the driving signal until the actual phase of the measured current matches that of the given set point. An additional active electronically compensated CT (CT2 in Fig. 1) and reference power meter is used to verify the readings from the digital feedback loop.

The accuracy of reference setup is determined by its main components. The current is measured with electronically

compensated CTs [15] that have very small ratio errors and phase displacements up to 2 kA, less than 2 μA/A and 2 μrad. The two 24-bit analog-to-digital converters (ADCs) inside the DSP that are used to measure the CVD and CT outputs have a relative phase accuracy of better than 0.1 μrad, due to the fact that they are on the same printed circuit board and share the same local clock signal. The ADC gains are calibrated with the reference wattmeter to an uncertainty better than $20 \times 10^{-6}(k = 2)$. The wattmeter itself is calibrated with 10-μW/VA uncertainty ($k = 2$) over the complete power factor range with the VSL primary power setup [16]. Considering all uncertainty contributions, if the total uncertainty of the entire setup needs to reach 20 μW/VA (0.2% in loss power at $\lambda = 0.01$), the phase uncertainty of the CVD should be better than 10 μrad. In an earlier verification of the VSL reference setup [17], the agreement between the VSL and Physikalisch-Technische Bundesanstalt (PTB) phase measurement results component was better than (2 ± 5) μrad, (5 ± 12) μrad, and (10 ± 15) μrad in current, voltage, and power, respectively $(k = 2)$. The aim of the present study is to bring the uncertainty of the phase verification of the voltage channel well below 10 μrad.

III. VERIFICATION METHODOLOGY

The principle of the current-comparator-based CVD is that the VD electronics convert the current generated by the high voltage and an HV capacitor C_{HV} into an output voltage. Ratio and phase accuracy are achieved by converting the output voltage into a current using an LV capacitor C_{LV} and comparing the two capacitive currents in a current comparator that forms the heart of the VD electronics. A feedback loop uses the error signal measured by the current comparator to adjust the output voltage until it exactly matches the applied test voltage, scaled with $C_{\text{HV}}/C_{\text{LV}}$ times the current comparator ratio [6]. Using current comparator ratios ranging from 1:1 to 1:100, a 100-pF HV capacitor, and a 1000-pF LV capacitor, voltages ranging from 1 up to 100 kV can be scaled down to the 100-V level.

Usually, traceability of the voltage channel of the VSL TLMS reference setup is achieved by calibrating its components: the VD electronics and the ratio of capacitors. The CVD total uncertainty can then be derived from the uncertainty in the two-component calibrations. However, practical conditions, which may impact the measurement accuracy, need to be considered as well. For instance, longer measurement cables are needed on-site due to the large dimensions of the test halls of the power transformer manufacturers. The harsh environment of such a test hall also requires measurement cables with better anti-interference performance and particular care to adequate grounding. Unfortunately, the calibration of the individual components is unable to include these effects. Therefore, even though calibrating the setup as a whole is more difficult to perform with low uncertainties, this approach is preferable since it covers all possible systematic measurement errors. The methodology of the present study is to compare the calibration results of the whole CVD with those from the component level under conditions representative for on-site use of the CVD, with the aim to verify and prove the traceability and declared uncertainty level of the component calibration.
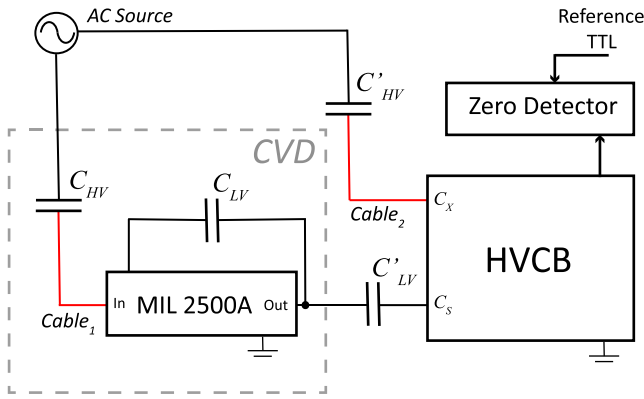
Fig. 2.   Measurement schematics for calibration of the CVD as a whole, using an HVCB and two additional HV and LV capacitors, C'_{HV} and C'_{LV}.
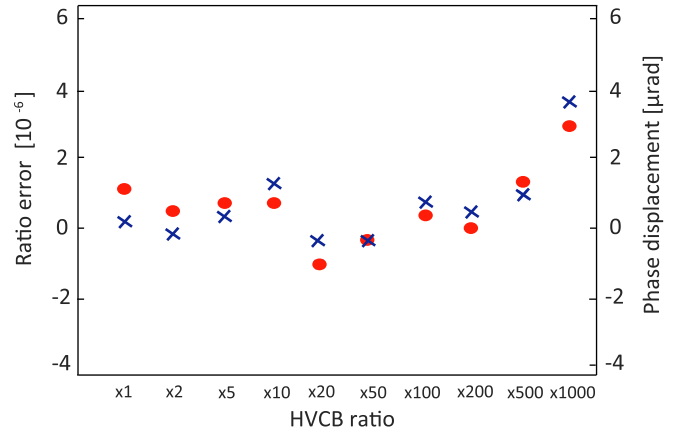

Fig. 3.   Difference in HVCB calibration results for ratio error (crosses) and phase displacement (circles) between VSL and NRC at 50 Hz for all HVCB ratios.

The CVD in the VSL reference setup for TLM system calibration is composed of an MIL2500A unit with either 100- or 200-kV range as the LV current-comparator unit, a Highvolt 100 kV or Vettiner 230-kV 100-pF HV capacitor C_{HV} and a General Radio (GR) 1404A 1000-pF LV capacitor C_{LV}. For the component calibration, the C_{HV}/C_{LV} capacitance ratio and the MIL2500A unit are calibrated using a highly accurate Guildline 9910A high-voltage capacitance bridge (HVCB) [18]. Fig. 2 shows the schematic of the setup for verification of the complete CVD using the HVCB. Here, the HVCB compares the two alternating currents generated by two additional HV and LV capacitors connected to, respectively, the CVD input and output voltage [19].

A. HVCB Uncertainty

The HVCB is a key instrument in both the component calibration of the CVD as well as in the calibration of the CVD as a whole. The uncertainty achieved in comparing these calibration methods thus strongly depends on a low uncertainty of the HVCB. Although the specification of the Guildline 9910A HVCB gives an uncertainty of 20×10^{-6} for ratio error and 20 μrad for phase displacement, a much lower uncertainty can be achieved by calibrating the bridge errors using a set of high-quality capacitors (like hermetically sealed GR 1404 capacitors) [20].

The HVCB at VSL has been calibrated regularly using this method, and the results are extremely stable with standard deviations of typically 0.8×10^{-6} for ratio error and 0.8 μrad for phase displacement in the past years. Fig. 3 shows the results of the differences in calibration results from VSL and NRC of the different HVCB ratios at 50 Hz for both ratio error and phase displacement. These differences are not more than 1.1×10^{-6} for ratio error and 1.1 μrad for phase displacement for the 1:1 up to 1:100 ratios used in the CVD verification [21]. This agreement is significantly better than up to 8×10^{-6} differences in ratio error found in the comparison of HVCB calibration results achieved earlier by the Korea Research Institute of Standards and Science (KRISS) and NRC [20].

In addition to the HVCB calibration uncertainty, the impedance of the internal windings of the HVCB will have an impact on the measurement results due to the
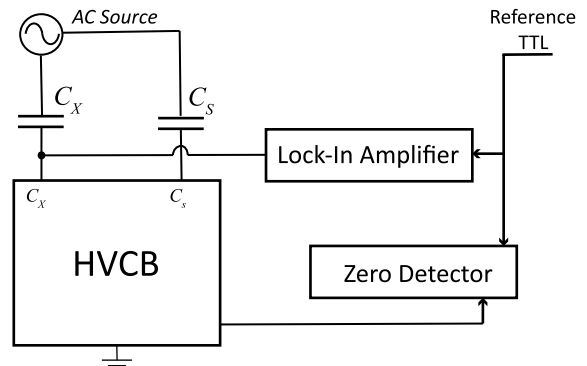
Fig. 4.   Measurement schematic for determining the N_x winding impedance of the HVCB. For each N_x winding value, the values of C_s and C_x are set to match the N_s/N_x winding ratio.

voltage drop across this impedance during the actual use of the HVCB. In order to quantify this impact, the winding impedance of the HVCB has been determined at 60 Hz for all N_x winding ratios in an experiment, as shown in Fig. 4. The voltage drop at the C_x arm has been measured with the lock-in amplifier for the bridge ratios used in the CVD verification and the resulting magnitude of the winding impedance is shown in Table I. The N_s winding impedance has been determined in a similar way and found to be equal to 6.0 Ω. The winding impedances have also been determined at 45 Hz, resulting in values that are (0.744 ± 0.010) $(k = 2)$ times those found at 60 Hz. It is, therefore, concluded that the HVCB input impedance essentially is inductive and thus will only impact the ratio error measurements and not the phase displacement results.

In the determination of the C_{HV}/C_{LV} ratio, the 100-pF capacitor C_{HV} is connected to the C_s input of the HVCB, and the 1000-pF capacitor C_{LV} is connected to the C_x input. Given the measured N_x and N_s winding impedances and the impedances of the 100- and 1000-pF capacitors at 60 Hz, the impact of the HCVB input winding impedance in this measurement is less than 1×10^{-6}. However, during the CVD calibration as a whole as shown in Fig. 2, the 1000-pF

TABLE I

VALUE OF THE N_x WINDING IMPEDANCE AT 60 Hz FOR THE DIFFERENT
HVCB N_s/N_x WINDING RATIOS USED IN THE CVD VERIFICATION

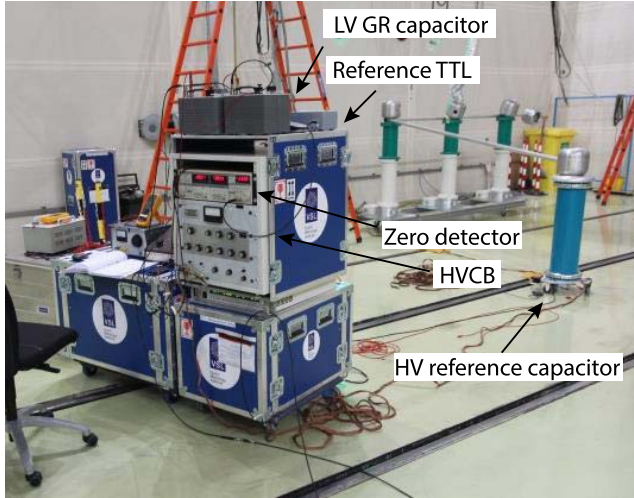| Ratio	x1	x2	x5	x10	x20	x50	x100
$\lvert Z \rvert$ [Ω]	10.2	5.1	2.2	1.2	0.7	0.4	0.3

Fig. 5. Measurement setup for on-site calibration of VDs, using an HVCB and additional HV and LV reference capacitors.

capacitor is connected to the C_s input of the HVCB. With a capacitor impedance of 2.65×10^6 Ω at 60 Hz, this causes a deviation of $6.0/(2.65 \times 10^6) = 2.3 \times 10^{-6}$ in ratio error. The 100-pF capacitor connected to the C_x input has at most an impact of $10.2/(2.65 \times 10^7) = 0.38 \times 10^{-6}$ in ratio error for the measurement of the lowest CVD voltage range where the HVCB is used in 1:1 ratio.

B. Calibration Procedure

The complete verification procedure of the CVD consists of the following three steps.

1) The ratios C_{HV}/C_{LV} and C'_{HV}/C'_{LV} are determined at 700 V using the HVCB. The capacitors C_{HV} and C'_{HV} are either GR 1404 capacitors for tests up to 700 V or HV capacitors (Vettiner and Highvolt) for tests between 1 and 100 kV.
2) The MIL2500A unit is calibrated with the HVCB using the known ratios of capacitors in a capacitor bank, calibrated immediately before use.
3) The entire CVD is calibrated as shown in Fig. 2 using C'_{HV} and C'_{LV} in combination with the HVCB. Since the ratio C'_{HV}/C'_{LV} as well as the HVCB errors are known, the deviation of the entire CVD can be determined.

Fig. 5 shows an overview of the actual measurement setup for the third step, the calibration of a VD using the HVCB.

Finally, the results of the calibration of the CVD as a whole (third step) are compared to the results expected based on the calibration of the individual CVD components (first two steps). The agreement of the two calibration approaches can

be evaluated by

$$\Delta = e_{sys} - e_{comp} \qquad (1)$$

where e_{sys} is the measured complex ratio error of the CVD as a whole and e_{comp} is the calculated complex CVD error based on the calibration of its individual components.

The value of e_{sys} can be determined as follows:

$$e_{sys} = \frac{C'_{HV}}{C'_{LV}} \cdot \frac{N_x}{N_s} \cdot \delta C'_{HV}(V) \cdot (A + jD) \qquad (2)$$

where N_x/N_s is the HVCB bridge ratio used in the CVD calibration as a whole (step 3), $\delta C'_{HV}(V)$ is a correction for the known voltage dependence of C'_{HV}, A is the ratio error reading, and D is the dissipation factor (DF) reading of the HVCB in the calibration. The correction for the voltage dependence of C'_{HV} is needed since the calibration of C'_{HV}/C'_{LV} is performed at 700 V and C'_{HV} is subsequently used at high voltages in the verification experiment. This voltage dependence only affects the ratio error and was determined by comparison against two 800- and 1000-kV capacitors whose voltage dependence is assumed to be negligible up to 230 kV. The values of e_{comp} for ratio error are obtained as given in the following equation:

$$e_{comp} = r_{MI} \cdot \frac{C_{HV}}{C_{LV}} \cdot \delta C_{HV}(V) \qquad (3)$$

where r_{MI} is the ratio of MIL2500A unit at the applied range and $\delta C_{HV}(V)$ is the correction for the known voltage dependence of C_{HV}. The values of r_{MI}, C_{HV}/C_{LV}, and C'_{HV}/C'_{LV} in (3) are the actual measured values, corrected for the ratio error and phase displacement of the 1:10 ratio of the HVCB bridge used in the measurement.

IV. MEASUREMENT RESULTS

In order to find out what agreement can be achieved in the CVD verification, first, an LV experiment was performed on the 2-kV range of the 200-kV CVD with high-quality (GR) reference capacitors. Following this experiment, an HV verification was performed for all CVD ranges of the 100-kV CVD. The experiments were completed by verification of the CVD voltage linearity, the effect of different grounding schemes, and the effect of different cable types and cable lengths.

A. LV Verification

To study the best-achievable uncertainty limits of the CVD verification, an experiment was performed on the 2-kV range of the 200-kV CVD, following the schematic shown in Fig. 2, using high-quality 100- and 1000-pF capacitors (GR, model 1404) for C_{HV} and C'_{HV} and C_{LV} and C'_{LV}, respectively. In this experiment, Cable$_1$ in Fig. 2 is a 2-m RG-58 coax cable and the regular C_s, C_x connections to the HVCB are made using 3-m RG-58 coax cables. Fig. 6 shows the results for this reference case at an input voltage of 700 V, 60 Hz, for different choices of GR capacitors for C'_{HV} and C'_{LV}. The results for the ratio errors have been corrected by -2.3×10^{-6} related to the nonnegligible N_s input impedance of the HVCB as discussed in Section II. It is noted that this correction incorrectly was

TABLE II

DIFFERENCES IN RATIO ERROR AND PHASE DISPLACEMENT, CALCULATED USING (1) AND MEASURED AT 700 V, 60 Hz, IN THE 2-kV RANGE OF THE 200-kV CVD BETWEEN THE REFERENCE CASE AND THAT USING 100-pF HV CAPACITORS (HIGHVOLT AND VETTINER) WITH ADDED 5-m TRIAXIAL CABLE. FOR EACH C'_{HV}-C_{HV} COMBINATION, TWO MEASUREMENTS (A AND B) ARE PERFORMED, ABOUT 20 min SEPARATED IN TIME

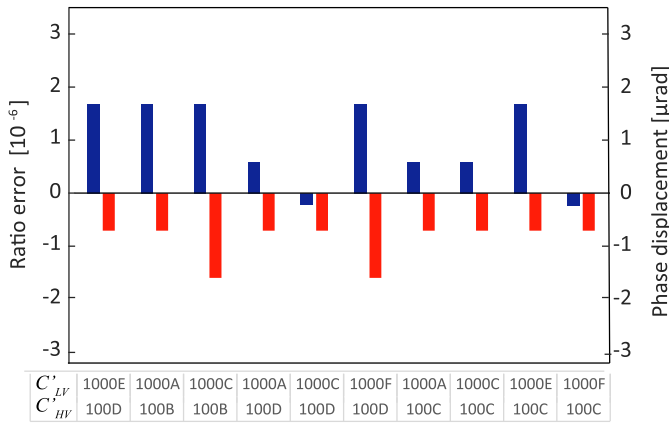| C'_{HV}	Highvolt		Vettiner	
C_{HV}	Vettiner		Highvolt	
Measurement	A	B	A	B
Ratio error [10^{-6}]	1	-1	0	-3
Phase displacement [μrad]	1	1	0	0

Fig. 6.   Values of differences in ratio error (blue) and phase displacement (red), calculated using (1) and measured at 700 V, 60 Hz, in the 2-kV range of the 200-kV CVD for the reference case with short cables for different GR model 1404 capacitors with different deviations from nominal capacitance value ($\pm$100 μF/F) and different phase displacements (differences $\pm$15 μrad).

not considered in an earlier presentation of the preliminary results of the LV verification [22].

It can be seen that the ratio error differences are all within 2×10^{-6}, and similarly, those for phase displacement are less than 2 μrad.

Following these excellent results, the 100-pF GR 1404B capacitors used as C_{HV} and C'_{HV} were replaced by two 100-pF HV capacitors (Highvolt 100 kV and Vettiner 230 kV). In this experiment, Cable$_1$ (see Fig. 2) still is a 2-m coax cable, but Cable$_2$ now is a 5-m triax cable (BELDEN 7784AF) plus the regular 3-m coax for connection to the HVCB. Table II shows the results for this case. For each combination of HV capacitors, two measurements were performed, approximately 20 min apart. The agreement in phase displacement is again excellent and stable in time, with a maximum difference of 1 μrad. The agreement in ratio error is similar but becomes slightly worse over time with a maximum difference of -3×10^{-6}. This very likely is caused by the significant temperature dependence of the HV capacitors of around $+20$ (μF/F)/K in combination with a temperature variation of the VSL laboratory environment. Changing the C_{LV} capacitor in the experiment gives very similar results as those given in Fig. 6: the variation in ratio error and phase displacement
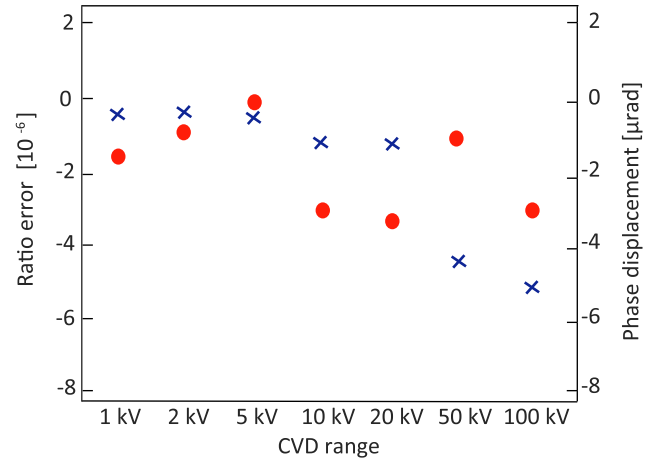

Fig. 7.   Values of differences in ratio error (crosses) and phase displacement (circles), calculated using (1) and measured at nominal input voltage, 60 Hz, for all seven ranges of the 100-kV CVD.

is at most 2×10^{-6} and 2 μrad, respectively. The conclusion is that the 100-pF HV capacitors essentially give similarly good results in the LV CVD verification as the 100-pF GR 1404B reference capacitors.

B. HV Verification

Once it was clear that the LV verifications described in Section IV-A gave good results, all ranges of the 100-kV CVD were verified at their nominal input voltages following the schematic given in Fig. 2 and with the Highvolt and Vettiner HV capacitors as C_{HV} and C'_{HV}, respectively. The HV capacitors were connected to the MIL2500A unit and HVCB using 5-m triax cables. Fig. 7 shows the result of this key experiment of the present study. For all ranges, the agreement in phase displacement between the CVD component calibration and the CVD full calibration is better than 4 μrad. The agreement in ratio error is better than 2×10^{-6} for the five lowest voltage ranges of the 100-kV CVD, i.e., up to 20 kV. For the 50- and 100-kV range, the agreement in ratio is slightly worse but still within 6×10^{-6}. This larger disagreement may be caused by insufficient knowledge of the voltage coefficient of the HV capacitors, which were determined as $((+16 \pm 3)\ \mu$F/F$)/(100$ kV$)^2$ for the Highvolt HV capacitor and $((+4 \pm 2)\ \mu$F/F$)/(200$ kV$)^2$ for the Vettiner HV capacitor. Since the present verification measurements have been performed up to 100 kV, the voltage dependence of the Vettiner HV can almost be ignored and the main voltage dependence originates from the Highvolt HV capacitor.

Tables III and IV show the uncertainty budget for the phase displacement of the CVD component calibration and CVD system calibration, respectively. The uncertainty analysis for the ratio error gives similar budgets. However, in on-site applications of the CVD, there will be additional uncertainty contributions to the ratio error given the significant temperature coefficient of the capacitance of the HV capacitor in the CVD. Fortunately, in view of the CVD being (or intended to be) used for measuring transformer losses at low power factors, the impact of the ratio error decreases with decreasing power factor.   The first two uncertainty contributions in Table III

TABLE III
UNCERTAINTY BUDGET FOR THE PHASE DISPLACEMENT OF THE CVD
COMPONENT CALIBRATION ($k = 1$)

Quantity	standard uncertainty [μrad]
C_{LV}/C_{HV} ratio	0.8
MIL2500A calibration	1
HVCB 1 : 10 ratio (2x)	1.8
Capacitor build up	1
Cable effects	1.2
Total uncertainty	2.7
Total uncertainty ($k = 2$)	5.4

TABLE IV
UNCERTAINTY BUDGET FOR THE PHASE DISPLACEMENT OF THE CVD
SYSTEM CALIBRATION ($k = 1$)

Quantity	standard uncertainty [μrad]
C'_{LV}/C'_{HV} ratio	0.8
HVCB repeatability	0.8
HVCB 1 : 10 ratio	0.9
HVCB ratio	1.5
Cable effect	1.2
Total uncertainty	2.4
Total uncertainty ($k = 2$)	4.8

are the repeatabilities in the C_{LV}/C_{HV} capacitance ratio and MIL2500A calibrations, respectively. The 0.9-μrad standard uncertainty of the HVCB 1:10 ratio comes in twice (linear addition of uncertainties, fully correlated) since this bridge ratio is used both in the capacitance ratio measurement and the MIL2500A calibration. The final two uncertainty contributions are from the capacitor bank build up used in the MIL2500A calibration and the residual effects of cables on the CVD respectively. Table IV shows similar uncertainty contributions, with now the HVCB repeatability in the CVD calibration (see Section III-B, step 3 of the experiment) instead of the MIL2500A calibration repeatability. A further major difference is a single contribution of the HVCB 1:10 ratio since this ratio is only used during the C'_{LV}/C'_{HV} measurement. A 1.5-μrad uncertainty covers the uncertainty in the HVCB ratio used in the CVD calibration. This ratio ranges from 1:1 for the 1-kV CVD range to 1:100 for the 100-kV CVD range.

Based on these two budgets and considering the correlation between the HVCB 1:10 ratio contributions in both the CVD component and the system calibration, the expanded uncertainty in the difference Δ between the results of the system and component calibration (1) becomes 6 μrad ($k = 2$) . Therefore, the final result for the agreement in phase displacement between the CVD component calibration and the CVD system calibration is better than (4 ± 6) μrad for all CVD ranges.

One of the claimed major advantages of a CVD with respect to a conventional VT is the linearity as a function of input voltage. Therefore, the linearity of all seven ranges of the 100-kV CVD has been verified over 20%–120% of the range (with the verification of the 100-kV range limited to 100% of the range given the maximum voltage of the Highvolt
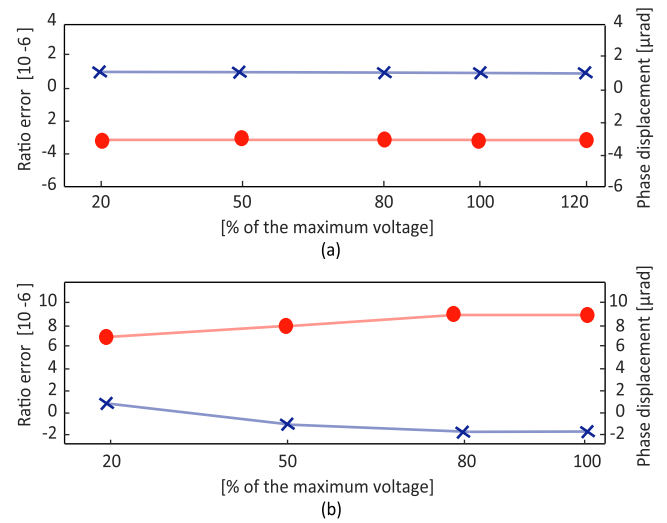

Fig. 8. Values of ratio error (crosses) and phase displacement (circles) as a function of input voltage for (a) 10-kV and (b) 100-kV voltage range of the 100-kV VSL CVD.

capacitor). Using the HVCB together with the Vettiner HV capacitor and a reference LV capacitor in a setup as in Fig. 2, for each voltage range of the CVD, the test voltage was changed from 20% up to 120% of the rated voltage of that range, and the variation in HVCB bridge reading at balance was recorded. Fig. 8 shows the results of this verification, where the changes in ratio error and phase displacement are shown as a function of input voltage for the 10- and 100-kV ranges of the VSL CVD. The result of the 10-kV range is typical for the five lowest CVD ranges: no change is observed in ratio error and phase displacement within the 1-ppm HVCB bridge resolution over the full range of 20%–120% input voltage. The 50- and 100-kV ranges show a slight variation of ratio error and phase displacement. The worst result that of the 100-kV range with changes of 3×10^{-6} and 2 μrad in ratio error and phase displacement, respectively, is given in Fig. 8. The change in ratio error as a function of input voltage becomes negligible for both the 50- and 100-kV ranges if a voltage coefficient of $(+13 \ \mu F/F)/(100 \ kV)^2$ is assumed instead of the $(+16 \ \mu F/F)/(100 \ kV)^2$ mentioned above. For the measurement executed in Sections IV-C and IV-D, the applied testing voltage is 100% of the rated voltage of each range with an error less than 1%.

C. Shielding and Grounding

Correct shielding and grounding is extremely important in high-accuracy HV measurements, in particular in on-site measurement campaigns [23], [24].

To limit interference from the mains supply within the measurement instrumentation, both the LV electronics of the CVD and the HVCB are supplied from a separate APT LS500 AC power source set at an output voltage of 220 V and an output frequency different from the 50-Hz mains, e.g., 56.3 Hz. It is found that this is crucial for achieving high-accuracy results, such as those shown in Section IV-B and in Fig. 3 on the HVCB calibration. Another measure taken to limit the interference of the applied HV voltage and ground

TABLE V

CHANGE IN RATIO ERROR AND PHASE DISPLACEMENT FOR SEVERAL CVD VOLTAGE RANGES WHEN DIFFERENT LENGTHS OF COAX CABLE ARE ADDED AT THE CABLE$_1$ POSITION IN FIG. 2

CVD Voltage range	1 kV			2 kV			10 kV			100 kV		
Cable length	5 m	10 m	20 m	5 m	10 m	20 m	5 m	10 m	20 m	5 m	10 m	20 m
Ratio error [10^{-6}]	0	0	0	-1	0	-1	0	0	0	0	0	0
Phase displacement [μrad]	-7	-22	-44	-3	-10	-18	0	-2	-5	0	-1	-3

currents running in the safety ground is the use of triax cables between the output of the HV capacitors and their respective LV electronics. The main advantage of the triax cables is the shielding of the inner signal wire by the intermediate (guard) shield from the outer cable shield.

The CVD allows for different grounding configurations that appear to result in slightly different measurement results. The MIL2500A unit of the CVD is placed in a mobile rack, which is convenient for on-site usage. This rack, as well as the HVCB, is always connected to the star ground in the HV room. However, the analog (measurement) ground of the MIL2500A electronics can be grounded separately. One option is to determine the low potential of the electronics ("ANA" terminal) via the guard of the triax cable that is connected to the ground inside the HV capacitor. A second option is to connect the ANA terminal to the HVCB ground. The third option is to have both ground connections in place, which refers to the case that the ANA terminal is grounded via the guard of the triax cable connected to the HV capacitor and also grounded to the HVCB ground. The results of measurements in these three configurations show that the best results are achieved in the second and third configurations; it is very important that the low potential of the output voltage generated by the MIL2500A unit is equal to that of the HVCB measurement bridge. Even though the third configuration results in a ground loop of the measurement circuit, it resulted in slightly better Δ values, and therefore, the third option is recommended. Having both the MIL2500A ANA terminal and the HVCB connected to the same measurement ground via a low impedance apparently is important for getting the best results. In general, the most significant impact of the different grounding configurations is for the CVD voltage ranges above 20 kV, where changes are up to 3×10^{-6} and 5 μrad for the first grounding option. For the third grounding option, the typical impact is only 1×10^{-6} and 2 μrad, and for option, two this is 2×10^{-6} and 3 μrad.

D. Impact of Cable Type and Length

In on-site TLM system calibrations, long cables are needed to cover the physical distances in the test laboratory of the customer. Extension cables may, for example, be needed at the position Cable$_1$ in Fig. 2. Similarly, when calibrating VTs and CVDs on-site, a long cable is required in position Cable$_2$. In order to investigate the impact of cable length in the measurement, a new index is defined as

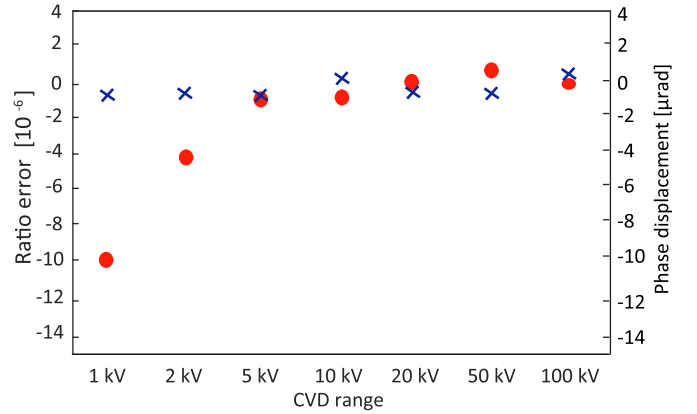$$\Delta_2 = \Delta_s - \Delta_r \qquad (4)$$

Fig. 9.   Change in ratio error (crosses) and phase displacement (circles) for all seven ranges of the 100-kV CVD when a 20-m triax cable is added at the Cable$_1$ position of Fig. 2.

where Δ_r is the Δ value of the reference case with short measurement cables and Δ_s is the Δ value of the specific scenario with extended measurement cables.

Table V shows the results of Δ_2 when a 5-, 10-, or 20-m coax cable is added at the Cable$_1$ position in the CVD verification measurement. The impact of the added cable length appears quite significant for the low-voltage ranges of the CVD. With 20-m coax cable, the impact on the phase displacement of the 1-kV range is more than 40 μrad, but even for the 10-kV range, the effect is still 5 μrad. For the ratio error, the impact of adding additional lengths of coax cable is not significant for all tested ranges.

To improve the on-site phase displacement performance, especially in the lower ranges of the CVD, a triax cable is used instead of the coax cable. Fig. 9 shows the measured values of Δ_2 when a 20-m triax cable is added at the Cable$_1$ position. Similar to the coax cable, the impact of adding the triax cable is negligible for the ratio errors and has a significant influence on the phase displacement for the lower CVD voltage ranges. However, the impact of the triax cable is much less than that of the coax cable. More specifically, the value of Δ_2 with 20-m coax cable for the 1-kV CVD range is -44 μrad, while the effect with the 20-m triax cable is reduced to -10 μrad. For the 2-kV range, these values are -18 μrad and -4 μrad. All practical TLM system calibrations are performed using the 5-kV range or higher CVD ranges. For these ranges, the effect of adding a 20-m triax cable between the CVD HV capacitor and the LV CVD electronics is at most 1×10^{-6} and 1 μrad in ratio error and phase displacement respectively.
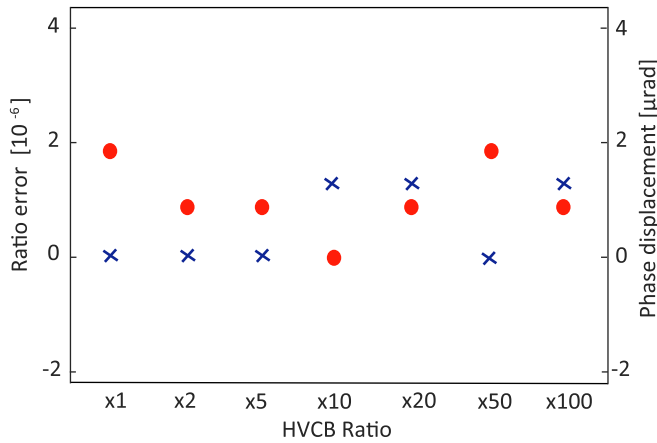
Fig. 10. Change in ratio error (crosses) and phase displacement (circles) for the lower seven ratios of the HVCB when a 20-m triax cable is added at the Cable$_2$ position of Fig. 2.

In on-site VT or CVD calibrations, a long cable may be needed between the HVCB and C'_{HV}, shown as Cable$_2$ in Fig. 2. Fig. 10 shows the impact of adding a 20-m triax cable at this position. Compared to the situation of adding a long cable at the Cable$_1$ position, the impact is much less, not more than 2×10^{-6} or 2 μrad. Therefore, adding a 20-m triax cable at the Cable$_2$ position only has a very marginal effect on the measurement result.

V. CONCLUSION

For calibrations of industrial power TLM systems with 20-μW/VA overall uncertainty level, the voltage channel of the TLM reference setup used in this calibration should have a phase displacement uncertainty of less than 10 μrad for voltages up to 100 kV. We have evaluated the uncertainty ($k = 2$) of the current-comparator-based CVD of the VSL TLM reference setup by calibrating this divider both from the component level and as a whole, for all ranges at nominal input voltage. The uncertainties in these respective calibrations are 5×10^{-6} in ratio error and 5 μrad for phase displacement. For short connection cables, the differences of the measurement values between the whole CVD and the component level are less than (4 ± 6) μrad in phase displacement for all CVD ranges. The agreement for ratio error is at the level of $(2 \pm 6) \times 10^{-6}$ for voltages up to 20 kV and $(6 \pm 6) \times 10^{-6}$ for the 50- and 100-kV CVD range. The slightly higher deviations in ratio error for the highest voltage ranges may be limited by the knowledge of the voltage dependence of one of the HV capacitors used in the experiment. This is also seen in the measurements of the voltage linearity of the different CVD ranges; for all ranges, the ratio error and phase displacement does not change within the 1-ppm measurement resolution between 20% and 120% of the voltage range, except for the 50- and 100-kV CVD range.

For the CVD voltage ranges above 20 kV, the measurement results are sensitive to the different grounding configurations. To achieve the best measurement performance, the analog ground of MIL2500A electronics and the HVCB ground need

to be grounded to the same measurement ground via a low-impedance ground connection. Adding a 20-m coax cable at the MIL2500A unit for the 1-kV voltage range has an unacceptable impact of more than 40 μrad on the phase displacement. Using a triax cable instead, the effect is reduced to around 10 μrad, which is a remarkable improvement. For the voltage ranges of 5 kV and higher, used in practice in the TLM system calibrations, the impact of 20-m triax cable is less than 1×10^{-6} and 1 μrad on ratio error and phase displacement, respectively. Adding the same 20-m triax cable at the HVCB C_{x} input in on-site VT or CVD calibrations has a similarly marginal effect of less than 2×10^{-6} in ratio error and 2 μrad in phase displacement.

In conclusion, our studies confirm that calibration of the components of a current-comparator-based CVD is representative for the behavior of the CVD as a whole within (4 ± 6) μrad ($k = 2$) for phase displacement and $(6 \pm 6) \times 10^{-6}$ ($k = 2$) for ratio error up to 100 kV, provided that the CVD is correctly grounded and that high-quality triax cable is used to connect the HV capacitor with the input of the CVD LV electronics. The uncertainty in ratio error during actual on-site TLM calibrations will be larger due to variations in temperature in combination with the temperature coefficient of the HV capacitor used in the CVD. Fortunately, the effect of temperature on the phase displacement of the current-comparator-based CVD is very small and can be neglected in practice. The (4 ± 6) μrad ($k = 2$) agreement in phase displacement is well within the required 10 μrad limit for voltage measurements as part of TLM system calibrations with 20-μW/VA overall uncertainty at low power factors.

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