# Enhancing Nutt-Based Time-to-Digital Converter Performance With Internal Systematic Averaging

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*Abstract*—A time-to-digital converter (TDC) often consists of sophisticated, multilevel, subgate delay structures, when time intervals need to be measured precisely. The resolution improvement is rewarding until integral nonlinearity (INL) and random jitter begins to limit the measurement performance. INL can then be minimized with calibration techniques and result postprocessing. The TDC architecture based on a counter and timing signal interpolation (the Nutt method) makes it possible to measure long time intervals precisely. It also offers an effective means of improving precision by averaging. Traditional averaging, however, demands several successive measurements, which increases the measurement time and power consumption. It is shown here that by using several interpolators that are sampled homogeneously over the clock period, the effects of limited resolution, interpolation nonlinearities, and random noise can be markedly reduced. The designed CMOS TDC utilizing internal systematic sampling technique achieves 3.0-ps root mean square (RMS) single-shot precision without any additional calibration or nonlinearity correction.

*Index Terms*—Averaging, CMOS, delay-locked loop (DLL), integral nonlinearity (INL), jitter, Nutt method, quantization error, time interval measurement, time-to-digital converter (TDC).

## I. INTRODUCTION

A TIME-TO-DIGITAL converter (TDC) measures the time interval between two or more timing signals and presents the result in digital form. For the sake of simplicity, the timing signals are often called start and stop signals. High precision TDCs are used in many applications, such as laser distance measurement [1], [2], high energy physics [3], [4], timing parameter verification of high-speed circuits and components [5], [6], medical imaging [7], [8], single-photon detectors [9], [10], and Raman spectroscopy [11], [12]. The use of TDC techniques is increasing as traditional analog signal processing is challenged by modern scaled IC-circuit technologies, which favor signal processing in the time domain. The critical analog circuit blocks can be often replaced with a TDC-based architecture in all-digital PLLs [13], [14] and in analog-to-digital conversion (ADC) [15], [16], for example.
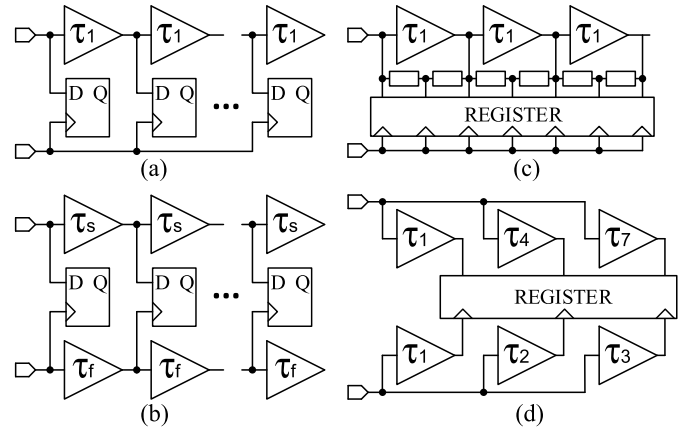
Fig. 1. Architectures for time digitizing: (a) successive delay line, (b) Vernier delay line, (c) successive delay line with resistors, and (d) parallel load-capacitor scaled interpolation.

Many techniques have been developed for the time interval digitization, perhaps the most common of which, as shown in Fig. 1(a), uses the constant propagation delays of identical successive delay elements [17]. The start signal propagates in the delay line and the stop signal registers the state of the delay line, which reveals the number of LSBs between the start and stop. The resolution, $\tau_1$ in this case, is limited by the gate delay, which is the main technology-dependent parameter. A Vernier delay line, shown in Fig. 1(b), uses slow and fast delay elements, $\tau_s$ and $\tau_f$, respectively, to reach subgate delay resolution [17], [18]. The stop-edge propagates in the faster delay line and reaches the slower start-edge of every element after an interval of $\tau_s$-$\tau_f$, which is the resolution (LSB) of the Vernier method. Again, the register result reveals the number of LSBs between the start and stop. A subgate delay resolution can be achieved by dividing the propagation delay using passive resistors, as shown in Fig. 1(c) [19]. Another approach, shown in Fig. 1(d), connects the delay elements in parallel and creates differences into their delays ($\tau_1$-$\tau_7$) with unit capacitor scaling [20]. Several other efficient measurement methods and their combinations have recently been proposed for time digitizing and be able to achieve picosecond-level measurement performance [21]–[28].

As in ADCs, several error sources in TDCs give rise to the measurement uncertainty. The high-resolution conversion structure is necessary to minimize quantization error. Relatively small variations in the delay element delays [differential nonlinearity (DNL)], can accumulate to a high measurement error [integral nonlinearity (INL)] when the timing signals

propagate in a long delay line, for example. Thermal noise and noise in the supply and delay adjusting voltages also create random jitter in the critical time measurement signals. The effect of the error sources becomes more serious as the dynamic range of the TDC increases. For this reason, the direct conversion architectures shown in Fig. 1, with only start and stop timing signals, are not typically used in wide-range TDCs aiming at high (ps-level) precision.

Instead of digitizing the time interval between the start and stop signals directly, the edges of a precise reference clock can be exploited. A simple counter can count the reference clock edges between the timing signals, providing a wide total measurement range at a "low price." In order to achieve subclock period resolution, an interpolator digitizes the time interval between the timing signal and the next/previous reference clock edge. Hence, two high-resolution interpolators are needed for the start and stop signals, but the dynamic range of the interpolators needs to cover only one reference clock cycle. The low jitter and stable reference clock can also be used for stabilization of the TDC under different operating conditions in this measurement technique, often called the Nutt method [29].

This article initially reviews how the interpolation errors get produced within the interpolation cycle and how the systematic errors repeat themselves identically in different clock cycles. It is shown that the measurement error for a certain time interval depends on the location of the start signal within the reference clock cycle. This makes averaging with varying start locations an effective method for reducing the measurement error. This is not always possible, however, due to the single-shot character of the measurement or otherwise limited measurement time.

Generally, ps-level measurement resolution is often achieved with the modern high-speed technology and sophisticated, sometimes multi-level, interpolation structures. The nonlinearities (delay element mismatch) often limit the measurement range and performance and force to utilize lookup tables (LUTs) for INL compensation and calibration steps to ensure high enough accuracy in the measurement. A totally different approach is, however, presented in this article for high-performance time digitizing. A stable, wide range, moderate resolution measurement architecture is created, where the interpolation channel can be easily duplicated. In the proposed approach, a bunch of parallel measurement channels measure in the flash mode the same time interval between the start and stop signals with delayed sampling that covers the full clock period of the TDC (or several clock periods). Thus, the proposed TDC can employ internal systematic averaging to minimize the effect of measurement errors, even in a single measurement shot.

Section II goes through the operation and characteristics of a Nutt-based TDC and explains how averaging can be used to enhance the performance of the method. Section III presents the TDC developed here based on the internal systematic averaging. The full measurement results prove the effectiveness of the concept demonstrating 3.0-ps single-shot measurement precision.
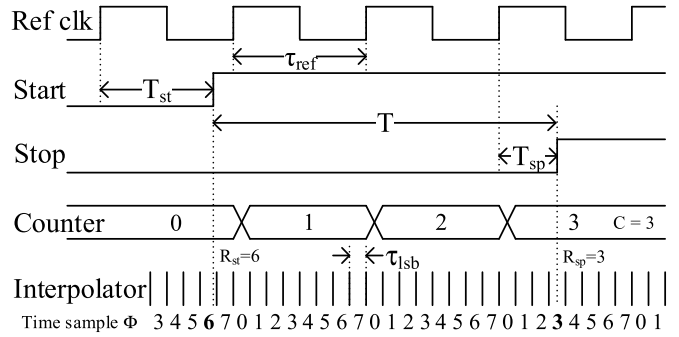


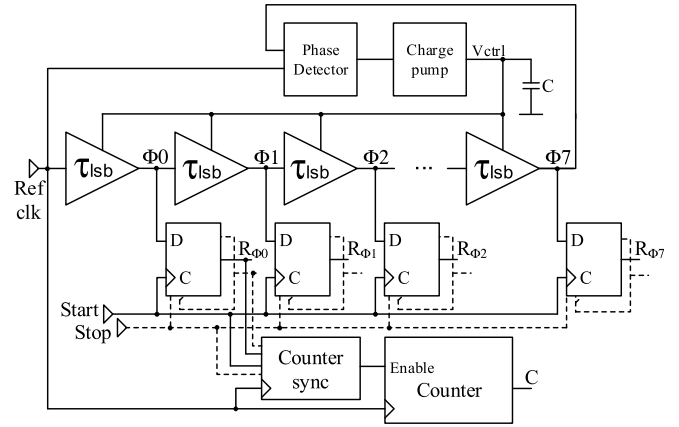Fig. 2. Timing diagram of a Nutt-based TDC.



Fig. 3. TDC realization based on delay line interpolation.

## II. TIME INTERVAL DIGITIZATION BASED ON A COUNTER AND TIMING SIGNAL INTERPOLATION

### A. Operation

The use of a counter together with timing signal interpolation, also known as the Nutt method, is a well-known method for long-range, high-resolution time interval measurement [29], [30]. The counter calculates the periods of a known frequency reference clock between the timing signals start and stop. The measurement range can be extended easily by increasing the width of the counter. The interpolators resolve the time intervals between the timing signals and the nearest reference clock edges ($T_{st}$ and $T_{sp}$ in Fig. 2) with high resolution ($\tau_{lsb}$). Hence, the dynamic range of the interpolator needs to be only one reference clock cycle time ($\tau_{ref}$). The estimate of the time interval $T_m$ is formed by combining the result of the counter $C$ and the interpolator results $R_{st}$ and $R_{sp}$

$$T_m = C \times \tau_{ref} + (R_{sp} - R_{st}) \times \tau_{lsb}. \tag{1}$$

### B. Realization

A Nutt-based TDC in which the interpolation is based on a delay line is a common approach on account of its stability, simplicity, and effectiveness. The example structure, as shown in Fig. 3, relies on the constant propagation delays of matched delay-adjustable digital cells connected in series. The reference clock signal propagates in the delay line and its rising edge

creates time samples $\Phi 0 \ldots \Phi 7$ for the interpolation. The edge of the reference clock arrives at the beginning of the delay line at the same time as the previous edge leaves the chain. A phase detector detects these two signals and controls a charge pump to adjust the delay line control voltage $V_{\text{ctrl}}$ in the case of delay offset due to the temperature or supply voltage change, for example. This delay-locked loop (DLL) structure locks the delay line delay to the reference clock cycle time $\tau_{\text{ref}}$ and forces the interpolation resolution $\tau_{\text{lsb}}$ to a known fraction of $\tau_{\text{ref}}$.

The start and stop timing signals connection to register clock inputs store the state of the delay line at the moment of their arrival, and the interpolation result can be decoded from the registers. The counter shown in Fig. 3 counts the number of full reference clock cycles between the timing signals, as stated above. Its counting, however, needs to be synchronized to the results of the interpolator so that the results are compatible in all cases [30]–[32].

### C. Measurement Uncertainty

Several error sources create measurement uncertainty in the Nutt-based time digitization. Quantization error results in finite measurement resolution when an analog quantity is converted to a discrete value. In the presented architecture, Fig. 3, the resolution corresponds to the delay element propagation delay $\tau_{\text{lsb}}$, which is highly technology-dependent.

The DNL describes the deviations of the quantization steps (resolution) from the ideal value of 1 LSB. Nonhomogeneity in the silicon process parameters or random variations in the layout and noise sources, which systematically interfere with the signal propagation, such as systematic crosstalk or supply voltage noise, create static delay differences in the delay elements, shown as nonhomogenous measurement resolution.

The INL is a consequence of the accumulation of errors in the resolution (DNL). When the reference signal propagates through the delay line, Fig. 3, the delay deviations of individual elements sum and cause nonlinearity in the interpolation. The total delay line delay, including the DNLs, is nevertheless locked to the reference clock cycle time with a DLL. Hence, the total sum of the DNLs over the delay line is 0, which sets the INL after the last element also at 0. The delay line shown in Fig. 3 is common and hence, the INL is quite similar for both interpolators. The differences between start and stop interpolator INLs result mainly from the registers threshold variations.

The jitter in the timing signals and interpolation phases causes random result variation. The jitter is caused by thermal noise, substrate noise, and noise in the control and supply voltages. In the DLL-based architecture, the effect of the reference clock jitter is low, usually below 1 ps [33]. The jitter of the delay elements, however, accumulates during the signal propagation and the maximum jitter is expected at the end of the delay line (in $\Phi 7$ in Fig. 3).

The systematic interpolation errors, quantization error, and interpolator INL repeat themselves identically in different clock cycles. Also, the random delay line jitter repeats its accumulation in every $\tau_{\text{ref}}$. Usually, the timing signals are asynchronous with respect to the reference clock, which means that the start has an equal probability of arriving at any location within $\tau_{\text{ref}}$. Hence, all the errors in the start and stop interpolations vary, when the same time interval is measured several times. It is important to note, that in the Nutt-based TDC, due to the asynchronous character of the timing signals, also the systematic interpolation errors achieve random-like nature. Hence, the architecture is linear by nature (the expected value of the linearity error is zero) [30], [34].

The measured values $T_m$ vary around the mean with a certain statistical variation that can be described with the standard deviation value $\sigma$, usually called the precision. The $\sigma$-value varies when the time interval changes, and hence, root-mean-square (RMS) value $\sigma_{\text{rms}}$ also known as single-shot precision, can be used to indicate the precision within a certain measurement range. In the Nutt-based measurement architecture

$$\sigma_{\text{rms}} \approx \sqrt{\sigma_q^2 + \sigma_{\text{inl-st}}^2 + \sigma_{\text{inl-sp}}^2 + \sigma_{\text{jitter}}^2} \qquad (2)$$

where $\sigma_q = \tau_{\text{lsb}}/\sqrt{6}$ defines the RMS effect of quantization, $\sigma_{\text{inl-st}}$ and $\sigma_{\text{inl-sp}}$ are the standard deviations of INLs in the start and stop interpolators, and $\sigma_{\text{jitter}}$ is the RMS effect of the jitter [35].

### D. Averaging

In the Nutt-based TDC, the results $T_m$ vary around the mean, expected value, when the same time interval is measured several times. The same time interval can be measured A times, for example, and an average value $T_{m-\text{ave}}$ can be calculated from the results. The variation between the averaged results becomes smaller, which means that the averaging improves the precision of the measurement.

The A samples can be collected simply just by repeating the measurement A times [simple random sampling (SRS) method], which improves the precision by $\sqrt{A}$. In this method, the time position of the start hit is random within $\tau_{\text{ref}}$ in each of the separate measurements. Hence, the collected samples may overlap or gather just to a certain part of the interpolator, which limits the precision improvement. A more representative sample group of the errors within $\tau_{\text{ref}}$ forms if the A samples would be collected from the whole nonlinear region not just with equal probability but also evenly. This, however, demands systematic sampling methods.

The averaging, in fact, repeating the same measurement many times, multiplies the measurement time, demands more resources for calculating the result, increases the power consumption, and may prove impossible in many cases. Hence, a TDC architecture providing high precision with a single-shot is still needed (would be preferred).

## III. TDC Based on Systematic Internal Averaging

This section presents a TDC that uses systematic internal (on-chip) averaging, whereupon the need for many successive measurements is replaced by the use of many parallel measurement channels, which provide interpolation results from all over the interpolation region. The goal was to minimize the interpolation error by multiple-sampling of nonrelated
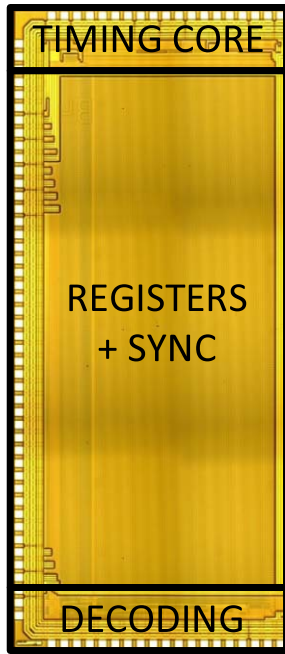
Fig. 4.    IC layout of the TDC.



Fig. 5.    TDC architecture.



Fig. 6.    Delay element structure with W/L ratios. $L$ is always 0.35 $\mu$m.

errors, which would partly compensate each other and thus improve the single-shot precision. The idea is not totally new [23], [26], but here the realization is totally different and the multi-sampling is combined to the linear Nutt-based architecture, which makes ps-level precision possible in a wide measurement range.

The TDC was realized with 0.35-$\mu$m CMOS technology, and the IC layout of the complete TDC is shown in Fig. 4. The layout shows the timing core, the measurement registers, and the decoding logic, which converts the raw measurement data into binary words. The size of the TDC part is 2.6 mm $\times$ 6.6 mm, including pads. The power consumption with a 3.3-V supply voltage and 300-kHz measurement rate is 215 mW.

### A. Operation and Architecture

The TDC developed here, the architecture of which is shown in Fig. 5, uses the DLL delay line interpolation method explained in Section II. The external oscillator, $f_{ref} = 220$ MHz, provides a low, stable jitter reference signal for the measurement. The phase detector and charge pump adjust the delay line delay control voltage $V_{ctrl}$, until the signals in the beginning and the end of the delay line, CLK+, are simultaneous, which stabilizes the delay line against PVT-variations. The delay element, shown in Fig. 6, consist of two parallel delay-adjustable (current starved) inverters, with outputs that are combined with smaller inverters operating in the opposite direction. This structure provides high resolution for the interpolation even though the resolution is based on the gate-delay principle, i.e., $\tau_{lsb} \sim$ inverter delay. The differential reference signal propagates through two parallel inverters, which are in the opposite phase and improve the nonlinearity and immunity to noise as compared with a single-ended structure. The two small inverters maintain the phase difference
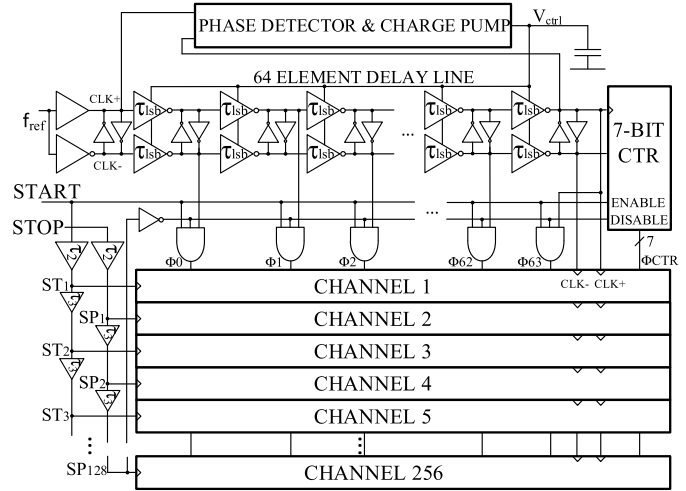
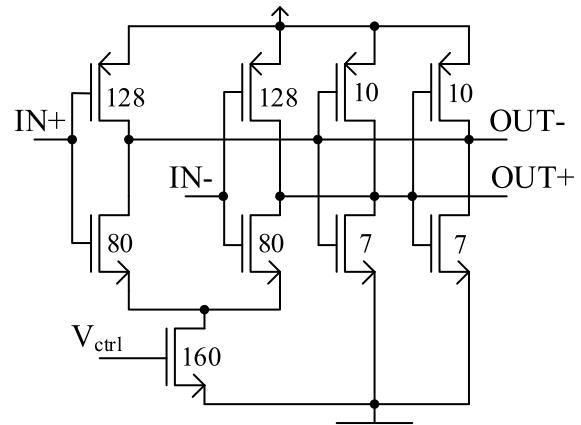between the two propagating signals, while the 64-element delay line creates 64 successive time phases of the reference signal with $\sim$71-ps resolution.

The timing core shown in Fig. 5, including delay line and 7-bit counter, is common to all the measurement channels. The counter provides the total measurement range up to 581 ns. The counter output signals $\Phi_{CTR}$ and the rapidly changing interpolator time phases, $\Phi0\ldots\Phi63$, are wired to a total of 256 parallel and identical measurement channels (interpolation registers). The power consumption is minimized by using AND-gates between the delay line and the measurement channels. The 7-bit counter begins counting when the rising edge of the start signal reaches the IC. At the same time, the AND-gates let the interpolation phases to the measurement registers. The timing signals, storing the state of the delay line, are delayed by $\tau_2$, in order that the interpolation phases have settled to register inputs. The counter counting is disabled and the interpolation phases go back low, after the last measurement channel, #256, has registered the delay line state.

The proposed architecture averages internally by providing 128 samples of the time interval between single start and
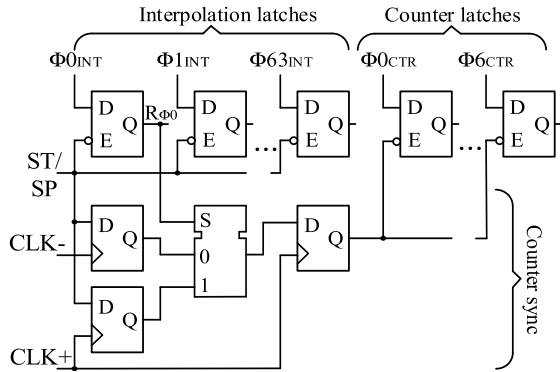
Fig. 7.   Measurement channel including latches and counter synchronization.



Fig. 8.   DNLs of all the 256 measurement channels.



Fig. 9.   INLs of all the 256 measurement channels.

stop input pair. Half of the measurement channels in Fig. 5, every second one, i.e., 128 in total, store the timing core state when the start signal occurs and the other half are for the stop signal. If all the 128 channels would register the timing signal at the same time, the measurement uncertainties would not vary and the averaging would not improve the precision. Hence, a buffer between every pair of measurement channels, delay $\tau_3$, will shift the sampling moment in the direction of the interpolation region, which provides variation in the interpolation error. The absolute value of the noncalibrated buffer-delay $\tau_3$ affects the total sampling time. Here, the sampling of a single timing signal takes $128 \times \sim 200$ ps $\approx 25$ ns and hence, covers over $5\tau_{\text{ref}}$, so that the reference clock jitter will also be averaged.

The measurement channel, in Fig. 7, consists of $64 + 7$ registers (latches), which store the state of the delay line and the counter value when the clock input (E) goes high. Latches were used instead of flip-flops and their dimensions were minimized to minimize the size and power consumption of the TDC. The compatibility of counter and interpolator results is verified with dual-edge counter synchronization structure, presented in detail in [31].

The two adjacent start and stop measurement channels shown in Fig. 5 give one estimate for the time interval with a 13-bit dynamic range and $\tau_{\text{lsb}} \approx 71$ ps resolution (1). The internally averaged total result can be calculated just by summing the results of 128 channel pairs, which creates a 20-bit value with 0.56-ps LSB size (LSB$_{\text{AVE}} = \tau_{\text{lsb}}/128$). The 2 LSB bits of the result do not provide improvement in the performance and can hence be removed, to decrease the width of the data bus, for example.

### B. Interpolator Nonlinearity

The interpolation DNL was estimated by collecting interpolation result histograms for 10-M asynchronous measurements. The number of hits gathered into each interpolation slot reveals the DNL. The time samples for which DNL is positive (LSB is wider) get more hits than average, for example. The TDC DNL variation for all 256 measurement channels (128 start and 128 stop channels), including the 64 interpolation slots, is shown in Fig. 8. The cross is the mean value for the slot DNL when all 256 channels are averaged. The crosses describe
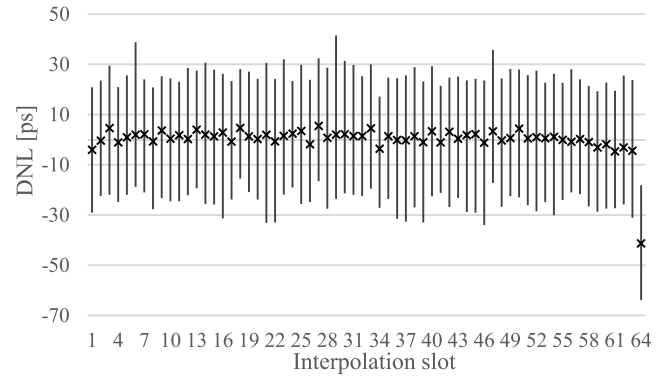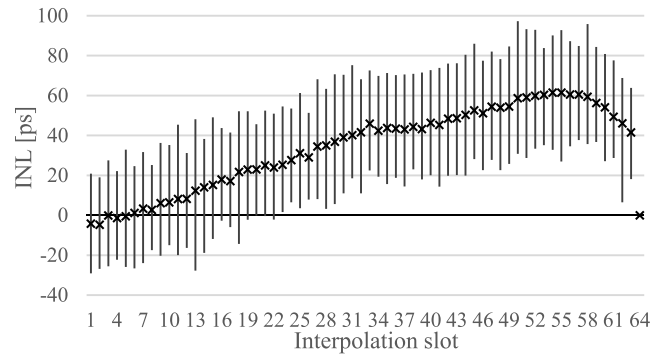
the delay element delay variation around the mean value of $\tau_{\text{lsb}} \sim 71$ ps, which varies very little because the transistor sizes in the delay line are large. The last slots get lesser hits than average, probably due to the nonhomogeneous layout. The max, min, and $\sigma$ values for the averaged delay element DNLs are 5.4, $-41.5$, and 5.7 ps, respectively. The line over each cross describes the DNL fluctuation (max-min) between the 256 measurement channels. Different channels can have a totally different DNL even though the interpolation slot is created by the same delay element. The variation between the measurement channels, $\sigma \sim 9$ ps for every slot, results mostly from variations in the interpolation register thresholds. The register transistor sizes were minimized to achieve small size, low input capacitance, and low power consumption, which at the same time will increase the variation in the time domain operation.

INLs were calculated for each interpolation slot in every interpolation channel based on the DNL data. Again, the crosses in Fig. 9 show the average INL for each interpolation slot and the line over each cross describes how much the INL varies between the 256 interpolation channels (max-min). The INL is at its maximum near the end of the interpolation cycle because the last slots are shorter than average. The most important parameter from the precision point of view is the INL variation. $\sigma_{\text{inl}-\text{st}}$ and $\sigma_{\text{inl}-\text{sp}}$ in different measurement channels fluctuated in the range of 17.5–24.8 ps. When the INL in each interpolation slot is known, the INL error can be subtracted from the measurement results. The INL data
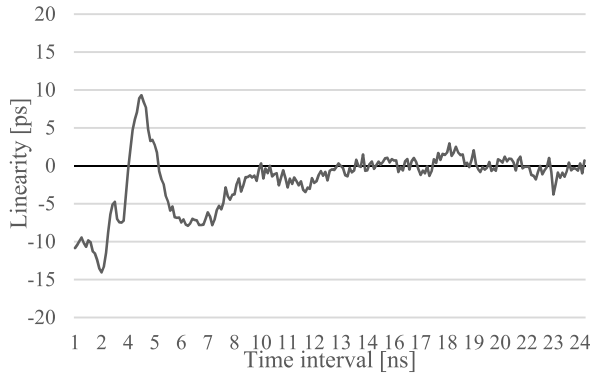
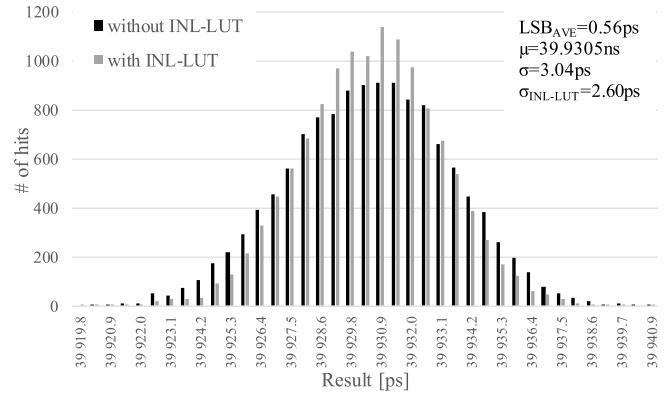Fig. 10.    Linearity error due to crosstalk.



Fig. 11.    Single-shot result distribution with and without INL-LUT when measuring the same time interval 12 800 times.
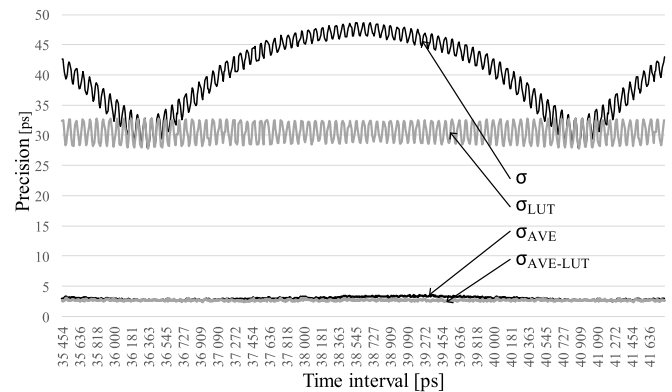


Fig. 12.    Precision variations with different time intervals (over $1\tau_{\text{ref}}$) with and without internal averaging and with and without INL-LUT.

were stored in an INL LUT (INL-LUT) for use in connection with the precision measurements. However, as shown below, by using the systematic internal averaging approach, this compensation is actually unnecessary for the ps-level single-shot precision.

### C. Crosstalk and Temperature Drift

As explained before, also the systematic error sources get randomized in the Nutt-based TDC architecture, which creates more variation to the measurement result but makes the mean, expected result linear. The crosstalk between the timing signals near each other, however, still creates some systematic nonlinearity in the measurement result. The high slew rate timing signals, when they reach the IC, create noise in the supply voltages. The short time supply ringing is systematic and does not cause nonlinearity if the ringing due to the start signal has ended before the stop arrives. With short time intervals, however, the noises of both timing signals combine and create static nonlinearity. The crosstalk error, shown in Fig. 10, was measured by comparing the measurement results with those achieved using another TDC of known nonlinearity. With time intervals between 8. . .581 ns, the nonlinearity was less than the margin of error of the measurement setup, ±4 ps.

Another reason for varying errors in accuracy results from temperature changes. The delay-adjustable delay line controlled by DLL keeps the resolution constant but the reference clock has some temperature drift and the start and stop signal input paths (input-cells, logic, wires, and register thresholds) may also entail differences, which vary with the temperature. When a constant time interval (100 ns) was measured while the temperature of the measurement board was changed from −40 °C to +60 °C, the total drift in the averaged measurement result over the whole temperature range was only 5 ps.

### D. Precision

The precision was measured by means of a pulse generator, power splitter, and coaxial cables of various lengths. The differences in cable length provided a jitter-free time difference between the timing signals when the same pulse was fed to both cables. Fig. 11 shows an example of single-shot result distribution with and without INL-LUT when the same time interval was measured 12 800 times.

The precision measured at different time intervals is shown in Fig. 12. The uppermost curve shows the precision without internal averaging and without an INL-LUT. The precision curve repeats itself with a lapse of $\tau_{\text{ref}}$ due to identical interpolation INL after every new reference edge. The precision finds its minimums, when the time interval is a multiple of the reference clock cycle time because then the INLs in both interpolations are the same and get subtracted in the total result calculation (1). The traditional style of using two interpolation channels yielded $\sigma_{\text{rms}} \approx 42.0$ ps, which can be also calculated with (2).

The second curve from the top shows the precision variation also without internal averaging but when using an INL-LUT, which fixes the INL errors and leaves only the precision variation due to the quantization. Hence, the RMS precision follows $\tau_{\text{lsb}}/\sqrt{6}$, $\sigma_{\text{rms-LUT}} \approx 30.6$ ps. The RMS effect of random jitter, $\sigma_{\text{jitter}}$, in (2), can be calculated to be 9.8 ps.

Fig. 12 also shows the precision and its variation when the internal averaging was used. The two curves in the lower part are precisions with and without an INL-LUT. This architecture collects 128 measurement results for the time interval between single start and stop signals. In the case of random start signal location between the measurements used in averaging (SRS method), the expected improvement in precision would be $\sqrt{128} \approx 11.3$ at the expense of 128 times longer measurement

TABLE I
STATE-OF-THE-ART INTEGRATED WIDE RANGE TDCs

| | This | [21] JSSC | [22] JSSC | [23] VLSI S. | [24] TCASI | [36] GPX2 |
|---|---|---|---|---|---|---|
| Technology | 0.35μm CMOS | 0.35μm CMOS | 0.35μm CMOS | 65nm CMOS | 0.13μm CMOS | NA |
| Type | Flash averaging | Cyclic | Success. approxi. | Parallel sampling | 3D Vernier | NA |
| Range [ns] | 581 | 327000 | 327000 | 98 | 14 | 1.6e10 |
| LSB [ps] | 0.56 | 0.61 | 1.22 | 6 | 7 | 10 |
| INL [ps] | (1) | (1) | (1) | 3 | 10.5 | 20 |
| Single-shot precision[ps] | 3.0 $(2.6)_{(2)}$ | 4.2 $(1.2)_{(2)}$ | 11 $(3.2)_{(2)}$ | <11 | <20.8 | 10 |
| Power [mW] | 215 | 80 | 33 | 0.28 | 0.329 | 60-450 |
| Area [mm$^2$] | 17.2 | 0.61 | 4.45 | 0.12 | 0.28 | NA |

(1) Linear due to Nutt principle (less than margin of error after crosstalk effects)
(2) INL compensated

time. In the proposed design, the interpolation samples are collected evenly over the nonlinear interpolator. The systematic internal sampling method improves the precision by 13.9 in a single measurement shot, so that the RMS values for $\sigma_{\mathrm{rms-AVE}} \approx 3.0$ ps and $\sigma_{\mathrm{rms-AVE-LUT}} \approx 2.6$ ps. Hence, averaging renders the use of an INL-LUT unnecessary.

## IV. CONCLUSION

The Nutt-based TDC architecture consists of the counter and two interpolators, which solve the locations of the timing signals within the reference clock cycle. The counter makes the long measurement range possible and the interpolators define the measurement precision. A remarkable feature is that the interpolation errors vary with asynchronous timing signals. The quantization error, interpolator INL, and random jitter can be noticed as a result variation around the mean value, which changes linearly with the time interval. The result variation can be decreased by making many measurements with the same time interval and calculating the average result.

The TDC developed here exploits internal averaging to achieve picosecond-level single-shot precision with relatively modest delay line resolution ($\sim$71 ps). The measurement architecture was kept as simple as possible, and the measurement channels consist of simple registers so that the number of channels can be easily multiplied. The 256 measurement channels were integrated into the same circuit. Half of them sample the error-free time location for the start-signal and the other 128 channels similarly for stop. The sampling time covers several reference clock cycles and hence averages also the jitter of the external clock.

The prototype and the measurement results prove the efficiency of the TDC concept based on the internal systematic averaging. An RMS single-shot precision of 3.0 ps was reached in a wide measurement range without manual calibrations or LUTs, and this performance was attained with a quite robust 0.35-$\mu$m standard CMOS technology. The nonlinearities do not set the limit for the performance enhancement of the concept, as it is often the case, and even better, below 1-ps precisions, can be expected just by scaling

the technology. More modern technology reduces the result variation in the averaging (especially $\sigma_q$), makes it easier to add even more measurement channels, reduces the circuit size and economizes on the power consumption. The calculation of the average result could also be integrated, which would reduce data transmission and increase feasible measurement rates. The developed architecture is compared to other high performance integrated wide range TDCs in Table I. The proposed straightforward concept offers stable operation, wide range, high linearity, and high precision without technology limitations, external calibrations, or LUTs.

## REFERENCES

[1] B. Turko, "A picosecond resolution time digitizer for laser ranging," *IEEE Trans. Nucl. Sci.*, vol. 25, no. 1, pp. 75–80, Feb. 1978. doi: 10.1109/TNS.1978.4329280.

[2] J.-P. Jansson, V. Koskinen, A. Mäntyniemi, and J. Kostamovaara, "A multichannel high-precision CMOS time-to-digital converter for laser-scanner-based perception systems," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 9, pp. 2581–2590, Sep. 2012. doi: 10.1109/TIM.2012.2190343.

[3] D. I. Porat, "Review of sub-nanosecond time-interval measurements," *IEEE Trans. Nucl. Sci.*, vol. 20, no. 5, pp. 36–51, Oct. 1973. doi: 10.1109/TNS.1973.4327349.

[4] H. Brockhaus and A. Glasmachers, "Single particle detector system for high resolution time measurements," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 4, pp. 707–711, Aug. 1992. doi: 10.1109/23.159692.

[5] J. C. Hsu and C. Su, "BIST for measuring clock jitter of charge-pump phase-locked loops," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 2, pp. 276–285, Feb. 2008. doi: 10.1109/TIM.2007.910109.

[6] C.-W. Fan and J.-T. Wu, "Jitter measurement and compensation for analog-to-digital converters," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 11, pp. 3874–3884, Nov. 2009. doi: 10.1109/TIM.2009.2021209.

[7] W. W. Moses, "Time of flight in PET revisited," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 5, pp. 1325–1330, Oct. 2003. doi: 10.1109/TNS.2003.817319.

[8] A. S. Yousif and J. W. Haslett, "A fine resolution TDC architecture for next generation PET imaging," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 5, pp. 1574–1582, Oct. 2007. doi: 10.1109/TNS.2007.903183.

[9] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128×128 single-photon image sensor with column-level 10-bit time-to-digital converter array," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2977–2989, Dec. 2008. doi: 10.1109/JSSC.2008.2006445.

[10] S. Jahromi, J.-P. Jansson, and J. Kostamovaara, "Solid-state 3D imaging using a 1 nJ/100 ps laser diode transmitter and a single photon receiver matrix," *Opt. Express*, vol. 24, pp. 21619–21632, 2016. doi: 10.1364/OE.24.021619.

[11] L. Pancheri and D. Stoppa, "A SPAD-based pixel linear array for high-speed time-gated fluorescence lifetime imaging," in *Proc. IEEE ESSCIRC*, Athens, Greece, Sep. 2009, pp. 428–431. doi: 10.1109/ESSCIRC.2009.5325948.

[12] I. Nissinen, J. Nissinen, P. Keränen, D. Stoppa, and J. Kostamovaara, "A 16×256 SPAD line detector with a 50-ps, 3-bit, 256-channel time-to-digital converter for Raman spectroscopy," *IEEE Sensors J.*, vol. 18, no. 9, pp. 3789–3798, May 2018. doi: 10.1109/JSEN.2018.2813531.

[13] R. Tonietto, E. Zuffetti, R. Castello, and I. Bietti, "A 3 MHz bandwidth low noise RF all digital PLL with 12 ps resolution time to digital converter," in *Proc. 32nd Eur. Solid-State Circuits Conf.*, Montreux, Switzerland, Sep. 2006, pp. 150–153. doi: 10.1109/ESSCIR.2006.307553.

[14] J.-Y. Lee, M.-J. Park, B.-H. Min, S. Kim, M.-Y. Park, and H.-K. Yu, "A 4-GHz all digital PLL with low-power TDC and phase-error compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1706–1719, Aug. 2012. doi: 10.1109/TCSI.2012.2206500.

[15] C. S. Taillefer and G. W. Roberts, "Delta–Sigma A/D conversion via time-mode signal processing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 1908–1920, Sep. 2009. doi: 10.1109/TCSI.2008.2010144.

[16] M. Park and M. H. Perrott, "A single-slope 80 MS/s ADC using two-step time-to-digital conversion," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 2009, pp. 1125–1128. doi: 10.1109/ISCAS.2009.5117958.

[17] T. E. Rahkonen and J. T. Kostamovaara, "The use of stabilized CMOS delay lines for the digitization of short time intervals," *IEEE J. Solid-State Circuits*, vol. 28, no. 8, pp. 887–894, Aug. 1993. doi: 10.1109/4.231325.

[18] P. Chen, C.-C. Chen, J.-C. Zheng, and Y.-S. Shen, "A PVT insensitive Vernier-based time-to-digital converter with extended input range and high accuracy," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 2, pp. 294–302, Apr. 2007. doi: 10.1109/TNS.2007.892944.

[19] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1666–1676, Jul. 2008. doi: 10.1109/JSSC.2008.922712.

[20] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "An integrated 9-channel time digitizer with 30 ps resolution," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, vol. 1, Feb. 2002, pp. 266–465. doi: 10.1109/ISSCC.2002.993038.

[21] P. Keränen and J. Kostamovaara, "A wide range, 4.2 ps(rms) precision CMOS TDC with cyclic interpolators based on switched-frequency ring oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 12, pp. 2795–2805, Dec. 2015. doi: 10.1109/TCSI.2015.2485719.

[22] A. Mantyniemi, T. E. Rahkonen, and J. Kostamovaara, "A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3067–3078, Nov. 2009. doi: 10.1109/JSSC.2009.2032260.

[23] S. Liu and Y. Zheng, "A low-power and highly linear 14-bit parallel sampling TDC with power gating and DEM in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 3, pp. 1083–1091, Mar. 2016. doi: 10.1109/TVLSI.2015.2447001.

[24] Y. Kim and T. W. Kim, "An 11 b 7 ps resolution two-step time-to-digital converter with 3-D Vernier space," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2326–2336, Aug. 2014. doi: 10.1109/TCSI.2014.2304656.

[25] K. Kim, W. Yu, and S. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, Apr. 2014. doi: 10.1109/JSSC.2013.2297412.

[26] S.-J. Kim, W. Kim, M. Song, J. Kim, T. Kim, and H. Park, "A 0.6 V 1.17 ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with $16\times$ spatial redundancy in 14 nm FinFET technology," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2015, pp. 1–3. doi: 10.1109/ISSCC.2015.7063035.

[27] A. I. Hussein, S. Vasadi, and J. Paramesh, "A 450 fs 65-nm CMOS millimeter-wave time-to-digital converter using statistical element selection for all-digital PLLs," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 357–374, Feb. 2018. doi: 10.1109/JSSC.2017.2762698.

[28] J. P. Caram, J. Galloway, and J. S. Kenney, "Time-to-digital converter with sample-and-hold and quantization noise scrambling using harmonics in ring oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 1, pp. 74–83, Jan. 2018. doi: 10.1109/TCSI.2017.2712518.

[29] R. Nutt, "Digital time intervalometer," *Rev. Sci. Instrum.*, vol. 39, no. 9, pp. 1342–1345, Sep. 1968.

[30] J. Kostamovaara and R. Myllylä, "Time-to-digital converter with an analog interpolation circuit," *Rev. Sci. Instrum.*, vol. 57, no. 11, pp. 2880–2885, 1986. doi: 10.1063/1.1139008.

[31] J.-P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "Synchronization in a multilevel CMOS time-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1622–1634, Aug. 2009. doi: 10.1109/TCSI.2008.2010111.

[32] P. Michalik, J. Madrenas, and D. Fernandez, "Result-consistent counter sampling scheme for coarse-fine TDCs," *Electron. Lett.*, vol. 48, no. 19, pp. 1195–1196, Sep. 2012. doi: 10.1049/el.2012.1465.

[33] P. Keränen and J. Kostamovaara, "Oscillator instability effects in time interval measurement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 7, pp. 1776–1786, Jul. 2013. doi: 10.1109/TCSI.2012.2230502.

[34] J. Kalisz, M. Pawlowski, and R. Pelka, "Error analysis and design of the Nutt time-interval digitiser with picosecond resolution," *J. Phys. E, Sci. Instrum.*, vol. 20, no. 11, pp. 1330–1341, 1987. doi: 10.1088/0026-1394/41/1/004.

[35] J.-P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, Jun. 2006. doi: 10.1109/JSSC.2006.874281.

[36] *TDC-GPX2 4-Channel Time-to-Digital Converter, Datasheet*, Providence, RI, USA: AMS, Dec. 2017.

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