An FPGA-Based Hardware Platform for the Control of Spin-Based Quantum Systems

Xi Qin, Wenzhe Zhang, Lin Wang, Yuxi Zhao, Yu Tong, Xing Rong, and Jiangfeng Du

***Abstract*— This paper reports the development of a highly efficient, flexible hardware platform, which is suitable for the control of spin-based quantum systems including quantum computation and quantum metrology. A two-channel arbitrary waveform generator (AWG), an eight-channel pulse/sequence generator, a two-channel analog-to-digital converter (ADC), and a two-channel high-speed time-to-digital converter (TDC) are fully integrated on a printed circuit board (PCB). The AWG has a 1-GSa/s sampling rate and a 16-bit amplitude resolution. The pulse/sequence generator can continuously output pulse/sequence signals with a 50-ps time resolution and a dynamic range from 5 ns to 2 s. The ADC provides a 1-GSa/s sampling rate and a 12-bit amplitude resolution for analog signal acquisition. The TDC provides a 6-ps time resolution and a maximum sampling frequency of 125 MHz. All these modules are realized utilizing a field-programmable gate array (FPGA). Customized data calculation modules are also implemented with the FPGA logic. The hardware was tested and implemented in a pulsed electron spin resonance (ESR) spectrometer and an optically detected magnetic resonance (ODMR) spectrometer.**

***Index Terms*— Analog-to-digital converter (ADC), arbitrary waveform generator (AWG), field-programmable gate array (FPGA), pulse generator, quantum systems, solid spin, time-to-digital converter (TDC).**

I. Introduction

THE spin-based quantum techniques play an important role in quantum computation [1]–[3] and quantum metrology [4], [5]. The novel quantum techniques promote further development of instruments, such as electron spin resonance (ESR) spectrometers [6]–[8], and nitrogen-vacancy (N-V) center-based optically detected magnetic resonance (ODMR) spectrometers [9], [10]. Recent progress of instrumentation and measurement techniques will be helpful to enhance the performance of quantum tasks [11], [12] and pave the way toward practical applications of quantum computation and quantum metrology.

The control signal generation and output signal readout are required in spin-based quantum systems. Arbitrary waveform generators (AWGs) [13], [14] are usually utilized to generate radio frequency (RF)/microwave (MW) signals for controlling the spin-based quantum state [15], [16], and pulse/sequence generators are applied to obtain precise timing and synchronization [17], [18]. Amplitude and time measurements for the output signal are commonly realized with analog-to-digital converters (ADCs) [19] and time-to-digital converters (TDCs) [20], [21]. A complete experimental setup could be obtained by combining commercial-off-the-shelf (COTS) equipment. However, this solution is costly. On the other hand, the COTS equipment normally is specified and operates independently; thus, the flexibility in the system design and the synchronism of the signals will be limited using such solution.

Scientific researchers have put considerable efforts into developing customized hardware to meet the new demands of instrumentations for recent quantum applications. Specified hardware has been developed to realize the control signal generation and output readout for certain quantum systems [18], [22]–[27]. We reported the development of an integrated device with multifunction signal generators and TDCs in [28]. The integrated device can be used to control and readout the quantum state of the single electron spin in N-V centers. However, such device is not suitable for use in those spin-based quantum systems with ensemble samples, as there is no ADC-based data acquisition module integrated and the capacity of data processing is still undeveloped. Generally, customized device holds the potential to improve project management efficiency for certain tasks. However, the device should be redeveloped to meet some special requirements in spin-based quantum system. The undesirable repeated investment in device design is costly and time-consuming. Thus, a flexible hardware platform, which is compatible with different types of spin-based quantum systems, is meaningful to the scientific researchers of quantum technology.

In this paper, we present the design and fabrication of a high flexible, efficient hardware platform for the control of spin-based quantum systems. This hardware platform is implemented with a field-programmable gate array (FPGA), which is an integrated circuit to be configured by the designer. The platform cannot only be used in quantum systems based

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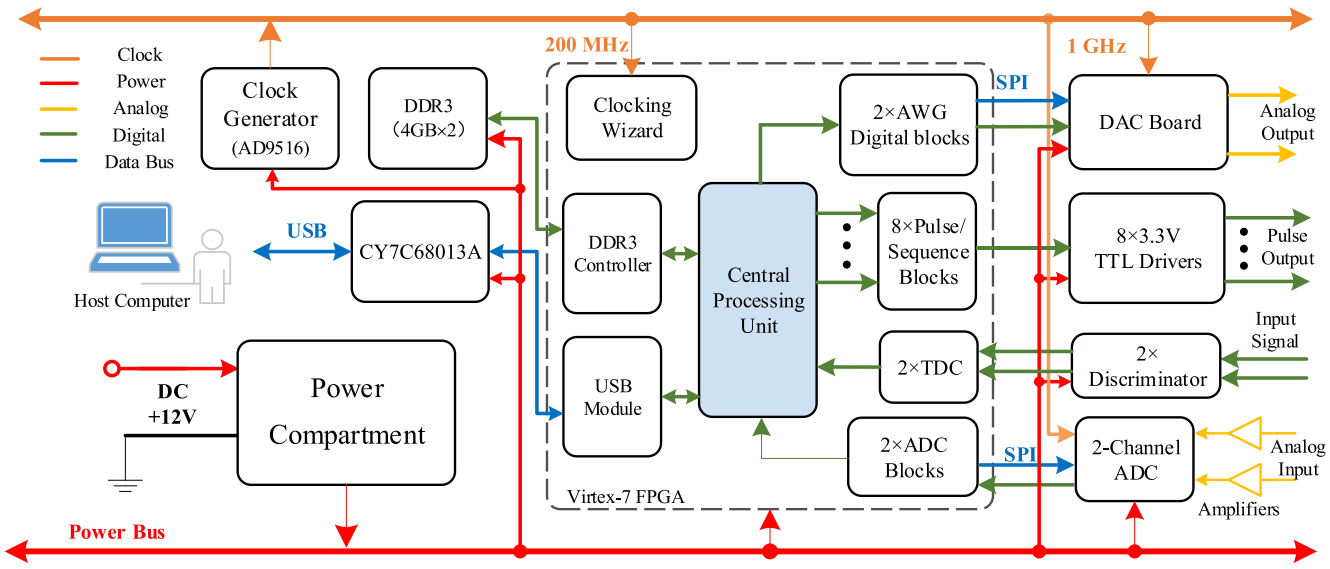

Fig. 1. Architecture of the FPGA-based hardware platform. Two-channel AWG, eight-channel 50-ps resolution pulse generator, two-channel ADC, and two-channel TDC are integrated on the hardware.

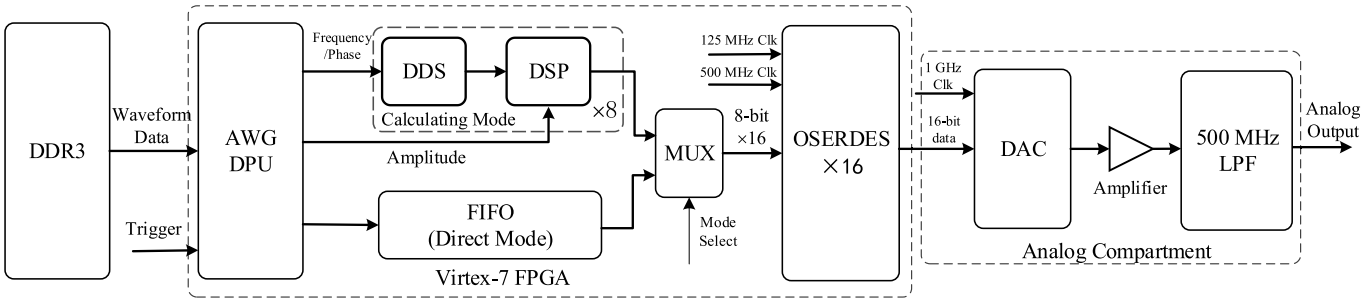

Fig. 2. Block diagram of a single-channel AWG.

on a single spin but it can also be used in those systems with ensemble samples. We report the architecture, performance characterization, and the experimental results of applying the hardware platform in ESR and ODMR spectrometers to measure spin dynamics [29], [30]. The test results prove its performance and flexibility.

II. Architecture

The architecture of the hardware platform is shown in Fig. 1. A Xilinx Virtex-7 FPGA is utilized as a central control unit. The digital signal management for the platform is fully controlled by the programmable digital logic inside the FPGA chip. The power compartment is used to generate power supplies for both the analog and digital circuits. Communications between the host computer and the hardware are handled by a universal serial bus (USB) microcontroller CY7C68013A [31]. A clock generator AD9516-3 [32] is utilized to manage clock distribution. A two-channel AWG, an eight-channel pulse/sequence generator, a two-channel ADC, and a two-channel TDC are integrated on the platform. Two 4-GB double-data-rate-III (DDR3) memories are implemented to provide adequate data storage capacity and memory bandwidth. The hardware platform requires a stable, low noise clock source to achieve high-quality signal generation, and high precision measurement. An oven-controlled crystal oscillator AOCJY [33] which has a phase noise of −145 dBc/Hz (1-kHz offset) is applied to provide the clock signal. The clock can also be provided by an external signal generator via an input interface on the board. All the input and output channels are equipped with 50-Ω Sub-Miniature Version A (SMA) termination. A single set of the hardware platform can be used for a two-qubit system, and it can be used in the multiqubit systems by cascading and synchronizing the duplications. The reprogrammable FPGA chip can provide favorable flexibility and scalability for various requirements.

A. Arbitrary Waveform Generator

The AWG is implemented with two digital-to-analog converter (DAC) AD9139 [34] chips, which provide a 1-GSa/s sampling rate and a 16-bit amplitude resolution. Fig. 2 shows the block diagram of a single AWG channel. Two operating modes are available for waveform generation: “direct mode” and “calculating mode.” In “direct mode,” the amplitude data of the user-defined waveform are prestored in the DDR3 memory and can be directly converted to analog signals by the DAC board. The DAC chips are installed on a separated board; thus, the AWG can be upgraded by replacing the DAC board when

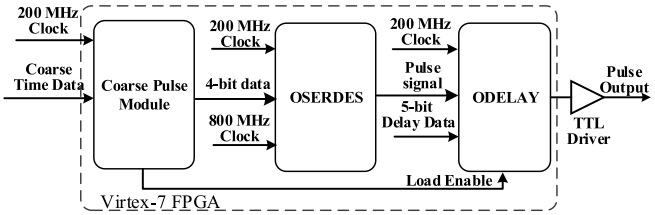

Fig. 3. Block diagram of a single channel 50-ps resolution pulse/sequence generator. The coarse pulse module manages the data flow of the pulse duration time. The OSERDES module accelerates the data rate and outputs pulse signals with a 1.25-ns time resolution. The ODELAY module is implemented to achieve fine time interpolating for the pulse signals; thus, a 50-ps time resolution can be obtained.

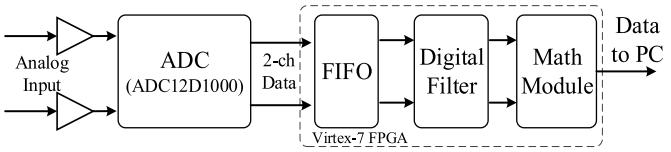

Fig. 4. Block diagram of the ADC module.

signals with higher sampling rate or higher bandwidth are required to control the spins. In [28], we reported the implementation of a 1-GSa/s AWG which operates in "direct mode." However, the maximum waveform length is less than 1 s due to the storage capacity of the DDR3 memory, and it requires a long time to transmit digital data of long waveforms from host computer to the hardware. In this design, a "Calculating mode" is developed. In "calculating mode," the waveform parameters, including signal frequency, amplitude, and initial phase, are prestored in the DDR3, and the output digital waveform data are on-board calculated according to these parameters. The data size in "calculating mode" can be significantly reduced comparing to that in "direct mode" when generating sine signal sequences; thus, the maximum waveform length can be increased, and the time for data transmission can be decreased accordingly. The AWG data processing unit (DPU) imports the arbitrary waveform data from the DDR3 memory and decodes the data flow. The direct digital synthesis (DDS) module and the digital signal processing (DSP) module are used to achieve on-board digital waveform calculation. The first-in–first-out (FIFO) module is the buffer memory for data output. Since OSERDES [35] is a high-performance parallel-to-serial converter integrated in the I/O resources in Xilinx 7 series FPGA, we use 16 parallel OSERDES cells to raise the output data rate. Eight input digital lines are connected to each OSERDES cell according to a 125-MHz clock, and the output data rate is raised up to 1 Gbits/s. Thus, a 16-Gbits/s digital data flow can be obtained. The utilization of the parallel interface contributes to a latency time within nanoseconds. The low latency from the input of OSERDES to the parallel output for DAC gives the opportunity to realize closed-loop control systems, which are meaningful to the further development of the spin-based quantum techniques. An analog amplifier and a low-pass filter (LPF) are integrated on the DAC board to improve output signal qualities. The output peak to peak voltage amplitude is 2 V, and the LPF has a -3-dB bandwidth of 500 MHz.

B. Pulse/Sequence Generator

The pulse/sequence generator is implemented to generate high precise timings for spin-based instruments. A time interpolating method [36] is applied to enhance the time resolution of the pulse sequences. Fig. 3 shows the simplified block diagram of a single channel pulse/sequence generator. The coarse pulse module manages the data flow of the pulse signals and outputs four parallel pulse signals with a 5-ns resolution according to the 200-MHz clock. The OSERDES module is used to accelerate the data rate; thus, the time resolution is improved to 1.25 ns. ODELAY [35] is a high-resolution delay cell integrated in the FPGA I/O logic. The ultimate time resolution of the pulse/sequence generator is determined by the averaged cell delay of ODELAY, which equals 50 ps. Thus, the arrival time of each rising and falling edge of the pulse signals can be real-time adjusted with a 50-ps resolution accordingly. Each pulse data are composed of a 31-bit coarse data and a 5-bit fine delay data. The 31-bit coarse data contributes to a maximum pulsewidth equaling 1.25×2^{31} ns $=$ 2.68 s. The total delay time of the delay chain should be longer than 1.25 ns; thus, a 5-bit fine delay data width is required to manage a 50-ps resolution delay chain. The dynamic range of each pulsewidth is from 5 ns to exceeding 2 s.

C. Analog-to-Digital Converter

The ADC chip used on the hardware platform is ADC12D1000 from Texas Instruments [37]. The chip provides two-channel 1-GSa/s sampling rate and 12-bit amplitude resolution. The bandwidth of the analog input is dc—400 MHz, and the input analog range is ± 400 mV. Fig. 4 shows the data flow management of the ADC module. A reconfigurable digital finite-impulse response (FIR) filter is implemented in the FPGA to eliminate the noise components from input signals. A customized math module is also implemented in the FPGA to achieve specified computations, such as amplitude addition, subtraction, and integration. The output data size can be reduced remarkably with the math module. The filter type, orders, input–output parameters, as well as the configuration of the math module are configurable; thus, favorable flexibility can be obtained to meet the requirement of spin-based applications.

D. Time-to-Digital Converter

TDC can be applied to measure the arrival time of output signals from the instruments and can also be used to calibrate the pulse/sequence generators. A high-resolution TDC is realized with FPGA resources, and the TDC architecture is shown in Fig. 5. A coarse counter is implemented for coarse time measurement, and dedicated carry chains are used to achieve fine time measurement [38]–[40]. A 23-ps resolution can be obtained using a single carry chain for time measurement [28]. In this paper, a multichain method [41] is used to improve the time measurement resolution. Increasing the number of parallel chains in a single TDC channel will be helpful to

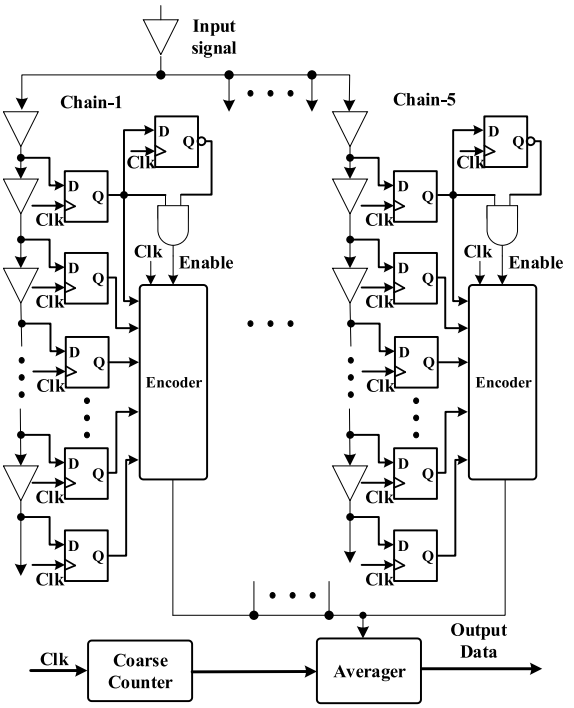

Fig. 5. Architecture of a single-channel multichain TDC.

improving the time resolution, whereas the occupied resources will also be increased. The time resolution cannot be improved significantly by increasing the chain numbers when more than five parallel chains are integrated in a single TDC channel [41]. Therefore, we designed a five-carry-chain TDC in order to obtain a good performance-to-cost ratio, and a 6-ps resolution has been achieved. The "Averager" is implemented to calculate the averaged time measurement result from the parallel chains. Once the TDC receives an input signal, an "Enable" signal which has a pulsewidth of one clock period will be generated at the next clock rising edge. The TDC measures the arrival time according to the "Enable" signal, and it cannot respond to another input signal when "Enable" is high. The TDC module operates with a 250-MHz clock, and the maximum sampling rate is 125 MHz. The dynamic range of the TDC is from 0 ns to 2.1 s.

E. Power Compartment

The block diagram of the power compartment for the hardware platform is shown in Fig. 6. The platform is powered by a +12-V direct current (dc) power supply. Adjustable switching regulators, which have a high converting efficiency up to 90%, are utilized to handle the input power and generate corresponding power sources for each circuit. The analog circuits require high-quality power supplies; thus, low-dropout regulators (LDO) are implemented to generate power outputs with low ripple voltages. The input and output drivers, the analog circuits of the ADC, and the clock circuits are powered by the LDOs. On the other hand, the power inputs of the digital circuits, including FPGA, on-board memories, and USB interface, are generated by the switching regulators. The DAC board has a power consumption of 6.8 W, and the power

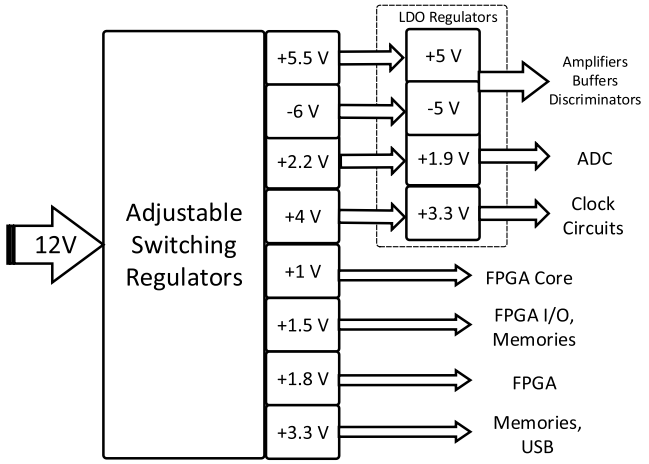

Fig. 6. Block diagram of the power compartment.

TABLE I
FPGA RESOURCE OCCUPATIONS OF THE HARDWARE PLATFORM

Resource[a]	LUT	SLICE	FF	BRAMs (36kb)	DSP	I/Os
AWG	2842	1062	3488	7	24	18
Pulse/Sequence Generator	1493	600	1623	7	0	1
TDC	11250	4230	12747	15	10	2
ADC Module	1483	1843	5024	55	162	54
DDR3 Controller	10847	4873	13309	0	0	114
USB Controller	67	43	88	1	0	29
Total Utilization	64855	28859	82568	211	392	473
Available	303600	75900	607200	1030	2800	700
Occupation	21.7%	38.0%	13.6%	20.5%	14%	67.8%

[a]6-input look up tables (LUT), slices and flip flops (FF) are the basic FPGA resources utilized by the hardware platform. The BRAMs and the DSP elements are the configurable functional cores integrated in the FPGA. The I/O ports are the digital channels to be defined by users.

consumption of the rest circuits of the hardware is 25 W. Thus, the total power consumption of hardware platform is 31.8 W.

F. Resource Occupation

FPGA resource occupation of the hardware platform is shown in Table I. The six-input lookup tables (LUTs), slices, and flip-flops are the basic resources inside the FPGA. The block random-access memories (BRAMs) and DSP cells are the internal hard cores of the FPGA. Input and output (I/O) ports are signal transmission channels to be configured by customers. The resource utilization of each functional module, the occupation of the entire design, and the total available resources in the Virtex-7 FPGA XC7VX485T-ffg1761 are listed. More than two-thirds of the available I/O ports are utilized to achieve the design, but there remain plenty of unoccupied FPGA logic resources after finishing the implementation. The redundancy of available resources and the

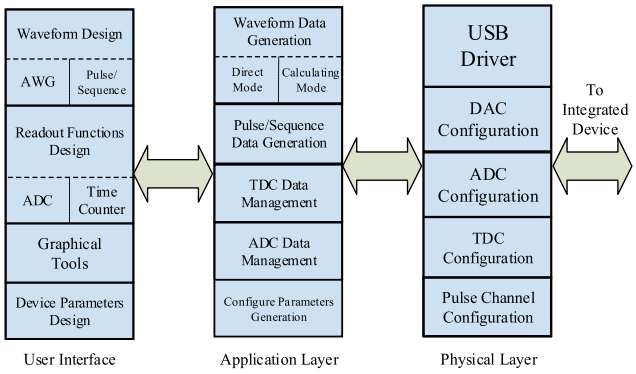

Fig. 7. Architecture of the customized software.

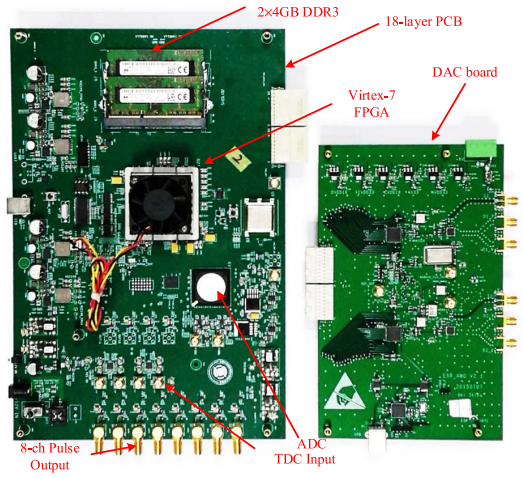

Fig. 8. Photograph of the hardware platform. The PCB on the left is the 18-layer hardware, and the PCB on the right is the DAC board. The Virtex-7 FPGA is located at the center of the 18-layer PCB, and a heat sink is installed at the top of FPGA chip.

reprogrammability of the FPGA chip give a great opportunity to improve the hardware function and flexibility. It will also be possible to use a smaller FPGA which has the same package to reduce the cost and the power consumption.

G. Customized Software

We also developed a customized software to handle the multiple modules of the hardware platform. Fig. 7 shows the architecture of the software. The software is developed in Python. The waveform data design for both AWG and pulse/sequence generator, the readout functions design for ADC and TDC, the graphical tool, and hardware configuration are fully managed by the software. Users can perform their operations and interact with the hardware platform via the user interface. The application layer is designed to encode users' commands and analyze the data flow. The physical layer is used to communicate with the hardware and realize the configuration through the USB port.

III. Performance Characterization

A Xilinx Virtex-7 FPGA is installed on an 18-layer PCB to implement the hardware platform, and the DAC board is a ten layer PCB. Fig. 8 shows the photograph of the hardware.

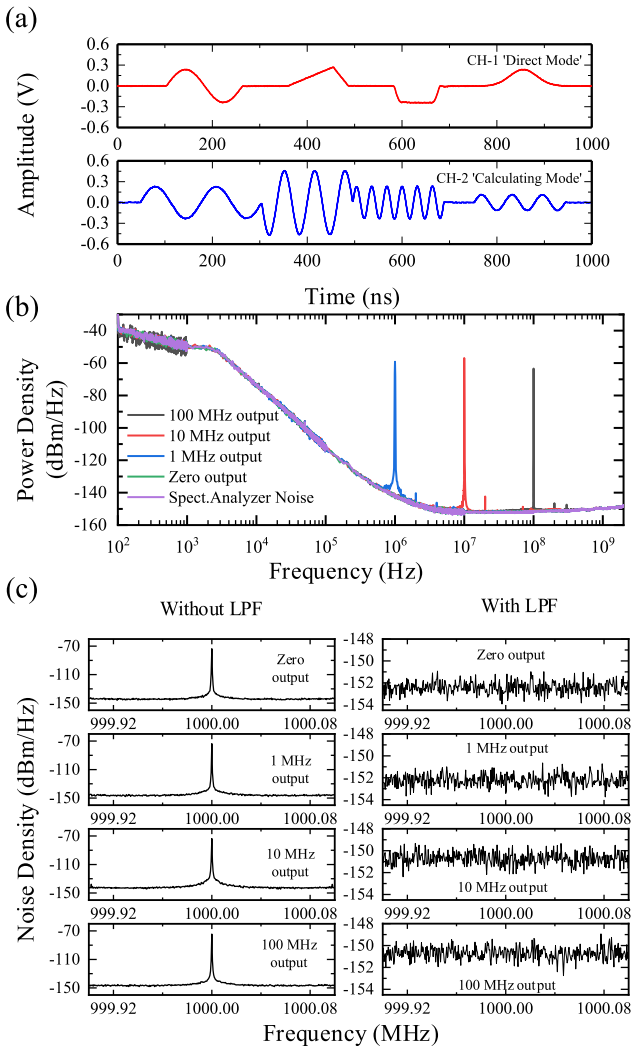

Fig. 9. Characteristics of the AWG channels. (a) Waveform signals generated in "direct mode" and "calculating mode." (b) Noise spectra measured up to 2 GHz. (c) Suppression of the 1-GHz clock noise.

The PCB on the left is the 18-layer hardware, and the other one is the DAC board. The Virtex-7 FPGA chip is located at the center of the 18-layer PCB, and a heat sink is located at the top of FPGA chip for heat dissipation. The two PCBs can be connected by two AMP-1469169-1 connectors. The hardware was fabricated and tested.

A. Arbitrary Waveform Generator

The characterization of the AWG channels is shown in Fig. 9. The analog waveforms was recorded by a LeCroy WavePro 735 Zi digital oscilloscope, which has a 40-GSa/s sampling rate and a 3.5-GHz bandwidth. Fig. 9(a) shows the waveforms from the AWG channels. AWG channel-1 is operated in the "direct mode" and generates user-defined arbitrary waveforms. AWG channel-2 operated in the "calculating mode" which utilized DDS and DSP cells to on-board calculating output digital waveforms. Amplitude, frequency, and phase angles of the signals from channel-2 can be real-time adjusted according to user-defined parameters. The noise spectra of the AWG were measured by a Keysight

TABLE II
DISTORTIONS' PERFORMANCE OF THE AWG

Frequency (MHz)	2nd harmonic (dBc)	3rd harmonic (dBc)	THD (dB)	SFDR (dB)
1	-81.4	-90.3	80.2	81.4
10	-73.71	-80.8	72.4	73.71
100	-72.4	-72.5	66.8	72.4

N9020A Spectrum Analyzer with a frequency ranging from dc to 2 GHz, and the test result is shown in Fig. 9(b). The noise floor of the AWG is identical to that of the spectrum analyzer; thus, the current test results for noise spectrum are limited by the performance of the measurement instruments. The noise spectra density was suppressed to below −150 dBm/Hz when outputting zero waveform, 1-, 10-, and 100-MHz sinusoidal signals. Fig. 9(c) demonstrates the measured noise from the 1-GHz sampling clock, and the clock noise is suppressed by two cascaded 11th-order low-pass Butterworth filters. The distortion performance of the AWG is shown in Table II. The power ratio of the second and third harmonics, the total-harmonic distortion (THD), and the spurious-free-dynamic range (SFDR) for generating 1-, 10-, and 100-MHz signals are reported, respectively. The signal power of the spectrum measurements in Fig. 9(b) and (c) and Table II is −12.5 dBm with a 50-Ω load.

B. Pulse/Sequence Generator

The performance of the pulse/sequence generator is demonstrated in Fig. 10. The oscillogram in Fig. 10(a) shows that both the rising edge and the falling edge from the pulse signals have a fine time resolution of 50 ps, and the pulse channels can output high-resolution continuous pulse signals with no dead time. In order to demonstrate the timing performance for the pulse signals, we measured the pulsed-delay intervals using a high-resolution TDC, which has a 1.15-ps averaged bin size, and a 3.5-ps single shot resolution [41]. An RF signal generator SG386 [42] which has a low phase noise of −145 dBc (1-kHz offset) is applied to provide the clock signal to the high-resolution TDC. Fig. 10(b) shows the fine-delay time variation when increasing the input code for ODELAY. A 50-ps increasing step and a favorable linearity can be obtained by using the high-performance pulse/sequence generator. Fig. 10(c) shows the statistical histogram for measuring fixed time intervals of pulse signals from two pulse channels. Time intervals of 0.75 ns, 1 μs, 1 ms, and 500 ms were measured, respectively. The standard deviation demonstrates that both the short term jitter and the long term jitter of the pulse signals are below 15 ps, which is less than the half of the 50-ps pulse resolution. The jitter of the long pulses increases due to the accumulation of the clock noise. The pulse/sequence generator shows a high stability within a large dynamic range.

C. Analog-to-Digital Converter

The ADC module is tested according to the IEEE standard 1241-2010. We utilized the RF signal generator SG386 [42]

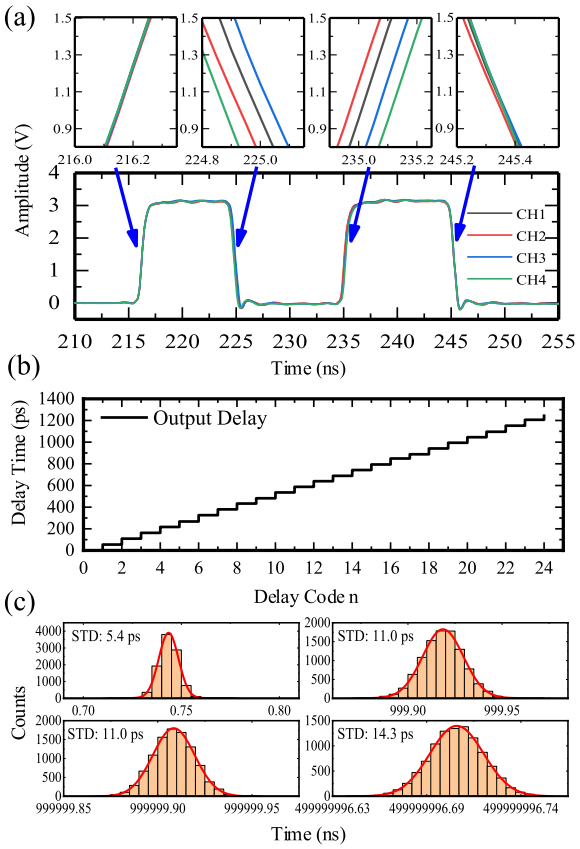

Fig. 10. Performance characterization of the pulse/sequence generator. (a) Oscillogram of the pulse signals from four pulse channels. (b) Increasing fine delay of the ODELAY cell. (c) Histograms for measuring time intervals of 0.75 ns, 1 μs, 1 ms, and 500 ms.

to generate the test signals. The parameters of the digital filter inside the ADC module are reloadable, as the filter is realized using reconfigurable FPGA logic. Thus, the filter can be applied to filter signals with different frequencies. Table III shows the test results of ADC performance with and without digital filters when acquiring signals with different frequencies, and considerable improvement was obtained after applying a digital band-pass filter (BPF). The passband of the BPF is also listed in Table III, and the filter bandwidth is various when recording signals with different frequencies. In Table III, SFDR stands for spurious-free-dynamic-range, SNR is signal-to-noise ratio, SINAD is signal-to-noise and distortion ratio, THD is total-harmonic distortion, and ENOB stands for the effective-number of bits. In order to observe the crosstalk between AWG and ADC, we record the acquired signals by the ADC when AWG channels are outputting waveforms with a 2-V peak-to-peak amplitude at a 500-MHz maximum frequency, and the test results are shown in Fig. 11. Fig. 11(a) shows the spectrum of the background noise recorded by the ADC when AWG is OFF, and Fig. 11(b) shows the background noise spectrum when AWG is operating. The power of the 500-MHz noise increases by 6 dB when AWG is operating. Fig. 11(c) and (d) show the spectra of 100-MHz signals acquired by the ADC. As the 500-MHz noise is modulated by the 100-MHz signal, the power of fourth harmonic which is located at 400 MHz increases by 6 dB when AWG is operating,

TABLE III
ADC CHARACTERIZATION WITH DIFFERENT INPUT FREQUENCIES

Input Signal Frequency (MHz)	SFDR (dB)		SNR (dB)		SINAD (dB)		THD (dB)		ENOB (bit)		Filter Bandwidth (MHz)
	Without Filter	With Filter	Without Filter	With Filter	Without Filter	With Filter	Without Filter	With Filter	Without Filter	With Filter	
10	56.23	69.32	51.05	66.9	49.69	64.74	55.37	68.78	8.03	10.52	5-15
20	50.25	84.23	51.04	67.75	47.26	67.66	49.61	83.98	7.64	11.01	15-25
30	47.25	82.77	50.87	67.53	45.24	67.39	46.62	82.22	7.29	10.97	25-35
40	51.14	82.95	50.96	65.88	46.49	65.78	48.41	81.9	7.51	10.71	30-50
50	49.69	86.03	51.08	66.07	47.23	66.07	49.54	97.49	7.64	10.74	40-60
60	51.72	82.74	50.65	65.66	48.04	65.66	51.5	92.38	7.75	10.69	50-70
70	46.53	77.3	50.52	65.54	44.9	65.54	46.28	92.63	7.23	10.67	60-80
80	43.15	82.97	50.34	65.77	42.26	65.74	43	86.81	6.8	10.7	70-90
90	41.61	69.85	50.25	63.8	40.86	63.75	41.39	83.39	6.55	10.37	80-100
100	54.76	80.39	50.58	65.75	48.43	65.76	52.51	104.72	7.82	10.69	90-110
110	49.82	76.15	50.22	64.67	45.81	64.67	47.76	96.26	7.38	10.5	100-120
120	51.69	80.96	50.27	65.18	46.52	65.18	48.89	99.99	7.5	10.61	110-130
130	47.48	77.29	50.05	64.47	44.43	64.47	45.82	95.03	7.16	10.48	120-140
140	48.36	80.36	5.1	64.46	44.85	64.35	46.39	80.09	7.21	10.48	130-150
150	47.93	82.41	50.06	64.52	44.38	64.53	45.75	103.26	7.14	10.49	140-160

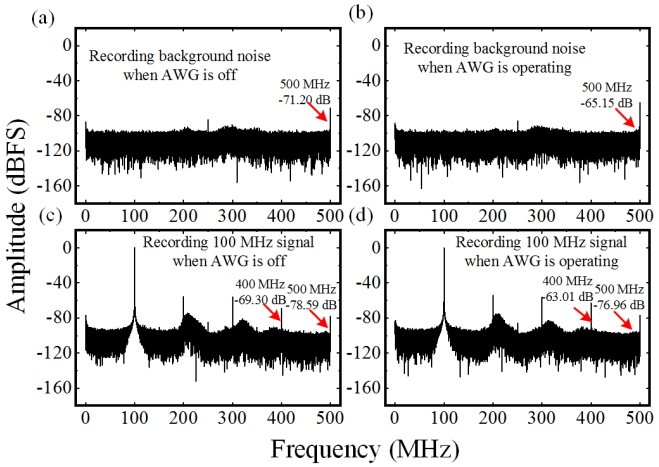

Fig. 11. Signal spectra of acquired background noise (a) when AWG is OFF and (b) when AWG is operating. Spectra of 100-MHz signals acquired (c) when AWG is OFF and (d) when AWG is operating.

and the power of the 500-MHz noise decreases compared to the test results when recording background.

D. Time-to-Digital converter

As mentioned above, five parallel carry chains are integrated in a single TDC channel to improve the time resolution, and the test results of the TDC are shown in Fig. 12. The TDC bin size is obtained with the "code density" method [43], and Fig. 12(a) shows the bin size of single-chain TDC and five-chain TDC. The averaged bin size is decreased from 23 to 4.6 ps with five chains in a single channel. The time resolution of the TDC channels is evaluated by "cable-delay test" [41].

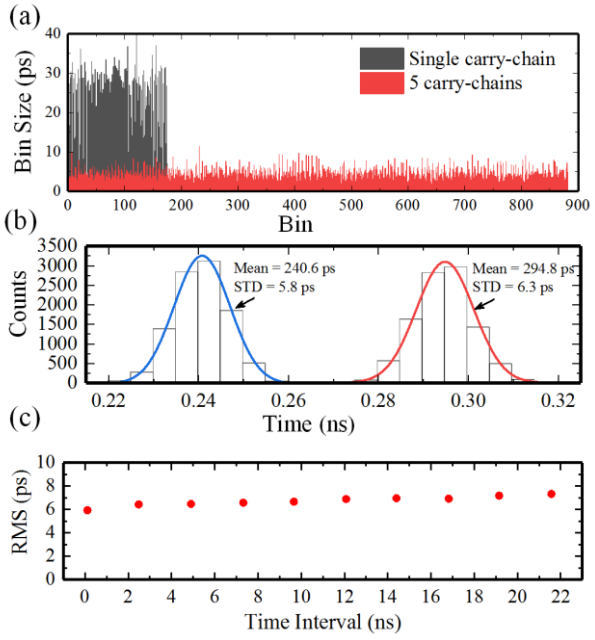

Fig. 12. Characterizations of the TDC. (a) Comparison of the averaged bin size between utilizing a single carry-chain and utilizing five chains. (b) Histogram of time intervals measurement. (c) RMS resolution of measuring different time intervals.

Pulse signals transmit through cables with different lengths to provide various time delays, and the arrival time of the pulse signals are measured by the TDC channels. Fig. 12(b) shows the statistical histogram of measuring mixed pulse signals with different time intervals. The time histograms which has a 54.2-ps difference were separated effectively, and the

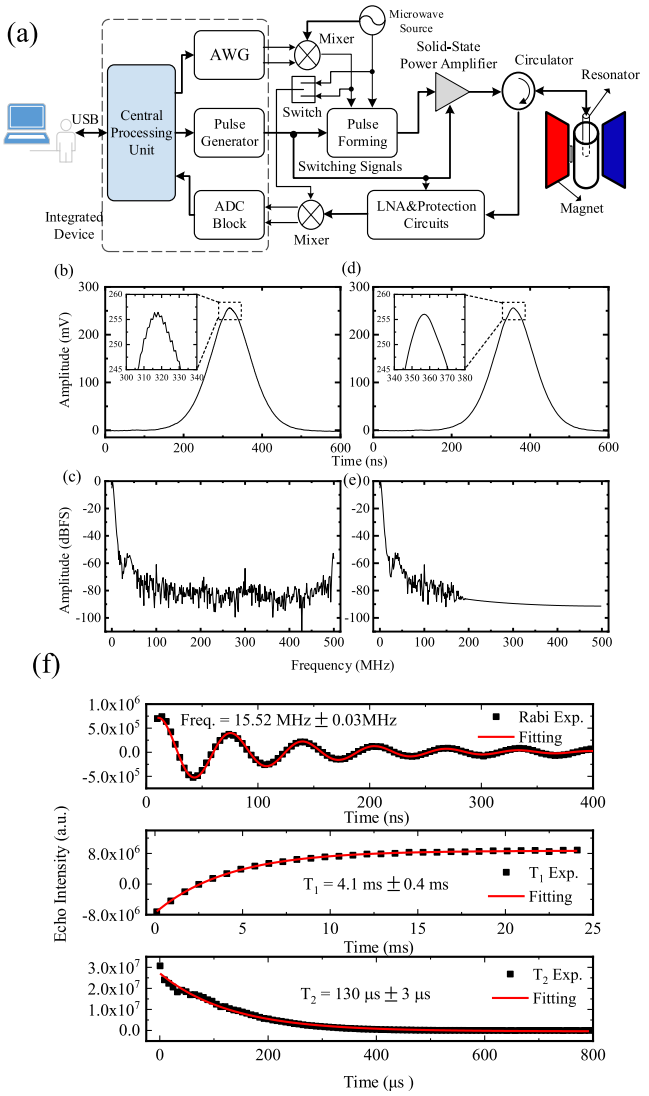

Fig. 13. (a) Architecture of a pulsed ESR spectrometer developed using the hardware platform. (b) Output echo signals from the spectrometer. (c) Spectrogram of the output signals. (d) Echo signals after the digital LPF. (e) Spectrogram of the output signals after the digital LPF. (f) Rabi oscillation and relaxation time for the silicon samples.

standard deviation of the statistical results were 5.8 and 6.3 ps, respectively. Fig. 12(c) shows the test results when applying the TDC in measuring time intervals from 0 to 22 ns, and the standard deviations are below 7 ps.

IV. Spin Dynamics Measurement

In order to demonstrate the performance of the hardware platform when it is used to measure spin dynamics in spin-based quantum systems, we implemented the hardware in a pulsed ESR spectrometer and an ODMR spectrometer. A frequency synthesizer FSW-0010 [44], which is provided by National Instruments, is used to generate the MW signals for the spectrometers. The frequency synthesizer has a phase noise of -112 dBc/Hz (1-kHz offset) at 10 GHz.

The architecture of the pulsed ESR spectrometer developed using the hardware platform is shown in Fig. 13(a). The samples to be tested in the ESR experiments are located in the resonator which exhibits the magnetic resonant behavior. Signals from the AWG module, which are mixed with the MW signals, are fed into the resonator. The reflected signals from the resonator are amplified by a low noise amplifier (LNA). A mixer is used to perform the frequency downconversion, and the amplified output signals can be converted to low frequency signals that can be measured by the ADC module. The pulse/sequence generator is utilized to realize the switching control for the pulse forming module, the solid-state amplifier, and the protection circuits. Fig. 13(b) shows the output echo signal measured using the ESR spectrometer, and the signals are from a sample of phosphorous donors in silicon (P:Si) material [45]. The experiments were performed with a 3496 Gauss static magnetic field and a 9.714-GHz MW at a temperature of 8 K. A Hahn echo pulse sequence [45] is applied to obtain the reflected signals. Fig. 13(c) shows its spectrogram. As the output signal was modulated by high frequency noise, we configured the digital filter in the ADC module as an LPF with a passband from dc to 150 MHz. The waveform in Fig. 13(d) and spectrogram in Fig. 13(e) show that the high frequency noise is eliminated. The plots of Rabi oscillation, spin–lattice relaxation time (T_1), and spin–spin relaxation time (T_2) [8] for the P:Si samples are demonstrated in Fig. 13(f). The echo intensity, which presents the resonant information of the samples, is obtained by calculating the time-domain integration of the echo signal. Three types of specified sequences are applied to obtain the three plots. The horizontal axis of the Rabi plot is the pulsewidth of the MW sequence. The curves of T_1 and T_2 are plotted with a horizontal axis standing for the free evolution time in the sequences [45]. A 64.4-ns Rabi oscillation period (15.52 MHz), a 4.1-ms T_1, and a 129-μs T_2 was obtained. Compared with the experimental results (5.6-ms T_1 and 120-μs T_2) of using a Bruker E580 ESR spectrometer [46] to acquire echo signals from a P:Si sample [45], similar results can be obtained using the ESR spectrometer based on the hardware platform in this paper. The test results prove that a qualified hardware platform has been developed for measuring spin dynamics with the pulsed ESR spectrometer. The P:Si sample is an attractive candidate for spin-based quantum computing. The test result in Fig. 13(f) shows that the length of T_2 is more than much longer than the Rabi period. The long relaxation time T_2 and the short single operation time (one-fourth of the Rabi period) allow the complex operations to control the spin state within the relaxation time, and fault tolerant quantum computing can be achieved [47]. On the other hand, the ESR spectrometer is widely applied to the scientific research fields including chemistry [48], biology [49], and medicine science [50]. The test results in Fig. 13 also prove the capacity of using the hardware platform to perform basic ESR experiments; thus, the platform has the potential to be used in the applications mentioned above.

We also implemented the hardware platform in an ODMR spectrometer, and the system architecture is demonstrated in Fig. 14(a). The platform can be used to measure spin dynamics for both systems of a single N-V center and N-V ensembles. In N-V center-based ODMR experiments, the spin in N-V center can be optically initialized and readout, and the spin state can be control by MW sequences [51].

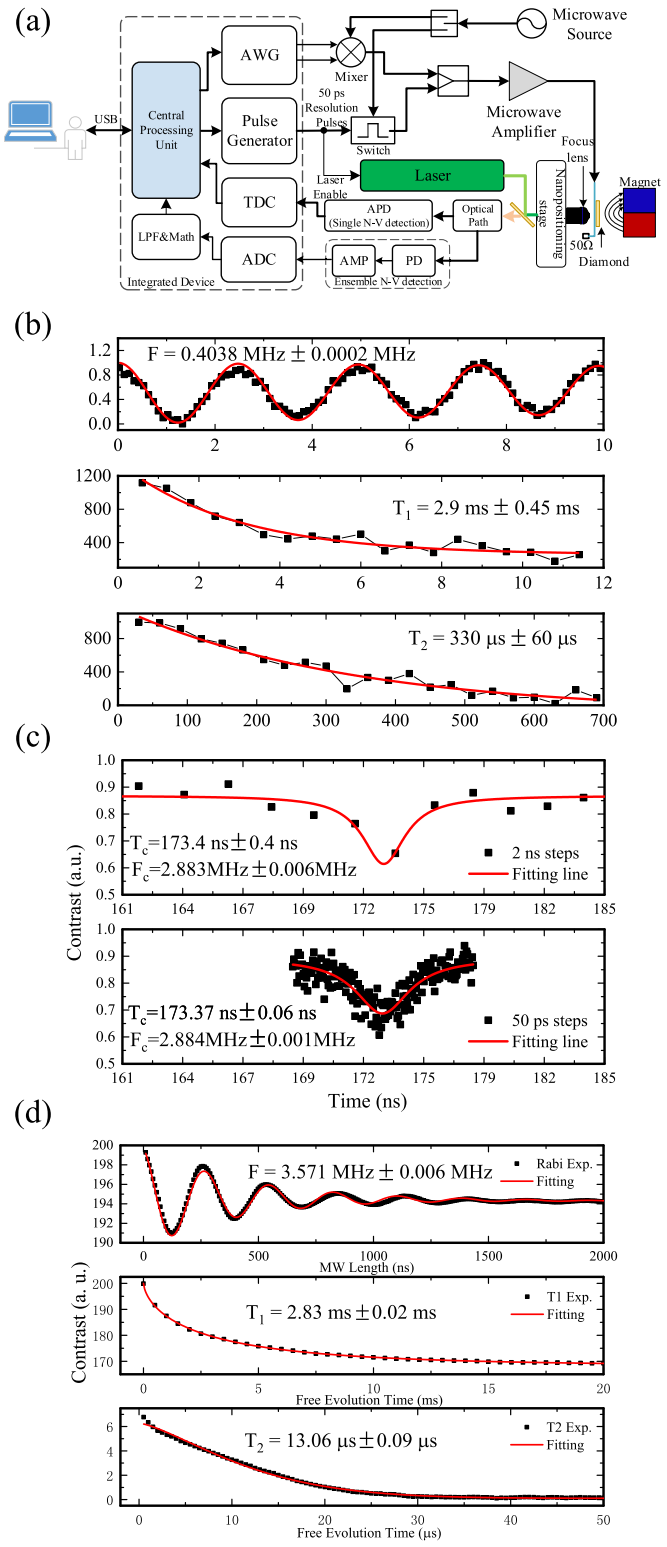

Fig. 14. (a) Architecture of the N-V center-based ODMR spectrometer using the hardware platform. (b) Test results of measuring spin dynamics for a single N-V center. (c) Nanoscale NMR for hydrogen atoms with a 50-ps time resolution. (d) Experimental results of measuring spin dynamics for an ensemble of N-V centers.

The AWG module is used to modulate the MW signals, and the pulse/sequence generator is used to switch the modulated MW and to enable laser output. The MW is preamplified before being delivered to the N-V center in diamond. The laser is utilized to initialize the quantum state of the single electron spin in the N-V center. The fluorescence intensity of N-V center depends on its spin state, and an optical path is used to collect the photons output from the N-V center. A single photon detection method is required readout the photon signal from the samples of single N-V center. An avalanche photodiode (APD) which can convert the single photon to an electric pulse signal is applied to detect the photons emitted by a single N-V center. As the APD outputs discrete pulses which stand for the arrival of photons, the TDC is utilized to measure the arriving time of the output signal from APD and to record the photon counts. The fluorescence intensity is represented by the photon counts. On the other hand, a great number of photons will arrive simultaneously when using an ensemble of N-V centers; thus, the APD cannot be used to record the intensity of fluorescence. A photodetector (PD) which can convert the fluorescence intensity to analog signal is used to collect the photons from the ensemble of N-V centers. The output signal of PD can be measured by the ADC on the hardware platform.

Fig. 14(b) shows the test results of measuring spin dynamics for a single N-V center. The experiment was done at room temperature, with a 423-G static magnetic field and a 4.054-GHz MW. The period of the Rabi oscillation is 1/0.4038 MHz = 2.48 μs, T_1 is 2.9 ms, and T_2 is 330 μs. The experimental results show no obvious difference comparing to the previous experimental results which are obtained at a similar condition (T_1 = 5.93 ms and T_2 = 0.4 ms) [52]. The single N-V center is another candidate for quantum computation, and the long spin–spin relaxation time T_2 in the experimental results proves that the hardware platform can be applied in the study of high fidelity quantum computations based on N-V center [16], [53]. In order to show the potential of measuring high-time resolution nanoscale nuclear magnetic resonance (NMR) spectroscopies, the hardware platform is used to measure the nanoscale NMR signals from hydrogen atoms in oil. Fig. 14(c) shows the experimental results which is obtained with a 677-G static magnetic field at room temperature, and a 50-ps resolution 16-step XY-8 sequence [15] was applied using the integrated pulse/sequence generator. Comparing to the experimental results with 2-ns resolution sequences, the peak position of the NMR spectrum for hydrogen was located more precisely with 50-ps resolution sequences. The spectrum resolution is similar to that reported in [36]. Due to the strong performance in pulse/sequence generation, the hardware platform can be further applied to study high resolution quantum sensing [54], [55]. Test results of measuring spin dynamics for an ensemble N-V sample are shown in Fig. 14(d), and the experiment is also performed at room temperature, with a 7.7-G static magnetic field and a 2.891-GHz MW. The Rabi oscillation frequency of the N-V ensemble is 3.571 MHz, the spin–lattice relaxation time T_1 is 2.83 ms, and the spin–spin relaxation time T_2 is 13.06 μs. The reported T_2 of the N-V ensemble is within 5–20 μs [56], [57]. The N-V center ensemble has a potential to be applied in magnetometry [58]. The test results prove that the hardware platform can be used in the studies of magnetometry with ensembles of N-V centers.

TABLE IV
PERFORMANCE COMPARISON AMONG CUSTOMIZED HARDWARE

Parameter		This work	RSI'17 [22]	RSI'17 [23]	RSI'17 [24]	RSI'17 [18]	ACM'17 [25]	PRApp'18 [26]	arXiv'18 [27]	RSI'17 [28]
AWG	Sampling Rate	1 Gsps	N/A	1.2 Gsps	1.6 Gsps	2 Gsps	N/A	1 Gsps	2 Gsps	1 Gsps
	Bandwidth	500 MHz	N/A	600 MHz	330 MHz (DC) 800 MHz (AC)	800 MHz	N/A	300 MHz	N/A	500 MHz
	Number of Channels	2	N/A	4	2	16	2 (single board)	2	4	2
	Amplitude	2 Vpp	N/A	1 Vpp	1.2 Vpp (DC) 0.4 Vpp (AC)	N/A	N/A	2 Vpp	N/A	2 Vpp
	Amplitude Resolution	16-bit	N/A	16-bit	14-bit	12-bit	14-bit	10-bit	16-bit	16-bit
Pulse Generator	Time Resolution	50 ps	N/A	N/A	5 ns	40 ns	N/A	N/A	N/A	50 ps
	Dynamic Range	5 ns – 2.68 s	N/A	N/A	16 days	N/A	N/A	N/A	N/A	5 ns - 2 s
	Number of Channels	8	N/A	N/A	5	32	8	N/A	N/A	8
ADC	Sampling Rate	1 Gsps	1.2 Gsps	1 Gsps	800 Msps	N/A	N/A	105 Msps	N/A	N/A
	Bandwidth	400 MHz	15 MHz	N/A	550 MHz	N/A	N/A	65 MHz	N/A	N/A
	ENOB	10.52-bit (100 MHz)	6-bit (@1 MHz)	8.6-bit (71 MHz)	11.2-bit（70 MHz）	N/A	N/A	12.2-bit (@40.2 MHz)	N/A	N/A
	Input Range	-400 mV – 400 mV	0.9 V – 1.6 V	2 Vpp	2.2 Vpp	N/A	N/A	2 Vpp	N/A	N/A
	Number of Channels	2	N/A	2	2	N/A	2	2	N/A	N/A
TDC	Time Resolution	6 ps	16 ps	N/A	N/A	10 ns	N/A	N/A	N/A	23 ps
	Dynamic Range	5 ns – 2.1 s	N/A	N/A	N/A	N/A	N/A	N/A	N/A	5 ns – 42 s
	Number of Channels	2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2
	Max. Sampling Frequency	125 MHz	100 MHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Application Fields		Spin-based quantum systems	Cryogenic temperature quantum computing	Supercon-ductor quantum computing	Nuclear Magnetic Resonance	Cold trapped ions and atoms	Supercon-ductor quantum computing	Supercon-ductor quantum computing	Supercon-ductor quantum computing	Single N-V center

The comparison among various customized hardware for quantum application is listed in Table IV. A reconfigurable cryogenic platform which is designed for the classical control of quantum processors operating at cryogenic temperatures is reported in [22], FPGA-based TDCs which have a 16-ps time resolution are used to implement the ADC modules, and a 1.2-GSa/s sampling rate has been obtained. In [26], a low-latency closed-loop system for superconductor quantum computing and communication is reported, and an FPGA is used to realize the feedback and feed-forward operations. The implementations of hardware for superconductor quantum computers are also reported in [23], [25], and [27]. Synchronized multichannel AWGs are used to generate the control signals for the quantum bits, and the ADCs are used to readout the output signals. The AWGs which are used to perform superconductor quantum computing generally have a sampling rate ranging from 1 to 2 GSa/s, and an amplitude resolution within 14–16 bit. Similar hardware designed for NMR spectrometers is presented in [24], and a multichannel pulse generator which has a 5-ns resolution is also implemented. The systems based on cold trapped ions and atoms also require multichannel AWGs and pulse generators to control the quantum state, and DDS modules are applied to generate the control signal [18]. The signal readout for this system is performed by a 10-ns TDC.

The quantum bits of the quantum systems mentioned above are commonly controlled by the analog signal sequences output from the AWG channels, whereas a sampling rate of around 1 GSa/s and an amplitude resolution of better than 10 bit are required. The signal readout for superconductor quantum computing and NMR applications is generally realized using high-performance ADCs, and a sampling rate ranging from 100 MSa/s to 1.2 GSa/s is needed. TDC modules, which have a time resolution better than nanoseconds, are

applied to measure the output signals of the quantum systems based on cold trapped ions and atoms, as well as that based on single N-V centers. In order to realize synchronous control for the devices in the systems including NMR as well as cold trapped ions and atoms, multichannel pulse generator which has a nanosecond time resolution is utilized.

In order to implement a flexible hardware platform for the control of spin-based quantum systems, high-performance AWGs and ADCs which have a sampling rate around 1 GSa/s, are also required to generate the RF control signals and to record the output signals. Pulse generators that have a high time resolution will be helpful to obtaining high time resolution spectra. Picosecond resolution TDCs can be used to achieve a precise measurement for the arrival time of the output signals from the spin-based quantum systems. The hardware platform described in this paper is an integration design including a two-channel AWG which has a 1-GSa/s sampling rate and 16-bit amplitude resolution, a two-channel 12-bit ADC with a 1-GSa/s sampling rate, an eight-channel pulse generator with a 50-ps resolution, and a two-channel TDC with a 6-ps time resolution. The performance of the AWG and the ADC modules on the hardware is similar to those described in [18] and [22]–[27]; whereas the time resolution of the pulse generator and the TDC is superior to those mentioned above, hence the spectra can be measured with a better time resolution. As discussed above, the performance of the AWG channels and the ADC channels on the hardware platform has a good compatibility with the requirements of the systems for superconductor quantum computing; thus, the hardware has the potential to be used to in quantum computations based on superconductors. On the other hand, the AWG can operate in a "calculating mode" which is based on DDS; hence, waveform generation of long sine signal sequences can be achieved. The parameters and the functions of AWG channels are similar to those used in the systems based on cold trapped ions and atoms. The performance of the high-resolution TDC and the pulse generators can also meet the requirement of signal arrival time measurement and synchronous control for such systems. Thus, the hardware platform can be used in the studies of cold trapped ions and atoms. The hardware platform is a full integration of the functional modules including signal generation and readout, and reconfigurable digital signal processing modules are also integrated using the programmable FPGA logic resources. Thus, the hardware platform provides a high flexibility and can meet the requirements of different types of quantum applications.

Designing application-specific-integrated-circuit (ASIC) chips can help to achieve superior performance comparing to the separate functionalities of the hardware platform. A 16-bit, 10-GSa/s DAC, a 12-bit, 6.4-GSa/s ADC, a 10-ps resolution pulse generator, and a TDC with better than 3-ps rms time resolution are reported, respectively, in [59]–[62]. However, it will be costly to develop such high-performance ASIC chips to build the hardware platform. Using commercial equipment is another solution to build such a system. However, the implementation of the full hardware platform requires many different commercial instruments and the design of peripheral custom circuits; thus, the system scalability is limited.

V. Conclusion

We described the design and implementation of a flexible hardware platform for the control of spin-based quantum systems. The platform was applied in ESR and ODMR spectrometers. Hardware performance and flexibility have been confirmed by the test results. The platform can also be used as a signal generator or as a data acquisition equipment for other instruments. The platform can be easily upgraded by reprogramming the FPGA logic. In the future studies, the modules including multiplexing, RF generation, mixing, and amplification can be integrated on the hardware platform to improve the functionality. The platform has a bright future to be applied in spin-based instrumentations as well as corresponding applications, such as quantum computation, high resolution quantum sensing, and interdisciplinary researches. The platform also has the potential to be implemented in those instruments for other quantum systems, such as superconductor quantum computations [63], cold atoms [64], and trapped ions [65].

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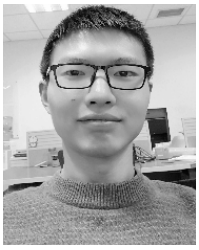

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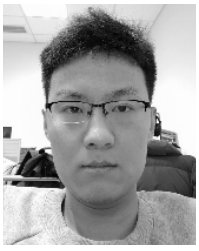

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